# 1 Tabelas Tutorial 2

| Event Name | Naive | Interchanged |
|---|---|---|
| cpu-cycles | 547997864 | 385408603 |
| instructions | 931779569 | 873670026 |
| cache-references | 8320994 | 379814 |
| cache-misses | 27905 | 18545 |
| branch-instructions | 133776058 | 126115011 |
| branch-misses | 277424 | 256916 |
| bus-cycles | 0 | 0 |
| L1-dcache-loads | 240142105 | 243739176 |
| L1-dcache-load-misses | 54162900 | 7343843 |
| L1-dcache-stores | 9683369 | 125326167 |
| L1-dcache-store-misses | 290076 | 98819 |
| LLC-loads | 7231132 | 274505 |
| LLC-load-misses | 3056 | 4625 |
| LLC-stores | 259152 | 203242 |
| LLC-store-misses | 27378 | 14222 |
| dTLB-load-misses | 5896 | 9885 |
| dTLB-store-misses | 722 | 445 |
| iTLB-load-misses | 633 | 0 |
| branch-loads | 131571446 | 123282031 |
| branch-load-misses | 6534783 | 5270872 |

Table 1: Todos os contadores Naive

| RATIO or RATE | NAIVE | INTERCHANGE |
|---|---|---|
| Elapsed time (seconds) | 0.189498719 | 0.144975696 |
| Instructions per cycle | 1.70 IPC | 2.27 IPC |
| L1 cache miss ratio | 0.2255 | 0.030 |
| L1 cache miss rate PTI | 58.13 | 7.88 |
| Data TLB miss ratio | 0.00071 | 0.026 |
| Data TLB miss rate PTI | 0.0063 | 0.011 |
| Branch mispredict ratio | 0.0021 | 0.00204 |
| Branch mispredict rate PTI | 0.29774 | 0.2940 |

Table 2: Todos os contadores Interchanged

## 2    Tabelas Tutorial 3

**2.1    Modo Contagem: large_naive vs. large_interchange**

**2.2    Modo Contagem: rates and ratios**

**2.3    Modo Amostras: large_naive vs. large_interchange**

**2.4    Modo Amostras: rates and ratios**