1 Tabelas Tutorial 2

Event Name	Naive	Interchanged
cpu-cycles	547997864	385408603
instructions	931779569	873670026
cache-references	8320994	379814
cache-misses	27905	18545
branch-instructions	133776058	126115011
branch-misses	277424	256916
bus-cycles	0	0
L1-dcache-loads	240142105	243739176
L1-dcache-load-misses	54162900	7343843
L1-dcache-stores	9683369	125326167
L1-dcache-store-misses	290076	98819
LLC-loads	7231132	274505
LLC-load-misses	3056	4625
LLC-stores	259152	203242
LLC-store-misses	27378	14222
dTLB-load-misses	5896	9885
dTLB-store-misses	722	445
iTLB-load-misses	633	0
branch-loads	131571446	123282031
branch-load-misses	6534783	5270872

Table 1: Todos os contadores Naive

RATIO or RATE	NAIVE	INTERCHANGE
Elapsed time (seconds)	0.189498719	0.144975696
Instructions per cycle	1.70 IPC	2.27 IPC
L1 cache miss ratio	0.2255	0.030
L1 cache miss rate PTI	58.13	7.88
Data TLB miss ratio	0.00071	0.026
Data TLB miss rate PTI	0.0063	0.011
Branch mispredict ratio	0.0021	0.00204
Branch mispredict rate PTI	0.29774	0.2940

Table 2: Todos os contadores Interchanged

2 Tabelas Tutorial 3

2.1 Modo Contagem: large_naive vs. large_interchange

EVENT NAME	NAIVE LARGE	INTERCHANGE LARGE
Elapsed Time	103.3436	10.5054
cpu-cycles	117011200000	17004500000
instructions	40648400000	39952000000
cache-references	5709100000	26100000
cache-misses	4898800000	22100000
LLC-loads	5781400000	25800000
LLC-load-misses	4930900000	22800000
dTLB-load-misses	1700000	100000
branches	3914700000	3786900000
branch-misses	2200000	1800000

Table 3: Modo Contagem: Interchange Large vs Naive Large

2.2 Modo Contagem: rates and ratios

EVENT NAME	NAIVE LARGE	INTERCHANGE LARGE
IPC	0.3474	2.3495
Cache miss ratio	0.85	0.86
Cache miss rate PTI	120.516	0.55
LLC load miss ratio	0.85	0.88
LLC load miss rate PTI	121.31	0.57
dTLB load miss rate PTI	0.042	0.0025
Branch mispredict ratio	0.00056	0.00048
Branch mispred rate PTI	0.054	0.045

Table 4: Modo Contagem: Rates and Ratios (Naive Large vs Interchange Large)

2.3 Modo Amostras: Naive Large vs. Interchange Large

2.4 Modo Amostras: Rates and Ratios

0.5

Figure 1: svg image

EVENT NAME	NAIVE LARGE	INTERCHANGE LARGE
Elapsed Time	103.3436	10.5054
cpu-cycles	1M amostras	170K amostras
instructions	406K amostras	399K amostras
cache-references	57K amostras	261 amostras
cache-misses	48K amostras	221 amostras
LLC-loads	57K amostras	258 amostras
LLC-load-misses	49K amostras	228 amostras
dTLB-load-miss	17 amostras	1 amostras
branches	39K amostras	37k amostras
branch-miss	22 amostras	18 amostras

Table 5: Modo Amostras: Naive Large vs Interchange Large

EVENT NAME	NAIVE LARGE	INTERCHANGE LARGE
IPC	0.406	2.35
Cache miss ratio	0.84	0.86
Cache miss rate PTI	118.23	0.55
LLC load miss ratio	0.86	0.88
LLC load miss rate PTI	120.68	0.57
dTLB load miss rate PTI	0.042	0.0025
Branch mispredict ratio	0.00056	0.00049
Branch mispred rate PTI	0.054	0.045

Table 6: Modo Amostras: Rates e Ratios (Naive Large vs Interchange Large