北京交通大学

Experiment 1
Full-Adder （全加器）

BJTU

http://www.dsvlab.cn/

https://mp.weixin.qq.com/s/Hhn0dJ_D1AcEB-6zcQyXVw

Contents

- Coding and circuitry - signal conversion
- Gate circuit - Signal correlation
- Adder - Signal calculation

Coding and circuitry

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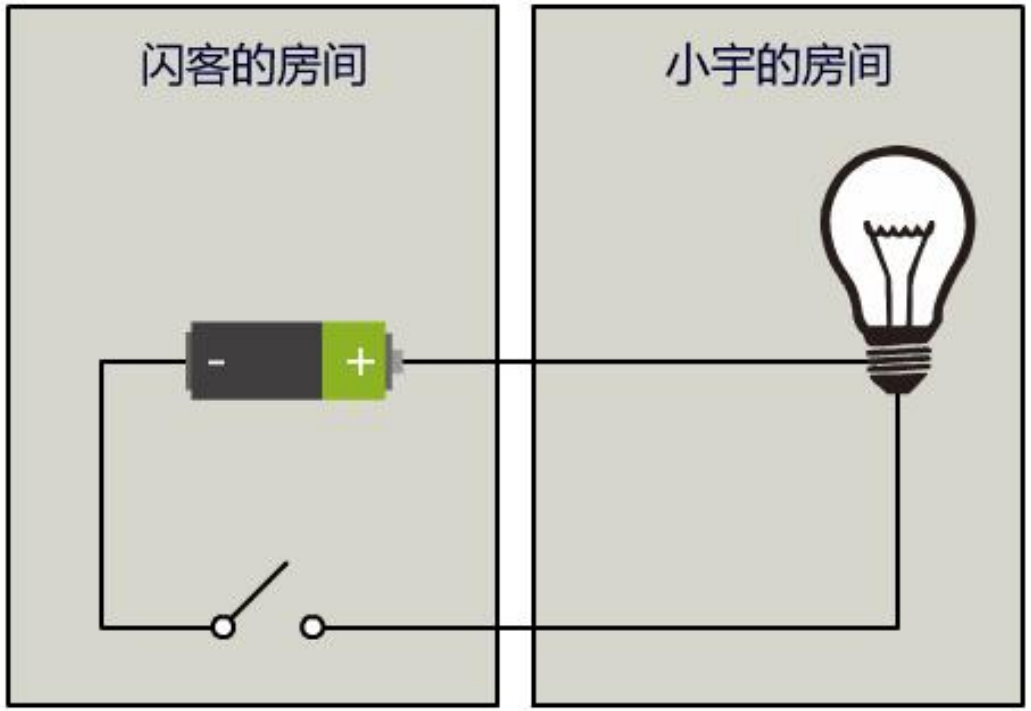
Suppose Shanke want to send signal to Xiaoyu：



Coding and circuitry

We use the combination of light bulbs to express all the words, and made an agreement to read the state of the light bulbs every second and record it, which is our code.

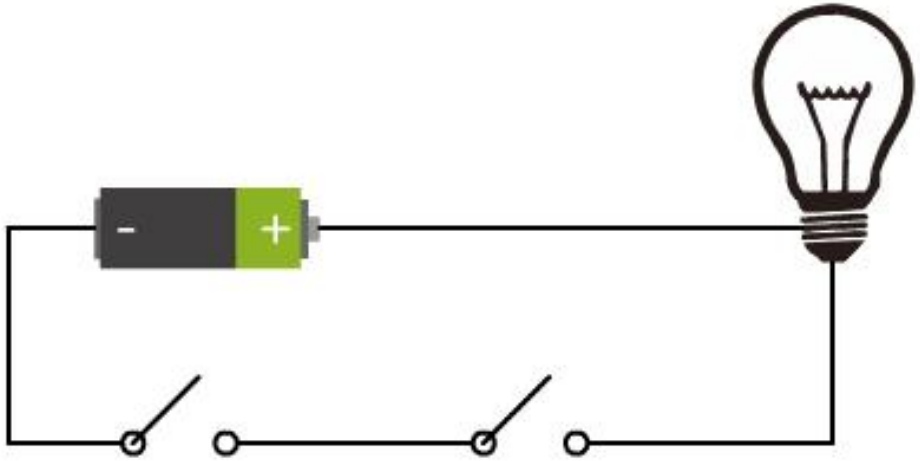
I: ON ON OFF OFF ON

Like: OFF ON ON OFF OFF

You: ON OFF ON OFF ON

Gate circuit

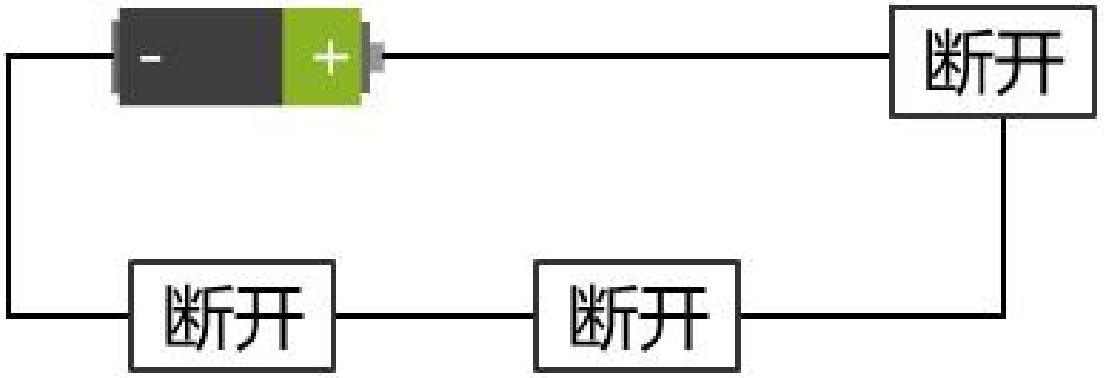
Make the code with two inputs



In this way, there is no longer a simple correspondence between the two switches and the bulb, but a **logic**.

Gate circuit

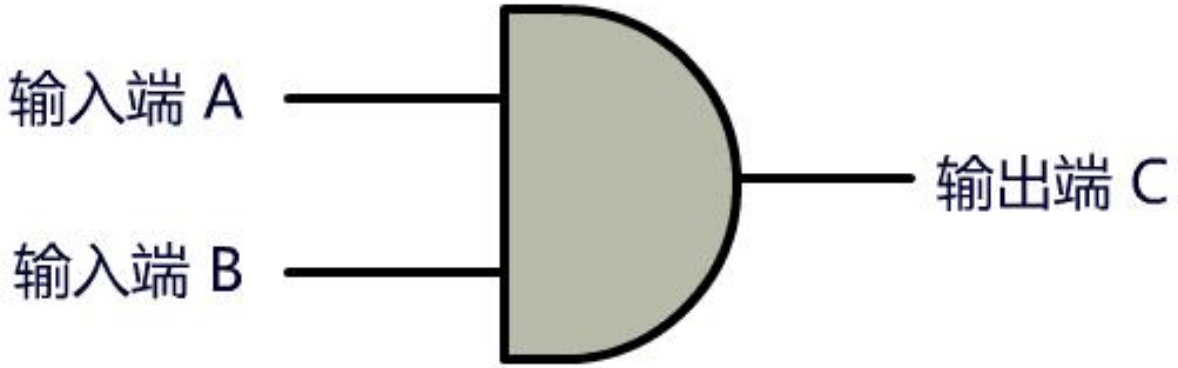
The disconnection and connection of the switch correspond to the disconnection and connection of the circuit respectively. The bulb is ON or OFF, also correspond to the circuit's condition. Then the two can be unified.

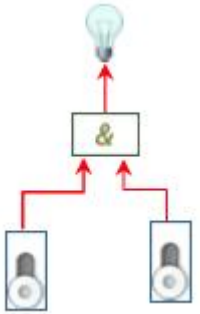


The connection and disconnection of the switch is active. The ON and OFF of the small bulb, is passive, is the result.

Gate circuit

We call the connection and disconnection of the switch as the input, and the connection and disconnection of the bulb as the output, and encapsulate the whole circuit in a graph:



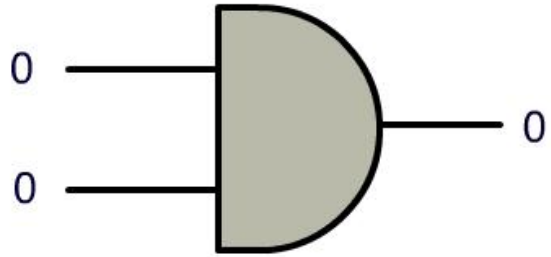


We decide to call this circuit a gate circuit(门电路), and the top one is called an **AND** gate.

Gate circuit

For more abstract exploration in the future, we will represent the circuit connection as the number 1 and the circuit disconnection as the number 0. We call this representation as **binary**.

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1



Gate circuit

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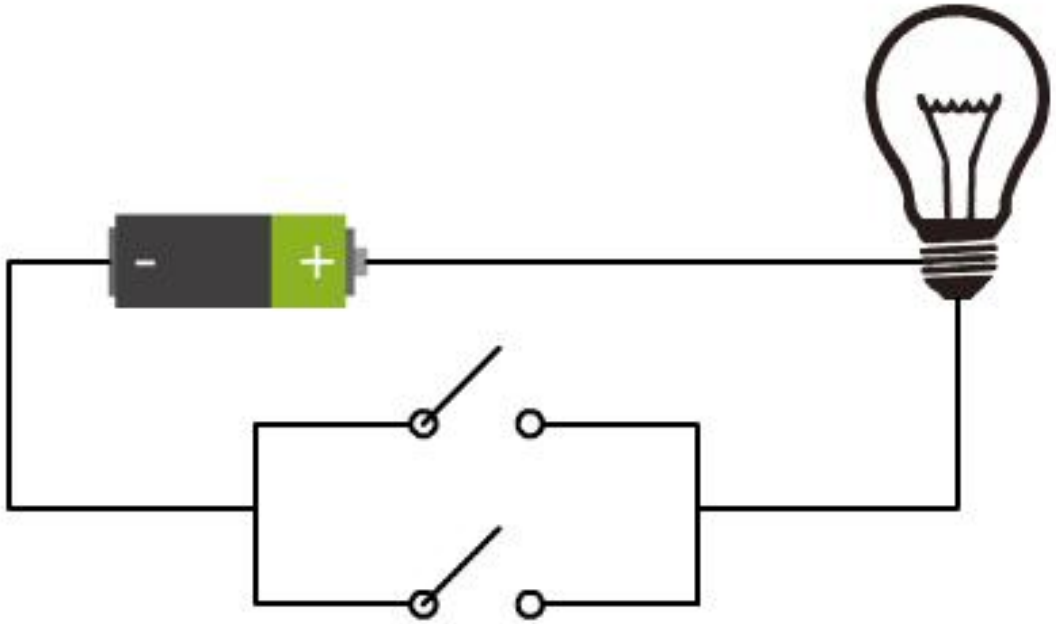
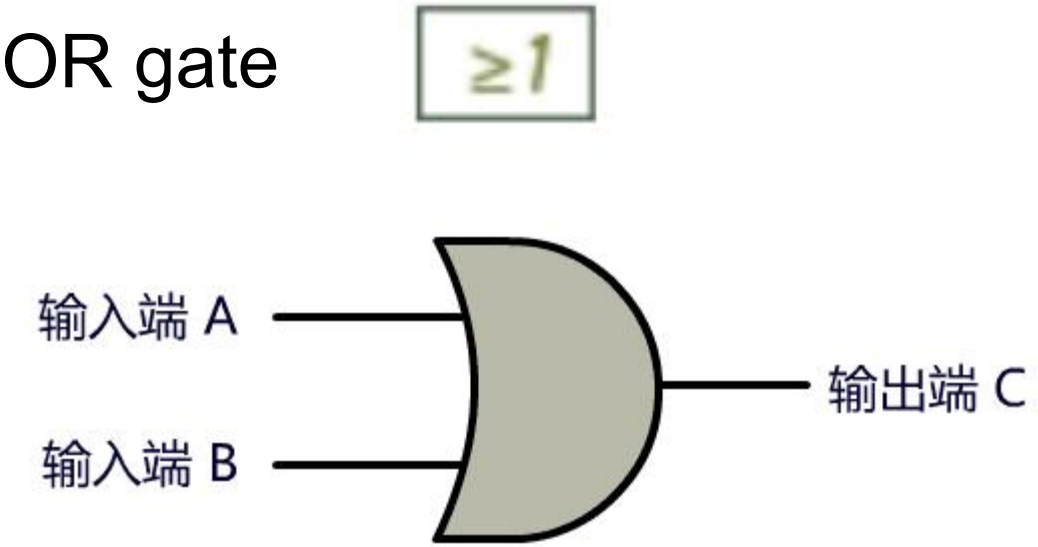
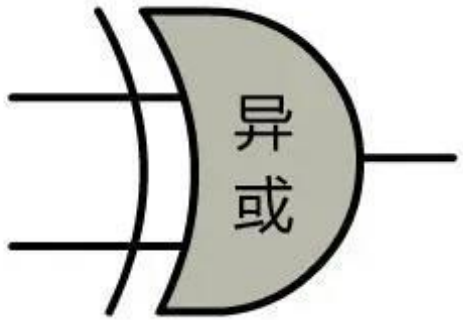
and MORE



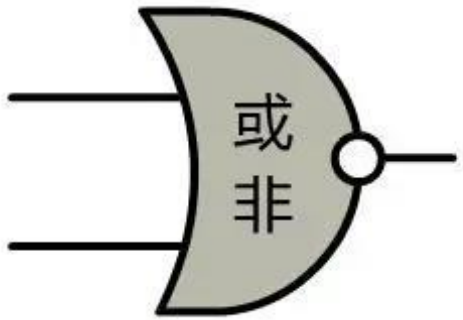
OR gate



XOR



NOR



Adder - Signal calculation

Let's start by adding the simplest bits of binary:

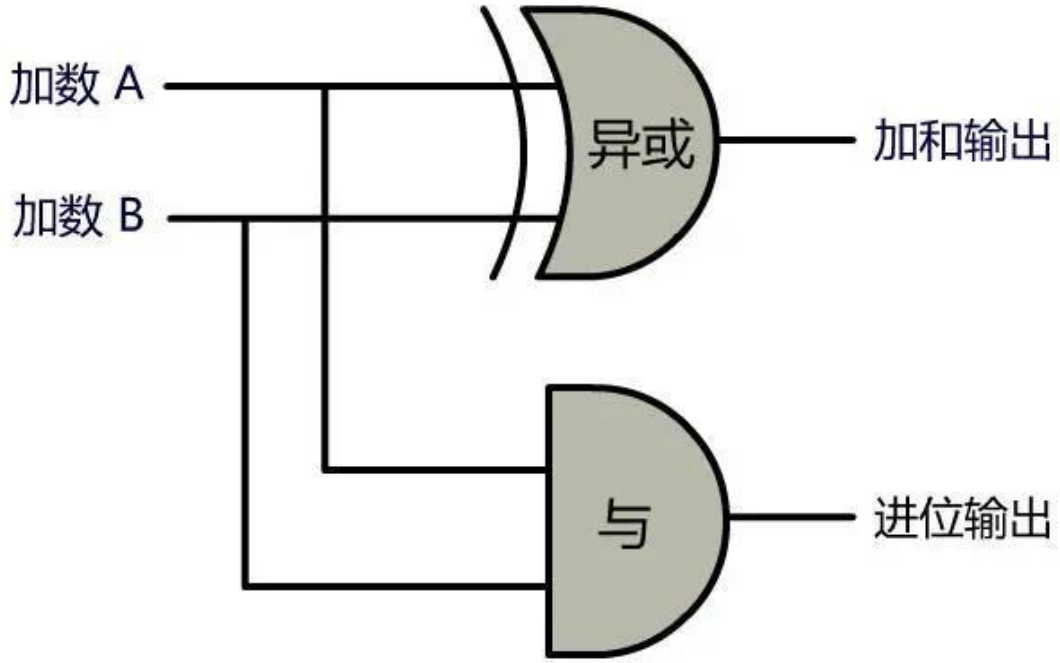
0+0=0; 0+1=1; 1+0=1;
1+1=10

The output can be reformed into

Addend A	Addend B	Sum bit	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Adder - Signal calculation

The circuit can be composed of XOR gate and AND gate.



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

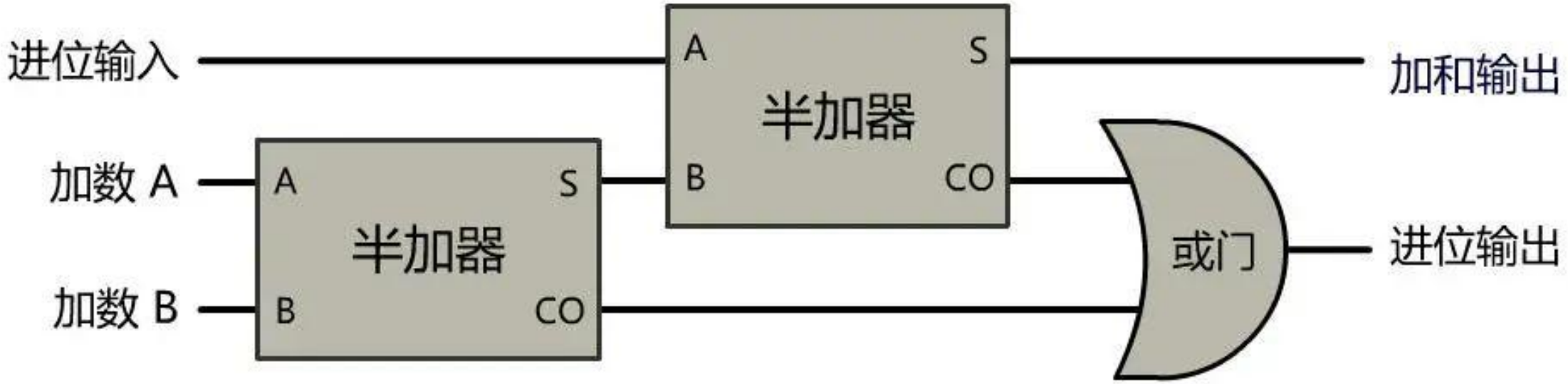
Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

Adder - Signal calculation

This device implements one bit addition in binary, but it is not perfect because it considers only the carry and output of the **two digits**, but not the carry of the **previous digits**, so it is only called a half adder (半加器).

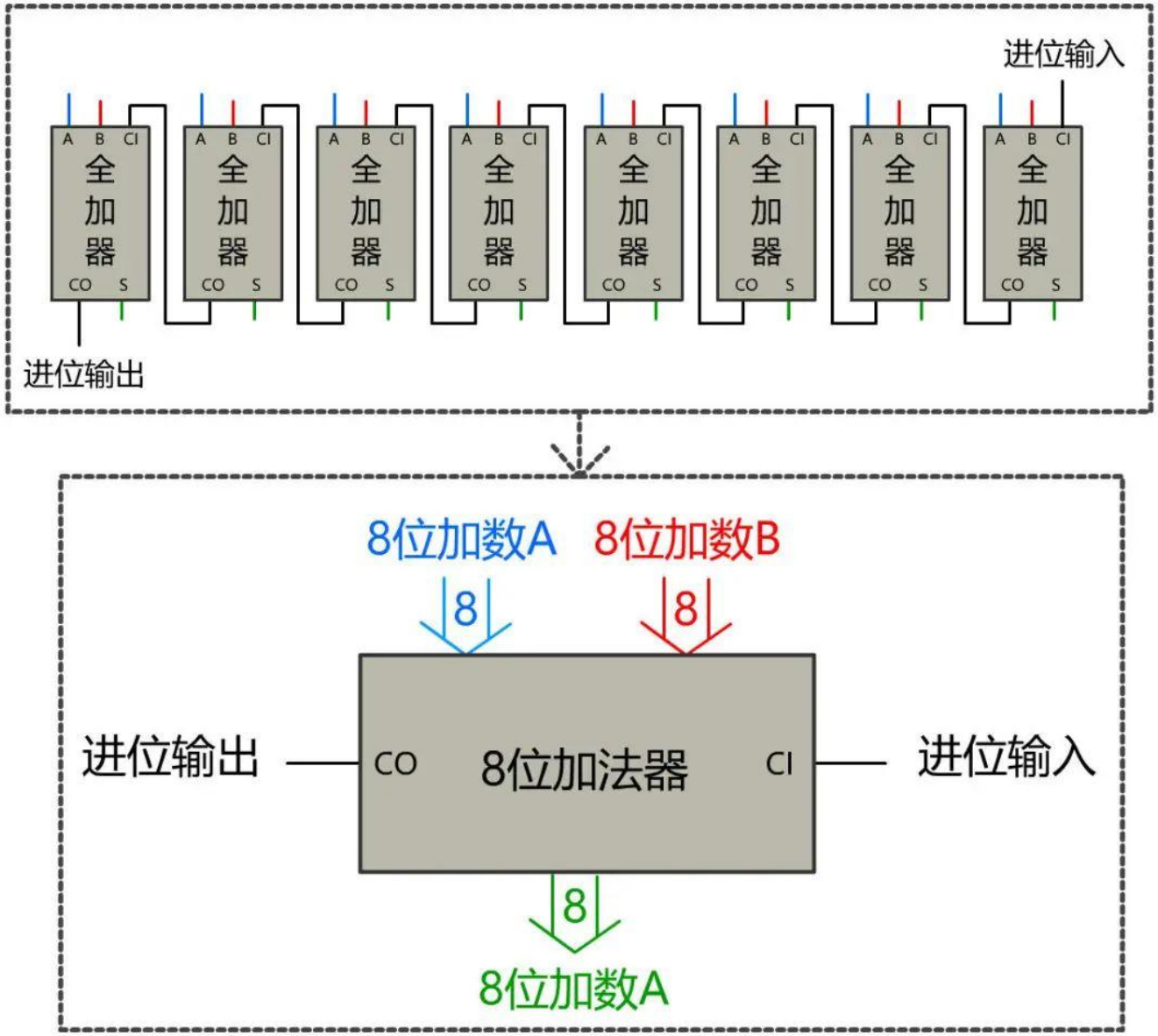
Adder -

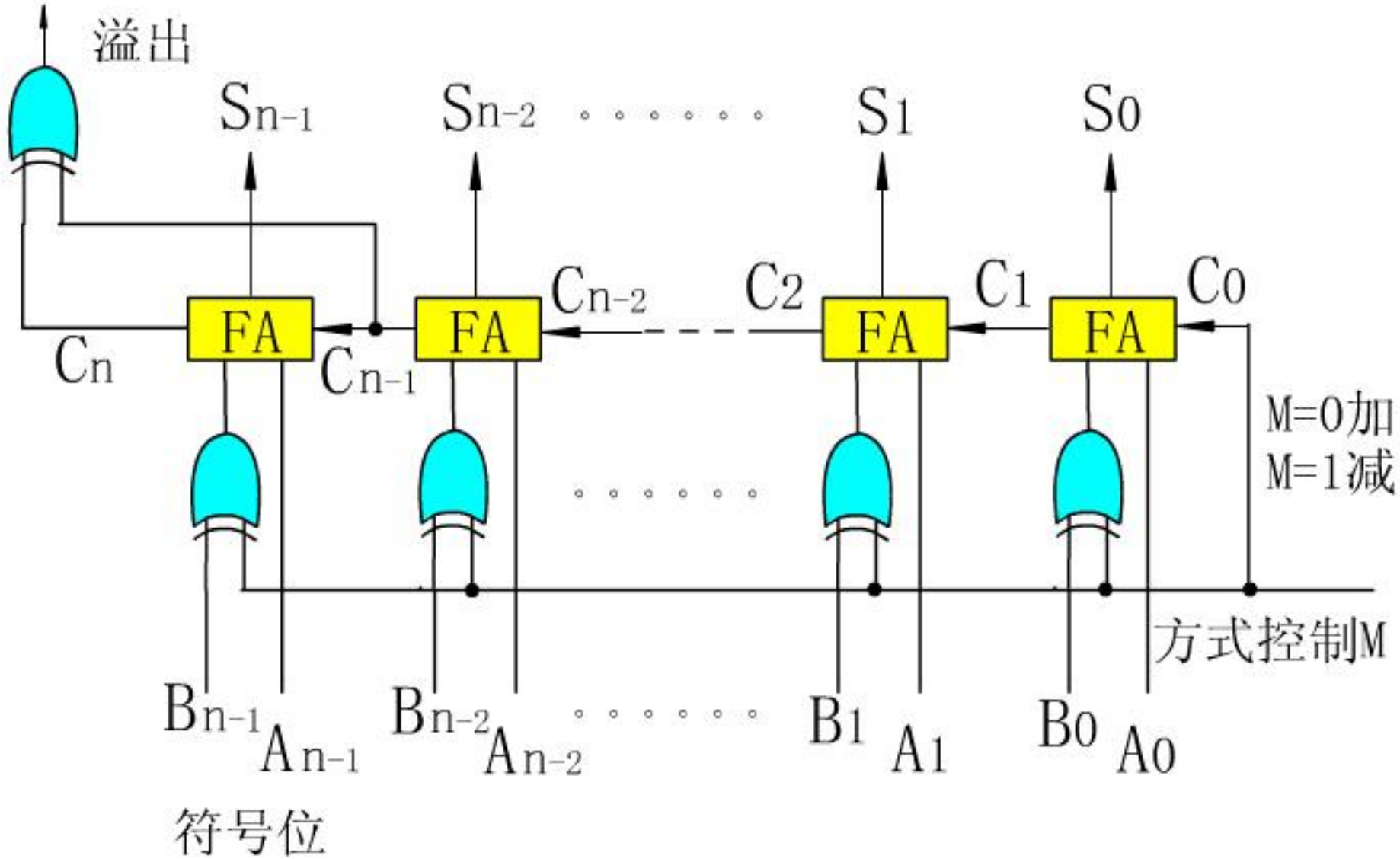
If the previou f more adders are n



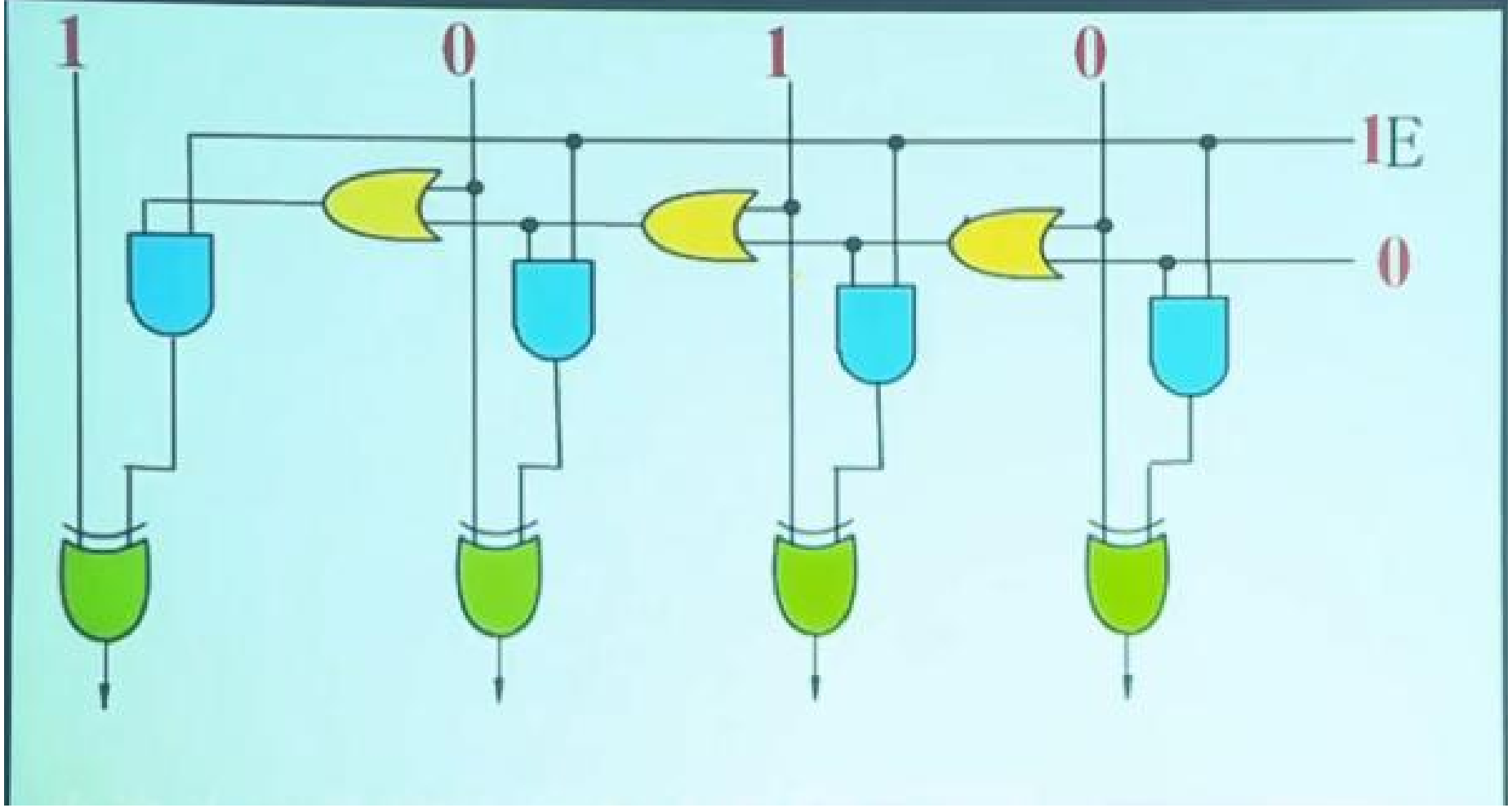
At this point, we have built a perfect one-bit adder, which we call it a full adder.

Adder - Signal calculation

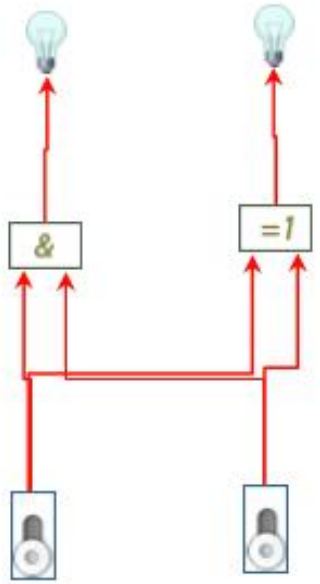



溢出
Sn-1
Sn-2
S1
S0
FA
FA
FA
FA
Cn
Cn-1
Cn-2
C2
C1
C0
M=0加
M=1减
方式控制M
Bn-1
An-1
Bn-2
An-2
B1
A1
B0
A0
符号位

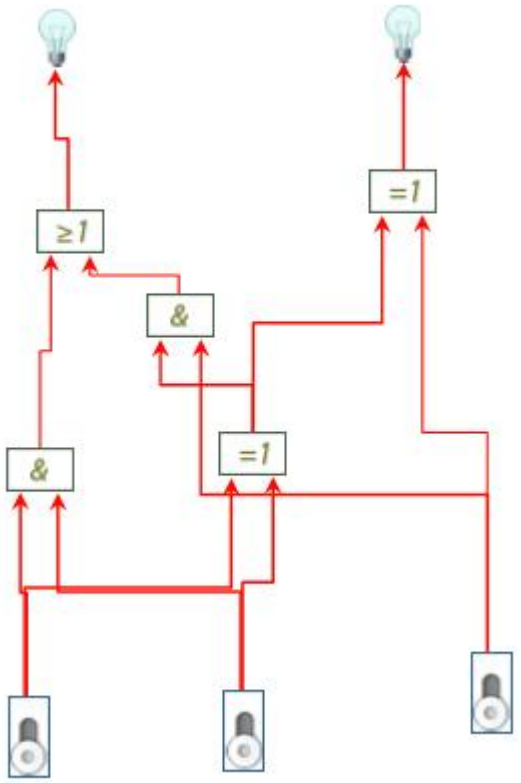
1010求补后为0110



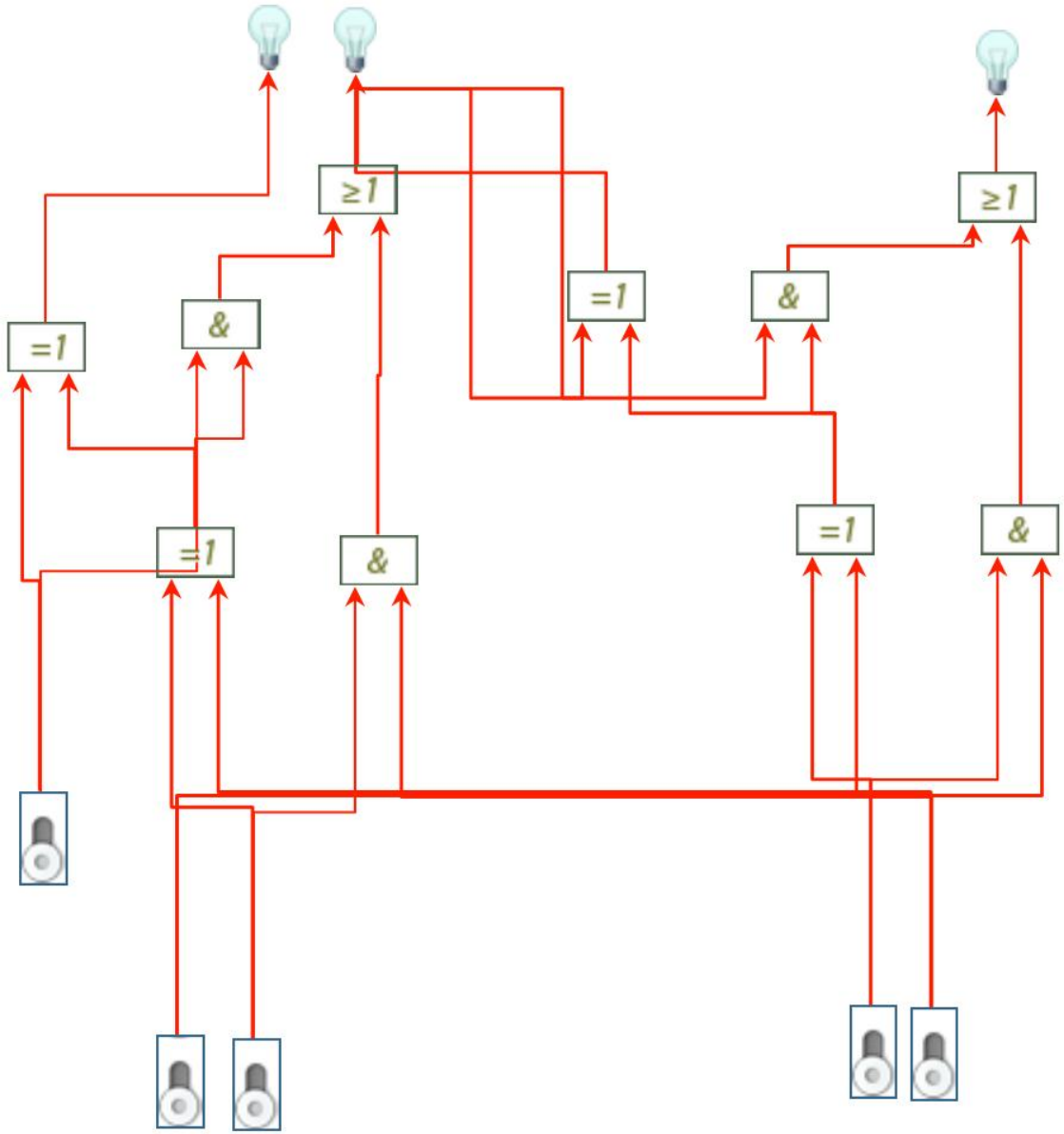
Half adder



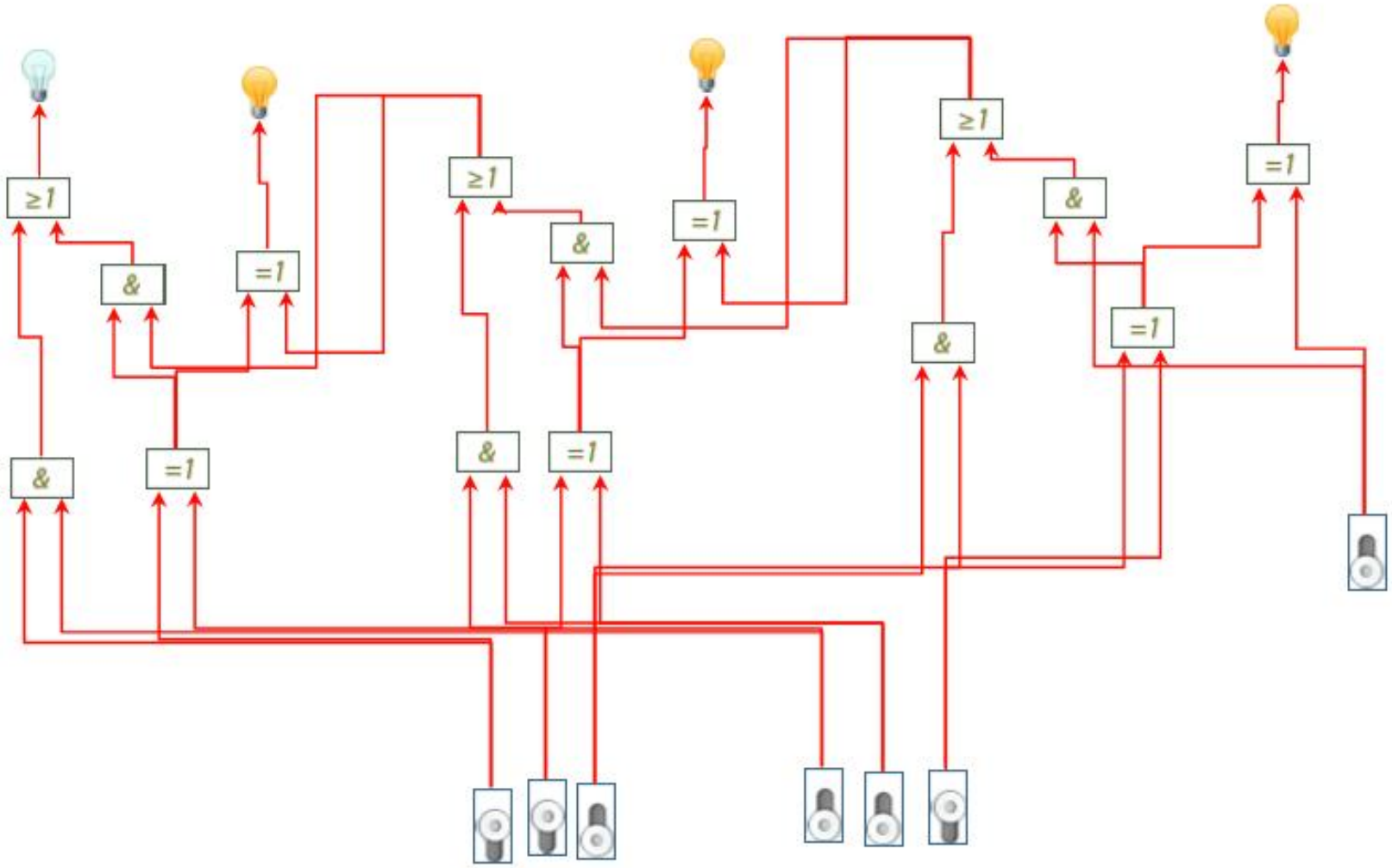
Full adder



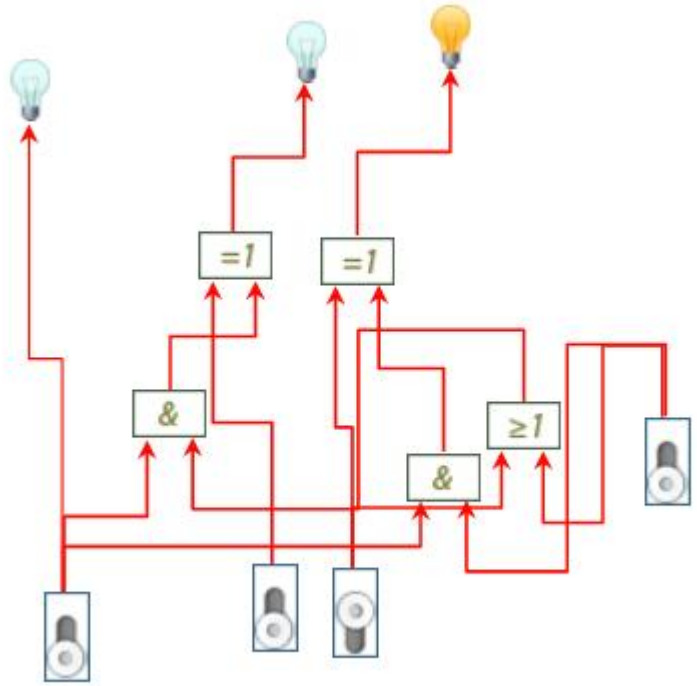
Two digits adder

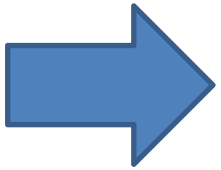


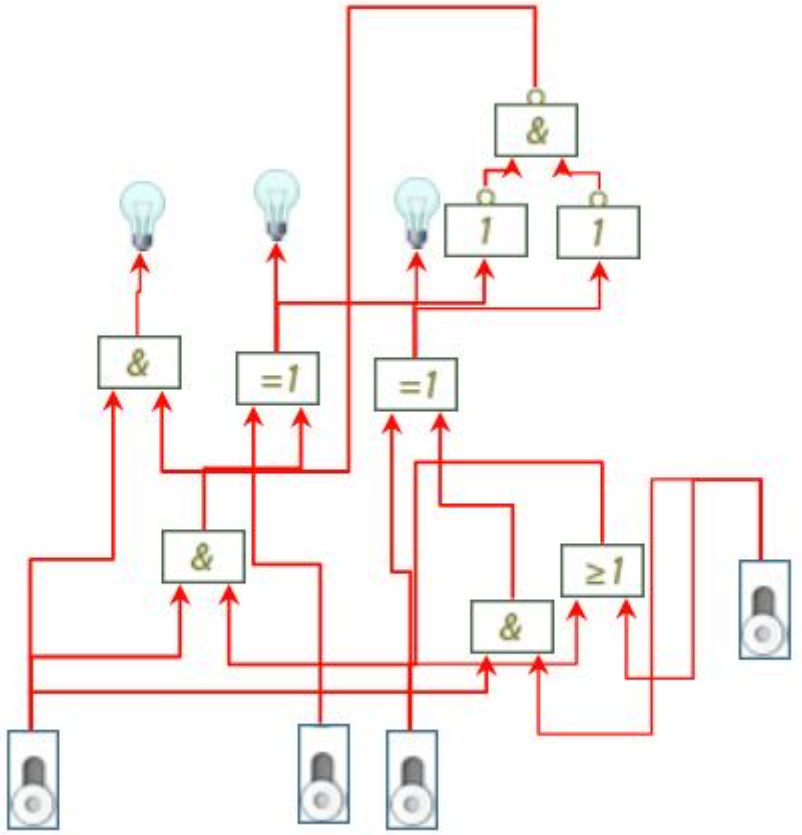
Three digits adder



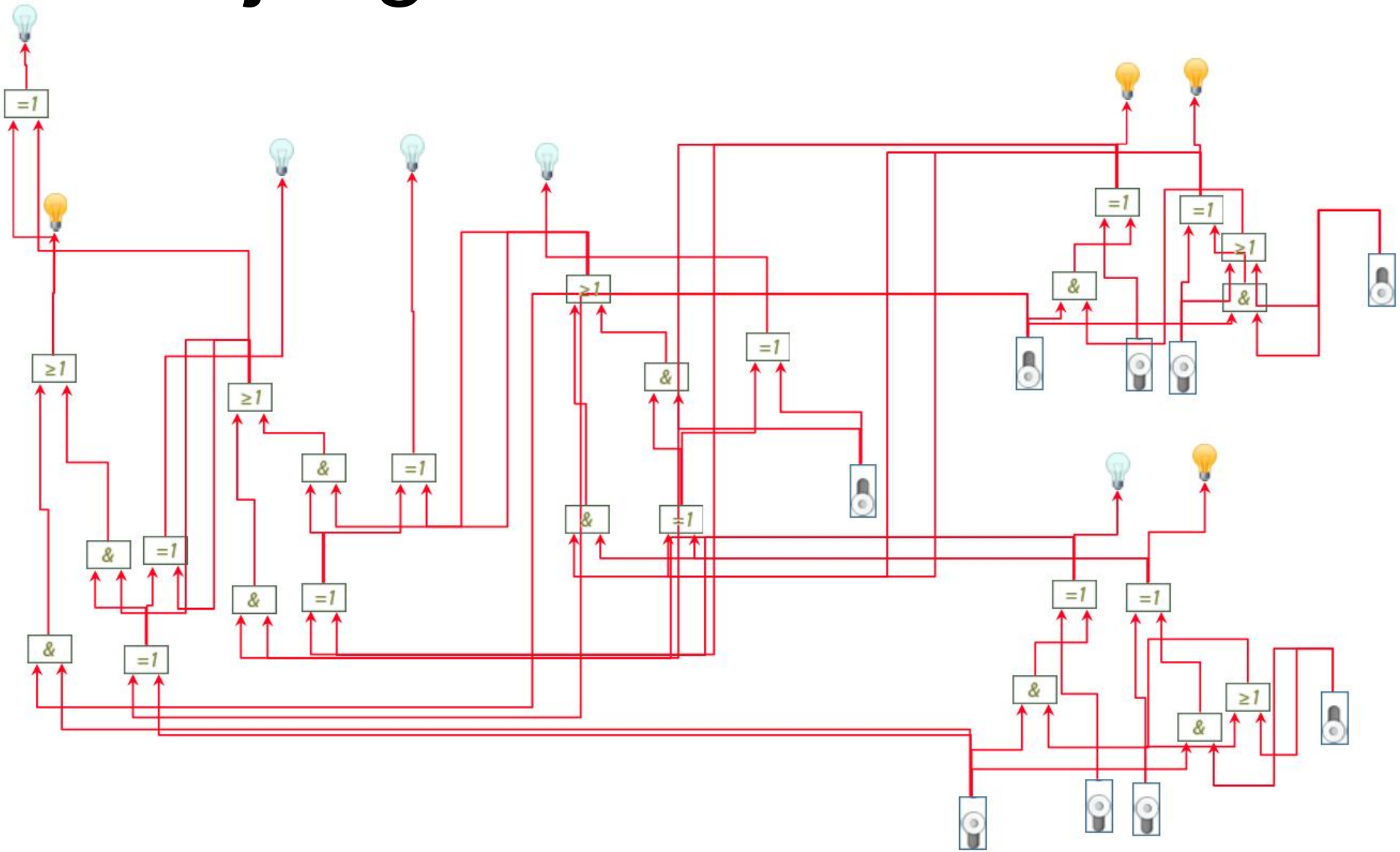
2’s complement







Adder – 2's Complement with overflow judgment



Adder – convert 2's into TF

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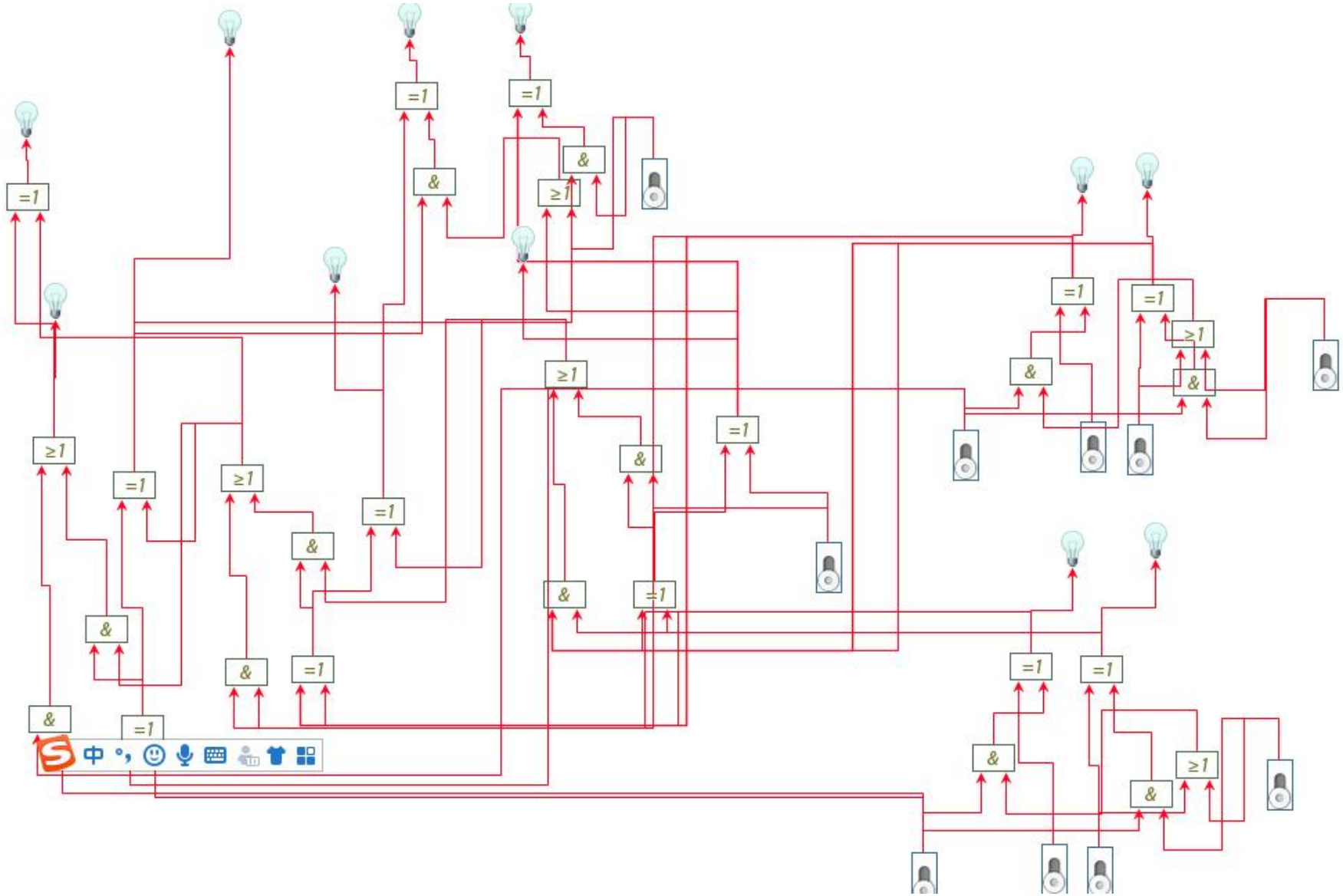

实验报告

包括：实验目的、实验原理、实验电路、实验步骤、

思考与分析（使用3位全加器构造出补码加法/减法。

输入为原码，转换为补码进行运算后再转回原码，

具有1位溢出判断位）