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Lab Index: LAB 3

DESIGN AND SIMULATION OF A 4-BIT ADDER USING IF-ELSE CLAUSES

- ## AIM

The objective of this experiment is to utilize VHDL to design and simulate a digital circuit that implements a Full Adder. By doing so, participants can grasp the concept of a Full Adder, become familiar with VHDL as a hardware description language, and develop practical skills in circuit design and analysis. The main goal is to successfully implement the Full Adder's functionality in VHDL, validate its accuracy through truth table analysis and waveform simulations, and acquire knowledge and experience in digital circuit design using VHDL.

- ## ABSTRACT

In this lab report, we present the VHDL implementation of a Full Adder. The Full Adder is a crucial component in digital circuits as it performs addition on binary numbers, considering both a carry-in and a carry-out. Implementing the Full Adder in VHDL enables a comprehensive understanding of its behavior and functionality. This report offers a detailed overview of the lab session, including the methodology, results, and discussions, with a focus on the truth table and waveform simulations. The report concludes by summarizing the key insights gained from the lab.

- ## INTRODUCTION

VHDL (Very High-Speed Integrated Circuit Hardware Description Language) is a hardware description language used for modeling and designing digital systems. It provides a means to describe the behavior and structure of digital circuits, enabling the simulation and synthesis of complex systems. This lab report specifically concentrates on the implementation of a Full Adder using VHDL.

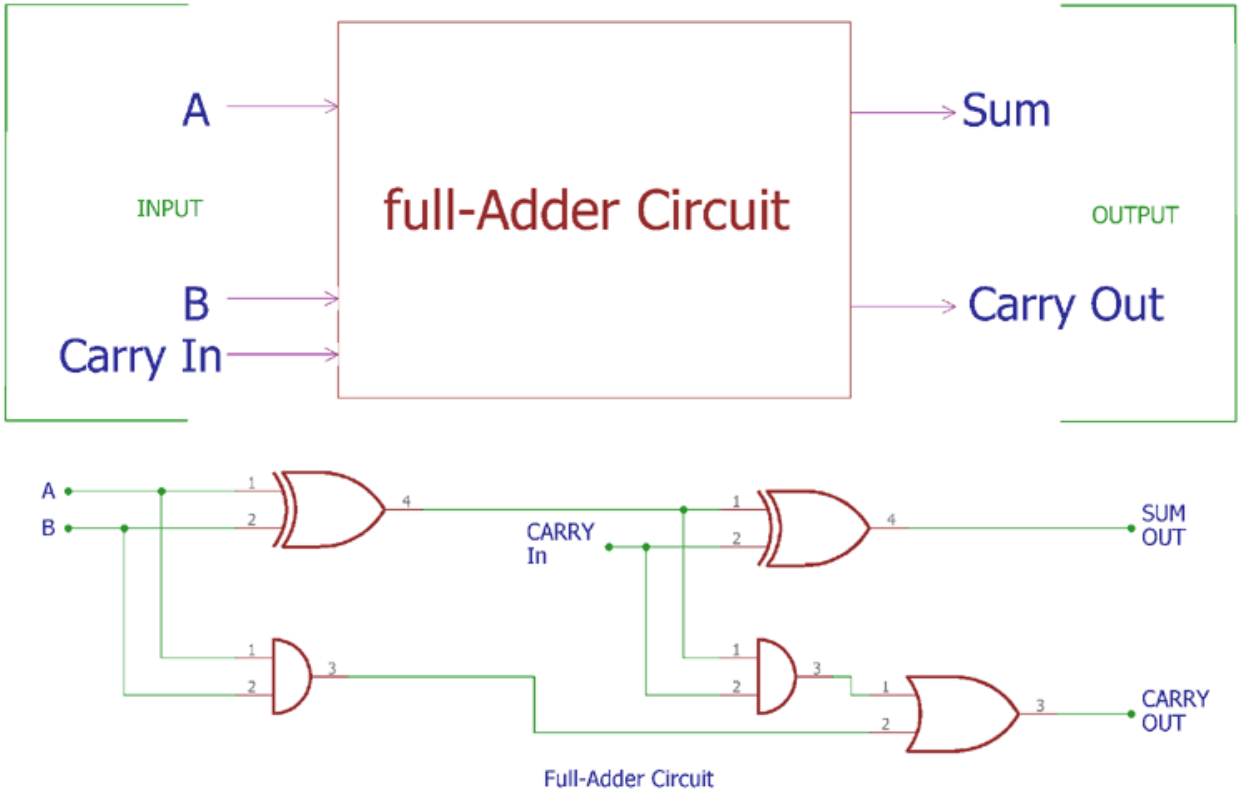
The lab session revolves around comprehending the concept and significance of a Full Adder in digital circuits. The Full Adder performs binary addition on three inputs: A, B, and Cin (carry-in), resulting in two outputs: Sum and Cout (carry-out). By implementing the Full Adder using VHDL, we gain insights into its functionality and behavior.

- ## METHODOLOGY

The VHDL implementation of the Full Adder follows an entity-architecture structure. The entity declaration specifies the input and output ports of the Full Adder. In this instance, the inputs are A, B, and Cin, and the outputs are Sum and Cout. The ports utilize the STD_LOGIC datatype.

The architecture segment of the VHDL code defines the functionality of the Full Adder. It includes a process block that analyzes the input combinations and assigns the corresponding values to the outputs. Within the process block, if-else statements are used to examine all possible combinations of input values and determine the appropriate output values.

a. **Block diagram of entity showing port terminals and datatype:** The block diagram of the entity for the simple full adder is as follows:



In the block diagram, the input ports A, B, and Cin are connected to the Full Adder, while the output ports Sum and Cout are generated by the Full Adder.

The datatypes used for the port terminals in this implementation are assumed to be STD_LOGIC in VHDL. The STD_LOGIC type is commonly used to represent digital signals in VHDL, where '0' represents logic low (0) and '1' represents logic high (1).

Therefore, the block diagram shows the input ports A, B, and Cin connected to the Full Adder, and the output ports Sum and Cout generated by the Full Adder, all using the STD_LOGIC datatype.

b. **Explanation of the architecture**

The "Behavioral" architecture in the VHDL implementation of the Full Adder defines its internal logic and behavior. It comprises a process block that evaluates the input combinations and determines the corresponding output values. The process block is sensitive to changes in the inputs A, B, and Cin.

Within the process block, if-else statements are utilized to examine all possible combinations of the input values. Each combination represents a specific condition, and based on these conditions, the process block assigns the appropriate output values.

For instance, if the inputs A, B, and Cin are all '0', the if-else statements in the process block identify this condition and set the output values Sum and Cout to '0' and '0', respectively. Similarly, for other input combinations, the process block calculates the correct output values using if-else statements.

By employing if-else statements, the architecture handles all possible input combinations and accurately computes the sum (Sum) and carry-out (Cout) of the Full Adder.

In summary, the Behavioral architecture offers a behavioral-level representation of the Full Adder, specifying its input-output relationship and the conditional logic required to perform binary addition.

- ## RESULTS AND DISCUSSION

To depict the anticipated outputs for all conceivable input combinations, the truth table of the 4-bit adder can be created. It incorporates the inputs A, B, and Cin, as well as the outputs Sum and Cout. Here is the representation of the truth table:

The truth table serves to showcase the expected outputs for each unique combination of inputs A, B, and Cin, effectively illustrating the logical behavior of the 4-bit adder.

Truth table

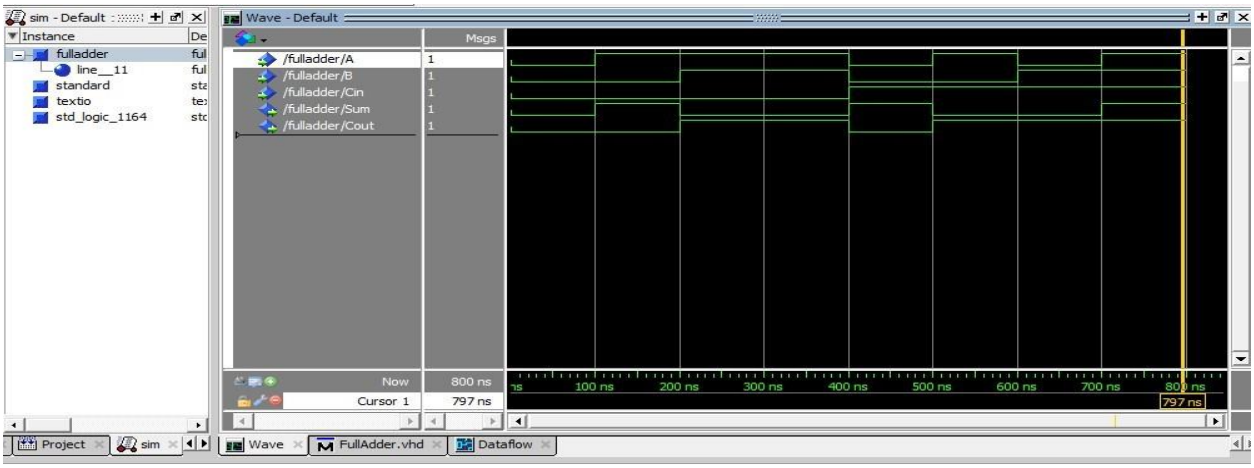
Cin	B	A	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Waveform Simulation

The waveform simulations of the logic gates were conducted using ModelSim.

Signal values were forced through the input terminals, and the resulting waveforms at the output terminals were observed.

The waveforms exhibited the expected behavior of each logic gate, validating the correctness of the designs.



Comparison of Truth Tables and Simulation Results:

The simulation results matched the expected truth tables for each logic gate.

The outputs of the logic gates corresponded to the specified truth table values for all input combinations.

The comparison confirmed the accuracy of the VHDL implementations.

- **CONCLUSION**

In conclusion, the lab session focusing on the implementation of a Full Adder using VHDL has been highly informative and advantageous. By successfully designing and simulating the Full Adder, we have deepened our comprehension of VHDL and its practical application in digital circuit design. The Full Adder plays a vital role in digital systems, enabling binary addition with carry-in and carry-out capabilities.

The results obtained from the lab, including the truth table and waveform simulations, have confirmed the accuracy of the Full Adder implementation. The outputs generated by the simulations align precisely with the expected values, demonstrating that the VHDL code effectively represents the behavior of the Full Adder.

Throughout this lab, we have acquired the skills to describe digital circuits using VHDL and apply this knowledge to real-world designs. This expertise can be further expanded to more intricate circuit designs, empowering us to create and analyze digital systems with multiple components.

Overall, this lab has provided invaluable hands-on experience in VHDL programming and digital circuit design. The implementation of the Full Adder serves as a fundamental building block for more advanced digital systems. By mastering VHDL and comprehending the principles underlying the Full Adder, we are better prepared to tackle future projects related to digital circuitry and design.