

KEY M

congatec Application Note

Affected Products	All products
Subject	M.2™ Pinout Descriptions and Reference Designs
Confidential/Public	Public
Author	SDA

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
1.0	2020-01-28	SDA	First release

Preface

This application note provides the pinout description, reference design and design notes for each of the three M.2™ sockets commonly implemented on embedded systems (Socket 1 – Key E, Socket 2 – Key B, and Socket 3 – Key M).

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Symbols

The following are symbols used in this application note.



Note

Notes call attention to important information that should be observed.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Warning

Warnings indicate that personal injury can occur if the information is not observed.

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1 Introduction

This application note provides the pinout description, reference design, and design notes for three M.2™ sockets and respective interfaces commonly used on embedded systems:

- Socket 1 – Key E (Section 2 of this application note)
- Socket 2 – Key B (Section 3 of this application note)
- Socket 3 – Key M (Section 4 of this application note)

Additional information is provided for sockets with configuration pins.

For information about less commonly used sockets and respective interfaces (e.g. SDIO, I2S, UART), refer to the PCI Express M.2 Specification available for purchase from PCI-SIG (<https://pcisig.com>).



Note

The content of this application note is based on the PCI Express M.2 Specification Revision 3.0, Version 1.2.

2 Socket 1 – Key E

2.1 Pinout Description

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/1.8 V)	GND	63
60	I2C_CLK (O)(0/1.8 V)	RESERVED/PETn1	61
58	I2C_DATA (I/O)(0/1.8 V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX_TXD (O)(0/1.8V)	REFCLKn0	49
46	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART TXD (O)(0/1.8V)	GND	33
Key E		Key E	
Key E		Key E	
Key E		Key E	
Key E		Key E	
Key E		SDIO RESET#/TX_BLANKING (O)(0/1.8V)	23
22	UART RXD (I)(0/1.8V)	SDIO WAKE# (I)(0/1.8V)	21
20	UART WAKE# (I)(0/3.3V)	SDIO DATA3(I/O)(0/1.8V)	19
18	GND	SDIO DATA2(I/O)(0/1.8V)	17
16	LED_2# (I)(OD)	SDIO DATA1(I/O)(0/1.8V)	15
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA0(I/O)(0/1.8V)	13
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
10	PCM_SYNC/I2S WS (I/O)(0/1.8V)	SDIO CLK/SYSClk (O)(0/1.8V)	9
8	PCM_CLK/I2S SCK (I/O)(0/1.8V)	GND	7
6	LED_1# (I)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

2.2 Reference Design

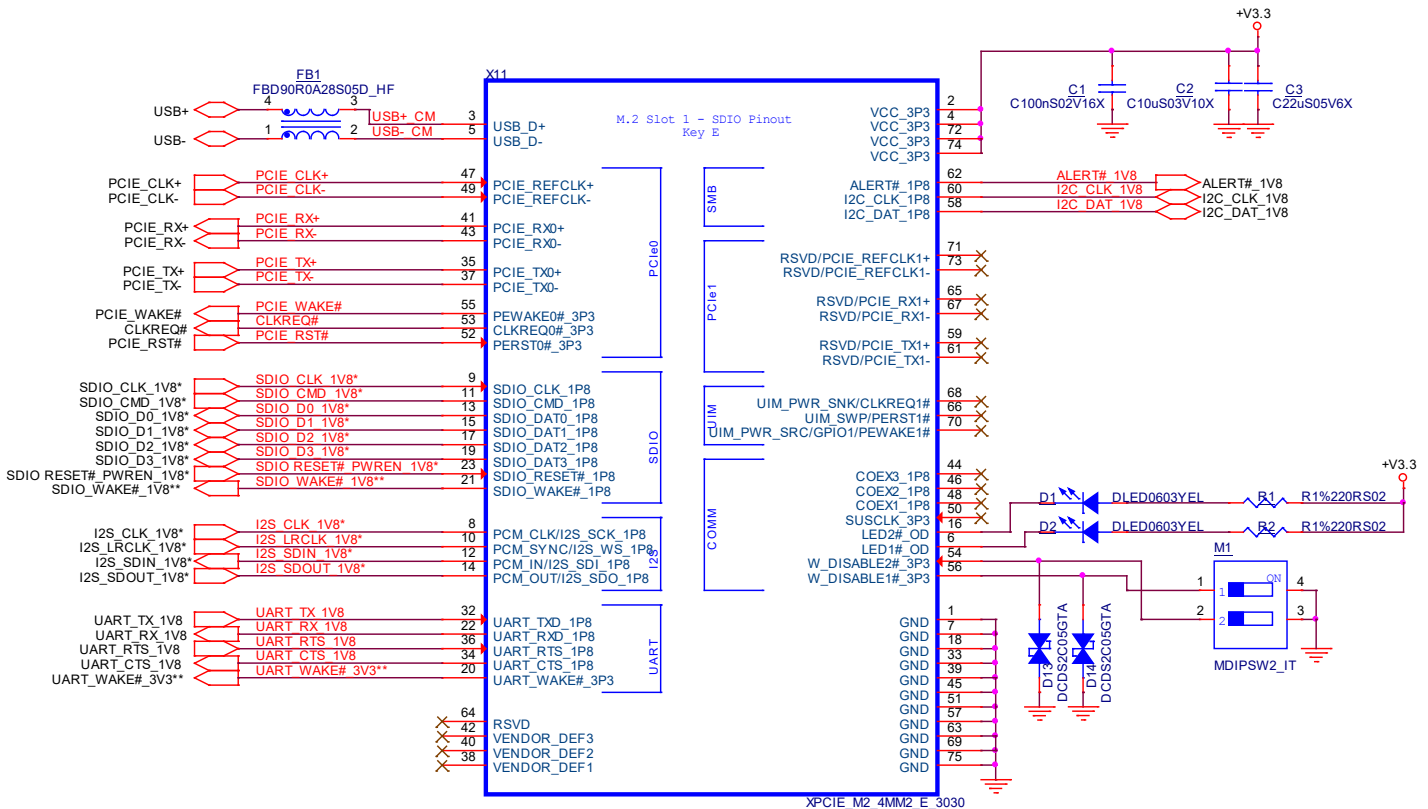


Figure 1: Socket 1 - Key E Reference Design

2.3 Design Notes

The reference design above (Figure 1) shows an M.2 Socket 1 – Key E used for connectivity applications. M.2 WiFi/Bluetooth expansion cards are usually connected via PCIe and USB. Other buses (e.g. SDIO and I2S) may not be supported by the COM.

The AC coupling capacitors are placed on the COM for the PCIe_TX+/- signals and for the PCIe_RX+/- signals on the M.2 expansion card. Therefore, it is not required to place AC coupling capacitors on the carrier board.

The M.2 clock request signal (CLKREQ#) enables the PCIe reference clock and should be connected to the output enable pin of the PCIe clock buffer. As the CLKREQ# signal is an active low, open drain output of the M.2 expansion card, a pull-up resistor is required on the carrier board.

3 Socket 2 – Key B

3.1 Pinout Description

74	3.3 V/VBAT	CONFIG_2	75
72	3.3 V/VBAT	GND	73
70	3.3 V/VBAT	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	CONFIG_1	69
66	SIM DETECT (O)	RESET# (O)(0/1.8V)	67
64	COEX_RXD (I)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
62	COEX_TXD (O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
58	NC	ANTCTL0 (I)(0/1.8V)	59
56	NC	GND	57
54	PEWAKE# (I/O)(0/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/3.3V)	REFCLKn	53
50	PERST# (O)(0/3.3V)	GND	51
48	GPIO_4 (I/O)(0/1.8V)	PETp0/SATA-A+	49
46	GPIO_3 (I/O)(0/1.8V)	PETn0/SATA-A-	47
44	GPIO_2 (I/O)/ALERT# (I)/(0/1.8V)	GND	45
42	GPIO_1 (I/O)/SMB_DATA (I/O)/(0/1.8V)	PERp0/SATA-B-	43
40	GPIO_0 (I/O)/SMB_CLK (I/O)/(0/1.8V)	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	UIM-PWR (I)	PETp1/USB3.1-Tx+/SSIC-TxP	37
34	UIM-DATA (I/O)	PETn1/USB3.1-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3.1-Rx+/SSIC-RxP	31
28	GPIO_8 (I/O) (0/1.8V)	PERn1/USB3.1-Rx-/SSIC-RxN	29
26	GPIO_10 (I/O) (0/1.8V)	GND	27
24	GPIO_7 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
22	GPIO_6 (I/O)(0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
20	GPIO_5 (I/O)(0/1.8V)	CONFIG_0	21
Key B		Key B	
Key B		Key B	
Key B		Key B	
Key B		Key B	
Key B		GND	11
10	GPIO_9/DAS/DSS (I/O)/LED_1# (I)(0/3.3V)	USB_D-	9
8	W_DISABLE1# (O)(0/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (O)(0/1.8V or 3.3V)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3	1

3.1.1 Host Interface Configuration

The four CONFIG_X pins select the intended host interface. The system shall read all four configuration pins to identify the selected pinout configuration. The system shall pull-up these configuration pins to an appropriate power rail so the configuration pins can be read even if the M.2 expansion card is not powered.

The table below shows how the CONFIG_X pins are connected on the M.2 expansion card to select the required host interface:

CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Host Interface
0	0	0	0	SSD - SATA
0	1	0	0	SSD - PCIe
0	0	1	0	WWAN – PCIe (Port Configuration 0*)
0	1	1	0	WWAN – PCIe (Port Configuration 1*)
0	0	0	1	WWAN – PCIe, USB3.1 Gen1 (Port Configuration 0*)
0	1	0	1	WWAN – PCIe, USB3.1 Gen1 (Port Configuration 1*)
0	0	1	1	WWAN – PCIe, USB3.1 Gen1 (Port Configuration 2*)
0	1	1	1	WWAN – PCIe, USB3.1 Gen1 (Port Configuration 3*)
1	0	0	0	WWAN – SSIC (Port Configuration 0*)
1	1	0	0	WWAN – SSIC (Port Configuration 1*)
1	0	1	0	WWAN – SSIC (Port Configuration 2*)
1	1	1	0	WWAN – SSIC (Port Configuration 3*)
1	0	0	1	WWAN – PCIe (Port Configuration 2*)
1	1	0	1	WWAN – PCIe (Port Configuration 3*)
1	0	1	1	WWAN – PCIe, USB3.1 Gen1 (vendor defined)
1	1	1	1	No Add-in Card Present



Note

*** Refer to the PCI Express M.2 Specification for different port configurations.**

3.2 Reference Design

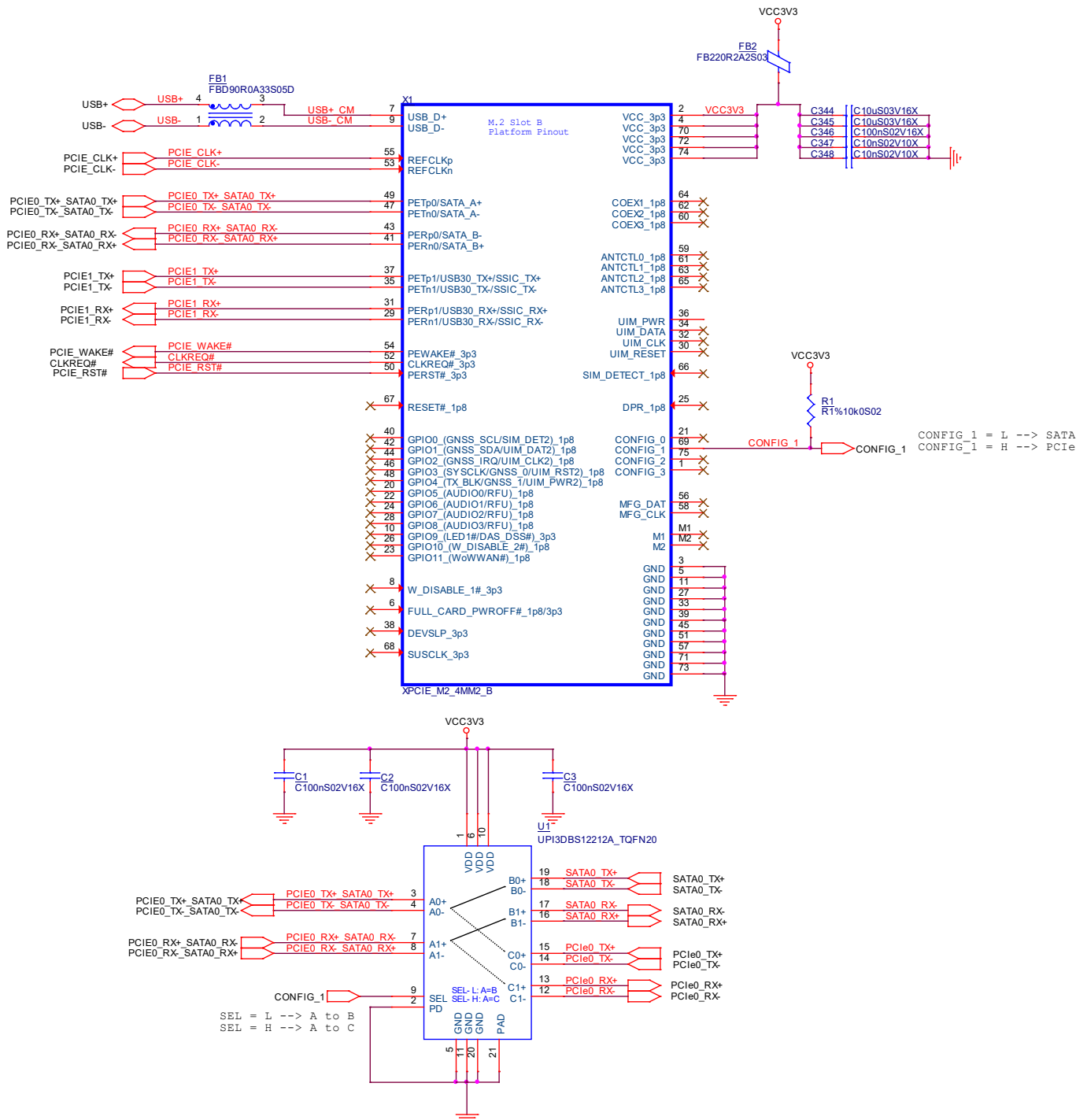


Figure 2: Socket 2 - Key B Reference Design

3.3 Design Notes

The reference design above (Figure 2) shows an M.2 Socket 2 – Key B used to connect PCIe or SATA based storage devices.

CONFIG_1 pin enables the appropriate host interface:

- CONFIG_1 low enables SATA
- CONFIG_1 high enables PCIe

The second PCIe lane enables support for PCIe x2 devices like Intel Optane memory. For PCIe x2 support, the PCIe lanes must be configured to a PCIe x2 link.



Note

As the CONFIG_1 signal is not connected on the M.2 expansion card when PCIe is enabled, a pull-up resistor is required on the carrier board.

If the M.2 socket is used for a SATA based storage device, pin 43 must be connected to the negative signal of the differential pair used for SATA Rx.

If the M.2 socket is used for a PCIe based storage device, pin 43 must be connected to the positive signal of the differential pair used for PCIe Rx.

4 Socket 3 – Key M

4.1 Pinout Description

74	3.3 V	GND	75
72	3.3 V	GND	73
70	3.3 V	GND	71
68	SUSCLK (O)(0/3.3V)	PEDET	69
	Key M	NC	67
	Key M	Key M	
	Key M	Key M	
	Key M	Key M	
	Key M	Key M	
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or NC	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or NC	GND	51
50	PERST# (O)(0/3.3V) or NC	PETp0/SATA-A+	49
48	NC	PETn0/SATA-A-	47
46	NC	GND	45
44	ALERT# (I) (0/1.8V)	PERp0/SATA-B-	43
42	SMB_DATA (I/O) (0/1.8V)	PERn0/SATA-B+	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	DEVSLP (O)	PETp1	37
36	NC	PETn1	35
34	NC	GND	33
32	NC	PERp1	31
30	NC	PERn1	29
28	NC	GND	27
26	NC	PETp2	25
24	NC	PETn2	23
22	NC	GND	21
20	NC	PERp2	19
18	3.3 V	PERn2	17
16	3.3 V	GND	15
14	3.3 V	PETp3	13
12	3.3 V	PETn3	11
10	DAS/DSS (I/O)/LED_1# (I)(0/3.3V)	GND	9
8	NC	PERp3	7
6	NC	PERn3	5
4	3.3 V	GND	3
2	3.3 V	GND	1

4.2 Reference Design

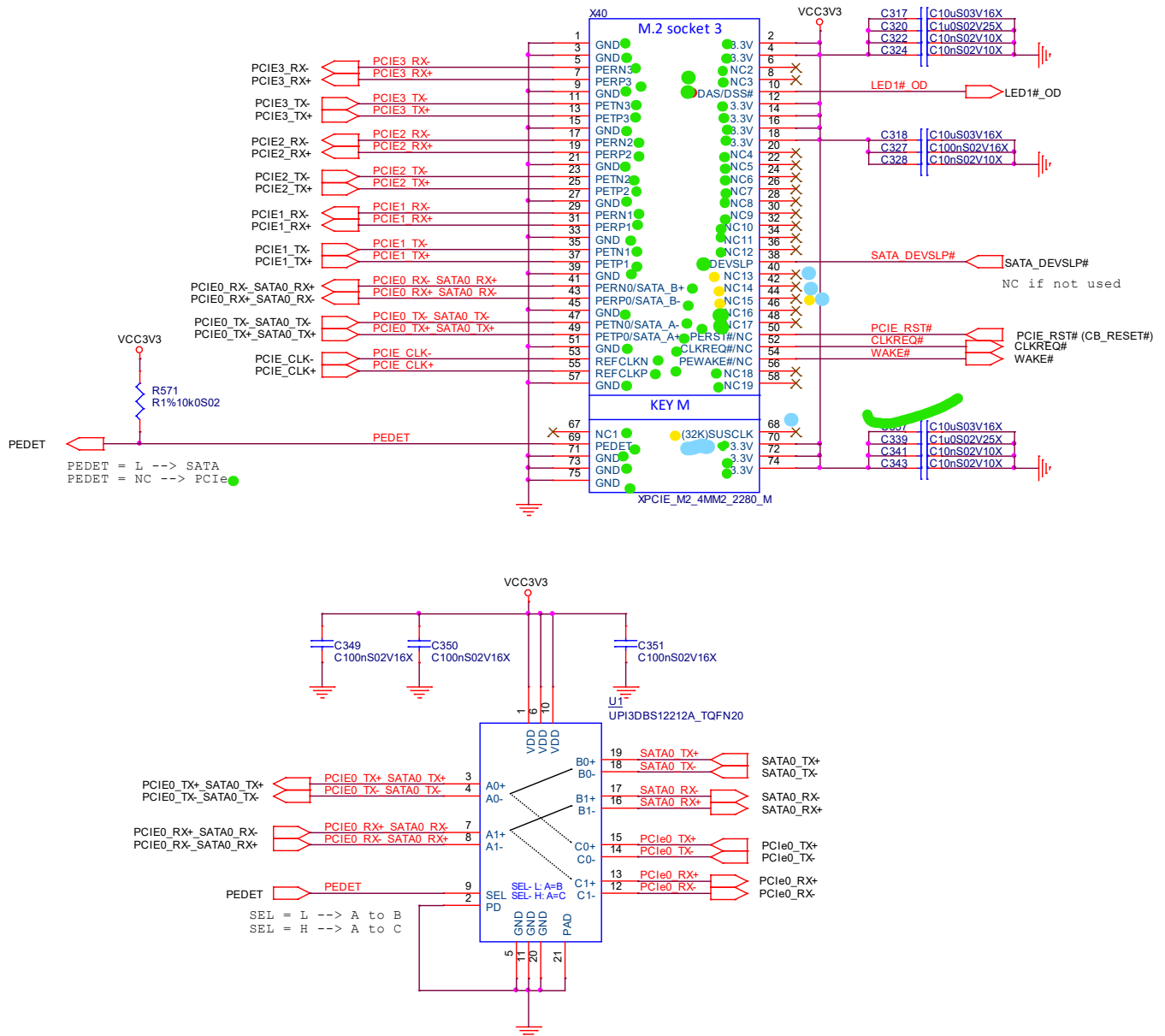


Figure 3: Socket 3 - Key M Reference Design

4.3 Design Notes

The reference design above (Figure 3) shows an M.2 Socket 3 – Key M used to connect PCIe or SATA based storage devices.

The PEDET signal enables the appropriate host interface. The M.2 expansion card connects the PEDET signal accordingly:

- PEDET low enables SATA (M.2 expansion card connects PEDET signal to GND)
- PEDET high enables PCIe (PEDET signal not connected on M.2 expansion card)

For maximum bandwidth, combine the four PCIe lanes to a x4 link.



Note

As the PEDET signal is not connected on the M.2 expansion card when PCIe is enabled, a pull-up resistor is required on the carrier board.

If the M.2 socket is used for a SATA based storage device, pin 43 must be connected to the negative signal of the differential pair used for SATA Rx.

If the M.2 socket is used for a PCIe based storage device, pin 43 must be connected to the positive signal of the differential pair used for PCIe Rx.