Hydra Hardware Design Notebook

|  |  |
| --- | --- |
| Rocket: | Gee-Force One |
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| Sub Team: | Avionics |
| Point of Contact: | Serban, Amanda, Liam |
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|  |  |  |
| --- | --- | --- |
| Revision | Description | Date |
| 0 | Baseline updated (Hydra V1) | Feb 1, 2023 |
| 1 | Updated design following first design review | Feb 11, 2023 |

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# Hydra V1

## Recovery Board (HYDRA\_V1\_RECOVERY)

### Overview

The Hydra V1 recovery board uses two RRC3 COTS recovery devices in tandem with two independent 9V batteries for power. As such, its only purpose is to add safety power disconnect switches and locking connectors for the batteries as well as the ejection wiring.

### Component List

Table 1. Hydra V1 Recovery Board Component List

|  |  |  |  |
| --- | --- | --- | --- |
| Part # | QTY | Purpose | Comment |
| PRT-12790 | 2 | Inter-board header | Standard component for all Hydra Boards |
| 172298-1104 | 2 | Recovery wiring connector | Chosen for locking ability and excessive current rating. Vertical connectors are preferred to limit the amount of space required by the connector on the PCB. |
| 43045-0402 | 1 | Battery connector | Chosen for locking ability and high current capacity. Horizontal connectors are preferred here since the battery wiring will be coming from the bottom of the stack and this board is at the top. |
| RRC3 | 2 | Recovery device | Idk, I was told to use these by people with more *influence* than I. |
| SS-5GL2D | 2 | Safety switch | Chosen for high current capacity and rocket mechanism which functions well with rod protruding from rocket. |

### Layout Considerations

This board is relatively simple, the power comes in as two separate sets of wires through the 4-pin 43045-0402 connector (J3) at which point the positive terminal of each separate set of wires goes to its corresponding RRC3 and the ground terminal goes to a SS-5GL2D switch. Two SS-5GL2D switches (SW1 and SW2) are used, one per RRC3 (U1 and U2), to keep the devices entirely independent from each other. The RRC3s have their power switch terminals shorted (pins 7 and 8) as the external SS-5GL2D switch takes care of toggling power delivery. We are using low-current e-matches so the 9V batter will suffice to ignite them no secondary battery is required thus there are only two safety switches on the board.

The ejection signals are sent out from two 172298-1104 headers (J4 and J5) on either side of the top half of the recovery board. These connectors are vertical since the structural element holding the GPS and RFD900 antennas above the avionics stack in the rocket is shaped to allow components to protrude vertically in those locations. Furthermore, lateral clearance was limited on the PCB.

All traces on the PCB are 2mm wide. Considering a board thickness of 0.03566mm, they should allow 2A of throughput however the RRC3 can output a maximum of 3A before damaging itself[1] and so all traces are mirrored on both sides of the board for a total current capacity of 4A. Some traces are wider at 2.5 or 3mm however we will consider the current limit to be 4A.

### Schematics

Diagram, schematic

Description automatically generated

Figure 1‑1. Hydra V1 Recovery Board Schematic

### PCB

A picture containing text, clock

Description automatically generated

Figure 1‑2. Hydra V1 Recovery Board PCB Layout (traces are mirrored on both sides)

## Communication Board (HYDRA\_V1\_COMMUNICATION)

### Overview

V1/V2 communication board skipped for financial reasons. Team is shifting directly to V3 board which includes an MCU to input telemetry directly to the CAN bus. The V3 board will include ‘bypass’ traces to connect the RFD900’s UART to the left header’s UART bus which can be severed when we implement the V3 circuitry.

## Logic Board (HYDRA\_V1\_LOGIC)

### Overview

The logic board is the most complex board of the Hydra V1 stack as it houses the sole MCU within the system. Its purpose is to process data generated by the SBG and log it to the onboard SD card while simultaneously transmitting it through the left header’s UART bus which goes directly to the RFD900 on the communication board. Overall, the board consists of a SAM E51 MCU, the SBG, an SD card, a CAN transceiver, a buzzer, and a set of status LEDs.

We elected to interface the SD card through SPI on SERCOM 4 as opposed to using one of the SAM E51’s integrated SDHC controllers to alleviate some load on the software side since SDHC controllers are overly complex for our purposes. Future iterations of this board may utilize a SDHC controller or another form of data storage entirely however we are keeping things simple for the time being.

#### SERCOM Pinouts

SERCOM pinouts are determined as per datasheet specifications; the datasheet has a section for each protocol (SERCOM SPI, SERCOM I2C, and SERCOM USART) in which there are I/O tables under the “Register Description” section. For SPI, these are called “Data In Pinout” (DIPO) and “Data Out Pinout” (DOPO) whereas for UART they are called “Transmit Data Pinout” (TXPO) and “Receive Data Pinout” (RXPO). For I2C just go to section 36.4. These tables specify which SERCOM pads can serve which purposes for a given protocol. The purpose assigned to each SERCOM pad is tabulated below:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Protocol[#] | SERCOM # | PAD # | MCU Pin | Function |
| SBG | UART[0] | 5 | 0 | PB02 | TX |
| 1 | PB03 | RX |
| SD Card | SPI[0] | 4 | 0 | PB12 | MOSI |
| 1 | PB13 | SCK |
| 2 | PB14 | CS |
| 3 | PB15 | MISO |
| General Purpose I/O | UART[1] | 2 | 0 | PA09 | TX |
| 1 | PA08 | RX |
| SPI[1] | 0 | 0 | PA04 | MISO |
| 1 | PA05 | SCK |
| 2 | PA06 | CS |
| 3 | PA07 | MOSI |
| I2C[0] | 1 | 0 | PA16 | SDA |
| 1 | PA17 | SCL |

#### Parent Schematic Considerations (Connectors.SchDoc)

This schematic offers a block-diagram view of how the logic board functions. The MCU, SBG, and SD card schematics are included as sub-schematic components. The CAN transceiver is included here as there was no room in the MCU\_PINOUT.SchDoc schematic. It uses a voltage divider on the RxD line since the CAN transceiver operates at 5V whereas the MCU operates at 3.3V. **Important note: UART lines (Tx/Rx) cross over (Tx goes to Rx on the receiving device and Rx goes to Tx) but CAN Tx/Rx lines DO NOT**. The CANH and CANL pins are defined as a differential pair such that Altium automatically ensures adequate routing.

P1 is a SWD JTAG programming header and conforms to the 10-pin JTAG pinout standard.

Finally, R23-R38 are included to provide pads on all the SERCOM lines in case they were connected wrong. Ideally, these pads will all be shorted however this provides us with the flexibility to rewire data bus lines on the fly ensuring the boards can be used for testing. These pads will not be included in the next iteration.

#### MCU Pinout Considerations (MCU\_PINOUT.SchDoc)

The inductors and capacitors connected to the MCU are chosen as per Figure 60-1 (p.1913) of its [datasheet](https://ww1.microchip.com/downloads/aemDocuments/documents/MCU32/ProductDocuments/DataSheets/SAM-D5x-E5x-Family-Data-Sheet-DS60001507.pdf). The two external crystals (Y1 and Y2) each have two capacitors between their pins and GND which were also chosen based on the MCU’s [datasheet](https://ww1.microchip.com/downloads/aemDocuments/documents/MCU32/ProductDocuments/DataSheets/SAM-D5x-E5x-Family-Data-Sheet-DS60001507.pdf) (Figure 60-9 and Figure 60-11 on p.1919 and p.1920, respectively) since the individual datasheets of each crystal did not define an ideal capacitance value.

The reset switch schematic conforms to Figure 60-7 of the [datasheet](https://ww1.microchip.com/downloads/aemDocuments/documents/MCU32/ProductDocuments/DataSheets/SAM-D5x-E5x-Family-Data-Sheet-DS60001507.pdf) and includes a RC-filter to reduce any parasitic inductance or other noise that may exist within the RESETN net as well as a pullup resistor (R39). **I’m realizing now that this RC filter should probably be placed close to the MCU and I did not do this so we should definitely fix this for V2. I only placed the capacitor (C6) close to the MCU which is likely acceptable but might as well move the resistor (R1) closer too.** Beyond this, the reset switches are OMRON dip switches which were chosen over simple momentary switches to prevent accidental actuation and ensure reliability.

The buzzer circuit uses a N-channel MOSFET (Q1) to drive the buzzer using a GPIO pin. R14 is a current-limiting resistor to prevent drawing excessive current from the MCU, R41 is a pull-down to ensure the MOSFET remains in its cut-off region when no input is provided, and R2 serves to discharge the piezo buzzer (LS1) since it acts as a capacitive load. A MOSFET was chosen since these are field-effect transistors and should not require much drive current.

Finally, two pullup resistors (R15, R16) are included on the I2C line as these are required by the endpoint of a I2C bus which may, at some point, be the logic board. These are not intended to be populated however they were included just in case a future application requires them.

#### SBG Considerations (SBG.SchDoc)

The SBG interfaces with the MCU using a MAX3232EUE+T UART to RS-232 converter since the SBG Ellipse2-N-G4A3-B1 can solely output serial data through RS-232 or RS-422 and, rather poetically, the SAM E51 solely has support for RS-485.

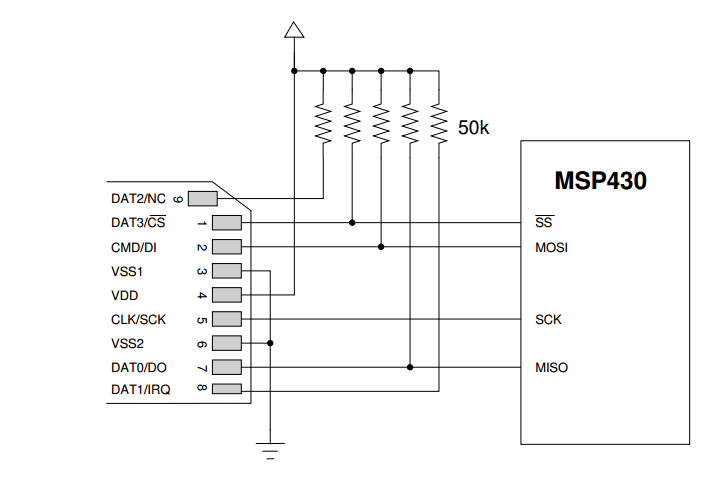
The MAX3232’s schematic is built according to the datasheet, with the capacitors (C15-C18) defined based on the 4.5-5.5V V­CC range in Table 2 (page 9) of its [datasheet](https://datasheet.ciiva.com/22828/0900766b810e26b2-22828277.pdf?src-supplier=Rs). The initial plan involved supplying the MAX3232 with 3.3V and using 100nF capacitors, as specified by the datasheet, but this was changed to ensure the MAX3232 could output +-5V on its RS-232 pins. As a result of powering the MAX3232 with 5V, it’s R1OUT pin which outputs UART to the MCU also functions at +-5V so a voltage divider was included to drop this to 3.3V (R17/R18) on the Rx pin. Finally, a decoupling capacitor (C14) is included between the MAX3232’s VCC pin and GND.

The SBG is connected directly to the 5V rail of the left header on this board and no additional power circuitry exists. Its connector (P2) is a separate component from the footprint to provide flexibility in its positioning relative to the SBG’s mounting holes since the mounting holes are fixed at the center of the board. In this case, the connector is placed close to the MAX3232 IC however its position may change with future iterations.

#### Diagram, schematic Description automatically generatedSD Card Considerations (SD.SchDoc)

The SD card circuit is built as a superposition of two SPI SD card shields. The first is the [DFRobot SD card shield](https://www.dfrobot.com/product-875.html) with a schematic as per figure to the right and the second is a generic [AliExpress SD card shield](https://www.aliexpress.com/item/1005001579168924.html) with a schematic as per the figure below. These two differ in schematics as the DFRobot shield is designed to operate at 5V whereas the AliExpress shield works directly on 3.3V which is what the SD card operates at.

Since the DFRobot shield is designed to operate at 5V, it contains a linear regulator to reduce the 5V supply voltage to 3.3V which is omitted in our design. Additionally, it includes voltage dividers on the data pins since it assumes the MCU’s data lines also operate at 5V. **I made a mistake here since I included a voltage divider on the MISO pin as opposed to the CS pin. This is not necessary since the MISO pin is an output of the SD card which will never exceed 3.3V. Luckily, we shouldn’t need these dividers at all and our CS should not exceed 3.3V so it’ll be ok. These dividers will most likely be removed in V2 since I doubt they provide any functionality.** This circuit was included in case we require voltage dividers of our own to fine tune the voltage levels delivered to the SD card.

The AliExpress shield simply has 10kOhm pullups on its MOSI, MISO, and SCK lines as well as on the SD card’s DAT1 and DAT2 pins. Since our MCU operates at 3.3V, the schematic below is all we should theoretically require. A decoupling capacitor (C19) is also included for the SD card.

### Component List

The following BOM has repeated Part # entries since the components are organized by subsystem such that their function can be described more accurately.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Part # | QTY | Purpose | Comment |
| HYDRA | PRT-12790 | 2 | Inter-board header | Standard components for all Hydra boards. |
| TSM-105-01-T-DV | 1 | JTAG header | Generic 2.54mm-pitch programming header |
| MCU + MCU power delivery | ATSAME51J18A-MFT | 1 | MCU | Contains a plethora of data transfer interfaces including two CAN buses which we require as well as a wealth of ADC-enabled pins. |
| NR6028T100M | 2 | 10uH power inductors for MCU supply rails | These components decouple various MCU power rails from the board-wide 3V3 rail. All chosen as per datasheet recommendation. |
| 1206ZD106KAT2A | 1 | 10uF decoupling capacitor |
| C0402C104K8PACTU | 6 | 100nF decoupling capacitors |
| GRM155R60J475ME47D | 1 | 4.7uF decoupling capacitor |
| ERA-3AEB102V | 1 | 1kOhm SWCLK pullup resistor | Used to pull up SWCLK pin of JTAG header as per datasheet recommendation |
| RC1206FR-0710KL | 2 | 10kOhm I2C pullup resistor | Pullup resistors are required at an I2C end point, included in case the logic board acts as an end point. |
| Clock crystals | ABM8-48.000MHZ-B2-T | 1 | 48MHz clock crystal | Chosen as per datasheet recommendation. |
| 08051A6R8CAT2A | 2 | 6.8pF decoupling capacitors |
| ECS-.327-12.5-1210-TR | 1 | 32.7680kHz clock crystal |
| C0805C180J5GACTU | 2 | 18pF decoupling capacitors |
| CAN | MCP2544FD-E/SN | 1 | CAN transceiver | Used to communicate with other HYDRA boards within the avionics stack. |
| C0402C104K8PACTU | 1 | 100nF decoupling capacitor | Decouples CAN transceiver from board-wide 5V rail. |
| CRCW12061K00FKEA | 1 | 1kOhm resistor | Voltage divider for CAN\_RX line to reduce voltage to the 3.3V that the MCU can accept. |
| CRCW12062K20FKEA | 1 | 2.2kOhm resistor |
| Status LEDs | LTST-C190GKT | 1 | Green status LED |  |
| TLMS1000-GS08 | 1 | Red status LED |  |
| LTST-C191TBKT | 1 | Blue power status LED | Turns on if board has power. |
| ERA8AEB331V | 3 | 330Ohm current limiting resistors for LEDs |  |
| Buzzer + amplifier | PS1240P02BT | 1 | Buzzer | Chosen for high sound output. Sole component connected to battery voltage on this board. |
| STD5N20LT4 | 1 | Buzzer amplifier MOSFET | MOSFET for amplifying a signal from the MCU to higher levels for the board’s buzzer. |
| CRCW12061K00FKEA | 2 | 1K current limiting and buzzer discharge resistors | R2 discharges LS1 (buzzer) when Q1 (amplifier) turns off, since LS1 acts as capacitive load. R14 limits gate current of Q1 from MCU pin (PA18). |
| RC1206FR-07100KL | 1 | 100K pull-down resistor | Ensures MOSFET is in cutoff region unless PA18 is providing voltage |
| SD card | 47219-2001 | 1 | SD card holder | Chosen for its hinged design that should hold the SD card more firmly than a traditional SD card holder. |
| CRCW12062K20FKEA | 3 | 2.1kOhm resistor | Act as voltage divider to lower SPI levels from MCU to lower signal voltages for the SD card. Used as per the DFRobot SD card shield schematic. |
| CRCW12061K00FKEA | 3 | 1kOhm resistor |
| ERJ3EKF1002V | 4 | 10kOhm pullup resistors | Used as per the AliExpress SD card shield schematic |
| C0402C104K8PACTU | 1 | Decoupling capacitor | Decouples SD card supply from board-wide 3V3 rail. |
| SBG + UART to RS-232 converter | SBG Ellipse2-N-G4A3-B1 | 1 | SBG sensor package | Provided by sponsor, contains accelerometer, barometer, gyroscope, magnetometer, and GPS as well as a common filter to ensure accurate sensor data. |
| MAX3232EUE+T | 1 | UART to RS-232 converter | Required since SBG uses RS-232 whereas MCU is only capable of UART. |
| C0402C104K8PACTU | 1 | Decoupling capacitor | Decouples MAX3232 from board-wide 5V rail. |
| GRM31CR71H475KA12L | 1 | 4.7uF capacitor | All four of these capacitors were chosen as per the MAX3232’s datasheet. |
| 12061C334KAZ2A | 3 | 330nF capacitor |
| Reset switch | A6H-2102 | 1 | Reset switch | Dip switch chosen instead of momentary to prevent accidental actuation on impact or from acceleration. |
| ERJ3EKF1002V | 1 | 10kOhm pullup resistor | Pulls up RESETN pin of MCU until dip switch closes at which point it limits current flow from the 3V3 rail to GND to 0.33mA. |
| C0402C104K8PACTU | 1 | 100nF filter capacitor | RC filter to prevent noise on the RESETN net. Capacitor also limits helps dampen current flow when SW1 closes and RESETN is pulled low. |
| ERJ-3EKF3300V | 1 | 330Ohm filter capacitor |

### Layout Considerations

The SBG needs to be along the rocket’s axis meaning that it had to be placed in the center of the board. The remaining components were molded around the SBG with the MCU being fitted in a relatively central location to allow as much access as possible to its pins. Each subsystem was built individually after which the subassemblies of components were aggregated together, as close as possible to the MCU. The MCU has a GND pad included below it because the VQFN package has a large ground plane to promote heat dissipation. The pad here serves the same purpose by promoting heat transfer with the board-wide GND plane.

The two exceptions to this rule are the SD slot and the buzzer that were mounted farther from the MCU. The SD slot was mounted farther to not interfere with the SBG’s footprint whereas the buzzer was mounted close to the V\_BATT pins of the right header since it is the sole component that requires V\_BATT.

The board has 4 layers to simplify the design process and allow more possibilities for future expansion as more features are added. The two intermediary layers are power planes for GND and 3V3 seeing as these are in high demand throughout the design. 5V is routed on the bottom layer through a thicker trace with the SBG’s connector being placed close to the left header since it draws the most power on this board. 5V power is then routed to the MAX3232 and the CAN transceiver.

The crystal layouts were kept close to the MCU such that the crystal’s traces remained as short as possible. Beyond this, the power and ground planes were removed below each crystal and the ground traces going to the capacitors were extended such that they reach a via just outside of the plane cutouts.

### Schematics

Chart, schematic

Description automatically generated

Figure 1‑3. Hydra V1 logic board hierarchy schematic

The schematic above includes the rough hierarchy for the MCU’s operation as well as the HYDRA board connectors and CAN transceiver. From the top right of the MCU and going clockwise, the MCU communicates with the SBG sub-schematic through UART, with the CAN transceiver using its onboard CAN controller, with the SD card using SPI, and with the UART, I2C, and SPI buses of the left header using their respective protocols. Finally, a SWD JTAG header is linked directly to the MCU’s pins as well as the board’s 3V3 and GND rails as per the standardized 10-pin JTAG pinout.

Diagram, schematic

Description automatically generated

Figure 1‑4. Hydra V1 logic board MCU pinout

The schematic above depicts the ATSAME51 to the left alongside its related power components with the exception of L2 and C13 which are included separately off to the top right of the MCU. The two crystals and reset switch are included next to the L2/C13 assembly. The status LEDs and RESET switch are included below the two crystals.

Diagram, schematic

Description automatically generated

Figure 1‑5. Hydra V1 logic board SBG pinout

The schematic above depicts the SBG alongside its UART to RS-232 converter that runs off of the board’s 5V rail. C15 through C18 were chosen as per the datasheet as depicted below for 4.5 < Vcc < 5.5 whereas C14 is a decoupling capacitor.

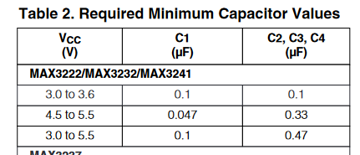


Figure 1‑6. MAX3232EUE+T datasheet recommended capacitor values

A picture containing chart

Description automatically generated

Figure 1‑7. Hydra V1 logic board SD card schematic

The SD card schematic includes three voltage divider pairs (R8/R7, R11/R10, R21/R20) alongside four pullup resistors (R6, R9, R19, R22) and a decoupling capacitor (C19).

### PCB

Schematic

Description automatically generated with medium confidence

Figure 1‑8. Hydra V1 logic PCB trace layout

Schematic

Description automatically generated

Figure 1‑9. Hydra V1 logic board 3D view

### Reflection

The following is a list of issues that should be fixed in the next iteration:

* Place reset switch RC filter closer to MCU
* Clear ground pad below MCU of silk screen (add to MCU part in Altium cloud?)
  + Ensure VIAs connecting this pad don’t have thermal reliefs
* Clean up SD card circuit
* Remove rewiring resistors where not needed
* Make whole top layer a ground pour
* Fix silkscreen
  + Make it readable
  + Omit certain component IDs but try to retain most
  + Add SBG outline to component
  + Add identifying text (place Altium project name and credits on PCB)
  + Add SBG logo (for picture I intend to send to SBG – Serban)
  + Label programming interface and each of the 3 status LEDs
* Make all components 0603s except decoupling capacitors which are 0402s
* Make buzzer MOSFET adequately sized à smaller
* Change SBG connector to something more sensible (not JST but maybe JST-SM?)
  + Molex might be best since we do have extras
    - Might not want this connector to be the same as ejection or power connectors to ensure the board is retard-proof
  + Also pay attention to vertical clearance, use right angled connector if possible pointing backwards towards rear wire channel of PCB stack
* Spread out components on PCB
  + Organize by system
  + Move MAX3232 and CAN transceiver away from MCU but keep power circuitry and crystals closeby
    - Not sure how long the traces can be between MCU and these ICs but it should be ok. Check with Simon or Seb or someone who knows what they’re doing before making these changes
  + Maybe at labelling text or some cool design on the board
* Move buzzer to PA19
* Change programming header to smaller size and fix programming pinout
* Add thermal pad to MCU footprint

## Power Board (HYDRA\_V1\_POWER)

### Overview

The first iteration of the power board is as barebones as possible and only includes a 3V3 regulator alongside a 5V regulator. Both of the power regulators receive power through a set of safety switches which interact with a rod protruding from the rocket’s body. This mechanism is redundant for Hydra V1 since the flight computer is not in charge of any flight functionality however it will be required with future Hydra versions.

Diagram

Description automatically generatedThe only circuit requiring explanation in this rendition of the power board is the reverse polarity protection included at the input. This circuit allows current to flow through Q1 when the polarity is correct since the GND power port will be ground and the MOSFETs drain (pin 4 of Q1) will be positive. In this configuration, the MOSFET’s body diode conducts current from the drain to the source (pin 3 of Q1). Additionally, R3 connects the ground power port to the MOSFET’s gate which pulls it low and excites the MOSFET such that it can conduct current in both directions. During a reverse polarity event, the MOSFET’s drain becomes negative whereas the GND power port becomes positive. This results in the gate (pin 1 of Q1) potential being higher than the source potential therefore shutting off the MOSFET and preventing current flow in both directions. The body diode will not conduct since it is oriented the wrong way and the MOSFET will prevent current flow in the other direction. The Zener diode (D3) prevents the voltage difference between the gate and source from ever exceeding 12V, during an overvoltage event for example, which could damage the MOSFET.

### Component List

Table 2. Hydra V1 Power Board Component List

|  |  |  |  |
| --- | --- | --- | --- |
| Part # | QTY | Purpose | Comment |
| C0805C103J5RACTU | 2 | 10nF 50V boost capacitor | Value based on datasheet[2]. Shared between both regulators since their datasheet both require identical values here. |
| B540C-13-F | 2 | 40V 5A Schottky Diode | Value based on datasheet[2]. |
| HSMG-C190 | 2 | Indicator LED | One used per regulator, these are arbitrarily chosen. |
| LM2677S-5.0/NOPB | 1 | 5V regulator | Chosen for simplicity of application circuit and high output current of 5A which is excessive for the Hydra V1. |
| 16TQC15M | 3 | 15uF 16V input surge capacitor | Number and value of capacitors used is based on datasheet[2]. |
| ANY | 1 | 470nF >15V 1812(4532) capacitor | Value based on datasheet[2]. |
| SRP6060FA-220M | 1 | 22uH 5A output inductor | Value based on datasheet[2]. |
| 25SVPF180M | 2 | 180uF output surge capacitor | Number and value of capacitors used is based on datasheet[2]. |
| CRCW1206140RFKEA | 1 | 140Ohm 1206(3216) LED resistor | Based on forward current[3]. |
| LM2678S-3.3/NOPB | 1 | 3V3 regulator | Chosen for simplicity of application circuit and high output current of 5A which is excessive for the Hydra V1. |
| EEHZA1V680XP | 2 | 65uF 35V input surge capacitor | Number and value of capacitors used is based on datasheet[2]. |
| 74477110 | 1 | 10uH 5.5A output inductor | Value based on datasheet[2]. |
| 16SVPC120M | 1 | 120uF output surge capacitor | Value based on datasheet[2]. |
| CRCW120660R4FKEA | 1 | 60Ohm 1206(3216) LED resistor | Based on forward current[3]. |
| 43045-0402 | 1 | Battery connector | Chosen for locking ability and high current capacity (5A per pin at 250VDC). It has 4 pins so each battery terminal uses two for a combined 10A current capacity. |
| FQD17P06TM | 1 | 60V 12A P-Channel reverse polarity protection MOSFET | Chosen since surface mount and enough current capacity for our purposes however may be switched due to availability issues at the time of this writing. |
| MMSZ5242BT1G | 1 | 12V Zener 0.5W diode to regulate reverse voltage for P-Channel MOSFET | Zener voltage was chosen to match nominal battery voltage. Current limiting resistor tabulated below ensures power through Zener does not exceed 0.5W. |
| CRCW12061K20FKEA | 1 | 1.2k 1206(3216) current limiting resistor for Zener | Maintains max current through Zener as |
| SS-5GL2D | 2 | 5A safety disconnect switch | Two are used in parallel since they are rated for 5A each and we need 10A. |
| EEEFK1H101P | 1 | 100uF 50V input surge capacitor | Acts as an input surge capacitor for the board as a whole. |
| PRT-12790 | 2 | Inter-board header | Standard component for all Hydra Boards |

|  |  |
| --- | --- |
|  | Common components |
|  | 5V regulator components |
|  | 3V3 regulator components |

### Layout Considerations

The current power board layout is concentrated to leave space for future power board upgrades and keep the traces as short as possible. The layout for each regulator is compacted to ensure the capacitors and inductors remain as close as possible to the regulation IC as per recommendation from the datasheet.

Additionally, this is a 4 layer board containing GND and VCC planes within the stack to simplify the board’s trace layout. This is not entirely necessary for the time being however it will be necessary with future power board versions that will integrate significantly more functionality. As such, 4 layers are kept to simplify the process of designing future boards as the power regulator layout will not need to be changed and we will have tested the layout prior to ordering a second board with more functionality.

### Schematics

Diagram, schematic

Description automatically generated

Figure 1‑10. Connectors and reverse polarity protection schematic

Diagram

Description automatically generated

Figure 1‑11. 5V and 3V3 regulator schematic w/ LEDs

### PCB

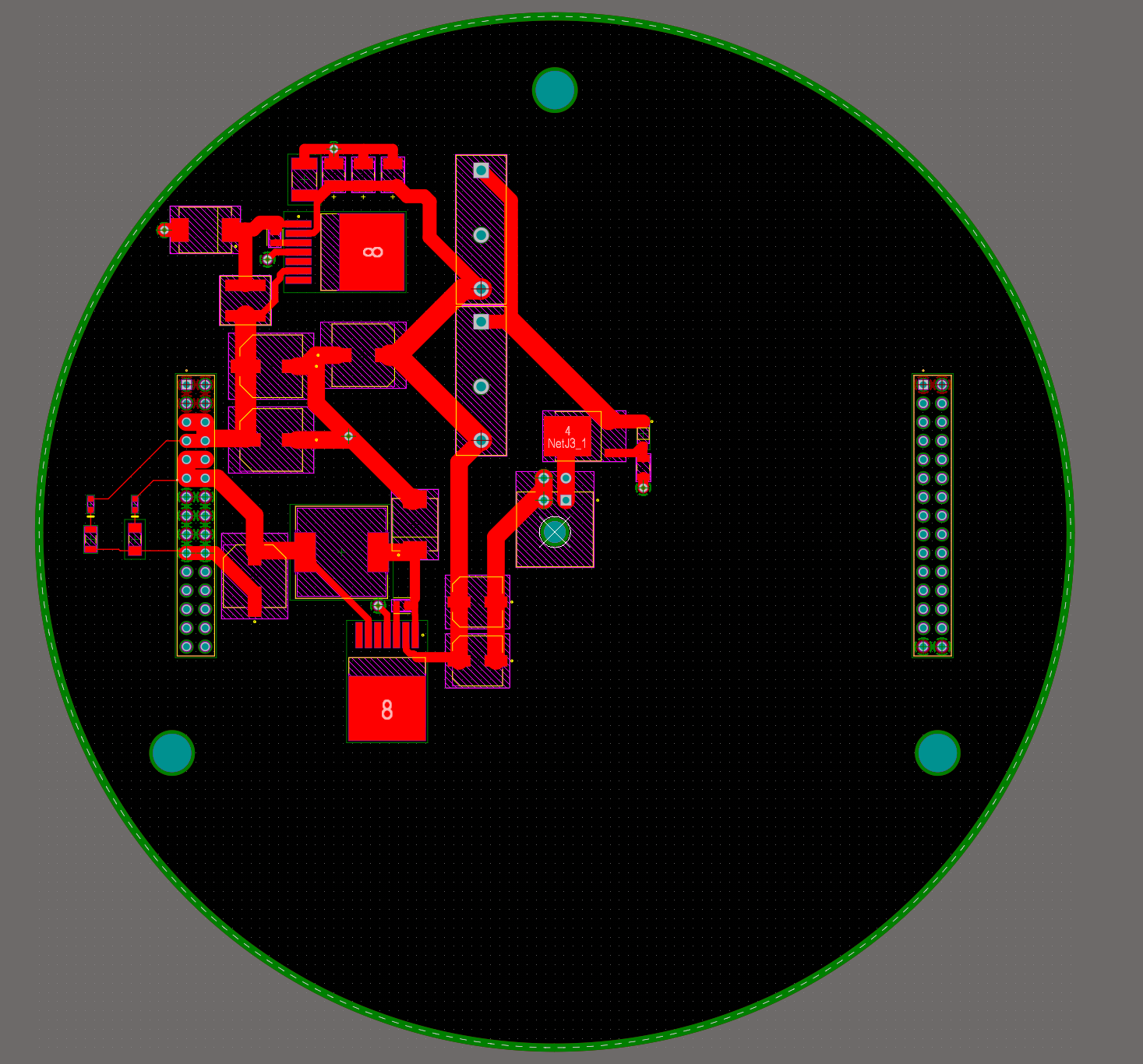


Figure 1‑12. Hydra V1 Power Board PCB Layout (PWR and GND planes omitted)

### Reflection

* Add VIAs to regulator back tabs to dissipate heat into ground plane

## MCU Pinout (HYDRA\_V1\_MCU\_PINOUT)

### Overview

The MCU pinout project is a barebones MCU schematic that includes MCU-specific power components, clock crystals, status LEDs, a reset switch, a CAN transceiver, and a 10-pin JTAG interface. Sections 1.5.2 and 1.5.3 are not included since the information can be found in Sections 1.3.2 and 1.3.3, respectively. Section 1.3.1.3 may be relevant with regard to the crystal and reset switch circuits. Additionally, Section 1.3.3 may be relevant when considering the PCB layout though the HYDRA\_Vx\_LOGIC (where ‘x’ is the most recent version) project should ideally be used for reference.

The remainder of this section covers the requirements to implement the MCU\_PINOUT schematic in another project. The following nets must be connected in order for the pinout to work:

|  |  |  |
| --- | --- | --- |
| Net name | Net type | Purpose |
| 5V | Power port | Supply 5V to CAN transceiver |
| 3V3 | Power port | Supply 3V3 to MCU |
| GND | Power port | Provide GND to board |
| CAN0\_P | Differential pair | CAN high (P) and CAN low (N) differential pair |
| CAN0\_N |

#### Power Requirements

The MCU\_PINOUT project does not incorporate any internal regulators since Hydra boards rely on the power board for 5V and 3.3V. In the case of a board that does not have access to regulated voltage rails, a separate regulator must be integrated. TALK ABOUT MCU PWR CONSUMPTION 5V should be provided to a power port object labelled “5V” whereas 3.3V should be provided to a power port object labelled “3V3”. No external components should be attached to the MCU’s internal power nets (VDD\_ANA or VDD\_IOB) and should instead use another supply such as the aforementioned 5V or 3V3 power port objects.

#### CAN Requirements

The CAN transceiver is the sole component within the MCU pinout that operates at 5V and, as such, its RxD pin has a voltage divider (R5/R7) to reduce the 5V to 3V3 before it reaches the MCU. Additionally, the CANH and CANL pins are marked as a differential pair such that Altium automatically matches the lengths of each trace and maintains constant spacing between the two. This differential pair must be connected to the left header or some other end spoint.

### Component List

See relevant components in Section 1.3.2.

### Layout Considerations

See relevant considerations in Section 1.3.3.

### Schematics

Diagram, schematic

Description automatically generated

Figure 13. MCU\_PINOUT MCU pinout including power components and SWCLK pullup

Diagram

Description automatically generated with medium confidence

Figure 14. MCU\_PINOUT status LED and crystal schematics

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Description automatically generated

Figure 15. MCU\_PINOUT reset switch and CAN transceiver schematics

Diagram, schematic

Description automatically generated

Figure 16. MCU\_PINOUT 10-pin JTAG header schematic

# Hydra V2

## Recovery Board (HYDRA\_V2\_RECOVERY)

## Communication Board

No communication board for V2, see V3.

## Logic Board (HYDRA\_V2\_LOGIC)

## Power Board (HYDRA\_V2\_POWER)

### Overview

The V2 power board uses identical regulators to the V1 power board albeit in parallel for redundancy. Each power rail (5V and 3V3) has two regulators whose outputs pass through back-to-back P-channel MOSFETs whose gate is driven such that it is impossible for both regulators to be simultaneously connected to the power rail.

From a macroscopic perspective, the power is received through a Molex connector (J1) and passed through two cutoff switches before entering the global power protection circuit. This circuit handles reverse polarity protection as well as overcurrent and overvoltage protection (in this order). Finally, the power protection circuit provides the MCU with input voltage and current data. Following the protection circuit, the power passes through two similar regulator circuits which power the 5V and 3V3 rails of the avionics stack. Both circuits consist of two identical regulators who largely share input and output capacitors and use hardware-based logic to determine if the output voltage of either regulator exceeds or falls below a predefined acceptable range. Finally, an MCU is included to manage the board and communicate with the remainder of the avionics stack as well as four thermistors which serve to measure the temperature of each individual regulator.

#### **Power Protection Considerations (PWR\_protection.SchDoc)**

The power protection schematic has three components: reverse polarity protection, overcurrent/overvoltage protection, and current sensing. The reverse polarity protection works identically to that of the V1 power board (see Section 1.4.1). The overcurrent/overvoltage protection is based on [this](https://www.ti.com/lit/an/snoaa39/snoaa39.pdf?ts=1681756702248)[4] paper from Texas Instruments using a TLV1805 op-amp. Fundamentally, this circuit is an op amp comparator which compares the voltage drop across a shunt with a fixed value provided by a carefully selected voltage divider. The schematic shown below is taken from the aforementioned paper and depicts the overcurrent circuit. For the purposes of this explanation, I will refer to the non-inverting input of the op amp as VP (since it’s denoted by a plus sign) and the inverting input as VN (since it’s denoted by a negative sign).

Diagram, schematic

Description automatically generatedThe power is passed from the top left, through the V­S power object, through a shunt (R1), and finally though a P-channel MOSFET before reaching the load at the bottom left. The voltage post-shunt, VN, will be marginally less than the supply voltage VS. The voltage divider (R2/R3) is selected such that it produces a voltage analogous to the drop that would occur across R1 at the maximum allowable current flow. Initially, the current draw is below the limit and so the voltage drop across the shunt is small and therefore the post-shunt voltage is higher than the voltage generated by the divider. Since VN is higher V­P, the op amp’s output will be low (op amp output ~ V­P – VN). This output does two things: firstly, it pulls the gate of the P-channel MOSFET low thereby turning it on, and secondly it maintains the right side of the R2/R3 voltage divider low. Once an overcurrent condition is reached and the voltage drop across the shunt causes VN to be less than VP, the op amp’s output will go high. This high output cuts off the MOSFET but also effectively sets both sides of the R2/R3 voltage divider high so VP will now be effectively equal to VS. In this manner, VP = VN and the op-amp will be stuck in its hysteresis zone where there is not enough of a difference between VP and VN for the output to change state.

Add overvoltage protection, numbnuts (or don’t idc)

Aside from protection, this schematic provides the MCU with information about battery voltage using the R13/R16 voltage divider as well as an instrumentation amplifier built with U8. In the figure below, U8A and U8B are voltage followers to prevent this circuit from altering the post-shunt voltage used by the over-current protection circuit. The voltage followers’ output is then passed into a differential amplifier (U8C) with a gain of 10 since the voltage drop across the shunt during the maximum possible current condition is computed to be 200mV. Therefore, U8C amplifies the shunt voltage to 2V after which U8D is used to shift the voltage up by one volt since the MCU’s ADCs can only sense voltages between 1V and 3V3.

A screenshot of a computer

Description automatically generated with medium confidence

#### **Redundant Regulator Considerations (5V\_regulators.SchDoc and 3V3\_regulators.SchDoc)**

The explanation here will use part designators from the 5V schematic though both 5V and 3V3 schematics are very similar with the only difference being that voltage dividers are used to decrease the logic voltage to 3V3 in the 5V schematic.

**Parallel Regulator Arrangement**

Two regulators are included in parallel (U1 and U2) and share input/output capacitors. A picture of the regulators for the 5V rail is included below where U1 and U2 are the 5V regulators used for the avionics stack and U6 is a smaller linear regulator used both to power the protection logic as well as to provide a 5V reference. The logic regulator is not redundant since component failure is not considered to be a significant failure vector and the redundancy is focused on mediating regulators overheating or temporary short circuits within the stack.

A picture containing text, indoor

Description automatically generated

The outputs from U1 and U2 pass through two back-to-back P-channel MOSFETs that serve to cut off or connect each regulator to the power rail as required. The remaining components are chosen as per the datasheet with the only notable modification being C4 and C11 which are appended after the back-to-back MOSFETs. C3, C4, C10, and C11 are all identical. The datasheet recommends using two of these at the output of each regulator, but I have moved one from each regulator to after the MOSFET to alleviate the temporary loss of power that will occur when the active regulator is switched. I kept one close to the regulator in case it provides some functionality when combined with the inductor and diode included next to each regulator.

**Regulator Failover Logic**

Diagram, schematic

Description automatically generated Regulator failover functions by monitoring the output voltage of each regulator and acting accordingly. Two comparators are used for each regulator to monitor the output voltage (the comparators for U1 are shown here). U5A monitors for an overvoltage condition by comparing a 5V reference (5V\_REF) to the regulator’s output passed through a voltage divider. The R4/R29 voltage divider is computed such that its output voltage will be 5V when 5V\_1 is 5.5V. Therefore, the comparator’s output will swing high if the regulator’s voltage ever exceeds 5.5V. The undervoltage comparator (U5B) functions in the exact same way albeit with the 5V\_REF being passed through the regulator such that the op amp sees 4.5V at its non-inverting input. This comparator will also swing high if 5V\_1 ever falls below 4.5V. To unify these output signals, they are passed through an OR gate (U12A) to produce the output signal 5V\_U1\_FAIL.

**Add one shot timer to pic**

Diagram

Description automatically generated with medium confidence The 5V\_U1\_FAIL pin is immediately followed by a SR-latch (U11). This specific latch has an output enable (OE) pin which is tied to the 5V rail using a pullup resistor (R48, not pictured) to prevent the latch from changing states while the MCU is booting. Once the MCU has booted, it will drive the OE pin low thereby enabling Q and avoiding erroneous behaviour while the regulators boot and their output voltage is not within the acceptable range of the comparator circuit. Finally, the MCU will also drive the latch enable (LE) pin high once it has booted which allows the latch’s output to follow the 5V\_U1\_FAIL signal.

During normal operation, 5V\_U1\_FAIL is low and therefore the latch’s output, Q, will also be low. Q is connected directly to the gate of Q7 which is a small N-channel MOSFET used to drive the gate of the larger P-channel MOSFETs included in the regulator schematic (Q3/Q4). With the gate being low, Q7 will be off and therefore the 5V\_MOSFET\_2 net will be driven high by the **PULLUPS I FORGOT TO INCLUDE**. Conversely, the gate of Q8 is driven high by an inverter (U13A) and therefore the gates of Q10 and Q11 are pulled low to allow U1 to supply power to the 5V rail. N-channel MOSFETs needed to be used here since U11 cannot provide enough current to charge the gate-source capacitance of Q3/Q4. Additionally, U13A was included to ensure that the regulators can never both be connected to the 5V rail.

Should the first regulator ever fail, 5V\_U1\_FAIL will go high and reverse the state of the MOSFETs. To latch in this failed state, the 5V\_U1\_FAIL pin is connected to an interrupt pin on the MCU who is in charge of driving LE low once a failure has occurred. A one-shot timer, pictured below, is included on the 5V\_U1\_FAIL net since the LE pin is effectively controlled through software and it is impossible to know how fast the LE pin will be set to low following a failure. The concern is that, once the load of the 5V rail is transferred to U2, the voltage output of U1 will rise back to an acceptable level since no current is being drawn. Therefore, the 5V\_U1\_FAIL net would go low, and the output of the SR-latch would also go low thereby transferring the load back to U1 before the LE pin is driven low by the MCU.

You might say this seems like poor design and it kinda is but the point of connecting the LE to the MCU is to provide us with the ability to revert to U1 if U2 starts acting up. In this configuration, we can set LE to high at which point the load will be transferred back to U1 provided U1’s output voltage is within the acceptable range and the 5V\_U1\_FAIL net is low. This would be useful should the regulators overheat, for example, since we could swap back and forth to afford each regulator some amount of time to cool down.

**Other Stuff**

As previously mentioned, voltage dividers are used on all outputs of the 5V regulator schematic to drop voltage levels to the 3V3 logic that the MCU uses. Additionally, a pull-up is included on the SR latch’s OE pin since it is active low and, conversely, a pull-down is included on the SR latch’s LE pin since it is active high. Finally, a bicolor LED is included (DS2) to provide information about the regulator’s status. The green LED is connected to the 5V rail and will therefore turn on if power is being supplied from the board. The red LED is connected to the output of the SR-latch and will therefore be off during normal operation and on if the board is now using U2 as opposed to U1 for supplying power. Therefore, the LED will be green if everything is ok, orange if power is being supplied but U1 failed, and red if both U1 and U2 are incapable of supplying 5V.

#### MCU Considerations (MCU\_PINOUT.SchDoc)

Figure out pin assignment on MCU

# References (force of habit)

[1] “RRC3 ‘Sport’ Altimeter.” https://www.apogeerockets.com/Electronics-Payloads/Altimeters/RRC3-Sport-Altimeter (accessed Feb. 01, 2023).

[2] “getdatasheetpartid-55536-15112621.pdf.” Accessed: Feb. 01, 2023. [Online]. Available: https://datasheet.ciiva.com/15112/getdatasheetpartid-55536-15112621.pdf?src-supplier=Verical

[3] “LED Series Resistor Calculator | DigiKey Electronics.” https://www.digikey.ca/en/resources/conversion-calculators/conversion-calculator-led-series-resistor (accessed Feb. 01, 2023).

[4] “Overcurrent latch circuit,” 2019.