UI-RI Hybrid Lookup Table Method With High Linearity and High-Speed Convergence Performance for FPGA-Based Space Solar Array Simulator

Shanshan Jin, Donglai Zhang, *Senior Member, IEEE*, and Chao Wang

***Abstract*—Most existing high-power solar array simulators are suitable for simulating solar array energy sources in terrestrial applications. However, they are not sufficiently fast for spacecraft power-system testing using terrestrial testing applications. This paper proposes a UI-RI hybrid lookup table method with high linearity and high-speed convergence performance, which outperforms the traditional single UI lookup table method by employing a field-programmable gate array digital *I–V* outer loop. The proposed method overcomes the difficulty in guaranteeing stable output characteristics of the current output-type space solar array simulator (SSAS) because of the nonlinear *I–V* curves and slow convergence speed to the target operating point of the latter. The new lookup method is applied to a 2.4-kW hardware power platform of SSAS, and the SSAS can quickly respond to a load step between the short-circuit and open-circuit (OC) states, which is the harshest working condition, using the UI-RI hybrid lookup table method with a shunt switching frequency of 2 kHz. It can also quickly respond to a load step between the OC and rated-load states using a series-switching frequency of 10 kHz. The experimental data-point distribution trajectory of the switching process shows a greater tendency to converge to the designed *I–V* curve compared with the single UI lookup table method.**

***Index Terms*—High dynamic performance, *I–V* curve, linear power stage, lookup table method, multilevel tracking converter, solar array simulator.**

I. Introduction

IN THE field of space power systems, satellite power is known to be mainly obtained from solar cells as the power source. The performance of satellite power systems directly affects the performance and operational life of satellites, and it has a significant impact on the normal operation and use of satellites. Therefore, to improve the performance and reliability of space power systems, it is crucial to evaluate the output characteristics of the solar array source in conditions that are very similar to those in a real space environment. Further, space satellites operate in harsh and complex conditions, such as a wide range of temperatures and rapidly changing solar conditions. Moreover, space solar panels are subjected to high-energy particle radiation. The aforementioned conditions experienced by satellites in orbit cannot be reproduced using solar panels on the earth. Hence, there is a need a for space solar array simulator (SSAS) to simulate the solar array in space working conditions. SSAS is an important component of satellite power systems. Its main functions are to closely mimic the space solar array in a variety of space load conditions and to output real characteristics of the curve in the space power system ground test phase. Thus, it can be employed instead of using solar cells as the power supply for each satellite subsystem [1], and the specific requirements for a SSAS are presented in [2].

Currently, spacecraft power systems use the sequential switching shunt regulator (S3R, introduced by the European Space Agency in the seventies) architecture widely, because of its high efficiency, low mass, simplicity, and high reliability [3], as shown in Fig. 1.

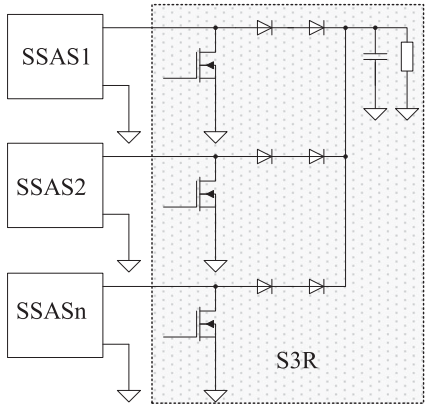

Fig. 1. S3R with the SSAS as a testing power source.

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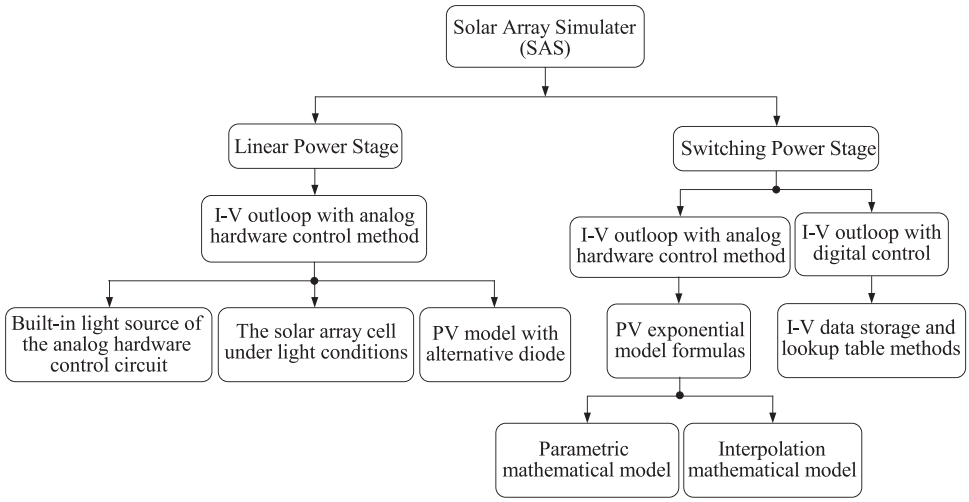


Fig. 2. Classification of solar array simulator.

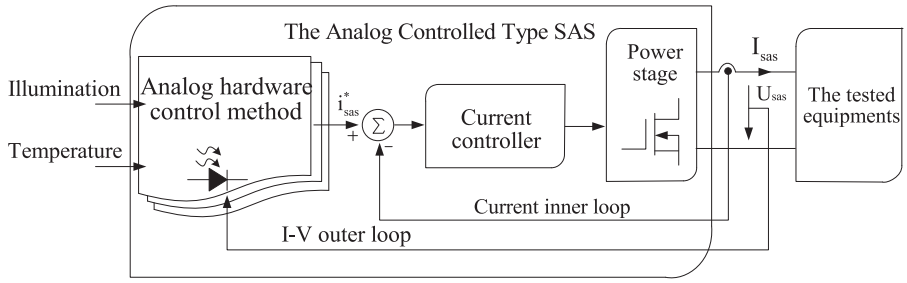


Fig. 3. Basic structure of SAS based on analog signal generation circuit.

The main feature of this topology, when used as a load for the SSAS, is the production of a step voltage with a high frequency, because the main bus voltage of the S3R is always regulated [4]. The dynamic response of the SSAS should be sufficiently fast, to meet the power needs of the shunt regulator, implying that the solar array simulator (SAS) should have a current-output-type framework. Essentially, the solar array panel output is also a current output. A solar array panel has a highly nonlinear capacitance [5]. In particular, the GaAs solar array panel capacitance is much larger than its silicon counterpart, and because of this nonlinear capacitance, the output power state of a solar array panel is also an important factor to consider in SSAS. As reported in [6], the transition capacitance is dominant in the range of 0–U_{MPP}, and it practically remains constant. In addition, the sequential switching shunt regulator (S3R) normally operates below U_{MPP}, and therefore, a practically constant capacitance can be assumed [5]. Hence, SSASs usually directly connect a specific capacity of the capacitor to the output port, which can directly simulate the effect of solar panel parasitic capacitance on the output power.

In general, the SAS design consists of three basic aspects: power stage design, control system, and *I–V* outer loop design, as shown in Fig. 2. The power stage design can be categorized into a linear power stage scheme and a switching power stage scheme [7], [8]. The PV power simulator with a linear power stage scheme has excellent dynamic characteristics. However, owing to its limited power, low efficiency, high heat generation, and bulky size, it is not suitable for use in high-power applications. In general, it uses the switching power stage scheme, i.e., a switch-type SAS, to achieve the *I–V* power curve output function in high-power applications, and it needs to operate in the buck mode. The different types of switch topologies include single-phase dc–dc buck converter [9], three-phase ac–dc voltage source and current source rectifier [10], half-bridge and full-bridge dc–dc converter [11], [12], *LLC* resonant dc–dc converter [13], and other power-level topologies, such as dc programmable power supplies with current thresholds [14] and dc power supplies with variable resistors [15] or controllable switching resistors and active power loads [16].

I–V voltage current signal generation technology can be classified into the analog hardware circuit control method [17] and the digital control method [18]. A SAS based on an analog hardware circuit is a simple and low-cost power source, as shown in Fig. 3. Such a simulator has two control loops, namely an inner loop (current loop) and an outer loop (reference loop).

The inner loop mainly controls the output power current of the SAS [19]. In general, for a SAS based on an analog hardware circuit, the following types of *I–V* reference generation circuits may be employed:

1) a small PV cell unit with a light source;

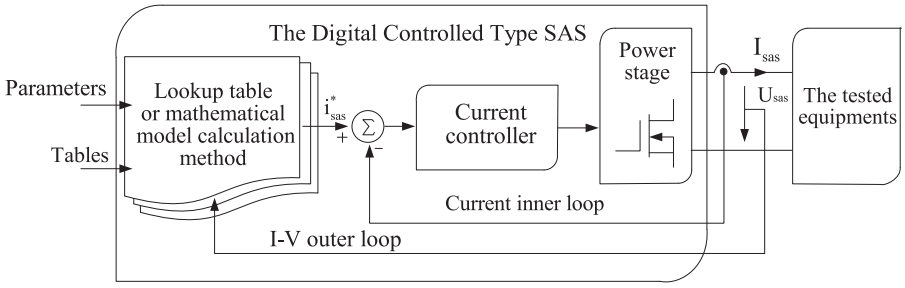


Fig. 4. Basic structure of SAS based on digital control method.

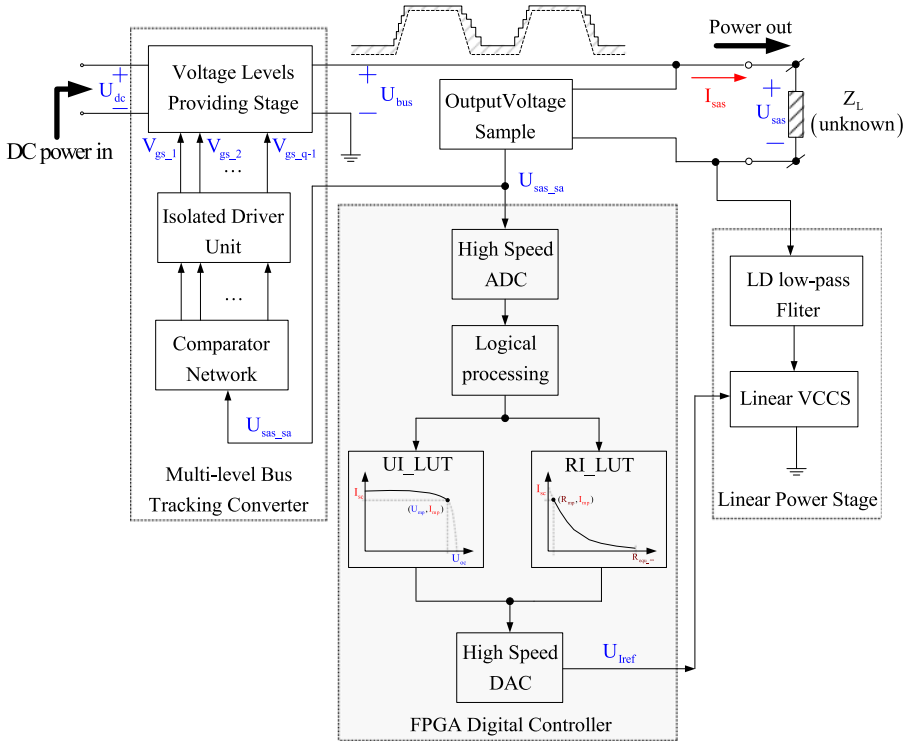


Fig. 5. Proposed system configuration.

2) a photodiode with a light-emitting diode;
3) the PV model with an alternative diode [20].

This approach can be simulated online in real time. Hence, it is more accurate than other analog *I–V* generation methods. The analog *I*–V reference from the hardware circuit can be controlled accurately and flexibly. Thus, the *I–V* signal curves can be effectively simulated under occlusion conditions as well as under varying light intensity and temperature.

In addition to analog hardware for generating *I–V* reference curves, a digital technique can also be used to produce the corresponding reference curves [21]. The power *I–V* curve generated by an SAS based on the digital control method is more flexible and reliable, and its antiinterference ability against high-frequency noise is stronger. However, digital delay may affect the characteristics and design of the control loop. Fig. 4 shows a basic block diagram of an SAS based on digital control.

In order to realize the output characteristics of the actual solar array panels, it is necessary to adopt two control loops in an SAS based on digital control [22], which generates *I–V* reference signals by two methods:

1) The first method is to use tables to store the current and voltage data that have been measured under different environmental conditions and load conditions in advance [23], [24]. These tables are usually called UI lookup tables. The larger the amount of stored data, the higher is the resolution and accuracy of the power adjustment.
2) The second method is to use the PV mathematical model, which gives the parameters required for the logarithmic model to make corresponding calculations. The most commonly used models are the solar cell parameter model and solar cell interpolation model [25], [26]. In general, the parameters of the PV unit are known (from the data sheet of the PV unit). The interpolation model only needs to know the open-circuit (OC) voltage, short-circuit (SC) current, and maximum power point (MPP) voltage and current, i.e., U_{mp} and I_{mp}.

II. Proposed Space Solar Array Simulator

The proposed system configuration is shown in Fig. 5, and the system structure is based on the published article in [27], where the structural design and theoretical analysis are described in detail. The innovation of this study is based on the same system platform and proposes a new digital *I–V* outer loop control method that overcomes the difficulty in guaranteeing stable output characteristics of the current output-type SSAS because of the nonlinear *I–V* curves and slow convergence speed to the target operating point.

The system consists of three parts: the multilevel bus tracking converter unit, the linear power stage, and the field-programmable gate array (FPGA) digital controller [28]. The load Z_L connected to the SSAS output terminal is unknown and is usually the tested power supply device. The output voltage sample circuit should sample the SSAS output voltage into the low-voltage sampling signal U_{sas_sa}, and then send it to the multilevel bus tracking converter unit and FPGA digital controller. The multilevel bus tracking converter must produce the corresponding switching control instructions based on the given U_{sas_sa} signal, so that an appropriate bus voltage level can be established. We must emphasize that in the multilevel bus-tracking converter unit and linear voltage-control current-source power stage unit of a SSAS with this structure, which is shown in Fig. 5, the detailed theoretical analysis and parameter-design conclusions are presented in a published paper [27]. Thus, the same contents are not repeated in this paper.

The FPGA digital controller is used to output the reference controlling voltage $U_{I\mathrm{ref}}$ of the linear voltage-controlled current source (VCCS) to control the expected SSAS output power current, which is an operating point of the set *I–V* power curve. In general, the current-output SSAS only obtains the corresponding current reference value on the desired *I–V* curve by sampling the output terminal voltage, and the lookup tables are usually UI tables. However, the UI lookup table method suffers from the obvious problem of nonlinear oscillations. Here, the UI-RI hybrid lookup table method is used. On the left side of the MPP of the set *I–V* curve, the FPGA uses the UI subtable to obtain the SSAS output steady power current by exploiting the better linearity characteristics in this part of the set *I–V* curve. Similarly, on the right side of the MPP of the set *I–V* curve, the FPGA uses the RI subtable with better linearity and fast convergence speed. A certain $U_{I\mathrm{ref}}$ is dependent on the given U_{sas_sa} on the basis of the lookup table [29] that is prestored in the RAM of the digital controller.

The block diagram of the entire SSAS system structure can be obtained by reviewing previous articles, as shown in Fig. 6. The mathematical model $G_{\mathrm{Linear\_20\,path}}$ of the linear VCCS, from the reference voltage $U_{I\mathrm{ref}}(s)$ to the output current $I_{\mathrm{Lin}}(s)$, is known from a previous article [30]. The model $G_{\mathrm{PSRR\_iin}}$ of the linear VCCS, from the drain voltage of linear power transistor $U_d(s)$ to output power current $I_{\mathrm{in\_tot}}(s)$, and the mathematical model $G_{\mathrm{multi\text{-}level}}$ of the multilevel bus tracking converter, from $U_{sas}(s)$ to $U_{\mathrm{bus}}(s)$, have been derived and analyzed in a previous article.

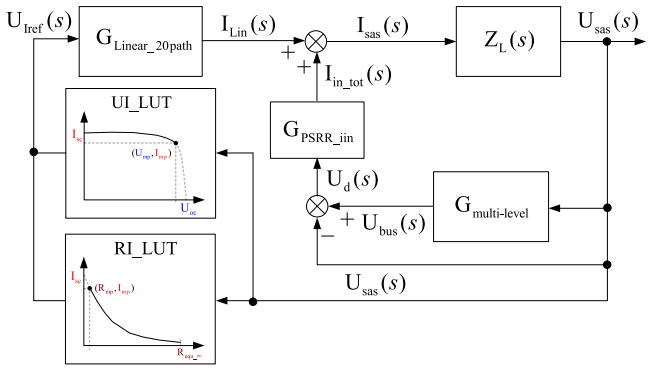


Fig. 6. Block diagram of entire SSAS system structure.

III. Proposed High-Speed Convergence Performance UI-RI Hybrid Lookup Table Method

A. Existing Nonlinear Problems Using a Single Lookup Table Method

The required *I–V* operating curve can be divided into two working regions, namely the constant current region and the constant voltage region [31]. The problem of using a single lookup table is manifested in two main aspects. The first problem is that the operating point changes in the nonlinear work area of the set *I–V* curve, leading to instability in the steady-state working conditions. The second problem is convergence to the target operating point and the convergence speed in two different regions [32].

Using a single UI lookup table and a single RI lookup table will lead to nonlinear issues in a certain region of the set *I–V* curves, as shown in Fig. 7. The working point MPP is the MPP of the set *I–V* curve (U_{mp}, I_{mp}). There are two different working points, namely $A_{\mathrm{ML}}\,(U_{\mathrm{AL}}, I_{\mathrm{AL}})$ and BML $(U_{\mathrm{BL}}, I_{\mathrm{BL}})$, on the left side of the MPP point in positions close to the constant current area. The other two working points, namely $A_{\mathrm{MR}}\,(U_{\mathrm{AR}}, I_{\mathrm{AR}})$ and $B_{\mathrm{MR}}\,(U_{\mathrm{BR}}, I_{\mathrm{BR}})$, on the right side of the MPP point are in positions close to the constant voltage area. The corresponding operating point positions may be equivalent to the IR table with the same set *I–V* curve.

The SSAS works at point A_{ML} and should change to the working point B_{ML}. The voltage difference between the two operating points is ΔU_{ML}; the current difference is ΔI_{ML}. From the working principle of the SSAS, a large voltage difference can only cause a slight current change, which means that the output current could be steady because of the better linearity of the *I–V* control loop. However, the change between points A_{MR} and B_{MR} will cause a large and rapid current change ΔI_{MR} within a very small voltage range ΔU_{MR} because the *I--V* setting curve has poor linearity in the area near the OC voltage. Similarly, the converse conclusion can be drawn from a single RI table, which is in poor linearity operation condition between points A_{ML} and B_{ML} and in better linearity operation condition between points A_{MR} and B_{MR}. Thus, it is difficult to obtain stable working conditions of the entire *I–V* curve using a single lookup table method.

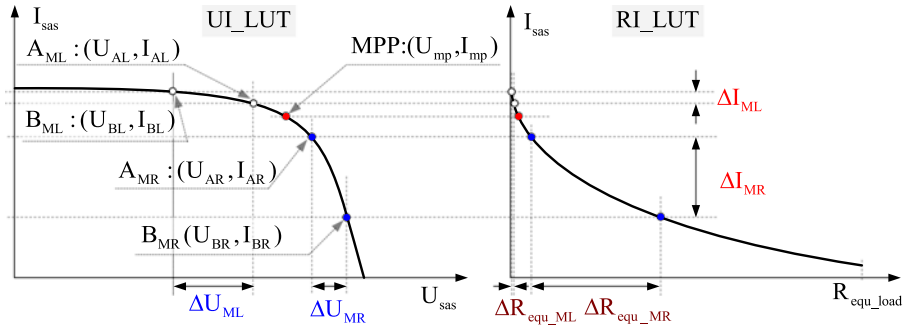


Fig. 7. Nonlinear issues using a single UI lookup table and a single RI lookup table.

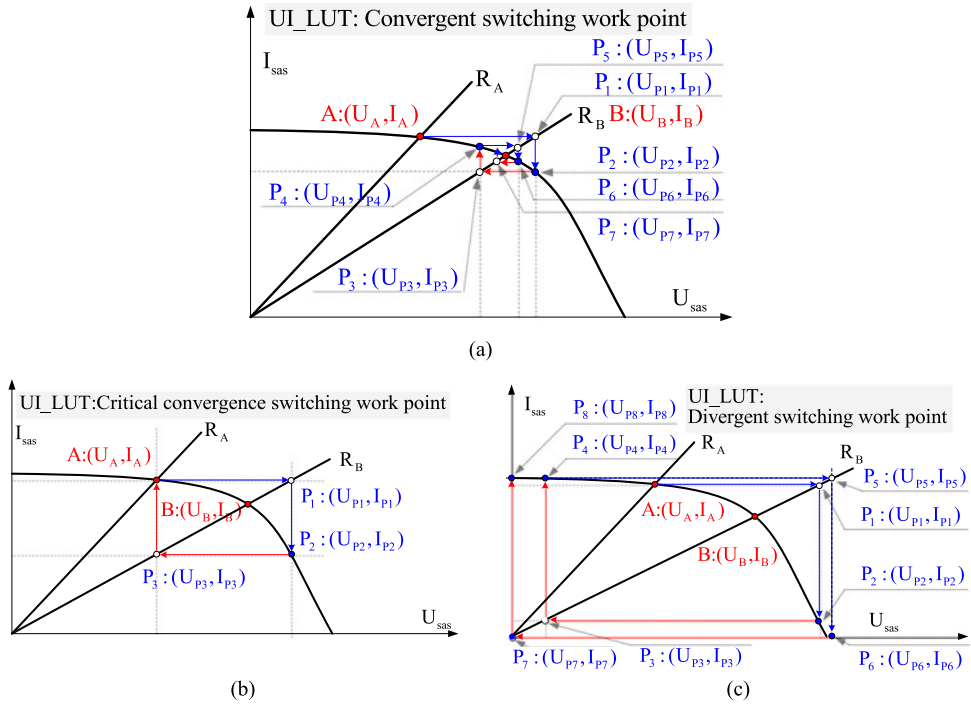


Fig. 8. Issue of convergence and convergence speed to the target operating point using a single UI lookup table: (a) the switch working points are very close, (b) the switch working points are in a critical convergence state, (c) the switch working points are in the divergence state.

The second problem is the issue of convergence to the target operating point and the convergence speed using a single UI lookup table, as shown in Fig. 8.

Fig. 8(a) shows the two step switching working points $A\,(U_A,\ I_A)$ and $B\,(U_B,\ I_B)$, which are very close. The FPGA digital controller should first sample the output voltage of the SSAS with a high-speed ADC, and it should not update the DAC output U_{Iref} until it completes the entire digital program process, which means that the power current state would remain unchanged. The working point A changes to $P_1\ (U_{P1},\ I_{P1})$ and $U_{P1} < U_{oc}$. The relationship is as follows:

$$A \rightarrow P_1 : \begin{cases} U_{P1} = I_A \cdot R_B|_{U_{P1}<U_{oc}} \\ I_{P1} = I_A \end{cases}. \tag{1}$$

The output voltage U_{sas} at which ADC can be sampled is U_{P1}, and the corresponding operating point on the *I–V* curve is $P_2\ (U_{P2},\ I_{P2})$. The power current is changed to I_{P2}. However, P_3 is still not the target operating point

$$P_2 \rightarrow P_3 : \begin{cases} U_{P3} = I_{P2} \cdot R_B|_{U_{P3}<U_A} \\ I_{P3} = I_{P2} \end{cases}. \tag{2}$$

The ADC samples the output voltage U_{P3}, and the corresponding operating point on the *I–V* curve is $P_4\ (U_{P4},\ I_{P4})$. The power current is changed to I_{P4}. The reached working point is $P_5\ (U_{P5},\ I_{P5})$:

$$P_4 \rightarrow P_5 : \begin{cases} U_{P5} = I_{P4} \cdot R_B|_{U_{P5}<U_{P2}} \\ I_{P5} = I_{P4} \end{cases}. \tag{3}$$

Following the same convergence logic steps, the working point then reaches $P_6\ (U_{P6},\ I_{P6})$, $P_7\ (U_{P7},\ I_{P7})$ and it will eventually converge to the target operating point $B\,(U_B,\ I_B)$. This is a cyclic convergence process, indicating that the UI

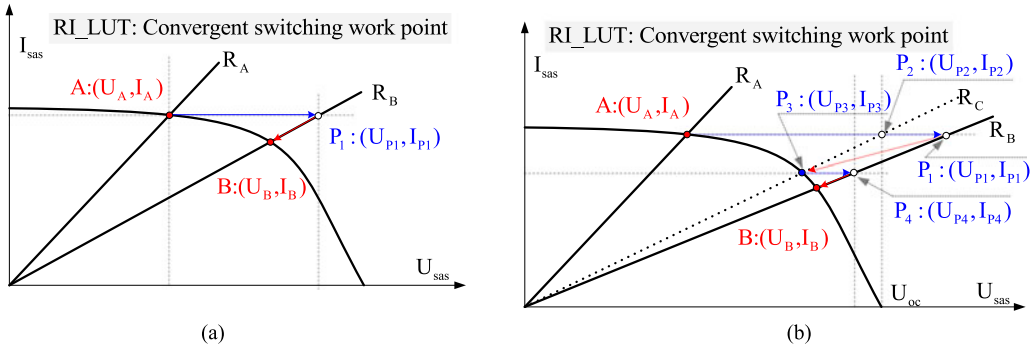


Fig. 9. Convergence process of stepping from the point A to the point B with RI lookup table method: (a) the convergence process which is in a critical convergence state with UI lookup table, (b) the convergence process which is in the divergence state with UI lookup table.

lookup table method can only achieve convergence to the target operating point after several lookup cycles.

However, there is also a situation in which the operating switching points do not converge, as shown in Fig. 8(b) and (c). Fig. 8(b) shows that the switch working points are in a critical convergence state when the output switch speed is sufficiently high, and the next working point after point $P_3\,(U_{P3},\,I_{P3})$ is coincident with point A. Fig. 8(c) shows that the switch working points are in the divergence state when the output current value of point $P_4\,(U_{P4},\,I_{P4})$, I_{P4} is greater than I_A.

From the analysis described above, it can be concluded that there will be operating points that do not converge to the desired operating point, and the convergence rate is extremely slow under the step switching conditions using a single UI lookup table method.

B. Proposed UI-RI Hybrid Lookup Table Method

The above analysis shows that, regardless of whether a single UI table or RI table is used, a nonlinear problem occurs in different areas of the set *I–V* curve. The RI lookup table method does not work well in the constant current region, but it achieves fast convergence to the target operating point under the step switching working points, as shown in Fig. 9. Fig. 9(a) shows the convergence process of stepping from $A\,(U_A,\,I_A)$ to $B\,(U_B,\,I_B)$ with the RI lookup table, which is in a critical convergence state with the UI lookup table method. Fig. 9(b) shows the convergence process of stepping from $A\,(U_A,\,I_A)$, to $B\,(U_B,\,I_B)$ with the RI lookup table, which is in the divergence state with the UI lookup table method.

From Fig. 9(a), the current working point is $A\,(R_A)$ and the unknown load will step to working point $B\,(R_B)$ very quickly. The FPGA makes the DAC remain at $U_{I\mathrm{ref}}(k-1)$, where k is the current work lookup cycle; the corresponding power current is $I_{\mathrm{sas}}(k-1)$. The FPGA should calculate the equivalent load resistance $R_{P1\_\mathrm{equ\_load}}(k)$ with $I_{\mathrm{sas}}(k-1)$, which is the stored current point of the *I–V* curve obtained in the previous lookup table cycle

$$A \rightarrow P_1 : \begin{cases} U_{P1} = I_A \cdot R_B \\ I_{P1} = I_A = I_{\mathrm{sas}}(k-1) \end{cases}. \tag{4}$$

The equivalent load resistance $R_{P1\_\mathrm{equ\_load}}(k)$ is given by

$$R_{P1\_\mathrm{equ\_load}}(k) = \frac{U_{P1}}{I_{\mathrm{sas}}(k-1)} = \frac{I_{\mathrm{sas}}(k-1)\cdot R_B}{I_{\mathrm{sas}}(k-1)} = R_B. \tag{5}$$

By looking up the corresponding RI table, obtain the current value given in the next cycle

$$I_{\mathrm{sas}}(k) = \mathrm{Table}_{\mathrm{RI}}\left(R_{P1\_\mathrm{equ\_load}}(k)\right) = f\left(R_B\right). \tag{6}$$

Only a lookup table cycle is required to make the working state converge to the target operating point B; the convergence speed is quite fast.

Fig. 9(b) shows the divergence state with the UI lookup table; the next working point is $P_1\,(U_{P1},\,I_{P1})$ and U_{P1} is greater than U_{oc}. In general, the digital value of the ADP sampling output voltage will be clipped before entering the lookup table process. The working point will be limited to point $P_2\,(U_{P2},\,I_{P2})$, i.e.,

$$P_1 \rightarrow P_2 : \begin{cases} U_{P2} = U_{oc} \\ I_{P2} = I_A = I_{\mathrm{sas}}(k-1) \end{cases}. \tag{7}$$

The equivalent load resistance $R_{P2\_\mathrm{equ\_load}}(k)$ is given by

$$R_{P2\_\mathrm{equ\_load}}(k) = \frac{U_{P2}}{I_{\mathrm{sas}}(k-1)} = \frac{U_{oc}}{I_{\mathrm{sas}}(k-1)} = R_C \tag{8}$$

$$\mathrm{I_{sas}(k)} = \mathrm{Table_{RI}\left(R_{P2\_equ\_load}(k)\right)} = f\left(\mathrm{R_C}\right). \tag{9}$$

Obviously, R_C is not the target working point; hence, the convergence process will enter the next lookup table cycle. Further

$$P_3 \rightarrow P_4 : \begin{cases} U_{P4} = \mathrm{Table}_{RI}\left(R_C\right)\cdot R_B = I_{\mathrm{sas}}(k)\cdot R_B \\ I_{P4} = I_{\mathrm{sas}}(k) \end{cases}. \tag{10}$$

The equivalent load resistance calculated for the next cycle is $R_{P4\_\mathrm{equ\_load}}(k+1)$ and the target current value $I_{\mathrm{sas}}(k+2)$ is

$$R_{P4\_\mathrm{equ\_load}}(k+1) = \frac{U_{P4}}{I_{\mathrm{sas}}(k)} = \frac{I_{\mathrm{sas}}(k)\cdot R_B}{I_{\mathrm{sas}}(k)} = R_B \tag{11}$$

$$I_{\mathrm{sas}}(k+1) = \mathrm{Table}_{\mathrm{RI}}\left(R_{P4\_\mathrm{equ\_load}}(k+1)\right) = f\left(R_B\right). \tag{12}$$

In this condition, only two lookup cycles are required for convergence to the target operating point B very quickly.

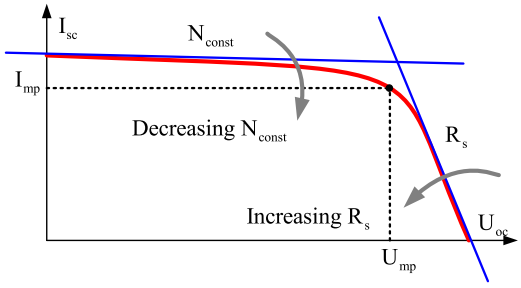


Fig. 10. Array *I–V* curve relationship of R_s, N_{const}, and I_{mp}, U_{mp}.

The above theoretical derivation and analysis show that the UI-RI hybrid lookup table method can not only improve the linearity of the entire set *I–V* curve, providing steady-state operating conditions with better stable performance; but also facilitate faster convergence to the target operating point under high-speed step switching working conditions.

C. Exponential Model for Generating UI-RI Hybrid Table

The UI data tables can be calculated using exponential model [33] equations of solar array panels, shown in (13)–(16). The following equations describe the SAS exponential model using the parameters R_s, N_{const}, and α, which are defined as functions of the four input parameter values for the OC voltage, U_{oc}, and the SC current I_{sc}. The additional parameters required by the UI table calculations are the MPP voltage U_{mp} and the MPP current I_{mp}

$$R_s = \frac{U_{oc} - U_{mp}}{I_{mp}} \tag{13}$$

$$N_{\text{const}} = \frac{\ln\left(2 - 2^{\alpha}\right)}{\ln\left(\frac{I_{mp}}{I_{sc}}\right)} \tag{14}$$

$$\alpha = \frac{U_{mp}\left(1 + \frac{R_s I_{sc}}{U_{oc}}\right) + R_s\left(I_{mp} - I_{sc}\right)}{U_{oc}} \tag{15}$$

$$U_{\text{sas}} = f(I_{\text{sas}}) = \frac{\frac{U_{oc}\ln\left(2 - \left(\frac{I_{\text{sas}}}{I_{sc}}\right)^{N_{\text{const}}}\right)}{\ln(2)} - R_s\left(I_{\text{sas}} - I_{sc}\right)}{1 + xst\frac{R_s I_{sc}}{U_{oc}}}. \tag{16}$$

Additional parameters required by the other format are N_{const}, which is strongly related to the array shunt resistance, and R_s which is essentially the output resistance of the array. The array *I–V* curve relationship of R_s, N_{const}, and I_{mp}, U_{mp} is shown in Fig. 10. Here, the slope of the "horizontal" part of the *I–V* curve is a strong function of N_{const}; the "vertical" section is a strong function of R_s, and it will generate an identical *I–V* curve. Decreasing N_{const} and increasing Rs results in decreasing I_{mp} and U_{mp}.

For the SSAS, the relationship between the output voltage and the current lies on the given *I–V* curve; hence, there is an equivalent load resistance for each operating point $R_{\text{equ\_load}}$

$$R_{\text{equ\_load}} = \frac{U_{\text{sas}}}{I_{\text{sas}}}. \tag{17}$$

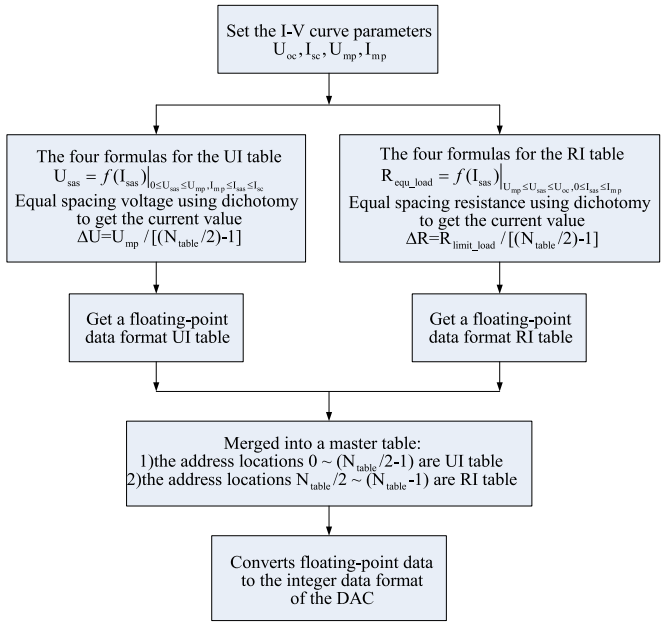


Fig. 11. Function flowchart for generating the UI-RI hybrid data lookup tables.

From the above four equations on U_{sas} and I_{sas}, the equivalent output load resistance formula can be obtained as follows:

$$R_{\text{equ\_load}} = f(I_{\text{sas}}) = \frac{\frac{U_{oc}\ln\left(2 - \left(\frac{I_{\text{sas}}}{I_{sc}}\right)^{N_{\text{const}}}\right)}{I_{\text{sas}} \times \ln(2)} - \left(R_s - \frac{I_{sc}}{I_{\text{sas}}}\right)}{1 + \frac{R_s I_{sc}}{U_{oc}}}. \tag{18}$$

Based on the known OC voltage U_{oc}, the SC current I_{sc}, and the voltage and current of the MPP, U_{mp} and I_{mp}, the UI lookup table can be calculated using the dichotomy method to obtain equal voltage spacing in a tabular form through (13)–(16). The RI lookup table can be calculated using the dichotomy method to obtain equal resistance spacing in tabular form with (13)–(15) and (18).

D. UI-RI Table Generation Method and FPGA Real-Time Lookup Table Method

Based on the exponential model described above, the remaining generation and application of the UI-RI hybrid table is divided into two major steps, i.e., completion of the functions in the computer and FPGA digital controller.

The first step is how to generate UI-RI hybrid data lookup tables, and the table generation function flowchart is shown in Fig. 11.

The UI-RI hybrid lookup table is the master table, and the number of the total points is N_{table}. In this master table, the first half of the table data corresponds to the UI data table, which inputs the voltage information to obtain the designed current value within the constant current region. The other half of the table corresponds to the RI data table, which inputs the equivalent load resistance information to obtain the designed current value within the constant voltage region. The formulas for the UI table are given by (13)–(16), and the relationship

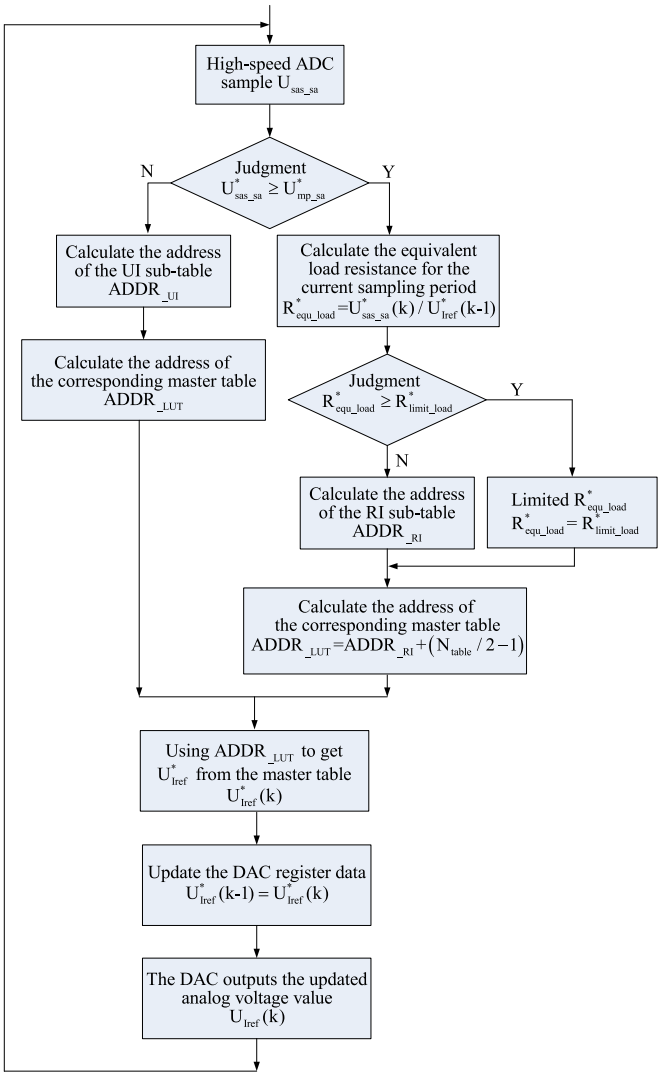


Fig. 12. Program function flowchart of how to accurately calculate the corresponding data table address of the UI-RI hybrid table for the PFGA digital controller.

between $U_{\rm sas}$ and $I_{\rm sas}$ is as follows:

$$U_{\rm sas} = f(I_{\rm sas})|_{0\leq U_{\rm sas}\leq U_{mp},I_{mp}\leq I_{\rm sas}\leq I_{sc}}. \tag{19}$$

The equal voltage spacing ΔU is calculated as follows:

$$\Delta {\rm U} = {\rm U}_{mp}/[({\rm N}_{\rm table}/2) - 1. \tag{20}$$

The formulas for the RI table are given by (13)–(15) and (18), and the relationship between $R_{\rm equ\_load}$ and $I_{\rm sas}$ is as follows:

$$R_{\rm equ\_load} = f(I_{\rm sas})|_{U_{\rm mp}\leq U_{\rm sas}\leq U_{oc},0\leq I_{\rm sas}\leq I_{mp}}. \tag{21}$$

The equal resistance spacing ΔR is calculated as follows:

$$\Delta R = R_{\rm limit\_load}/[(N_{\rm table}/2) - 1] \tag{22}$$

where $R_{\rm limit\_load}$ is the maximum equivalent output load resistance in the equivalent OC voltage working condition when the output current is quite small for the current output type SSAS [34]. The UI and RI subtables can be obtained separately by calculation, and the master table is the hybrid lookup table, which merges the two subtables together by reasonable allocation of the corresponding table data address locations. The address locations from 0 to $(N_{\rm table}/2-1)$ hold the contents of the UI data table, and the address locations from $(N_{\rm table}/2)$ to $N_{\rm table}$ hold the contents of the RI data table.

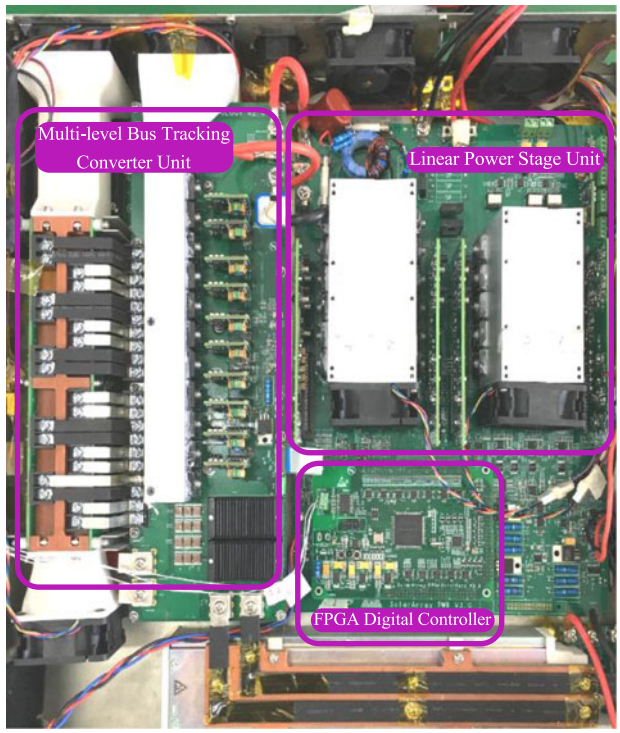


Fig. 13. Photograph of the prototype.

TABLE I
I–V CURVE SETTING FOR THE EXPERIMENT

Setting parameters	The setting *I–V* Curve
Open-circuit voltage (U_{oc})	120 V
Short-circuit current (I_{sc})	18 A
The maximum power point voltage (U_{mp})	100 V
The maximum power point current (I_{mp})	13 A

The second step is how to accurately calculate the corresponding data table address of the UI-RI hybrid table at a given sampling voltage and find the corresponding expected current value for the FPGA digital controller. The program function flowchart is shown in Fig. 12.

The above two functional flowcharts can accurately calculate the required UI-RI hybrid data table, and the FPGA can calculate and give the corresponding current expectations at the current operating point with minimum digital delay. The lookup table outer loop has a stable operation state within the full range of the set *I–V* curve, and it achieves high-speed convergence to the target point under different working point step switching conditions.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed high-power SSAS that uses the UI-RI hybrid lookup table method was tested under five typical

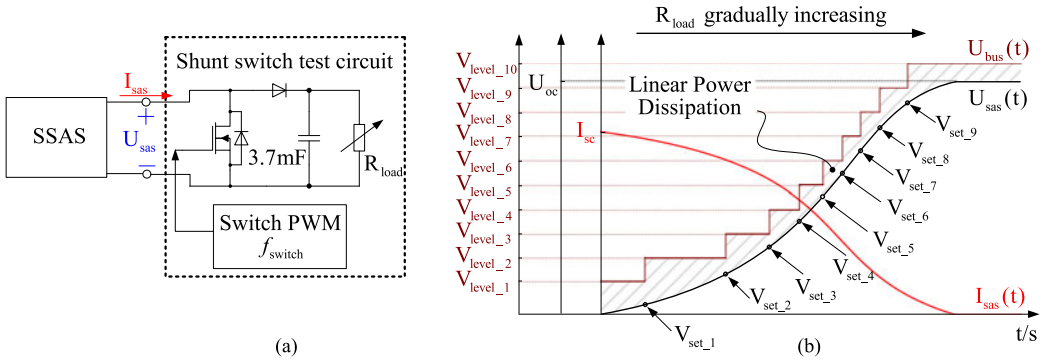


Fig. 14. Testing circuit and expected steady waveform diagram. (a) Testing circuit for steady response experiment with $M_{\rm switch}$ in the OFF state, (b) Diagram showing changes in multilevel bus voltage $U_{\rm bus}(t)$ and output current $I_{asa}(t)$ as $U_{\rm sas}(s)$ increases.

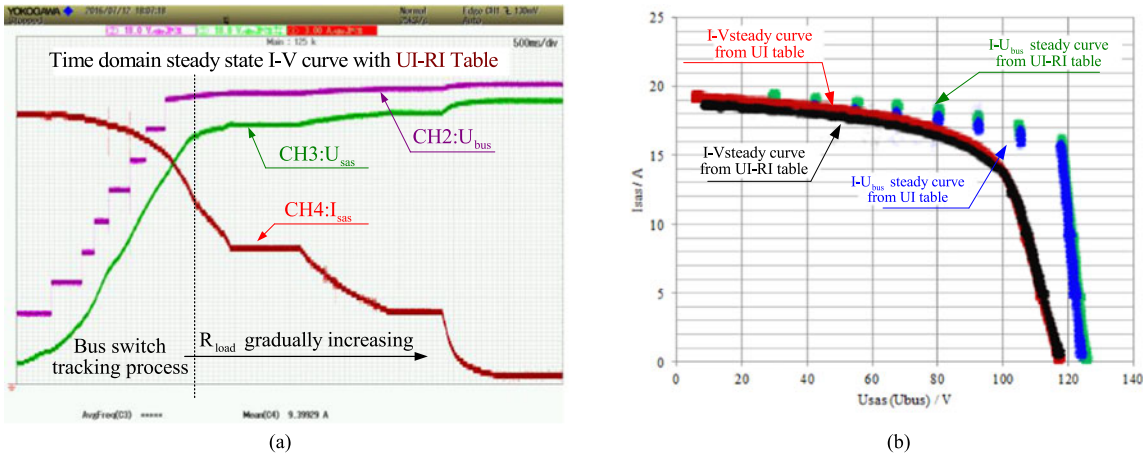


Fig. 15. Steady output current and voltage of the proposed SSAS. (a) Time-domain waveforms of SSAS output voltage $U_{\rm sas}$ and output current $I_{\rm sas}$, (b) *I–V* curve output of the experimental data from the oscilloscope.

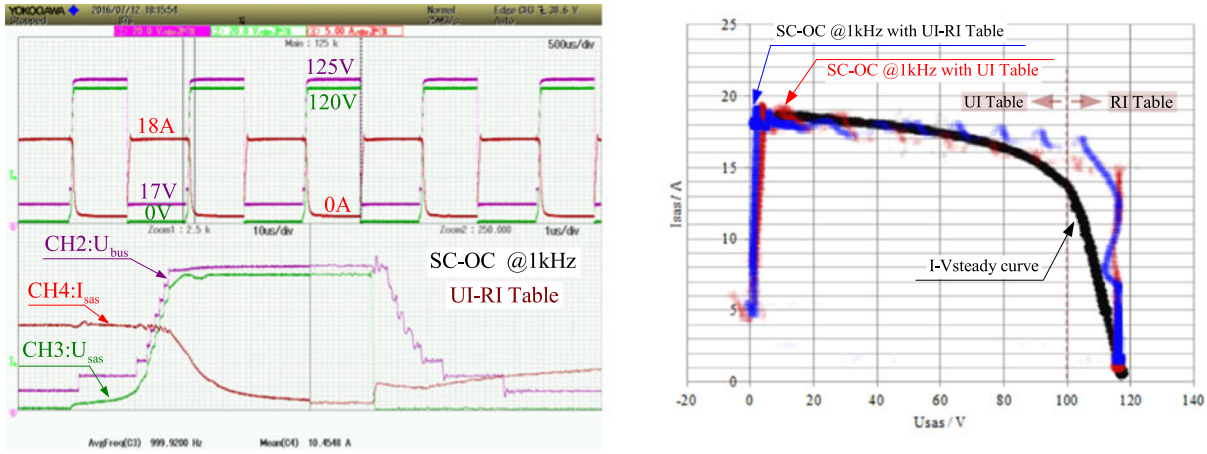
operating conditions usually encountered in nonterrestrial applications. These include the steady-state response along a static *I–V* curve; shunt-switching change in the output load between the SC and OC states, which represent the harshest working conditions of the SSAS at different switching frequencies; the series-switching change in the output load between the OC and rated-load (RL) states at different switching frequencies; and the output-noise testing. Here, the different experimental data distribution waveforms obtained using the single UI and UI-RI hybrid lookup table methods are compared. In addition, a fifth test is conducted wherein the spacecraft power converter with a shunt regulator structure is tested. A photograph of the prototype, which is proposed in [27], is shown in Fig. 13.

There are 20 linear VCCSs connected in parallel to provide a maximum current output of 20 A. Four dc fans operating at their highest speeds are installed at both ends of the radiator in order to dissipate the heat. The sealed air passage is not shown in this photograph so that the hardware circuit structure can be observed clearly. The setting of the *I–V* power curves is different under different testing conditions, as shown in Table I.

A. Experimental Comparison of Steady-State Response

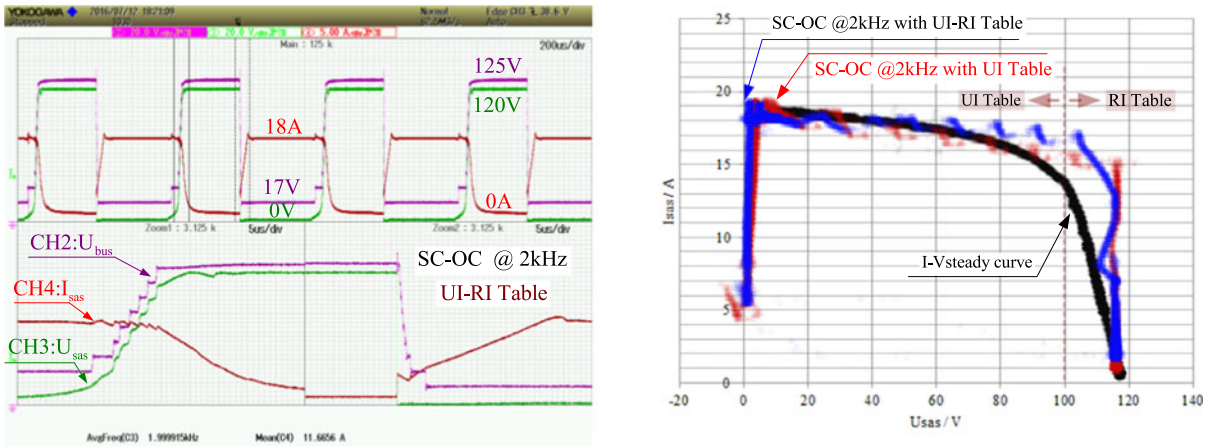
To examine the steady-state response of the SSAS, the output voltage $U_{\rm sas}$ and output current $I_{\rm sas}$ were tested by gradually increasing the resistance of the connected $R_{\rm load}$. The *I–V* curve specifications to be set for the experiment are summarized in Table I. The testing circuit is shown in Fig. 14(a) with the switching MOSFET $M_{\rm switch}$ kept in the OFF state so that the SSAS output terminal is connected with a capacitive load. Fig. 14(b) shows the expected steady waveform. $U_{\rm bus}(t)$ will always track the output voltage $U_{\rm sas}(t)$, and it will flip to the next adjacent level when $U_{\rm sas}(t)$ reaches the corresponding set voltage $V_{{\rm set}\_i}$. A detailed description has been provided in the previous paper. The output current $I_{\rm sas}(t)$ will decrease gradually owing to the working logic of the set of *I–V* curves. The partial area of shadows is the linear power dissipation $P_{\rm dis\_lin}$; $P_{\rm dis\_lin}$ can be controlled by reasonable design of the multilevel converter parameters.

Fig. 15 shows the steady-state response waveform of the SSAS with the UI-RI hybrid lookup table method. Fig. 15(a) shows the time-domain output voltage $U_{\rm sas}$ and the output current $I_{\rm sas}$. The operating point of the *I–V* curve changes from the SC region to an approximate OC region, with a gradual change in the resistance of the sliding rheostat connected to the output terminal of the SSAS. Fig. 15(b) shows the experimental data of $U_{\rm sas}$ and $I_{\rm sas}$, from the recorded oscilloscope data; the data are plotted in the second coordinate, with $U_{\rm sas}$ on the horizontal axis and $I_{\rm sas}$ on the vertical axis. To compare the differences between the two lookup table methods, the steady-state *I–V* curve using



(a) (b)

Fig. 16. Step working point between SC and OC at $f_{\mathrm{switch}} = 1$ kHz: (a) time-domain waveform of SSAS with UI-RI hybrid lookup table, (b) comparison of distribution of step switching data in SSAS output steady *I–V* curve with UI lookup table and UI-RI hybrid lookup table.



(a) (b)

Fig. 17. Step working point between SC and OC at $f_{\mathrm{switch}} = 2$ kHz: (a) time-domain waveform of SSAS with UI-RI hybrid lookup table, (b) comparison of distribution of step switching data in SSAS output steady *I–V* curve with UI lookup table and UI-RI hybrid lookup table.

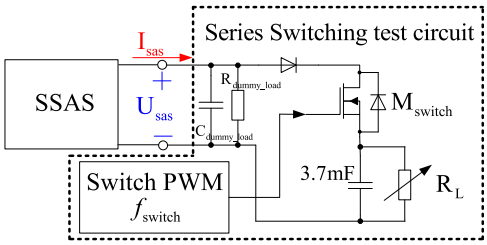


Fig. 18. Series-switching test circuit diagram.

the UI lookup method and the steady-state *I–V* curve using the UI-RI hybrid lookup method are shown in the same distribution diagram. The scatter plots of U_{bus} and U_{sas} are also shown in Fig. 15(b).

From the results of the steady-state experiment, it can be seen that the output *I–V* curve of the SSAS is the setting *I–V* curve, and the multilevel bus tracking converter can track U_{sas} well. A comparison with the steady experiment distribution waveform shows that, regardless of whether the single UI table lookup method or UI-RI hybrid lookup table method is used, the impact of the steady-state experimental data is not obvious. This is because for the SSAS based on the high-speed FPGA platform with the two lookup table methods, the steady-state process can converge to the desired operating point of the set *I–V* curve.

B. Experimental Comparison of Shunt-Switching Testing

The shunt-switching regulation experiment analyses the step from the SC to the OC, which is the harshest working condition for an SAS. As discussed in Section III, the UI-RI tables have a wide lookup linear range in the entire set *I–V* curve, and the RI table part shows fast convergence to the target

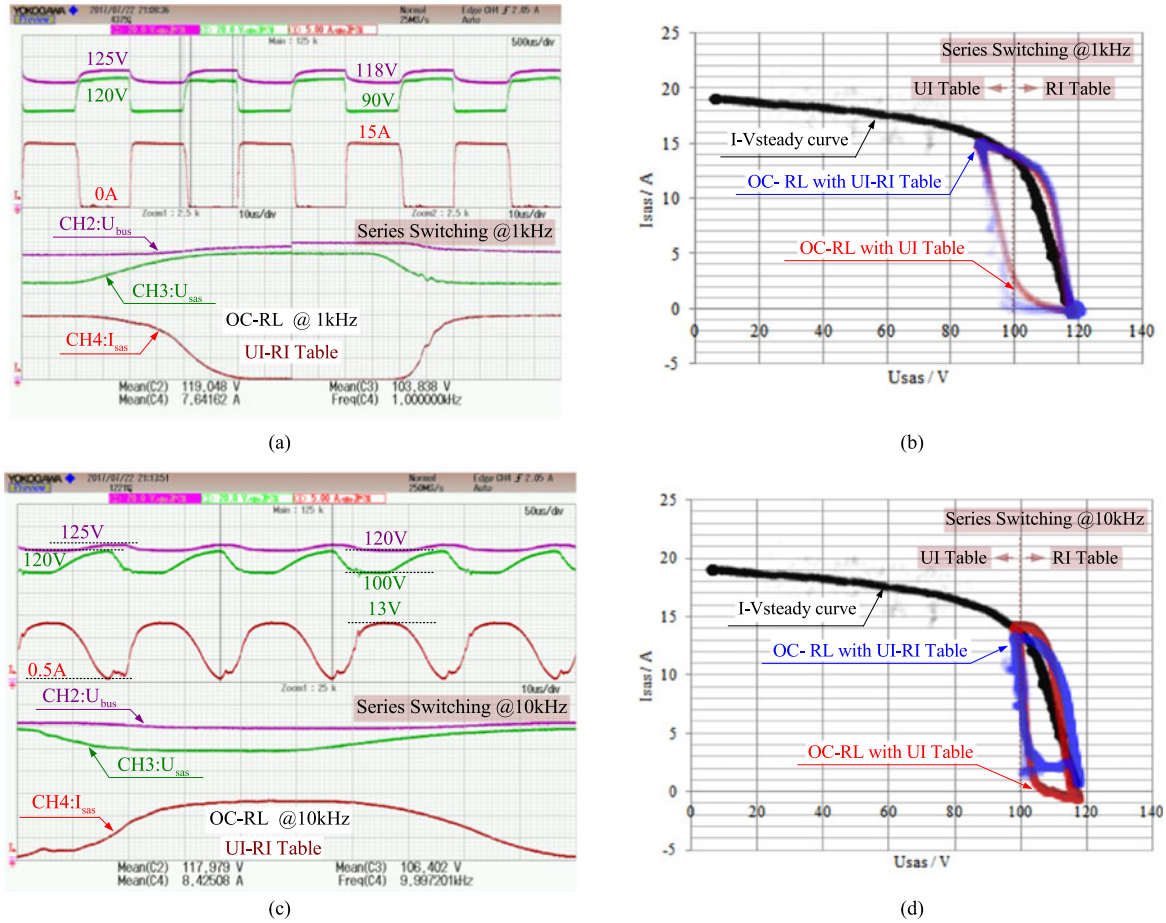


Fig. 19. Series-switching test between the OC and RL under different f_{switch} values. (a) Time-domain waveform of SSAS using the UI-RI hybrid lookup table at $f_{\mathrm{switch}} = 1$ kHz. (b) Comparison of the distribution of series-switching data in the SSAS output steady *I–V* curve using the UI and UI-RI hybrid lookup tables at $f_{\mathrm{switch}} = 1$ kHz. (c) Time-domain waveform of SSAS using the UI-RI hybrid lookup table at $f_{\mathrm{switch}} = 10$ kHz. (d) Comparison of the distribution of series-switching data in the SSAS output steady *I–V* curve using UI and UI-RI hybrid lookup tables at $f_{\mathrm{switch}} = 10$ kHz.

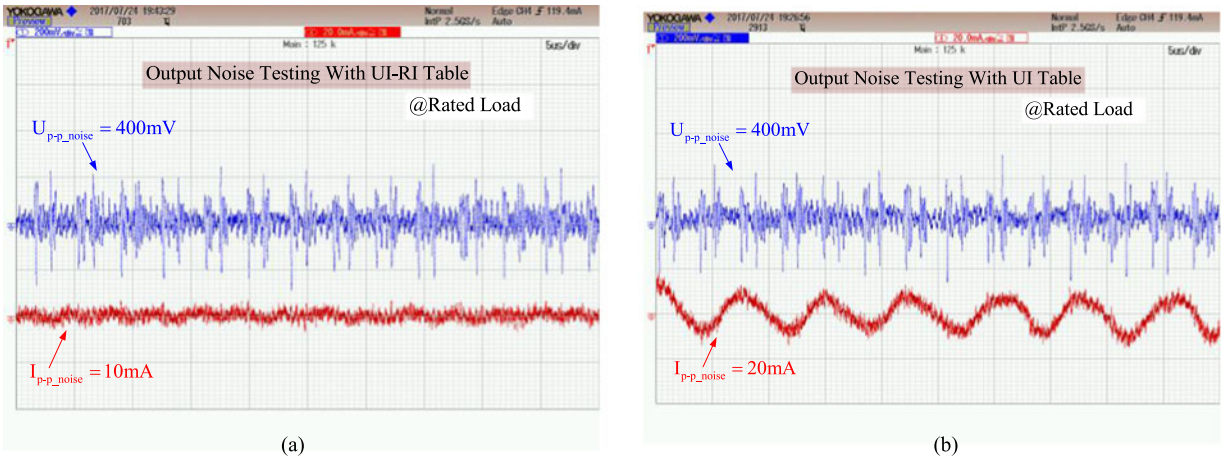
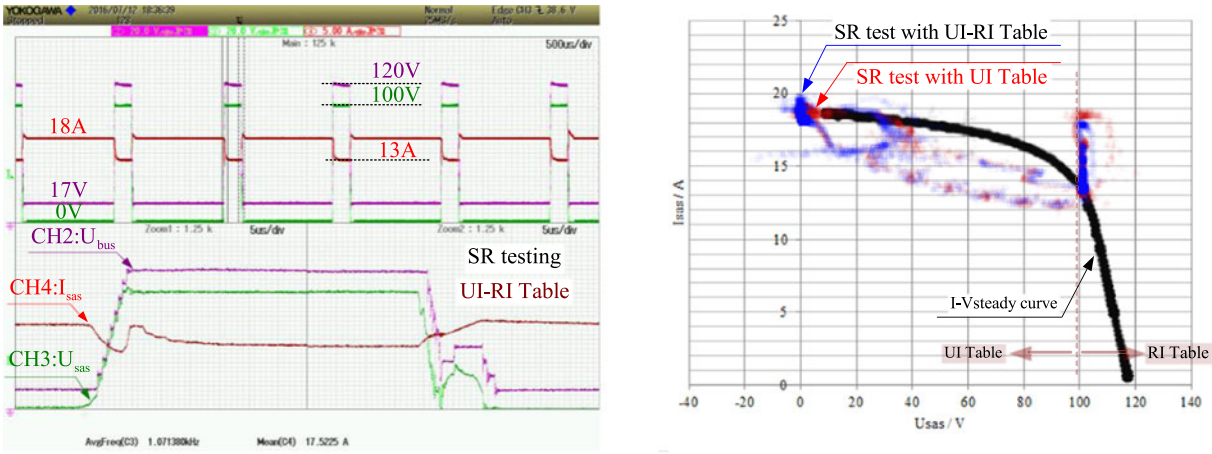


Fig. 20. Comparison of the output-noise test results of the SSAS using different lookup table methods: (a) using the UI-RI hybrid lookup table method, and (b) using the UI lookup table method.

operating point. To better verify the fast convergence characteristics, the stepping test frequency is 1 and 2 kHz. Figs. 16 and 17 show the experimental results at f_{switch} of 1 kHz and 2 kHz, respectively.

Figs. 16(a) and 17(a) show that the time-domain waveform of the step from the SC to the OC at f_{switch} of 1 and 2 kHz, for the designed switched working points, (0 V, 18 A) and (120 V, 0 A), is built steadily and quickly without any spike current. The



(a) (b)

Fig. 21. Experimental results with a shunt switching regulator: (a) time-domain waveform of SSAS with UI-RI hybrid lookup table, (b) comparison of distribution of step switching data in SSAS output steady *I–V* curve with UI lookup table and UI-RI hybrid lookup table.

time-domain waveform also shows quick convergence to the set *I–V* curve corresponding to the operating point using the UI-RI hybrid lookup table method.

The comparison of the distribution of step switching data in the SSAS output steady *I–V* curve with the UI lookup table and UI-RI hybrid lookup table is shown in Figs. 16(b) and 17(b); the blue data distribution curve is the experiment result using the UI-RI hybrid table, and the red curve is the experiment result using the UI table.

As shown in Figs. 16(b) and 17(b), in the section with the UI table part, the blue and red data distribution trends and trajectories nearly overlap; however, in the section with the RI table part, the blue data distribution trend and trajectory are more inclined to converge to the target set *I–V* curve than the red data trajectory, which is the UI table nonlinear performance in the right part of the MPP of the set *I–V* curve. Hence, it can be concluded that the use of the UI-RI hybrid lookup table method is more conducive to periodic high-frequency switching applications.

C. Experimental Comparison of Series-Switching Test

The series switching test is also a very important process in universal SSAS. In fact, the SSAS proposed in this paper is designed mainly for the shunt regulator architecture of the space power-system test application because the SSAS structure is a current-output type and is only fit for capacitive load, as discussed in [27]. However, the high dynamic switching performance using the UI-RI hybrid lookup table is more reliable in the series-switching test because the RI sub-table is mainly used in the constant voltage area in the *I–V* curve. By adding a capacitive dummy load branch, which was described in [34], we can easily test the series-switching performance of the SSAS. The series-switching test circuit is shown in Fig. 18; $\mathrm{R_{dummy\_load}} = 300\,\Omega$, and $\mathrm{C_{dummy\_load}} = 20\,\mu\mathrm{F}$.

The series-switching experimental test results at 1 and 10 kHz are shown in Fig. 19. The switching working points are between OC and RL, where R_L shown in Fig. 18 is 10 Ω. Fig. 19(a) and (b) shows the test results at 1 kHz, and Fig. 19(a) shows the time-domain waveform using the UI-RI hybrid lookup table. Fig. 19(b) shows the comparison of the distribution of the series-switching data in the SSAS output steady *I–V* curve using the UI and UI-RI hybrid lookup tables. For a better test process, in the high-speed convergence performance of the UI-RI hybrid lookup table method, the switching frequency is improved to 10 kHz, especially under a step-switching working condition, and the test results are shown in Fig. 19(c) and (d).

Fig. 19(a) and (b) shows that the two switching working points can be arrived using the UI-RI hybrid lookup table method. Through the comparison of the data distribution diagrams, the distribution of the data points during the switching process using the UI-RI hybrid lookup table method is significantly less than that using the UI lookup table method. When f_{switch} is improved to 10 kHz, as shown in Figs. 19(c) and (d), the two switching working points can also be reached, and the distribution of the data points during the switching process using the UI-RI hybrid lookup table method is more inclined to converge to the desired I–V curve compared with that using the UI lookup table method. The experimental results verify the analysis presented in Section III, that is, the UI-RI hybrid lookup table method yields better convergence performance.

D. Experimental Comparison of the Output Noise Test

Output noise testing is an important process proposed in [2]. Its main purpose is to evaluate the influence of the SAS output noise as a test power supply to the device under test. Fig. 20 shows the comparison of actual output noise performance of the SSAS using different lookup table methods. The test condition is with the SSAS output ON and external load is RL = 10 Ω.

Because the SSAS power output stage is a linear voltage-controlled current source, the peak-to-peak value of the output current noise is quite small whether the UI or UI-RI hybrid look-up table method is used. From the comparison of the experimental results, the peak value of the current noise obtained by the UI-RI hybrid look-up table is obviously smaller than that by the UI lookup table method at the same 400-mV peak-to-peak

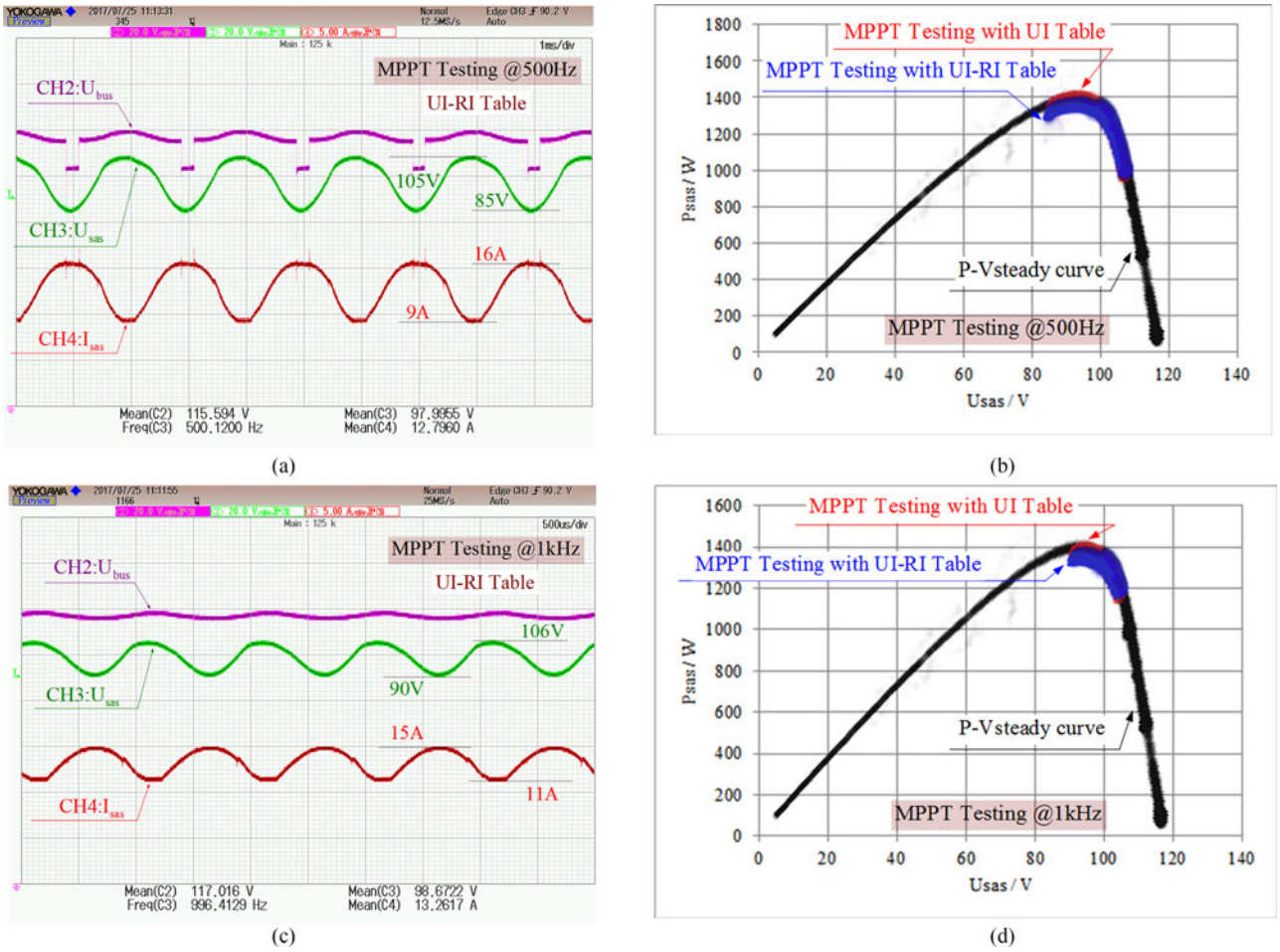


Fig. 22. Test results of the MPPT testing under different MPPT sweeping frequencies. (a) Time-domain waveform of SSAS using the UI-RI hybrid lookup table with MPPT sweeping frequency of 500 Hz. (b) Comparison of the distribution of the experimental data in the SSAS output steady *P–V* curve using the UI and UI-RI hybrid lookup tables with MPPT sweeping frequency of 500 Hz. (c) Time-domain waveform of SSAS using the UI-RI hybrid lookup table with MPPT sweeping frequency of 1 kHz. (d) Comparison of the distribution of experimental data in the SSAS output steady *P–V* curve using UI and UI-RI hybrid lookup tables with MPPT sweeping frequency of 1 kHz.

voltage noise. An ac frequency component with 7-μs oscillation period is also present using the UI lookup table method. The experimental results verify the analysis presented in Section III, that is, the UI-RI hybrid look-up table method has a better output-loop control linearity.

E. Testing and Evaluation of SR Regulator

Our final goal is to test the space power system, and [35] presented that the working state is not harsh for testing the SR of SSAS because the actual switching frequency is quite low. We obtain the experimental results shown in Fig. 21. For better clarity, the contrasting test result waveforms from the SSAS with the UI lookup table and the UI-RI hybrid lookup table methods are shown in Fig. 21. Here, $U_{\rm bus}$ is the SSAS multilevel bus tracking voltage and $U_{\rm sas}$ and $I_{\rm sas}$ are the SSAS output voltage and current, respectively.

In fact, the test with SR is equivalent to step switching from the SC load to a normal load, and this working condition is relatively easy to complete well for the SSAS. Fig. 21(a) shows the time-domain waveform of the SSAS and (b) shows the data distribution; the SSAS can reach the two operating points (0 V, 18 A) and (100 V, 13 A) in a very steady manner with fast response. Some unaltered data points are distributed around the set *I–V* curve because of the influence of multilevel tracking switching.

However, the step switching working points are included in the UI table part of the UI-RI hybrid lookup table. Thus, the difference in the experiment data distribution waveforms of the two lookup table methods is very small. From Fig. 21, it can be concluded that the experiment results for SR are not influenced by different lookup table methods.

F. Experimental Comparison of MPPT Test

MPPT testing is an important test process proposed in [2] for SSAS. Its main purpose is to evaluate whether the MPP of the *I--V* curve from the output power of SSAS could be found. This test method refers to the method presented in [2]. The $U_{\rm sas}$ range is swept from 85 to 105 V at 500-Hz MPPT sweeping frequency. The experimental results are shown in Fig. 22(a) and (b). Then, the MPPT sweeping frequency is increased to 1 kHz, and $U_{\rm sas}$

range is swept from 90 to 106 V. The experimental results are shown in Fig. 22(c) and (d). Fig. 22(a) and (c) shows that $U_{\rm sas}$ is the output voltage of SSAS, $I_{\rm sas}$ is the output current of SSAS, and $U_{\rm bus}$ is the multilevel bus tracking voltage of SSAS. Fig. 22(b) and (d) shows the comparison of the distribution of the experimental data in the SSAS output steady P-V curve using the UI and UI-RI hybrid lookup tables under different MPPT sweeping frequencies.

Fig. 22 shows that the SSAS can determine the MPP even at 1 kHz of MPPT sweep frequency whether the UI or UI-RI hybrid lookup table method is used. Fig. 22(b) and (d) shows that the blue data distribution trends of the UI-RI hybrid lookup table method and the red data distribution trends of the UI lookup table method nearly overlap because the UI-RI hybrid table is segmented at the MPP. The difference between the experimental data distributions is not sufficiently obvious to verify the advantages of the UI-RI hybrid lookup table, however, it shows that the SSAS is also available for testing the spacecraft power system with MPPT operating mode.

V. Conclusion

We have proposed and demonstrated a SSAS system with high power-output capability and high dynamic performance using a novel UI-RI hybrid lookup table method. The results indicated that a 2.4-kW SSAS could simulate a shunt-switching test from the SC state to the OC state at a stepping frequency of 2 kHz using the UI-RI hybrid lookup table method, which is the harshest working condition for a SSAS. It could also simulate a series-switching test from the OC state to RL at a switching frequency of 10 kHz, which verifies the high-speed convergence performance of the UI-RI hybrid lookup table method. Furthermore, the experimental data-point distribution trajectory of the switching process was shown to tend more to converge on the desired *I–V* curve compared with the single UI lookup table method.

In addition, experimental test results of the single UI lookup table method were presented for comparison under the same working conditions. The experimental results showed that the proposed UI-RI hybrid lookup table method has obvious advantages under periodic high-frequency operating point step switching conditions. Thus, this study proposed a state-of-the-art solution for simulating different types of nonlinear *I–V* curves for both nonterrestrial and territorial applications.

However, it must be acknowledged that the proposed method has several limitations. In the UI-RI synthesis table at the splicing point, the lookup table results of the UI sub-table and the RI sub-table differed during the steady-state experiment. Thus, there is a clear inflection point in the experimental distribution waveform. This is due to the MPP for the table demarcation point; the linearity is not sufficiently good for the RI sub-table, and a lookup table hysteresis should be included in the program to achieve seamless results of the hybrid table. Because the RI table needs to set a maximum equivalent load resistance to the equivalent OC operating point, it cannot achieve the OC working state without any capacitive dummy load branch.

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