Optimized Design of Space Solar Array Simulator With Novel Three-Port Linear Power Composite Transistor Based on Multiple Cascaded SiC-JFETs

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***Abstract*—Space solar array simulators (SSASs), which are used for testing space power systems, generally utilize linear power topologies owing to their fast dynamic performance and satisfactory simulation accuracy. However, to output a medium power level from a linear-power-topology SSAS, multiple parallel linear voltage-controlled current sources are required for addressing the redundant power dissipation, thereby limiting the overall mechanical structure and volume optimization; in addition, the presence of multiple parallel sources results in a complex circuit structure with poor reliability. In this context, in this study, we propose a novel three-port linear power composite transistor as a linear power dissipation device, which is composed of multiple cascaded SiC-JFETs to improve on the above-mentioned shortcomings. The proposed 510-W optimized SSAS requires only eight parallel linear current-source paths to form a linear power stage and uses a high-speed field-programmable gate array (FPGA) digital controller to quickly react to a load step between short circuit and open circuit (the harshest working condition for a solar array simulator) at a 1-kHz stepping frequency. Further, the device can react to a load step between short circuit and the nominal working point at 10-kHz stepping frequency, thus, offering a better dynamic performance over other similar devices.**

***Index Terms*—High dynamic performance, I–V curve, linear power stage, multiple cascaded SiC-JFETs, solar array simulator (SAS).**

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I. Introduction

IN THE field of space power, a vast majority of satellite power is harnessed from solar array panels. The performance of the satellite power supply directly affects the performance and working life of the satellite and significantly impacts normal satellite operation. Thus, it is of significant interest to simulate and test the satellite power system to improve its performance and reliability. Satellite space working conditions are harsh and complex, and previous reports [1] have indicated that solar panels experience gradual and abrupt power losses due to the typical space environment containing ultraviolet radiation and trapped electrons and protons. A reliable satellite power system should not only maintain a normal and stable bus power output under solar-array-panel windsurfing output power conditions, but also in the solar array panel with a significant reduction in the arc inception voltage after long operational periods [2]. However, a power system under test on the ground cannot use actual solar array panels to reproduce the satellite conditions in the space orbit in the working state, and therefore, space solar array simulators (SSASs) are required to simulate the power output of the solar array panel under space working conditions.

The SSAS forms an important part of the satellite power system, and its main task is to provide power for each subsystem of the satellite in place of the solar array panel during the ground testing period. The sequential switching shunt regulator (S3R, introduced by European Space Agency in the seventies) shown in Fig. 1 is most commonly used in satellite solar array power generation subsystems [3]. The main bus voltage of the S3R is always regulated, which means that the load for the SSAS is a high-frequency step switching load between a nominal load and short circuit (SC). The S3R uses a hysteresis controller to regulate the bus voltage, and the shunt switching frequency varies with the S3R load [4]. The maximum shunt switching frequency of the S3R is 5 kHz [5], and therefore, the SSAS should quickly react to shunt switching between the nominal load and SC at this stepping frequency.

Several recent studies on solar array simulators (SASs) have mainly focused on different power stage topologies to provide outputs as per the designed I–V power curves. High power output levels require the use of switch topologies such as full-bridge structures [6], buck converters with two-stage *LC* output filter

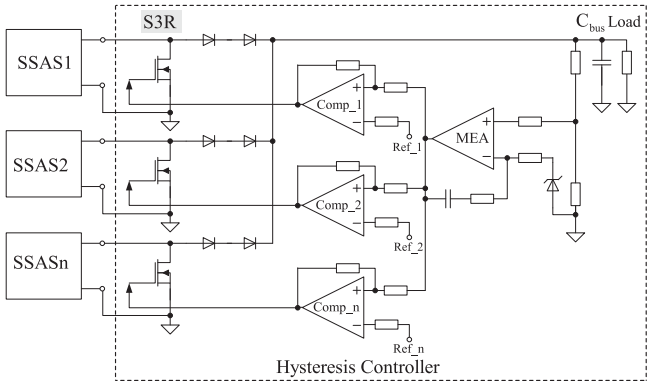

Fig. 1. S3R acts as device under test for the SSAS.

[7] or *LCL* output filter [8], and bidirectional dc–dc converters [9] for power conversion. Some studies have also used off-the-shelf dc power supplies by injecting variable analog voltage into the voltage feedback loop of the supply [10], and these supplies are mainly used for testing inverters for photovoltaic applications. The primary goals of SAS designs include design simplicity [11] and low cost [12], and such simulators are mainly used in laboratory application for evaluating MPPT algorithms. In [13], Vongkoon and Liutanakul use a classical dc–dc buck converter as the power stage with a digital R-S-T controller for achieving an accurate and steady I–V curve emulation with a response time of ∼5 ms to step load change. However, the results of such studies are more applicable to industrial or civil inverter equipment testing than space power testing; the above-mentioned dc–dc buck converter cannot be used in spacecraft power system testing applications mainly because of its relatively slow dynamic response capability as well as relatively low I–V curve simulation accuracy.

Reference [14] is a typical early work that introduces the concept of SASs used in the aerospace field, and the authors in their approach use operational and circuit features to simulate the dynamic electrical output characteristics of a solar array in orbital flight with a 1-ms dynamic response to sudden load changes. In order to improve the power handling capacity of the SSAS, one study [15] proposed the idea of modularity to design and construct satellite MPPT PV systems, similar to the envelope tracking power supply [16]. Another study [17] proposed a highly dynamic nonlinear PV simulator consisting of a fourth-order output filter buck converter and a novel nonlinear small-signal reference generator with a rapid settling time of only 10 μs. The system could respond to a step changing load from the nominal working state to open circuit (OC) at 1 kHz under the series switching regulator structure testing condition, which is not suitable for the S3R structure. In order to provide improved testing of spacecraft power supply systems with shunt regulator architecture, Jin *et al.* [18] proposed a linear power stage with multipath current sources in parallel to achieve an ultrafast dynamic performance for the S3R, which can respond to a 50-kHz step switching between the nominal operation point and SC operation point. Meanwhile, another design [19] was proposed to obtain a higher power handling capacity with a high dynamic performance comparable with similar SAS products, and this design is suitable for testing high power shunt regulators.

Our proposed optimized SSAS is an improvement on the SSAS proposed in [18]. We propose a novel three-port linear power composite transistor with three cascaded SiC-JFETs as a linear power dissipation device, which can considerably reduce the number of parallel current-source paths, thereby simplifying the circuit structure and improving the reliability and output current control accuracy of the multiple parallel linear current-source paths.

II. Proposed SSAS

A. Proposed System Schematic

The proposed system schematic shown in Fig. 2 is an optimized version of the one in [18], with a similar system configuration consisting of two main parts: the linear power stage and the FPGA digital controller.

The linear power stage proposed in this study with only eight parallel current sources is an optimized solution for the previous one with 20 parallel current-source paths to overcome the problem of poor reliability and complex circuit structure. The control principle of the single linear current source is similar to that in [18], and each current source has identical parameters, outputting the same path current with a certain reference voltage. The output path current is proportional to the reference voltage provided. The relationship between U_{Iref} and I_{sas} is as follows:

$$I_{\mathrm{sas}} = N \cdot I_{\mathrm{path}} = N \cdot K_I \cdot U_{\mathrm{Iref}} \tag{1}$$

where N denotes the number of linear current sources with identical parameters, I_{path} is the current of a single current path, and K_I is the scale factor of the given reference voltage. The number of current paths (N) depends on the designed maximum power output and the dynamic performance required.

The digital controller controls the output power current according to the output voltage of the SSAS and ensures that the redundant power dissipates in the linear power stage so that the designed I–V power curves are outputted for the SSAS. In this study, the digital controller hardware and the program are set to operate on the same platform to better verify that our optimized linear power stage can replace the previous linear power stage described in [18], with a slight compromise of the dynamic response performance.

B. Novel Linear Current-Source Path Circuit Design

The proposed linear current-source schematic for a single path is presented in Fig. 3(a). It consists of a driving circuit, a power stage circuit also called the current amplifier circuit, a differential current sampling circuit, and a compensating circuit [20]. The input is the controlled reference voltage U_{Iref} and the output is the power current I_{path} through the three-port linear power composite transistor [21], [22]. This optimized linear current source includes a driving and a compensating circuit, compared to a traditional linear current-source structure, to

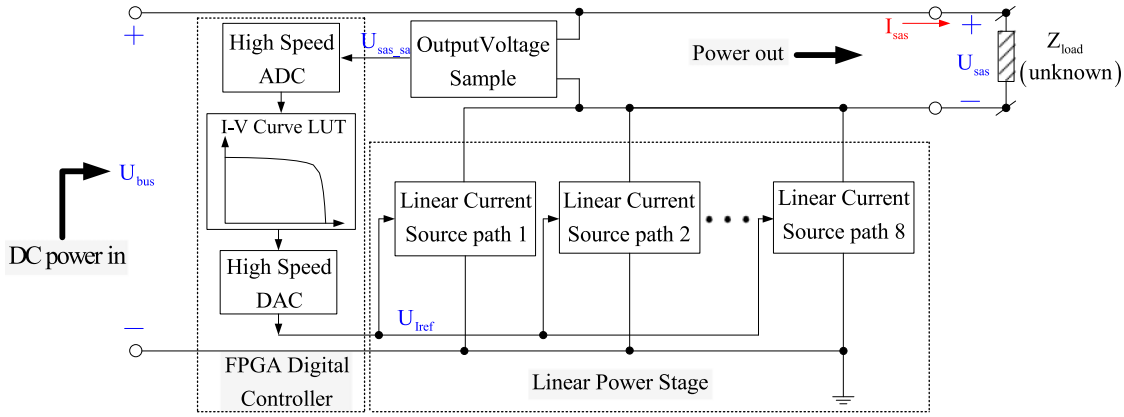

Fig. 2. Proposed system configuration.

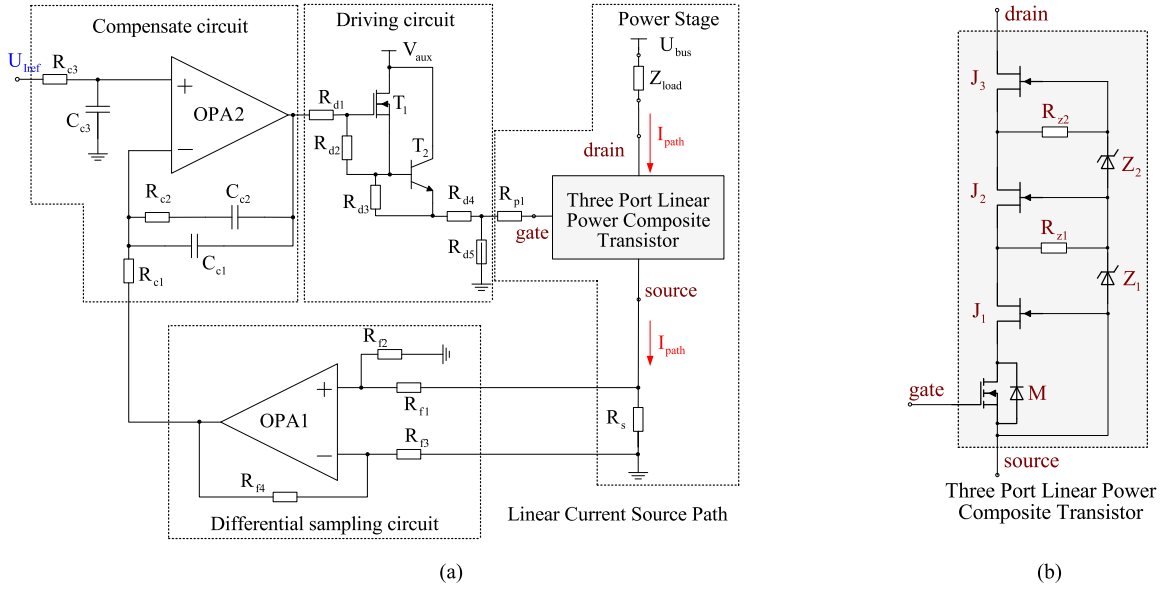

Fig. 3. Single path high-bandwidth linear current-source design. (a) Circuit schematic and (b) schematic of the three-port linear power composite transistor.

easily realize multipath paralleling. Differential current sampling and driving circuits are beneficial, if the physical distances from the power stage are considerable. This enables power MOSFETs at high temperatures to be located far away from the control circuit, decreasing the influences of the nonideal factors.

The three-port linear power composite transistor circuit is mainly composed of three cascaded SiC-JFETs, J_1, J_2, and J_3 in series with a MOSFET, M, at the bottom of the structure, responsible for linear power dissipation. J_1, J_2, and J_3 work in the constant current saturation zone or in a conductive state, whereas, M always works in the constant current saturation zone. Zener diodes Z_1 and Z_2 are used to stabilize the voltage characteristics for limiting the voltage difference between the cascaded JFET drain and source such that the maximum heat consumption in each JFET can be limited. R_{z1} and R_{z2} are used to ensure that the Zener diodes can reliably enter the reverse breakdown working state [23].

As per the structural principle of the above analysis, a single current-source path can handle the power dissipation as follows:

$$P_{\text{Lin\_1path\_optimized}} = p \cdot P_{\text{Lin\_1path}} \tag{2}$$

where $P_{\text{Lin\_1path}}$ is the maximum power dissipation of a traditional linear current source with a single power MOSFET for handling the entire linear power dissipation, p is the number of cascaded JFETs, and $P_{\text{Lin\_1path\_optimized}}$ is the maximum power dissipation of the proposed optimized linear current path. Using the three-port linear power composite transistor as the linear power dissipation device can considerably decrease the number of parallel current-source paths, optimizing the mechanical structure of the SSAS, improving the loop stability, and further increasing the power handling capacity of the SSAS.

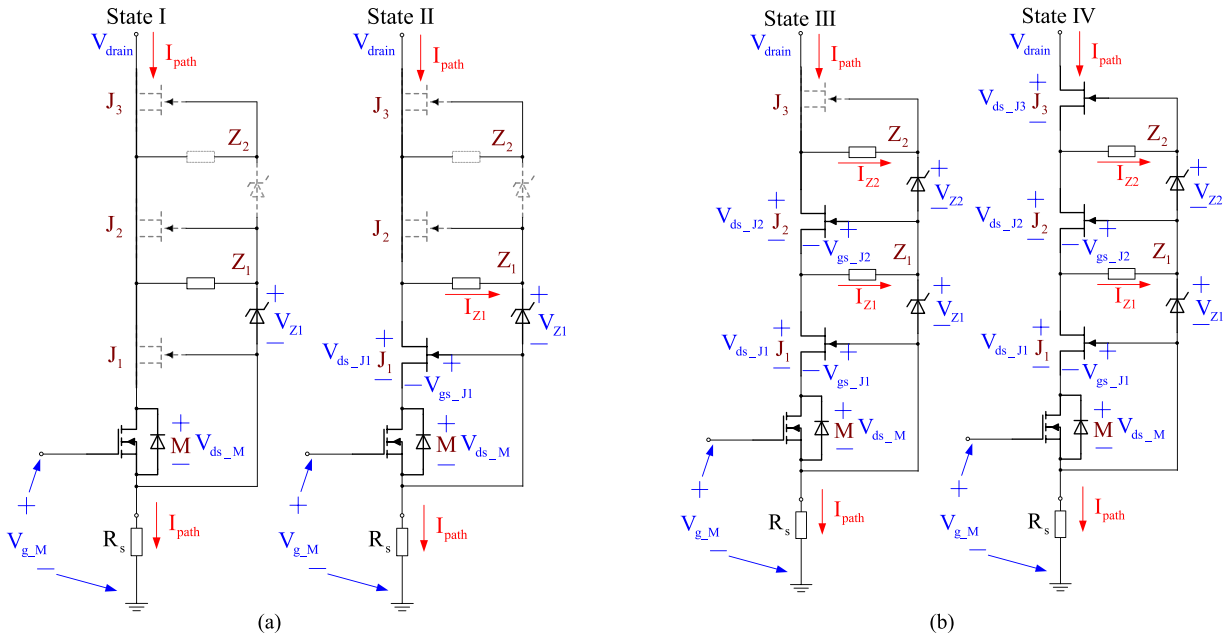

Fig. 4. Equivalent circuit under different operating state conditions. (a) Equivalent circuit of states I and II and (b) equivalent circuit of states III and IV.

C. Working-State Analysis of Three-Port Linear Power Composite Transistor

In the proposed three-port linear power composite transistor with three same-type JFETs in cascade, the working state can be changed on varying the equivalent drain voltage of the three-port linear power composite transistor $V_{\rm drain}$. By varying the $V_{\rm drain}$ voltage, the entire working state of the three-port linear power composite transistor can be divided into four different working states; the equivalent circuit of each is shown in Fig. 4 and the corresponding key operation voltage analysis waveforms, in the various states, are shown in Fig. 5.

State I: In this state, the voltage range of $V_{\rm drain}$ is as follows:

$$V_{\rm drain} < |V_{gs\_J\_sat}| \tag{3}$$

where $V_{\rm gs\_J\_sat}$ is the voltage between the gate and source of the chosen JFET, when working in the linear constant current saturation zone, where the constant current value is $I_{\rm path}$.

In this working state, J_1, J_2, and J_3 are in a conducting state, M is in the linear constant current saturation zone, and Z_1 and Z_2 are in the reverse cutoff state. For this process, the following equations can be derived:

$$V_{\rm drain} = V_{ds\_M} \tag{4}$$

$$V_{Z1} = V_{ds\_M} = V_{\rm drain}. \tag{5}$$

It can be observed that $V_{\rm ds\_M}$ would change with $V_{\rm drain}$ synchronously, as shown in the waveform of state I, in Fig. 5, $t_0 \sim t_1$.

State II: In this state, the voltage range of $V_{\rm drain}$ is as follows:

$$|V_{gs\_J\_sat}| \le V_{\rm drain} < |V_{gs\_J\_sat}| + V_{\rm ZT} \tag{6}$$

where $V_{\rm ZT}$ is the reverse breakdown voltage of the Zener diode.

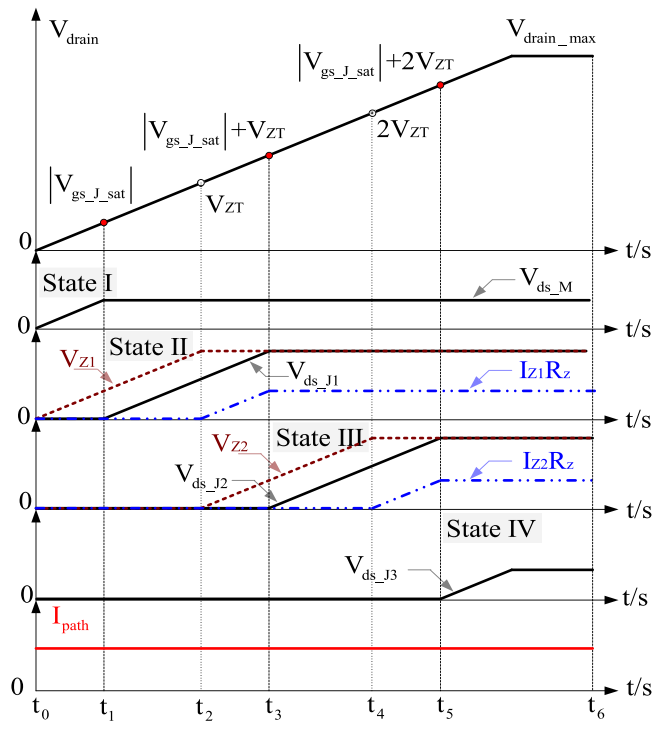

Fig. 5. Key operation waveforms of the proposed three-port linear power composite transistor.

In this working state, J_2, J_3 are in a conducting state, J_1 and M are in a linear constant current saturation zone, and Z_2 is in the reverse cutoff state but Z_1 starts to change from a reverse blocking state to a reverse breakdown voltage regulator working condition. For this process, the following equations can

be provided:

$$V_{\rm drain} = V_{ds\_J1} + V_{ds\_M} \tag{7}$$

$$V_{\rm drain} = I_{Z1}R_z + V_{Z1} \tag{8}$$

where R_z is equal to R_{z1} and R_{z2}. This process state can be divided into two small stages, states II_1 and II_2, and the available equations are different.

In state II_1, the voltage range of $V_{\rm drain}$ is

$$|V_{gs\_J\_sat}| \le V_{\rm drain} < V_{\rm ZT}. \tag{9}$$

Z_1 is in reverse cutoff state, combining with (7) and (8), the following equations can be derived:

$$V_{ds\_M} = |V_{gs\_J\_sat}| \tag{10}$$

$$V_{ds\_J1} = V_{\rm drain} - |V_{gs\_J\_sat}|. \tag{11}$$

In state II_2, the voltage range of $V_{\rm drain}$ is,

$$V_{\rm ZT} \le V_{\rm drain} < V_{\rm ZT} + |V_{gs\_J\_sat}| \tag{12}$$

Z_1 is in reverse breakdown working state, combining with (7) and (8), the following equations can be derived:

$$I_{Z1} = (V_{\rm drain} - V_{\rm ZT})/R_z. \tag{13}$$

It can be observed that V_{ds_M} would remain unchanged and V_{Z1} would change with $V_{\rm drain}$ synchronously, until it reaches the reverse breakdown voltage value; then, $(I_{z1}R_z)$ increases gradually from 0 V, as shown in the waveform of state II, in Fig. 5, $t_1 \sim t_3$.

State III: In this state, the voltage range of $V_{\rm drain}$ is as follows:

$$|V_{gs\_J\_sat}| + V_{\rm ZT} \le V_{\rm drain} < 2V_{\rm ZT} + |V_{gs\_J\_sat}|. \tag{14}$$

In this working state, J_3 is in a conducting state, J_2, J_1, and M are in a linear constant current saturation zone, Z_2 starts to change from a reverse blocking state to a reverse breakdown voltage regulator working condition, and Z_1 is in a reverse breakdown working condition. For this process, the following equations can be derived:

$$V_{\rm drain} = V_{ds\_J2} + V_{ds\_J1} + V_{ds\_M} \tag{15}$$

$$V_{\rm drain} = I_{Z2}R_z + V_{Z2} + V_{Z1}. \tag{16}$$

The process state can be divided into two small stages, states III_1 and III_2, and the available equations are different.

In state III_1, the voltage range of $V_{\rm drain}$ is

$$|V_{gs\_J\_sat}| + V_{\rm ZT} \le V_{\rm drain} < 2V_{\rm ZT}. \tag{17}$$

Z_2 is in reverse cutoff state, combining with (15) and (16), the following equations can be derived:

$$V_{ds\_J2} = V_{\rm drain} - V_{\rm ZT} - |V_{gs\_J\_sat}|. \tag{18}$$

In state III_2, the voltage range of $V_{\rm drain}$ is

$$2V_{\rm ZT} \le V_{\rm drain} < 2V_{\rm ZT} + |V_{gs\_J\_sat}|. \tag{19}$$

Z_2 is in reverse breakdown working state, combining with (15) and (16), the following equations can be derived:

$$I_{Z2} = (V_{\rm drain} - 2V_{\rm ZT})/R_z. \tag{20}$$

It can be observed that $V_{\rm ds\_M}$ and $V_{\rm ds\_J1}$ would remain unchanged and V_{Z2} would change with $V_{\rm drain}$ synchronously, until it reaches the reverse breakdown voltage value; then, $(I_{z2}R_z)$ begins to increase gradually from 0 V, as shown the waveform of state III, in Fig. 5, $t_3 \sim t_5$.

State IV: In this state, the voltage range of $V_{\rm drain}$ is as follows:

$$V_{\rm drain} \ge 2V_{\rm ZT} + |V_{gs\_J\_sat}|. \tag{21}$$

In this working state, J_3, J_2, J_1, and M are in the linear constant current saturation zone, and Z_2 and Z_1 are in a reverse breakdown working condition. For this process, the following equations can be derived:

$$V_{\rm drain} = V_{ds\_J2} + V_{ds\_J2} + V_{ds\_J1} + V_{ds\_M} \tag{22}$$

$$V_{\rm drain} = V_{ds\_J3} + 2V_{\rm ZT} + |V_{gs\_J\_sat}|. \tag{23}$$

Further,

$$V_{ds\_J3} = V_{\rm drain} - 2V_{\rm ZT} - |V_{gs\_J\_sat}|. \tag{24}$$

It can be observed that $V_{\rm ds\_M}$, $V_{\rm ds\_J1}$, and $V_{\rm ds\_J2}$ would remain unchanged and $V_{\rm ds\_J3}$ would change synchronously from 0 V, as shown in the waveform of state IV, in Fig. 5, $t_5 \sim t_6$.

From the above working-state analysis, it can be established that the voltage between each JFET drain and source can be controlled by selecting the appropriate reverse breakdown voltage value of the Zener diode such that the power consumption of each JFET is controllable. If the three-port linear power transistor is composed of p JFET cascades, the number, $N_{20\rm paths}$, of parallel linear current-source paths with single power MOSFETS can be decreased to $(N_{20\rm paths}/p)$, considerably simplifying the circuit structure.

D. Loop Analysis of Linear Current Source With Three-Port Linear Power Composite Transistor

As per the working principles of our novel linear voltage-controlled current source, the proposed linear power stage can meet the SSAS power demands under steady-state working conditions. However, the other important characteristic to consider is the dynamic performance of the linear power stage; hence, a small-signal model needs to be developed for obtaining the frequency-domain characteristics of the novel linear current source with the three-port linear power composite transistor. The parameters of the linear current source are listed in Table I, whereas those of the three-port linear power composite transistor are listed in Table II. The main considerations for choosing the SiC-JFET are based on three requirements, including the feature requirement of normally open power transistor devices, feature requirement of the drain and source voltage forward voltage conduction, and the thermal stability of SiC material in terms of its electrical performance and excellent heat dissipation capability, similar analysis content is already discussed in [18].

A Bode simulation with Saber, utilizes the parameters from Tables I and II, using a network frequency analyzer based on the small-signal circuit model of the novel linear current source; the open-loop frequency response curves are depicted in Fig. 6(a).

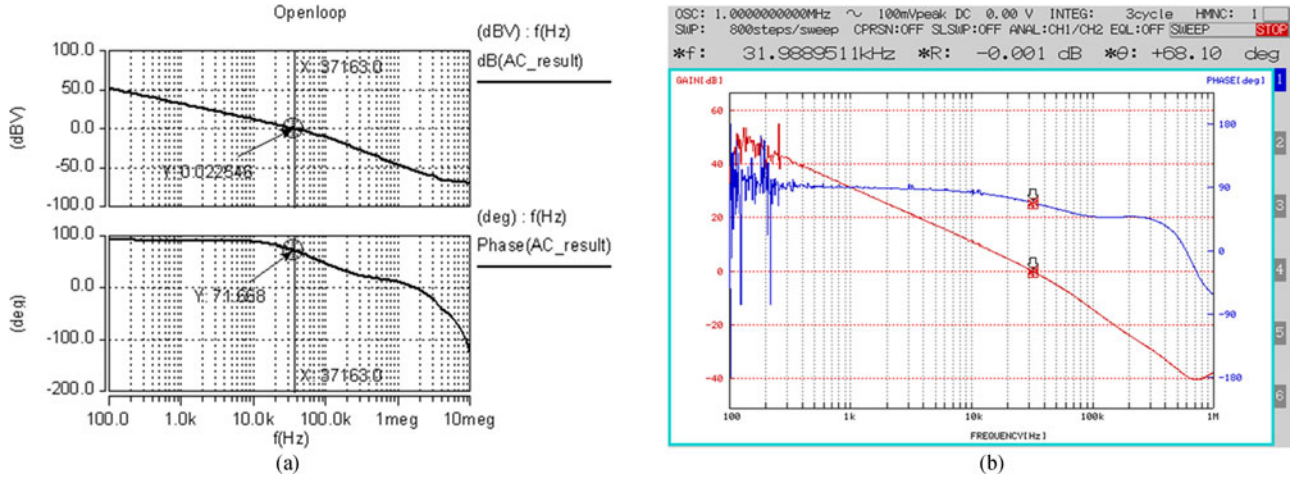

Fig. 6. Bode response for the proposed linear current-source path. (a) Open-loop Bode response from the simulation result of the small-signal circuit model for evaluating the stability margin and (b) measured open-loop Bode plot.

TABLE I
PARAMETERS OF THE LINEAR CURRENT SOURCE

Parameter	Value	Unit	Parameter	Value	Unit
R_{d1}	4.7	Ω	R_{f1}	10	kΩ
R_{d2}	10	kΩ	R_{f2}	100	kΩ
R_{d3}	2	kΩ	R_{f3}	10	kΩ
R_{d4}	100	Ω	R_{f4}	100	kΩ
R_{d5}	200	Ω	R_{c1}	36	kΩ
R_{p1}	3.6	kΩ	C_{c1}	133	pF
R_s	0.2	Ω	R_{c2}	1.5	kΩ
OPA 1, 2	LM6172	-	C_{c2}	100	pF
$G_{\mathrm{BW\_opa}}$	86	dB	R_{c3}	12	kΩ
R_{o_opa}	14	Ω	C_{c3}	100	pF

TABLE II
PARAMETERS OF THE THREE-PORT LINEAR POWER COMPOSITE TRANSISTOR

Parameters of the three-port linear power composite transistor	Parameter/Value	Unit
M	IRF520	–
*J*1, *J*2, *J*3	UJN1208K	–
Z1, Z2	1N4751	–
*Rz*1, *Rz*2	15	kΩ

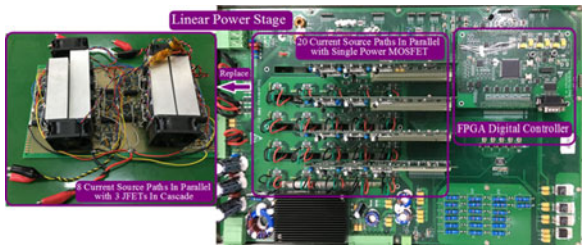

Fig. 7. Photograph of the prototype.

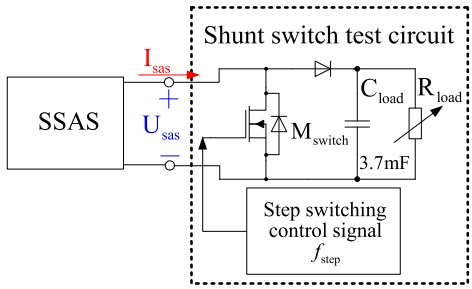

Fig. 8. Shunt switching test circuit to test the steady-state response and dynamic performance.

TABLE III
I–V CURVES SETTING FOR THE EXPERIMENT

Setting parameters	Value
Constant bus Voltage (U_{bus})	68 V
OC voltage (U_{oc})	60 V
SC current (I_{sc})	8.3 A
The maximum power point voltage (U_{mp})	55 V
The maximum power point current (I_{mp})	6 A
Number of parallel current-source paths (*N*)	8

From the open-loop simulation frequency Bode response, the phase margin is 71.6° and the cutoff frequency is 37.1 kHz.

A prototype is built to demonstrate the actual open-loop and closed-loop frequency responses using a frequency response analyzer, FRA5097, at the same working conditions. The sweep frequency responses for the open-loop Bode are shown in Fig. 6(b). As per the measured frequency response of a single linear current path, Fig. 8(a) depicts that the open-loop Bode plot has a phase margin $\Delta\varphi$ of 68.1° and a cut-roll frequency f_{cr} of 31.98 kHz, which are close to the simulated Bode results.

However, in the case of an SSAS with combined analog hardware and digital controller systems, the issue of the delay margin is much more critical because a satisfactory phase margin does not guarantee a satisfactory delay margin [24], particularly, in systems with high bandwidths and high dynamic response requirements. From the measured open-loop Bode plot, the cutoff frequency ω_{cr} is

$$\omega_{\mathrm{cr}} = 2\pi f_{\mathrm{cr}} = 2.01 \times 10^5 \text{ rad/s}. \tag{25}$$

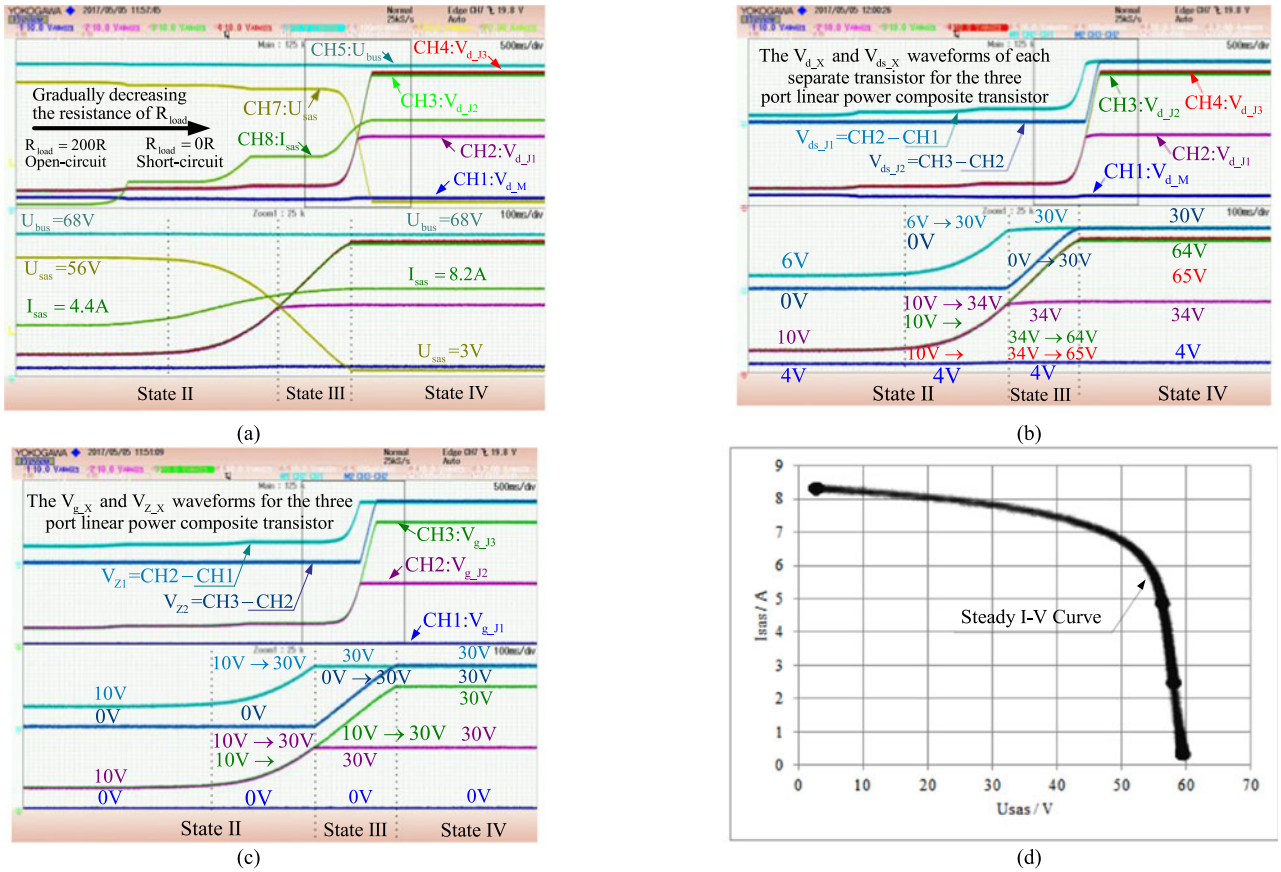

Fig. 9. Key-point time-domain voltage waveforms (a) overall waveform changing process, along with the change in the output voltage changing of the SSAS, (b) drain voltage waveforms, and (c) gate voltage waveforms of each cascaded JFET; and (d) I–V curve output.

The phase margin $\Delta\Phi$ is

$$\Delta\Phi = (\Delta\varphi/360^\circ) \times 2\pi = 1.188 \text{ rad}. \tag{26}$$

The delay margin $\Delta\tau_{\rm dm}$ can be calculated from the phase margin $\Delta\Phi$ and the cutoff frequency $\omega_{\rm cr}$ as follows:

$$\Delta\tau_{\rm dm} = \frac{\Delta\Phi}{\omega_{\rm cr}} = 5.91\ \mu\text{s}. \tag{27}$$

The FPGA digital controller uses a 40-MHz clock for the ADC and DAC and provides $U_{\rm Iref}$ as per the I–V lookup table. The total delay time T_s can be calculated to be 600 ns as

$$\Delta\tau_{\rm dm} > T_s = 0.6\ \mu\text{s}. \tag{28}$$

The index for selecting the delay margin for the system design is

$$\Delta\tau_{\rm dm} \geq T_s\ [\min : 0.75T_s]. \tag{29}$$

Therefore, the phase and delay margins of the linear power stage are satisfactory for use in high-dynamic-performance SSAS applications.

III. Experimental Results and Discussions

The proposed SSAS is examined under two typical operating conditions, usually involved in nonterrestrial applications: the steady-state response along the static I–V curve and the step change of the output load at different working points of the setting I–V curve, for different stepping frequencies.

A photo of the prototype is displayed in Fig. 7. There are eight linear voltage-controlled current sources connected in parallel to provide an 8.3-A current output. The volume of the entire linear power stage can be considerably reduced compared to [18], which has 20 linear current sources in parallel to provide the same current output.

The I–V curve specifications, to be set for the experiment, are listed in Table III and are the same as that in [18], for examining the steady-state and dynamic responses of the optimized SSAS. The dynamic response test results are compared to a type of SAS modular product in the market, which is widely used in space power system testing applications.

A. Steady-State Response

To examine the steady-state response of the SSAS, the output voltage $U_{\rm sas}$ and output current $I_{\rm sas}$ are tested by gradually decreasing the resistance of the connected $R_{\rm load}$. Fig. 8 depicts the steady-state testing circuit with $M_{\rm switch}$ in an open state.

Fig. 9 shows the steady-state response waveforms of the optimized SSAS, including the drain and gate waveforms of each cascaded JFET, which demonstrate whether the three-port linear power composite transistor with three SiC-JFET cascades can work well, as per the designed working state. Fig. 9(a) depicts

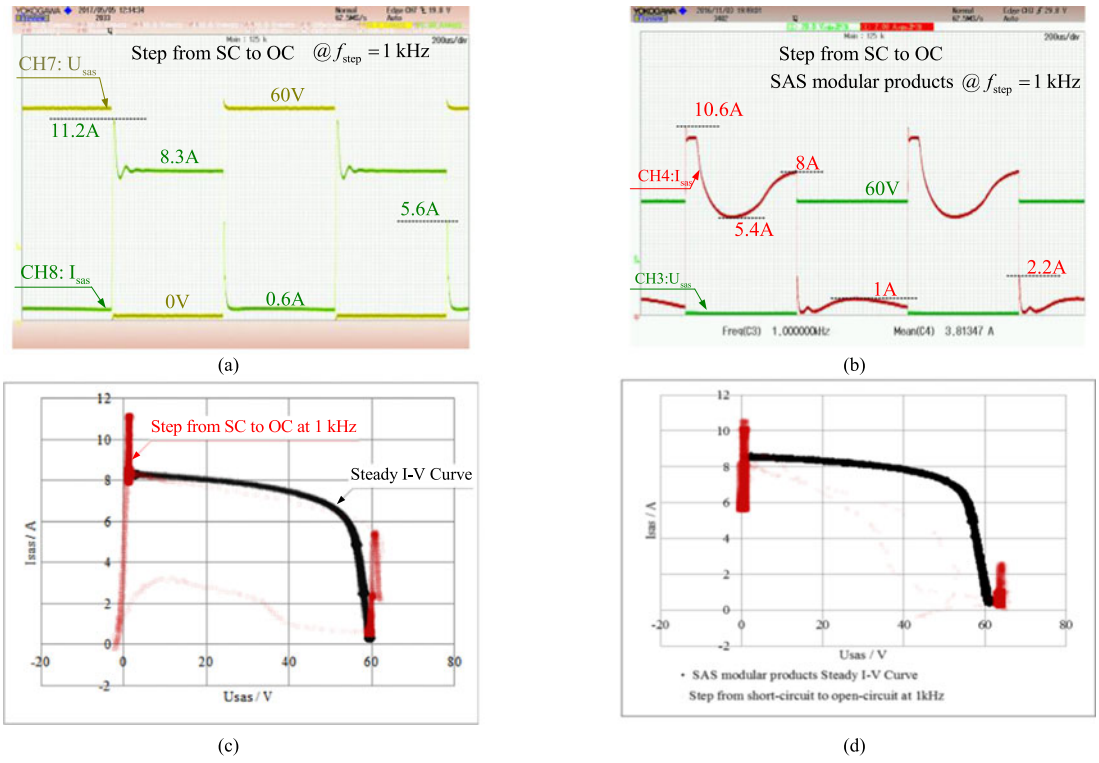

Fig. 10. Step working point between the SC and the OC at f_{step} = 1-kHz. (a) Time-domain waveform of the SSAS; (b) time-domain waveform of the SAS modular products; (c) distribution of the output voltage and current step switching data in the SSAS output steady I–V curve; and (d) distribution of the step switching data in the SAS modular products output steady I–V curve.

the overall waveform changing process along with the change in the output voltage U_{sas}.U_{bus} is the dc bus voltage, which is a constant voltage of 68 V; I_{sas} is the output current of the SSAS; V_{d_M} is the drain voltage waveform of the bottom MOSFET M; and $V_{d\_J1}, V_{d\_J2}, V_{d\_J3}$ are the drain voltage waveforms of each cascaded JFET. The equivalent drain voltage of the three-port linear power composite transistor V_{drain} is the difference between the bus voltage and the output voltage of the SSAS, i.e., $(U_{\text{bus}} - U_{\text{sas}})$.

From an OC to SC, the output voltage U_{sas} gradually decreases from the OC voltage of 60 V to SC voltage of 3 V and the equivalent drain voltage V_{drain} gradually increases, synchronizing from 8 to 65 V, indicating that the drain voltage of each cascaded JFET gradually increases, until it reaches 30 V, the reverse breakdown voltage of the Zeners. From Fig. 9(b), it can be observed that V_{d_J1} would reach the reverse breakdown voltage of Z_1 and remain unchanged at 34 V; however, V_{d_J2} and V_{d_J3} would still increase along with V_{drain} and V_{d_J2} would stop increasing at 64 V. Finally, the remaining voltage difference is assumed by J_3, and V_{d_J3} eventually becomes equal to V_{drain}.

Fig. 9(c) shows the gate voltage of each cascaded JFET, used to obtain the voltages across the cathode-to-anode of Z_1 and Z_2, respectively. The voltage across the cathode-to-anode of Z_1, V_{z1} can use V_{g_J2} voltage value subtracted V_{g_J1} voltage value, so as the V_{z2}. V_{z1} would increase the voltage to 30 V, followed by V_{z2} starting from 0 to 30 V. From the steady-state experimental analysis of the waveform, it is observed that it can work well during all the working points of the set I–V curve, for

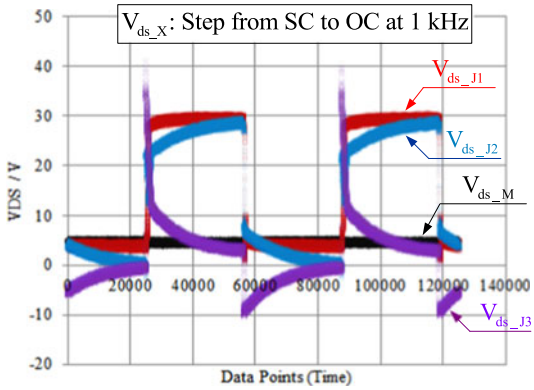

Fig. 11. Voltage waveform between drain and source of the each cascade JFET under step switching between SC and OC at f_{step} = 1-kHz working condition.

the optimized SSAS with the novel three-port linear composite transistor.

Fig. 9(d) shows the experiment data of U_{sas} and I_{sas} from the oscilloscope recorded data; the data are plotted in the second coordinate with U_{sas} on the horizontal axis and I_{sas} on the vertical axis. From the result of the steady-state experiment, the output I–V curve of the SSAS is the setting I–V curve; the voltage between the drain and source of each cascaded JFET should not exceed the 30 V limit as per the design requirements. Thus, the proposed optimized SSAS can well simulate a normal steady I–V curve.

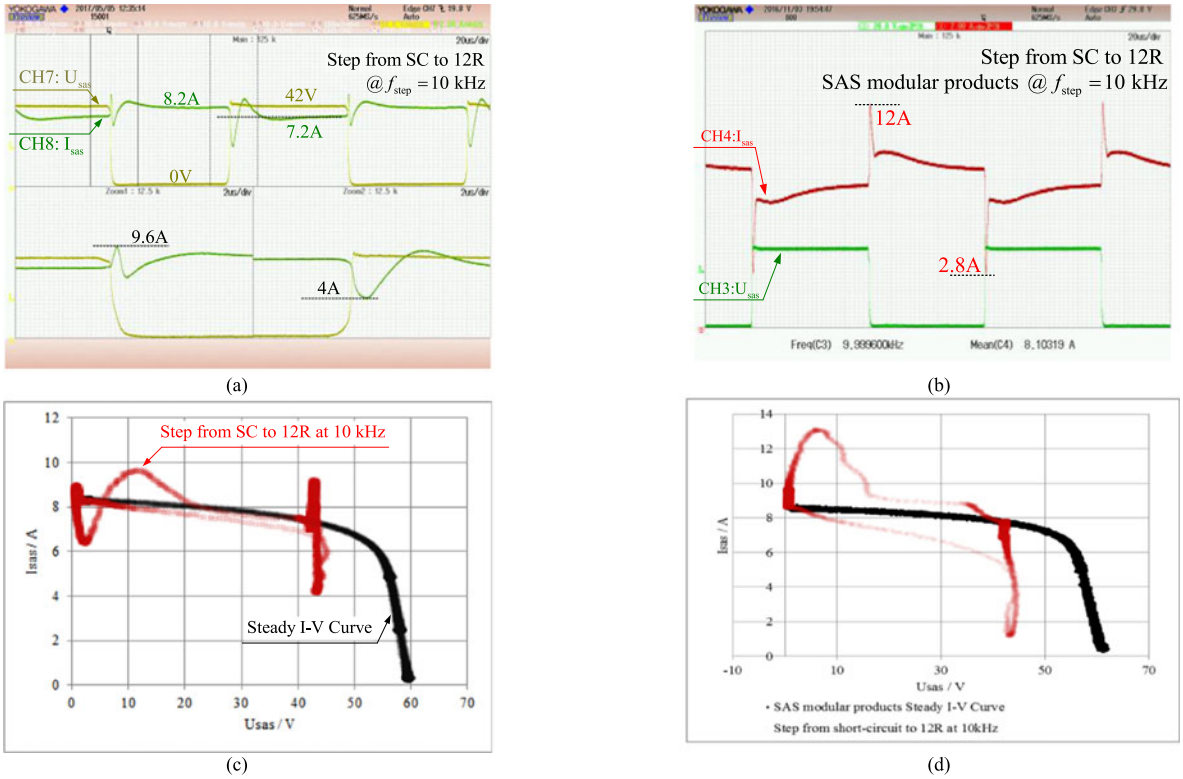

Fig. 12. Step working point between SC and nominal working point at $f_{\mathrm{step}} = 10$ kHz. (a) Time-domain waveform of the SSAS. (b) Time-domain waveform of SAS modular product. (c) Distribution of output voltage and current step switching data in SSAS output steady I–V curve. (d) Distribution of step switching data in SAS modular product output steady I–V curve.

B. Shunt Switching Between the SC and OC

The shunt switching test experiment is the harshest test condition for a SAS, involving a step from a SC to an approximate OC, when the output current is considerably less. Fig. 10 shows the shunt switching test waveform from SC to OC working condition at 1 kHz step switching frequency. Fig. 10(a) is the time-domain output voltage U_{sas} and output current I_{sas} waveforms; (c) is the distribution of the output voltage and current step switching data in the SSAS output steady I–V curve.

As shown in Fig. 10(a), the step switching working points can be reached precisely and stably with a maximum of 11.2 A current switch spikes which is similiar compare to that 10.6 A from one kind of SAS modular products on the market shown in Fig. 10(b), and only 4 A current falling down adjustment process which is better than 2.2 A current falling testing from the result from one kind of SAS modular products on the market. From the distribution of the testing data in the SSAS output steady I–V curve, Fig. 10(c), the switching experimental data are distributed around two desired working points, however, the switching experimental data from Fig. 10(b) cannot distribute around the designed two working points in the set I–V steady curve which means the dynamic response characteristic of optimized SSAS is much better than the SAS modular products on the market.

Fig. 11 is voltage waveform between drain and source of the each cascade JFET caculated from expriment data of the drain voltage waveforms of the each cascade JFET from the oscilloscope, $V_{\mathrm{ds\_J1}}, V_{\mathrm{ds\_J2}}, V_{\mathrm{ds\_J3}}$ under step switching between SC and OC at 1 kHz. It shows that the voltage between drain and source of the each cascade JFET is working well according to the designed work logic even under step switching working condition.

C. Shunt Switching Between the SC and Nominal Working Point

For better examining the limited dynamic characteristics to check whether the dynamic performance of the proposed optimized method is fit for testing the S3R, the stepping test frequency between the SC and nominal working point ($R_{\mathrm{load}} =$ 12 R, Fig. 8) is increased to 10 kHz. Fig. 12 shows the experimental results for the optimized SSAS for an f_{step} value of 10 kHz.

From Fig. 12(a), we observe that the optimized SSAS has a smaller current switching spike and current sag adjustment process, and most of the step switching testing data are distributed around the designed working points. The time-domain waveform and the distribution of the output voltage and current step switching data in the SSAS output steady I–V curve, shown in Fig. 12(a) and (c), exhibit improved characteristics over those of the SAS modular product [as shown in Fig. 12(b) and (d)] under the same test conditions. However, the voltage between the drain and source of each cascaded JFET (see Fig. 13) is distorted, exhibiting an insufficient dynamic response because of the poor dynamic performance of the Zeners. Consequently,

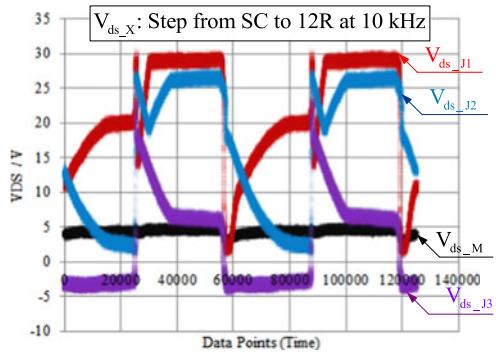

Fig. 13. Voltage waveform between drain and source of the each cascade JFET under step switching between SC and nominal working point at $f_{\text{step}} = 10$-kHz working condition.

the limited dynamic switching frequency between the SC and nominal working point is 10 kHz.

IV. Conclusion

This study proposes an optimized linear power stage for the SSAS with both high dynamic performance and simple circuit structure under the same output power level. The results demonstrate that the proposed 510-W SSAS can simulate a shunt switching test from SC to nominal working conditions at a 10-kHz stepping frequency. The SSAS also performs well when stepping from SC to OC at 1 kHz, which is the harshest working condition for an SAS. These results are also compared with the experimental results of other SAS modular products under the same working conditions as those presented in a previous study. The experimental results show that the proposed optimized SSAS exhibits a better dynamic performance than the other SAS modular products and is more suitable for spacecraft power supply testing applications.

However, it must be acknowledged that the optimized SSAS has a tradeoff of its dynamic response performance when compared with that of the previous 510-W platform [18] for considerably reducing the number of parallel current-source paths, simplifying the circuit structure, and improving the reliability and output current control accuracy. Second, the number of cascaded JFETs is limited, because, if more JFETs are cascaded, the dynamic performance deteriorates, and this would make the SSAS unsuitable for space power system testing applications.

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