6
Converter Circuits

We have already analyzed the operation of a number of different types of converters: buck, boost, buck–boost, Ćuk, voltage-source inverter, etc. With these converters, a number of different functions can be performed: step-down of voltage, step-up, inversion of polarity, and conversion of dc to ac or vice-versa.

It is natural to ask, Where do these converters come from? What other converters occur, and what other functions can be obtained? What are the basic relations between converters? In this chapter, several different circuit manipulations are explored, which explain the origins of the basic converters. Inversion of source and load transforms the buck converter into the boost converter. Cascade connection of converters, and simplification of the resulting circuit, shows how the buck–boost and Ćuk converters are based on the buck and the boost converters. Differential connection of the load between the outputs of two or more converters leads to a single-phase or polyphase inverter. A short list of some of the better known converter circuits follows this discussion.

Transformer-isolated dc–dc converters are also covered in this chapter. Use of a transformer allows isolation and multiple outputs to be obtained in a dc-dc converter, and can lead to better converter optimization when a very large or very small conversion ratio is required. The transformer is modeled as a magnetizing inductance in parallel with an ideal transformer; this allows the analysis techniques of the previous chapters to be extended to cover converters containing transformers. A number of well-known isolated converters, based on the buck, boost, buck–boost, single-ended primary inductance converter (SEPIC), and Ćuk, are listed and discussed.

Finally, the evaluation, selection, and design of converters to meet given requirements are considered. Important performance-related attributes of transformer-isolated converters include: whether the transformer reset process imposes excessive voltage stress on the transistors, whether the converter can supply a high-current output without imposing excessive current stresses on the secondary-side components, and whether the converter can be well-optimized to operate with a wide range of operating points,

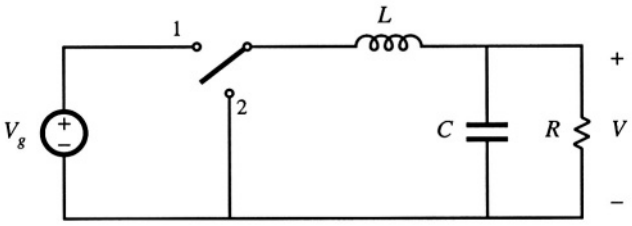

Fig. 6.1 The basic buck converter.

that is, with large tolerances in V_g and P_{load}. Switch utilization is a simplified figure-of-merit that measures the ratio of the converter output power to the total transistor voltage and current stress. As the switch utilization increases, the converter efficiency increases while its cost decreases. Isolated converters with large variations in operating point tend to utilize their power devices more poorly than nonisolated converters which function at a single operating point. Computer spreadsheets are a good tool for optimization of power stage designs and for trade studies to select a converter topology for a given application.

6.1 CIRCUIT MANIPULATIONS

The buck converter (Fig. 6.1) was developed in Chapter 1 using basic principles. The switch reduces the voltage dc component, and the low-pass filter removes the switching harmonics. In the continuous conduction mode, the buck converter has a conversion ratio of $M = D$. The buck converter is the simplest and most basic circuit, from which we will derive other converters.

6.1.1 Inversion of Source and Load

Let us consider first what happens when we interchange the power input and power output ports of a converter. In the buck converter of Fig. 6.2(a), voltage V_1 is applied at port 1, and voltage V_2 appears at port 2. We know that

$$V_2 = DV_1 \tag{6.1}$$

This equation can be derived using the principle of inductor volt-second balance, with the assumption that the converter operates in the continuous conduction mode. Provided that the switch is realized such that this assumption holds, then Eq. (6.1) is true regardless of the direction of power flow.

So let us interchange the power source and load, as in Fig. 6.2(b). The load, bypassed by the capacitor, is connected to converter port 1, while the power source is connected to converter port 2. Power now flows in the opposite direction through the converter. Equation (6.1) must still hold; by solving for the load voltage V_1, one obtains

$$V_1 = \frac{1}{D} V_2 \tag{6.2}$$

So the load voltage is greater than the source voltage. Figure 6.2(b) is a boost converter, drawn backwards. Equation 6.2 nearly coincides with the familiar boost converter result, $M(D) = 1/D'$, except that D' is replaced by D.

Since power flows in the opposite direction, the standard buck converter unidirectional switch

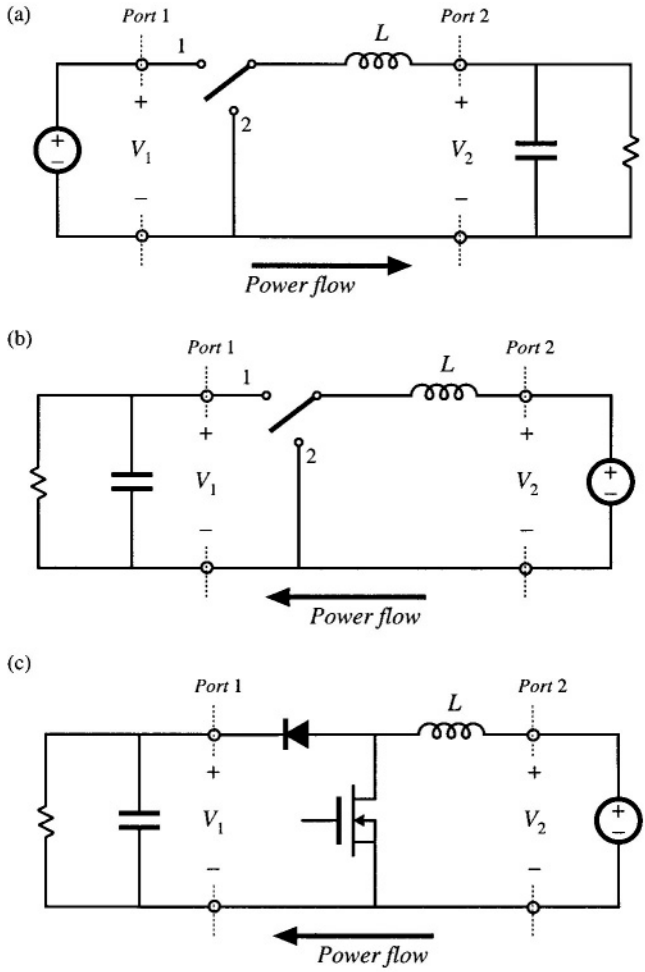

Fig. 6.2 Inversion of source and load transforms a buck converter into a boost converter: (a) buck converter, (b) inversion of source and load, (c) realization of switch.

realization cannot be used with the circuit of Fig. 6.2(b). By following the discussion of Chapter 4, one finds that the switch can be realized by connecting a transistor between the inductor and ground, and a diode from the inductor to the load, as shown in Fig. 6.2(c). In consequence, the transistor duty cycle D becomes the fraction of time which the single-pole double-throw (SPDT) switch of Fig. 6.2(b) spends in position 2, rather than in position 1. So we should interchange D with its complement D' in Eq. (6.2), and the conversion ratio of the converter of Fig. 6.2(c) is

$$V_1 = \frac{1}{D'} V_2 \tag{6.3}$$

Thus, the boost converter can be viewed as a buck converter having the source and load connections exchanged, and in which the switch is realized in a manner that allows reversal of the direction of power flow.

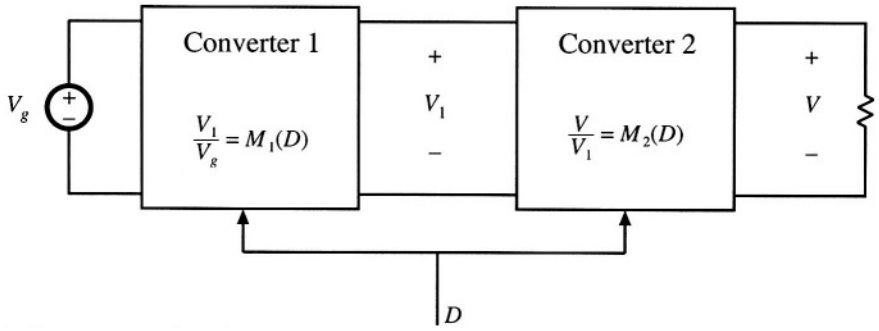

Fig. 6.3 Cascade connection of converters.

6.1.2 Cascade Connection of Converters

Converters can also be connected in cascade, as illustrated in Fig. 6.3 [1,2]. Converter 1 has conversion ratio $M_1(D)$, such that its output voltage V_1 is

$$V_1 = M_1(D)V_g \tag{6.4}$$

This voltage is applied to the input of the second converter. Let us assume that converter 2 is driven with the same duty cycle D applied to converter 1. If converter 2 has conversion ratio $M_2(D)$, then the output voltage V is

$$V = M_2(D)V_1 \tag{6.5}$$

Substitution of Eq. (6.4) into Eq. (6.5) yields

$$\frac{V}{V_g} = M(D) = M_1(D)M_2(D) \tag{6.6}$$

Hence, the conversion ratio $M(D)$ of the composite converter is the product of the individual conversion ratios $M_1(D)$ and $M_2(D)$.

Let us consider the case where converter 1 is a buck converter, and converter 2 is a boost converter. The resulting circuit is illustrated in Fig. 6.4. The buck converter has conversion ratio

$$\frac{V_1}{V_g} = D \tag{6.7}$$

The boost converter has conversion ratio

$$\frac{V}{V_1} = \frac{1}{1-D} \tag{6.8}$$

So the composite conversion ratio is

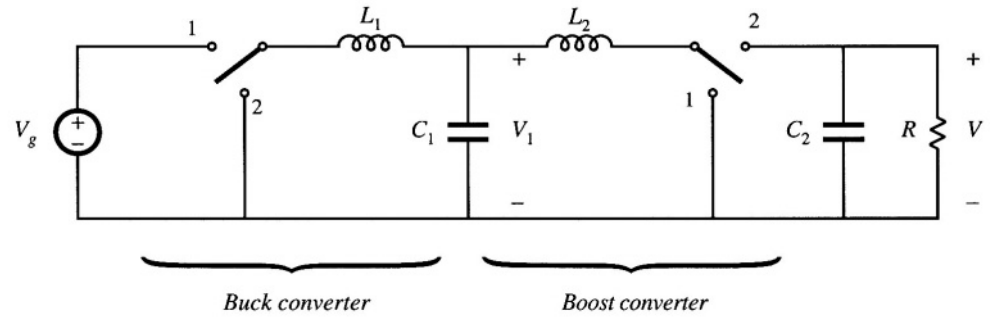

Fig. 6.4 Cascade connection of buck converter and boost converter.

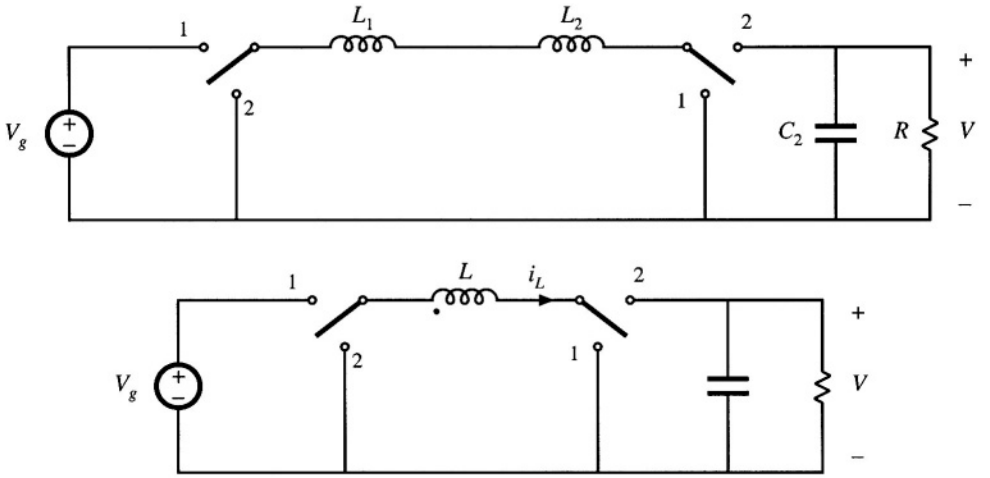

Fig. 6.5 Simplification of the cascaded buck and boost converter circuit of Fig. 6.4: (a) removal of capacitor C_1, (b) combining of inductors L_1 and L_2.

$$\frac{V}{V_g} = \frac{D}{1-D} \tag{6.9}$$

The composite converter has a noninverting buck–boost conversion ratio. The voltage is reduced when $D < 0.5$, and increased when $D > 0.5$.

The circuit of Fig. 6.4 can be simplified considerably. Note that inductors L_1 and L_2, along with capacitor C_1, form a three-pole low-pass filter. The conversion ratio does not depend on the number of poles present in the low-pass filter, and so the same steady-state output voltage should be obtained when a simpler low-pass filter is used. In Fig. 6.5(a), capacitor C_1 is removed. Inductors L_1 and L_2 are now in series, and can be combined into a single inductor as shown in Fig. 6.5(b). This converter, the noninverting buck–boost converter, continues to exhibit the conversion ratio given in Eq. (6.9).

The switches of the converter of Fig. 6.5(b) can also be simplified, leading to a negative output voltage. When the switches are in position 1, the converter reduces to Fig. 6.6(a). The inductor is connected to the input source V_g, and energy is transferred from the source to the inductor. When the

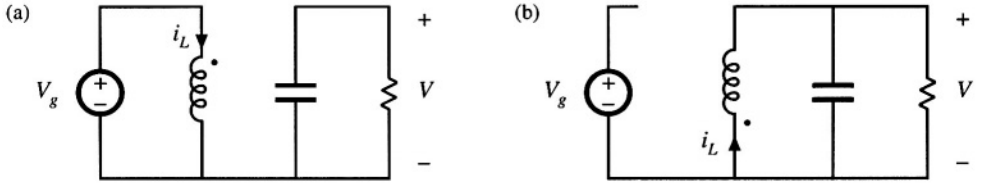

Fig. 6.6 Connections of the circuit of Fig. 6.5(b): (a) while the switches are in position 1, (b) while the switches are in position 2.

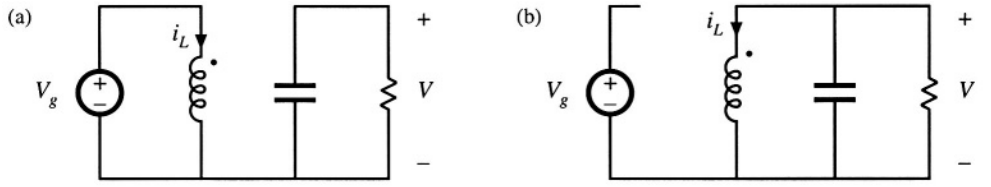

Fig. 6.7 Reversal of the output voltage polarity, by reversing the inductor connections while the switches are in position 2: (a) connections with the switches in position 1, (b) connections with the switches in position 2.

switches are in position 2, the converter reduces to Fig. 6.6(b). The inductor is then connected to the load, and energy is transferred from the inductor to the load. To obtain a negative output, we can simply reverse the polarity of the inductor during one of the subintervals (say, while the switches are in position 2). The individual circuits of Fig. 6.7 are then obtained, and the conversion ratio becomes

$$\frac{V}{V_g} = -\frac{D}{1-D} \tag{6.10}$$

Note that one side of the inductor is now always connected to ground, while the other side is switched between the input source and the load. Hence only one SPDT switch is needed, and the converter circuit of Fig. 6.8 is obtained. Figure 6.8 is recognized as the conventional buck–boost converter.

Thus, the buck–boost converter can be viewed as a cascade connection of buck and boost converters. The properties of the buck–boost converter are consistent with this viewpoint. Indeed, the equivalent circuit model of the buck-boost converter contains a 1:D (buck) dc transformer, followed by a D':1 (boost) dc transformer. The buck–boost converter inherits the pulsating input current of the buck converter, and the pulsating output current of the boost converter.

Other converters can be derived by cascade connections. The Ćuk converter Fig. 2.20) was originally derived [1,2] by cascading a boost converter (converter 1), followed by a buck (converter 2). A negative output voltage is obtained by reversing the polarity of the internal capacitor connection during one of the subintervals; as in the buck–boost converter, this operation has the additional benefit of reducing the number of switches. The equivalent circuit model of the Ćuk converter contains a D':1 (boost)

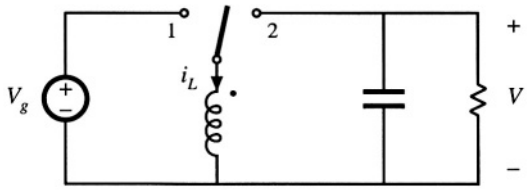

Fig. 6.8 Converter circuit obtained from the subcircuits of Fig. 6.7.

ideal dc transformer, followed by a 1:*D* (buck) ideal dc transformer. The Ćuk converter inherits the nonpulsating input current property of the boost converter, and the nonpulsating output current property of the buck converter.

6.1.3 Rotation of Three-Terminal Cell

The buck, boost, and buck–boost converters each contain an inductor that is connected to a SPDT switch. As illustrated in Fig. 6.9(a), the inductor-switch network can be viewed as a basic cell having the three terminals labeled *a, b,* and *c*. It was first pointed out in [1,2], and later in [3], that there are three distinct ways to connect this cell between the source and load. The connections *a–A b–B c–C* lead to the buck converter. The connections *a–C b–A c–B* amount to inversion of the source and load, and lead to the boost converter. The connections *a–A b–C c–B* lead to the buck-boost converter. So the buck, boost, and buck–boost converters could be viewed as being based on the same inductor-switch cell, with different source and load connections.

A dual three-terminal network, consisting of a capacitor-switch cell, is illustrated in Fig. 6.9(b). Filter inductors are connected in series with the source and load, such that the converter input and output currents are nonpulsating. There are again three possible ways to connect this cell between the source and load. The connections *a–A b–B c–C* lead to a buck converter with *L–C* input low-pass filter. The connections *a–B b–A c–C* coincide with inversion of source and load, and lead to a boost converter with an added output *L–C* filter section. The connections *a–A b–C c–B* lead to the Ćuk converter.

Rotation of more complicated three-terminal cells is explored in [4].

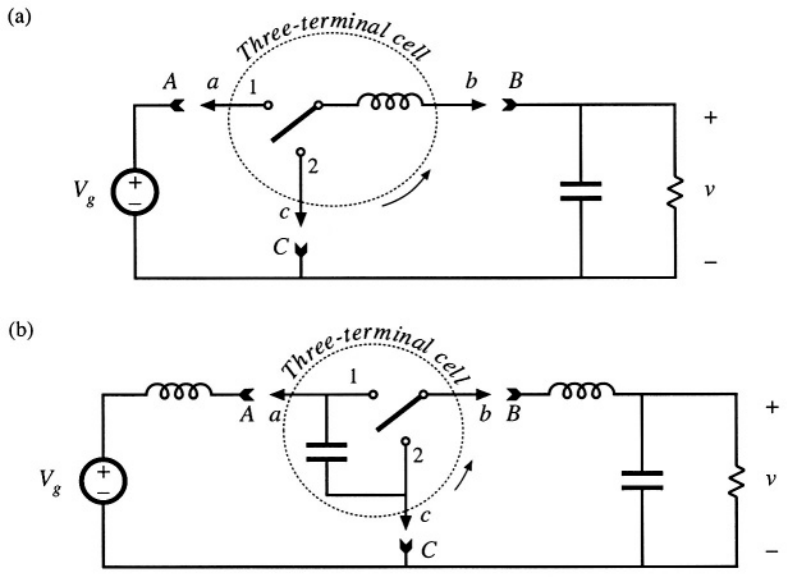

Fig. 6.9 Rotation of three-terminal switch cells: (a) switch/inductor cell, (b) switch/capacitor cell.

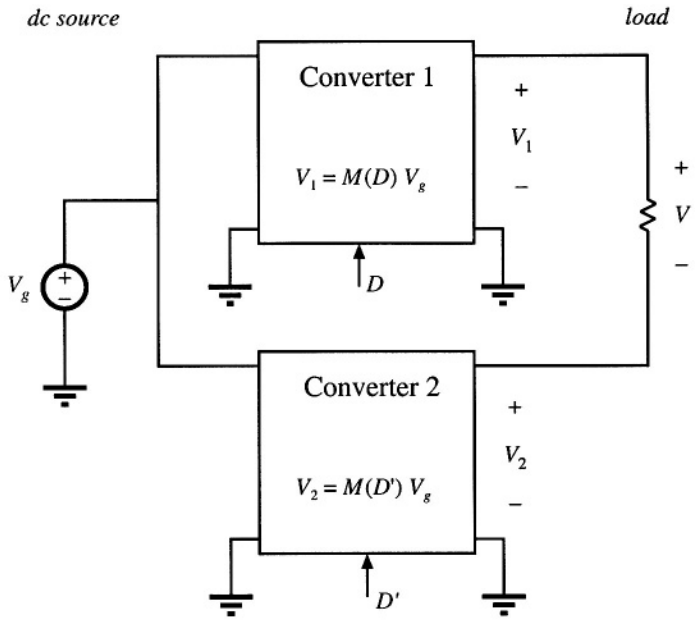

Fig. 6.10 Obtaining a bipolar output by differential connection of load.

6.1.4 Differential Connection of the Load

In inverter applications, where an ac output is required, a converter is needed that is capable of producing an output voltage of either polarity. By variation of the duty cycle in the correct manner, a sinusoidal output voltage having no dc bias can then be obtained. Of the converters studied so far in this chapter, the buck and the boost can produce only a positive unipolar output voltage, while the buck–boost and Ćuk converter produce only a negative unipolar output voltage. How can we derive converters that can produce bipolar output voltages?

A well-known technique for obtaining a bipolar output is the differential connection of the load across the outputs of two known converters, as illustrated in Fig. 6.10. If converter 1 produces voltage V_1, and converter 2 produces voltage V_2, then the load voltage V is given by

$$V = V_1 - V_2 \tag{6.11}$$

Although V_1 and V_2 mayboth individually be positive, the load voltage V can be either positive or negative. Typically, if converter 1 is driven with duty cycle D, then converter 2 is driven with its complement, D', so that when V_1 increases, V_2 decreases, and vice versa.

Several well-known inverter circuits can be derived using the differential connection. Let's realize converters 1 and 2 of Fig. 6.10 using buck converters. Figure 6.11 (a) is obtained. Converter 1 is driven with duty cycle D, while converter 2 is driven with duty cycle D'. So when the SPDT switch of converter 1 is in the upper position, then the SPDT switch of converter 2 is in the lower position, and vice-versa. Converter 1 then produces output voltage $V_1 = DV_g$, while converter 2 produces output volt-

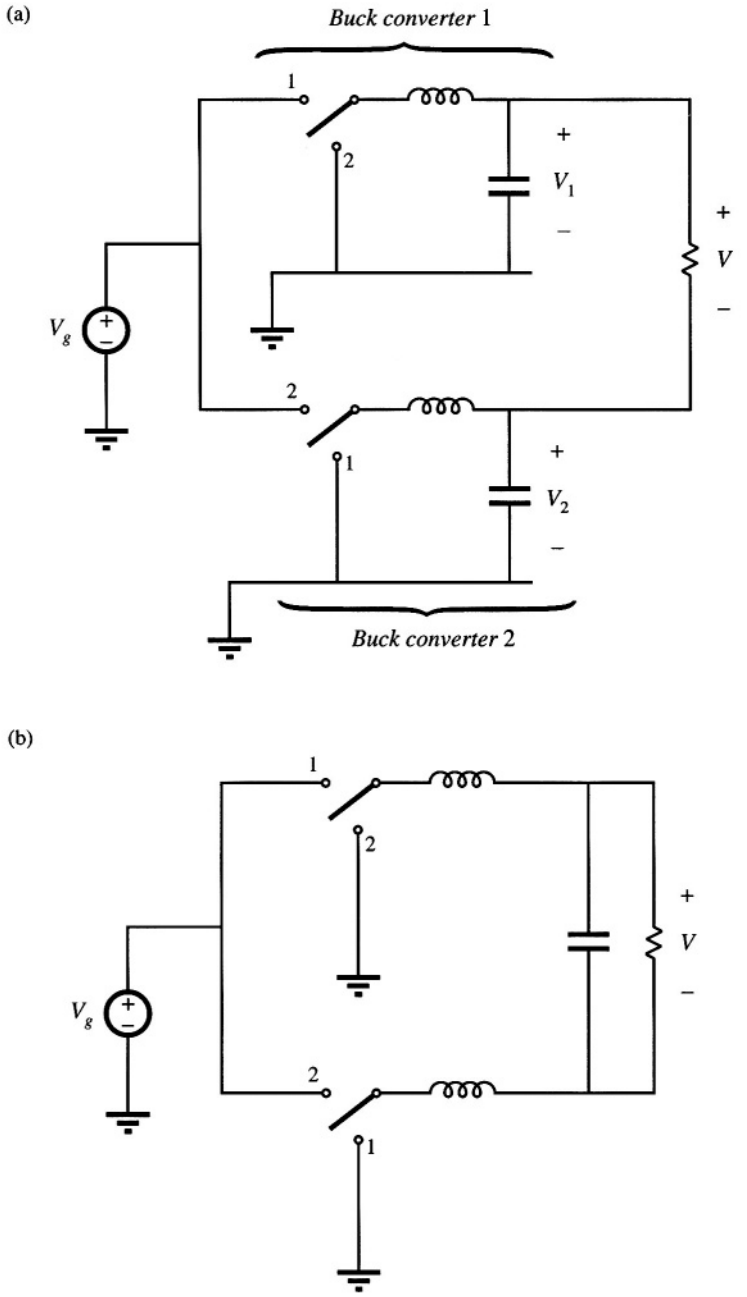

Fig. 6.11 Derivation of bridge inverter (H-bridge): (a) differential connection of load across outputs of buck converters, (b) bypassing load by capacitor, (c) combining series inductors, (d) circuit (c) redrawn in its usual form.

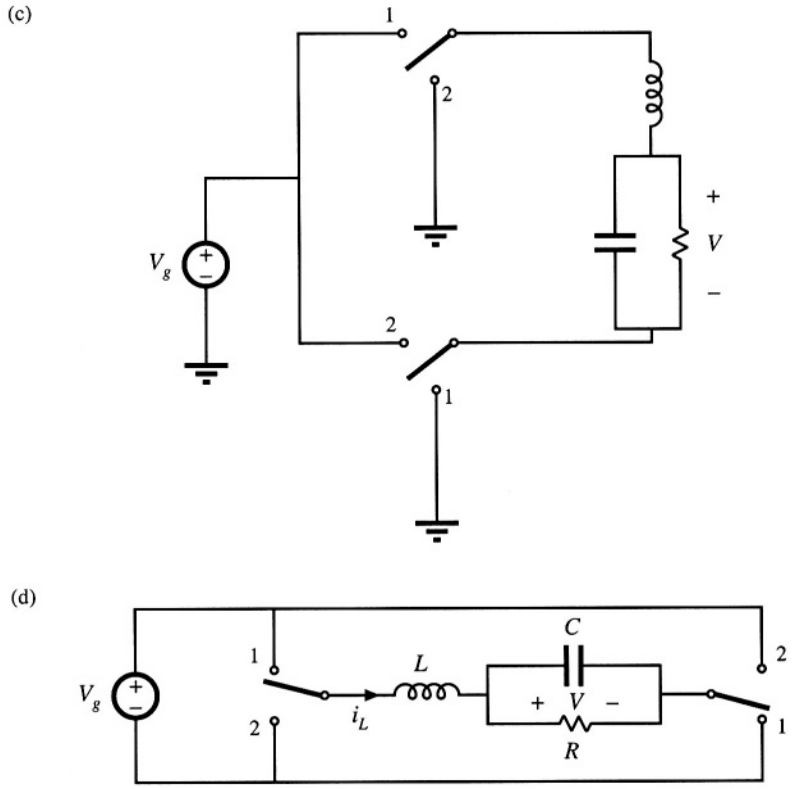

Fig. 6.11 Continued

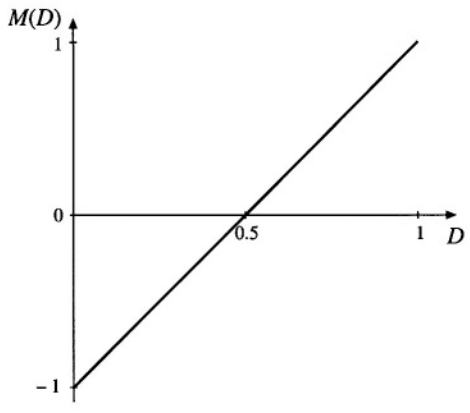

Fig. 6.12 Conversion ratio of the H-bridge inverter circuit.

age $V_2 = D'V_g$. The differential load voltage is

$$V = DV_g - D'V_g \tag{6.12}$$

Simplification leads to

$$V = (2D - 1)V_g \tag{6.13}$$

This equation is plotted in Fig. 6.12. It can be seen the output voltage is positive for $D > 0.5$, and negative for $D < 0.5$. If the duty cycle is varied sinusoidally about a quiescent operating point of 0.5, then the output voltage will be sinusoidal, with no dc bias.

The circuit of Fig. 6.11(a) can be simplified. It is usually desired to bypass the load directly with a capacitor, as in Fig. 6.1l(b). The two inductors are now effectively in series, and can be combined into a single inductor as in Fig. 6.1l(c). Figure 6.11(d) is identical to Fig. 6.1l(c), but is redrawn for clarity. This circuit is commonly called the H-bridge, or bridge inverter circuit. Its use is widespread in servo amplifiers and single-phase inverters. Its properties are similar to those of the buck converter, from which it is derived.

Polyphase inverter circuits can be derived in a similar manner. A three-phase load can be connected differentially across the outputs of three dc–dc converters, as illustrated in Fig. 6.12. If the three-phase load is balanced, then the neutral voltage V_n will be equal to the average of the three converter output voltages:

$$V_n = \frac{1}{3}\left(V_1 + V_2 + V_3\right) \tag{6.14}$$

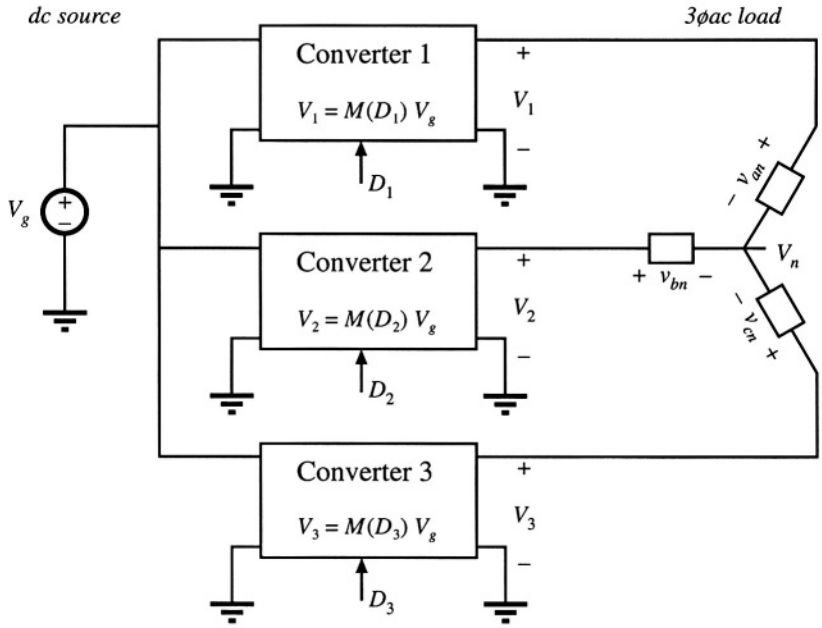

Fig. 6.12 Generation of dc–3φac inverter by differential connection of 3φ load.

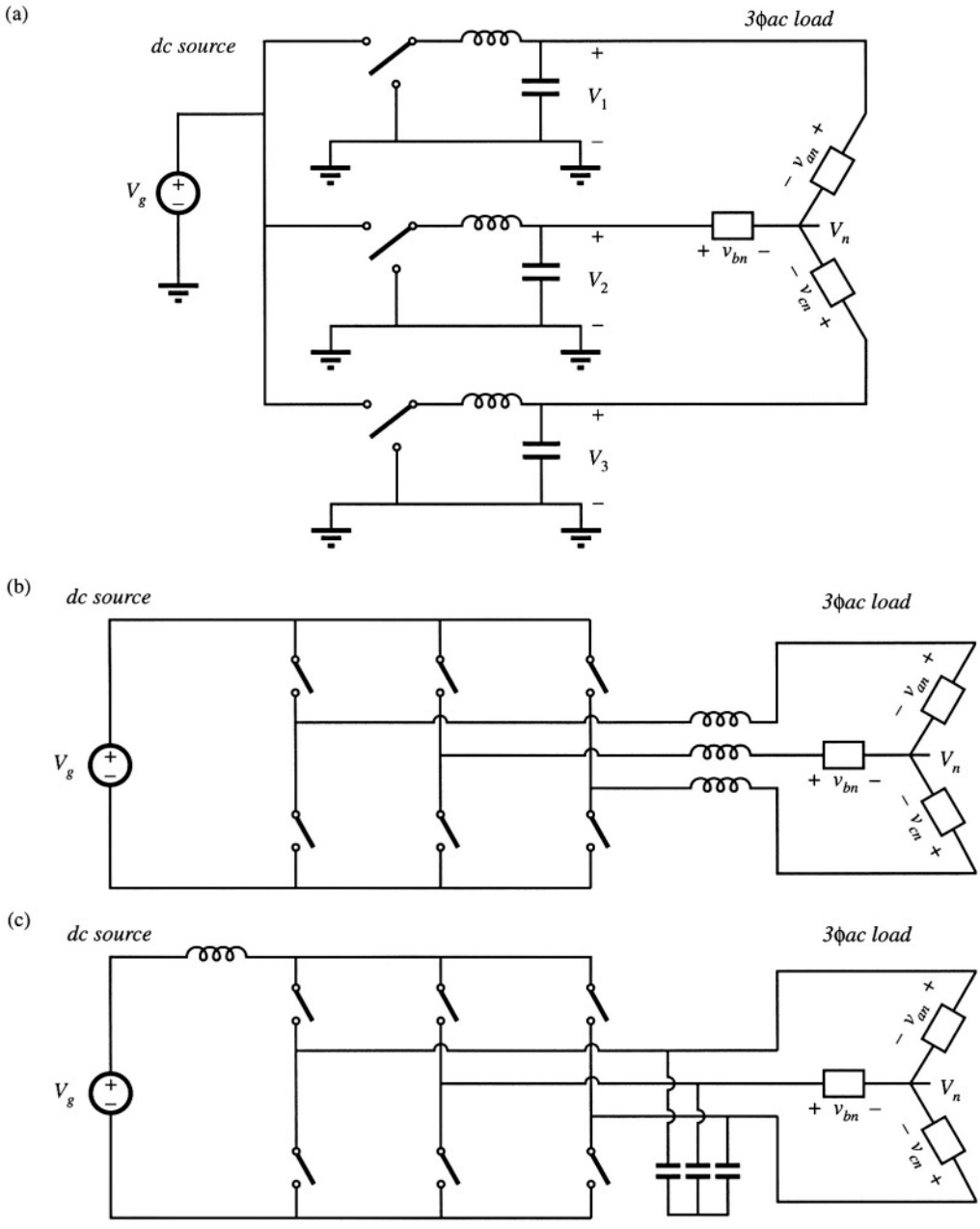

Fig. 6.13 Dc–3ϕac inverter topologies: (a) differential connection of 3ϕ load across outputs of buck converters: (b) simplification of low-pass filters to obtain the dc–3ϕac voltage-source inverter; (c) the dc–3ϕac current-source inverter.

If the converter output voltages V_1, V_2, and V_3 contain the same dc bias, then this dc bias will also appear at the neutral point V_n. The phase voltages V_{an}, V_{bn}, and V_{cn} are given by

$$\begin{aligned} V_{an} &= V_1 - V_n \\ V_{bn} &= V_2 - V_n \\ V_{cn} &= V_3 - V_n \end{aligned} \tag{6.15}$$

It can be seen that the dc biases cancel out, and do not appear in V_{an}, V_{bn}, and V_{cn}.

Let us realize converters 1, 2, and 3 of Fig. 6.12 using buck converters. Figure 6.13(a) is then obtained. The circuit is re-drawn in Fig. 6.13(b) for clarity. This converter is known by several names, including the *voltage-source inverter* and the buck-derived three-phase bridge.

Inverter circuits based on dc–dc converters other than the buck converter can be derived in a similar manner. Figure 6.13(c) contains a three-phase current-fed bridge converter having a boost-type voltage conversion ratio, also known as the *current-source inverter.* Since most inverter applications require the capability to reduce the voltage magnitude, a dc–dc buck converter is usually cascaded at the dc input port of this inverter. Several other examples of three-phase inverters are given in [5–7], in which the converters are capable of both increasing and decreasing the voltage magnitude.

6.2 A SHORT LIST OF CONVERTERS

An infinite number of converters are possible, and hence it is not feasible to list them all. A short list is given here.

Let's consider first the class of single-input single-output converters, containing a single inductor. There are a limited number of ways in which the inductor can be connected between the source and load. If we assume that the switching period is divided into two subintervals, then the inductor should be connected to the source and load in one manner during the first subinterval, and in a different manner during the second subinterval. One can examine all of the possible combinations, to derive the complete set of converters in this class [8–10]. By elimination of redundant and degenerate circuits, one finds that there are eight converters, listed in Fig. 6.14. How the converters are counted can actually be a matter of semantics and personal preference; for example, many people in the field would not consider the noninverting buck–boost converter as distinct from the inverting buck–boost. Nonetheless, it can be said that a converter is defined by the connections between its reactive elements, switches, source, and load; by how the switches are realized; and by the numerical range of reactive element values.

The first four converters of Fig. 6.14, the buck, boost, buck-boost, and the noninverting buck-boost, have been previously discussed. These converters produce a unipolar dc output voltage. With these converters, it is possible to increase, decrease, and/or invert a dc voltage.

Converters 5 and 6 are capable of producing a bipolar output voltage. Converter 5, the H–bridge, has previously been discussed. Converter 6 is a nonisolated version of a push–pull current-fed converter [11–15]. This converter can also produce a bipolar output voltage; however, its conversion ratio $M(D)$ is a nonlinear function of duty cycle. The number of switch elements can be reduced by using a two-winding inductor as shown. The function of the inductor is similar to that of the flyback converter, discussed in the next section. When switch 1 is closed the upper winding is used, while when switch 2 is closed, current flows through the lower winding. The current flows through only one winding at any given instant, and the total ampere-turns of the two windings are a continuous function of time. Advantages of this converter are its ground-referenced load and its ability to produce a bipolar output voltage using only two SPST current-bidirectional switches. The isolated version and its variants have found

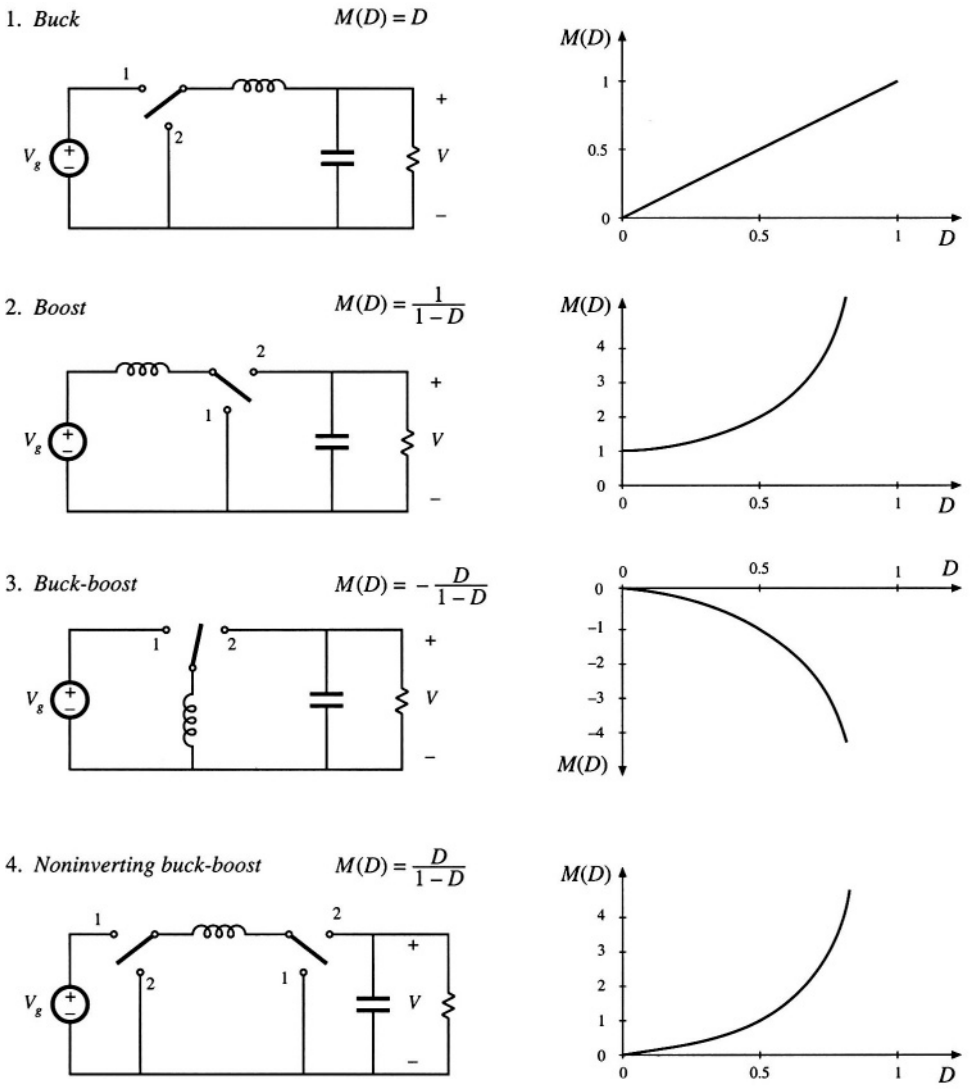

Fig. 6.14 Eight members of the basic class of single-input single-output converters containing a single inductor.

application in high-voltage dc power supplies.

Converters 7 and 8 can be derived as the inverses of converters 5 and 6. These converters are capable of interfacing an ac input to a dc output. The ac input current waveform can have arbitrary waveshape and power factor.

The class of single-input single-output converters containing two inductors is much larger. Several of its members are listed in Fig. 6.15. The Ćuk converter has been previously discussed and ana-

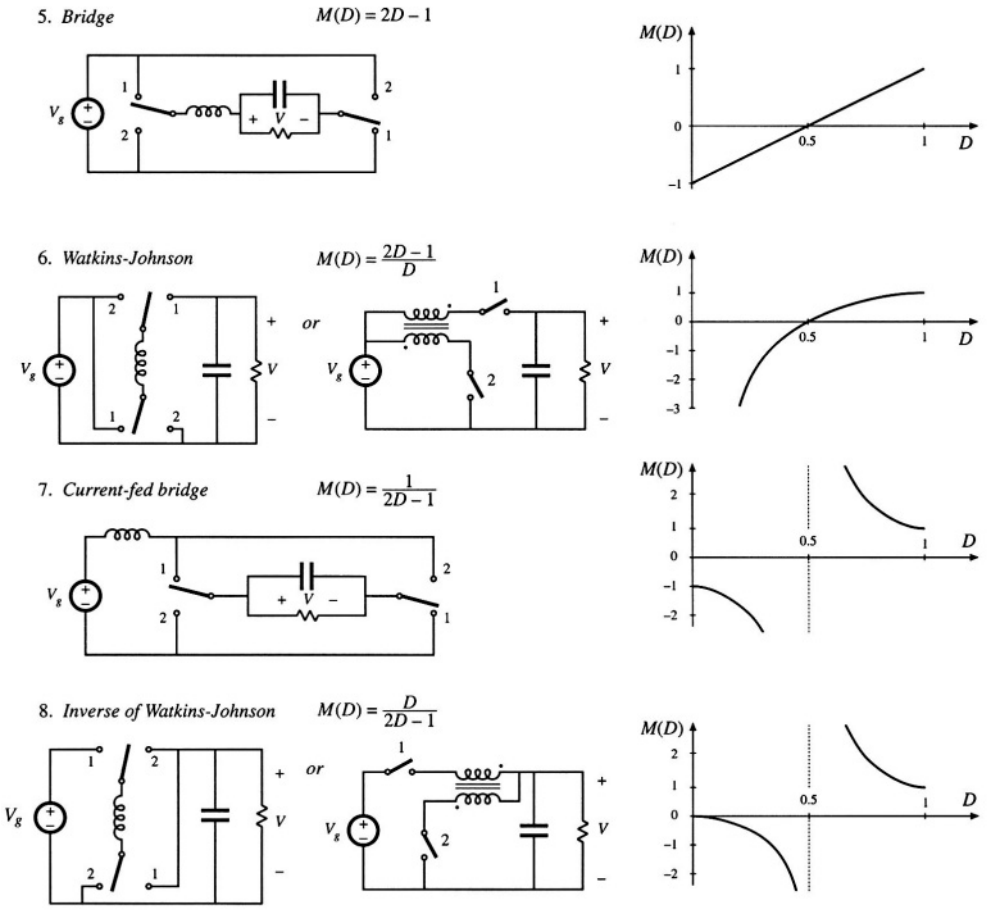

Fig. 6.14 Continued

lyzed. It has an inverting buck-boost characteristic, and exhibits nonpulsating input and output terminal currents. The SEPIC (single-ended primary inductance converter) [16], and its inverse, have noninverting buck–boost characteristics. The Ćuk and SEPIC also exhibit the desirable feature that the MOSFET source terminal is connected to ground; this simplifies the construction of the gate drive circuitry. Two-inductor converters having conversion ratios $M(D)$ that are biquadratic functions of the duty cycle D are also numerous. An example is converter 4 of Fig. 6.15 [17]. This converter can be realized using a single transistor and three diodes. Its conversion ratio is $M(D) = D^2$. This converter may find use in nonisolated applications that require a large step-down of the dc voltage, or in applications having wide variations in operating point.

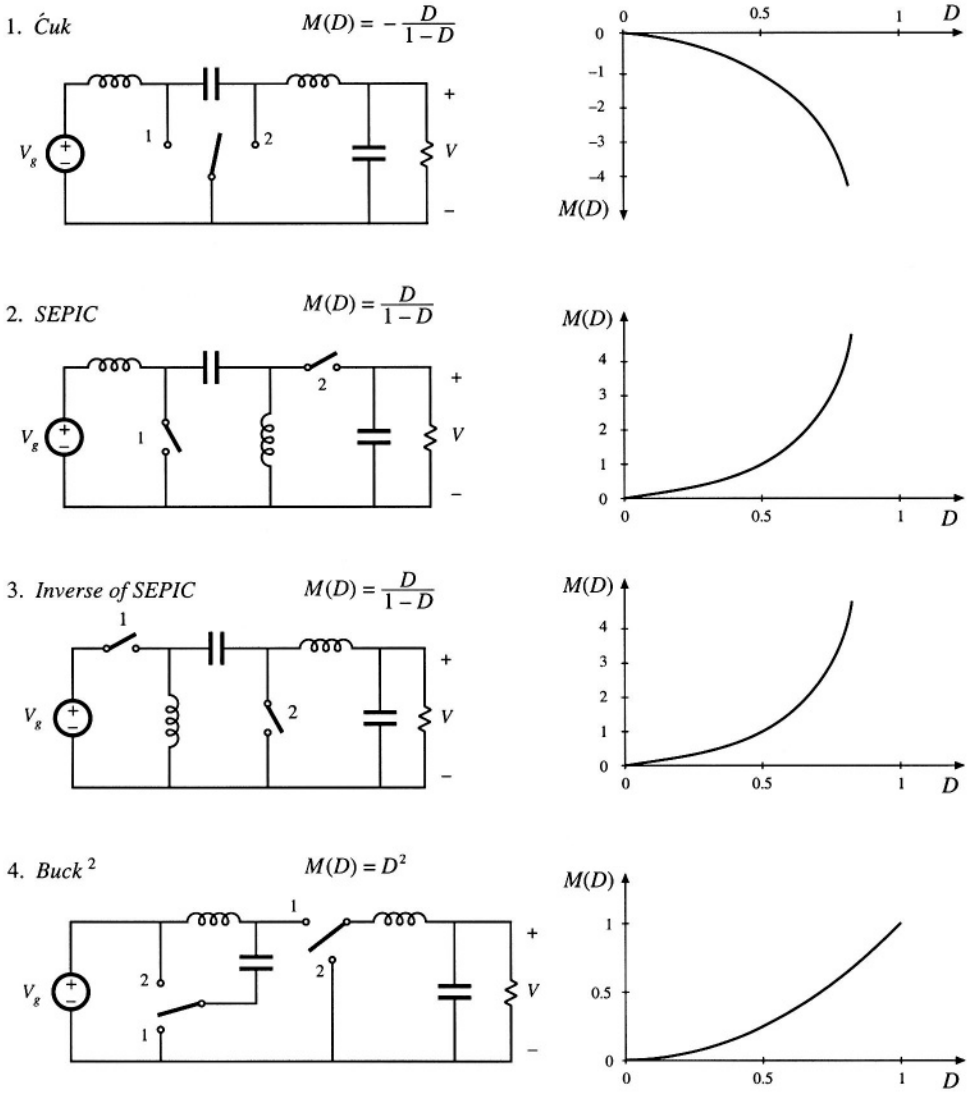

Fig. 6.15 Several members of the basic class of single-input single-output converters containing two inductors.

6.3 TRANSFORMER ISOLATION

In a large number of applications, it is desired to incorporate a transformer into a switching converter, to obtain dc isolation between the converter input and output. For example, in off-line applications (where the converter input is connected to the ac utility system), isolation is usually required by regulatory agen-

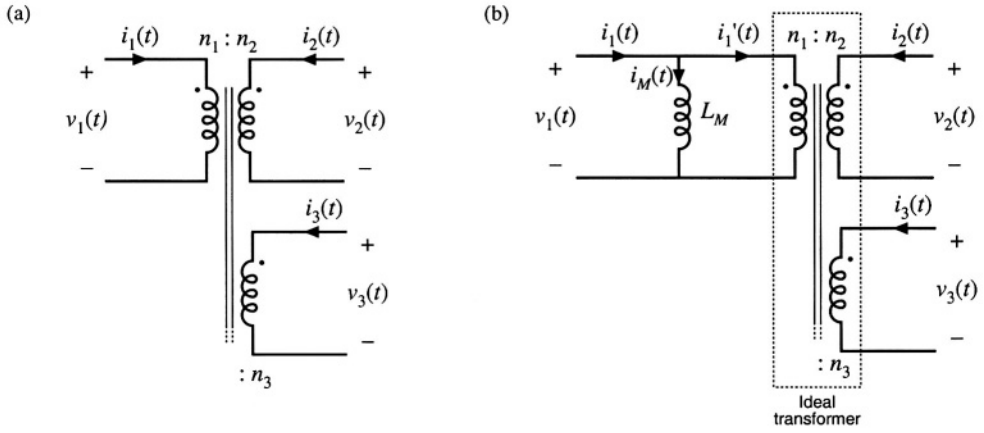

Fig. 6.16 Simplified model of a multiple-winding transformer: (a) schematic symbol, (b) equivalent circuit containing a magnetizing inductance and ideal transformer.

cies. Isolation could be obtained in these cases by simply connecting a 50 Hz or 60 Hz transformer at the converter ac input. However, since transformer size and weight vary inversely with frequency, significant improvements can be made by incorporating the transformer into the converter, so that the transformer operates at the converter switching frequency of tens or hundreds of kilohertz.

When a large step-up or step-down conversion ratio is required, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the transistors and diodes can be minimized, leading to improved efficiency and lower cost.

Multiple dc outputs can also be obtained in an inexpensive manner, by adding multiple secondary windings and converter secondary-side circuits. The secondary turns ratios are chosen to obtain the desired output voltages. Usually only one output voltage can be regulated via control of the converter duty cycle, so wider tolerances must be allowed for the auxiliary output voltages. *Cross regulation* is a measure of the variation in an auxiliary output voltage, given that the main output voltage is perfectly regulated [18–20].

A physical multiple-winding transformer having turns ratio $n_1 : n_2 : n_3 : \ldots$ is illustrated in Fig. 6.16(a). A simple equivalent circuit is illustrated in Fig. 6.16(b), which is sufficient for understanding the operation of most transformer-isolated converters. The model assumes perfect coupling between windings and neglects losses; more accurate models are discussed in a later chapter. The ideal transformer obeys the relationships

$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \ldots$$
$$0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + \ldots \tag{6.16}$$

In parallel with the ideal transformer is an inductance L_M, called the *magnetizing inductance,* referred to the transformer primary in the figure.

Physical transformers must contain a magnetizing inductance. For example, suppose we disconnect all windings except for the primary winding. We are then left with a single winding on a magnetic core—an inductor. Indeed, the equivalent circuit of Fig. 6.16(b) predicts this behavior, via the magnetizing inductance.

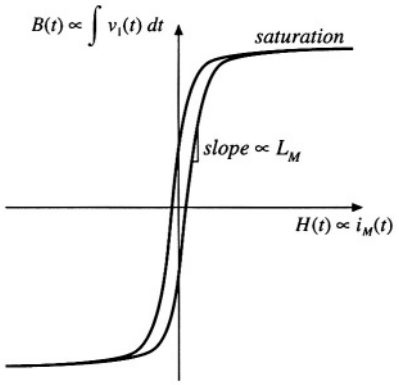

Fig. 6.17 *B–H* characteristics of transformer core.

The magnetizing current $i_M(t)$ is proportional to the magnetic field $H(t)$ inside the transformer core. The physical *B–H* characteristics of the transformer core material, illustrated in Fig. 6.17, govern the magnetizing current behavior. For example, if the magnetizing current $i_M(t)$ becomes too large, then the magnitude of the magnetic field $H(t)$ causes the core to saturate. The magnetizing inductance then becomes very small in value, effectively shorting out the transformer.

The presence of the magnetizing inductance explains why transformers do not work in dc circuits: at dc, the magnetizing inductance has zero impedance, and shorts out the windings. In a well-designed transformer, the impedance of the magnetizing inductance is large in magnitude over the intended range of operating frequencies, such that the magnetizing current $i_M(t)$ has much smaller magnitude than $i_1(t)$. Then $i_1'(t) \approx i_1(t)$, and the transformer behaves nearly as an ideal transformer. It should be emphasized that the magnetizing current $i_M(t)$ and the primary winding current $i_1(t)$ are independent quantities.

The magnetizing inductance must obey all of the usual rules for inductors. In the model of Fig. 6.16(b), the primary winding voltage $v_1(t)$ is applied across L_M, and hence

$$v_1(t) = L_M \frac{di_M(t)}{dt} \tag{6.17}$$

Integration leads to

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau) d\tau \tag{6.18}$$

So the magnetizing current is determined by the integral of the applied winding voltage. The principle of inductor volt-second balance also applies: when the converter operates in steady-state, the dc component of voltage applied to the magnetizing inductance must be zero:

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t) dt \tag{6.19}$$

Since the magnetizing current is proportional to the integral of the applied winding voltage, it is important that the dc component of this voltage be zero. Otherwise, during each switching period there will be a net increase in magnetizing current, eventually leading to excessively large currents and transformer saturation.

The operation of converters containing transformers may be understood by inserting the model of Fig. 6.16(b) in place of the transformer in the converter circuit. Analysis then proceeds as described in the previous chapters, treating the magnetizing inductance as any other inductor of the converter.

Practical transformers must also contain leakage inductance. A small part of the flux linking a winding may not link the other windings. In the two-winding transformer, this phenomenon may be modeled with small inductors in series with the windings. In most isolated converters, leakage inductance is a nonideality that leads to switching loss, increased peak transistor voltage, and that degrades cross-regulation, but otherwise has no influence on basic converter operation.

There are several ways of incorporating transformer isolation into a dc–dc converter. The full-bridge, half-bridge, forward, and push-pull converters are commonly used isolated versions of the buck converter. Similar isolated variants of the boost converter are known. The flyback converter is an isolated version of the buck–boost converter. These isolated converters, as well as isolated versions of the SEPIC and the Ćuk converter, are discussed in this section.

6.3.1 Full-Bridge and Half-Bridge Isolated Buck Converters

The full-bridge transformer-isolated buck converter is sketched in Fig. 6.18(a). A version containing a center-tapped secondary winding is shown; this circuit is commonly used in converters producing low output voltages. The two halves of the center-tapped secondary winding may be viewed as separate windings, and hence we can treat this circuit element as a three-winding transformer having turns ratio 1:*n*:*n*. When the transformer is replaced by the equivalent circuit model of Fig. 6.16(b), the circuit of Fig.

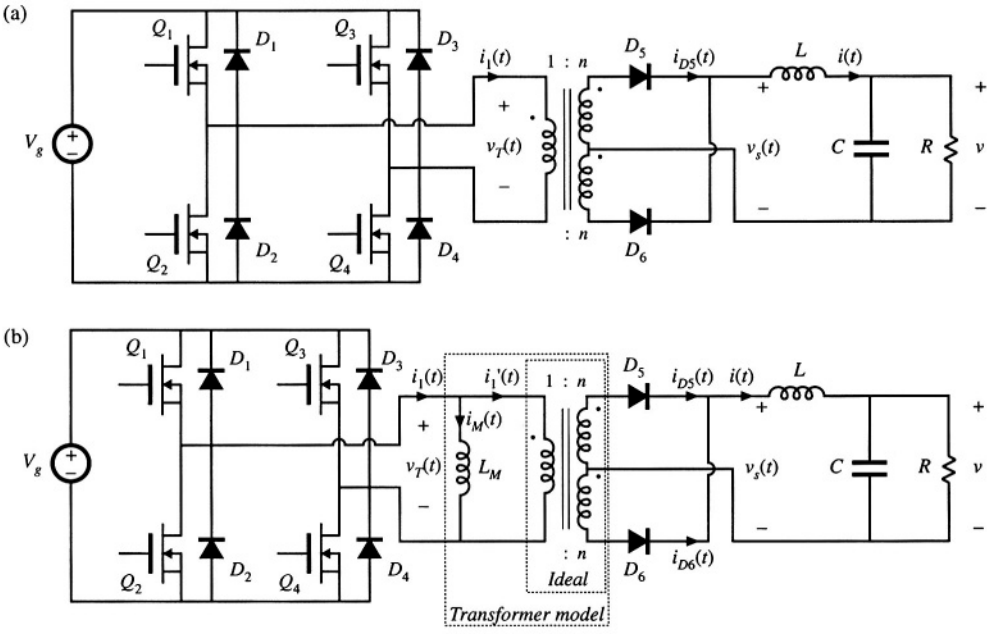

Fig. 6.18 Full-bridge transformer-isolated buck converter: (a) schematic diagram, (b) replacement of transformer with equivalent circuit model.

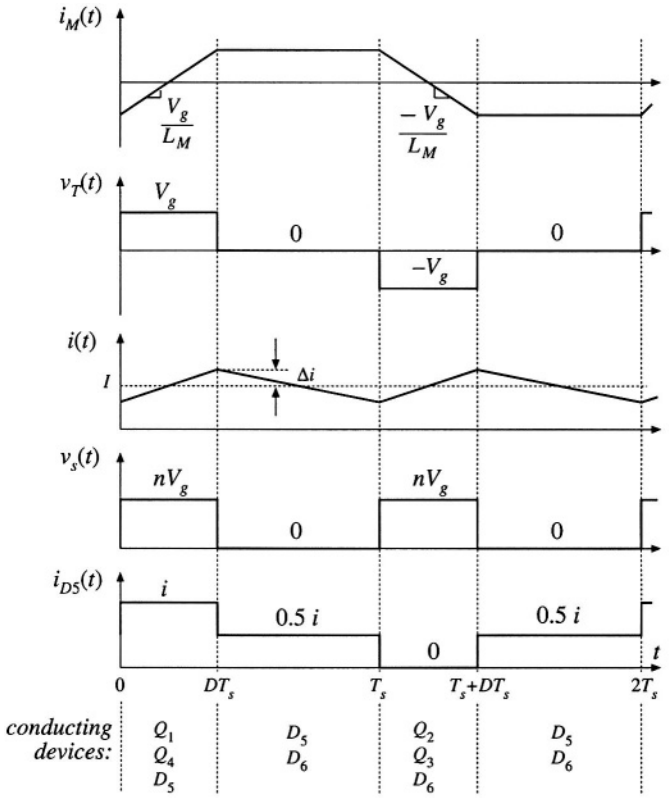

Fig. 6.19 Waveforms of the full-bridge transformer-isolated buck converter.

6.18(b) is obtained. Typical waveforms are illustrated in Fig. 6.19. The output portion of the converter is similar to the nonisolated buck converter—compare the $v_s(t)$ and $i(t)$ waveforms of Fig. 6.19 with Figs. 2.1(b) and 2.10.

During the first subinterval $0 < t < DT_s$, transistors Q_1 and Q_4 conduct, and the transformer primary voltage is $v_T = V_g$. This positive voltage causes the magnetizing current $i_M(t)$ to increase with a slope of V_g/L_M. The voltage appearing across each half of the center-tapped secondary winding is nV_g, with the polarity mark at positive potential. Diode D_5 is therefore forward-biased, and D_6 is reverse-biased. The voltage $v_s(t)$ is then equal to nV_g, and the output filter inductor current $i(t)$ flows through diode D_5.

Several transistor control schemes are possible for the second subinterval $DT_s < t < T_s$. In the most common scheme, all four transistors are switched off, and hence the transformer voltage is $v_T = 0$. Alternatively, transistors Q_2 and Q_4 could conduct, or transistors Q_1 and Q_3 could conduct. In any event, diodes D_5 and D_6 are both forward-biased during this subinterval; each diode conducts approximately one-half of the output filter inductor current.

Actually, the diode currents i_{D5} and i_{D6} during the second subinterval are functions of both the output inductor current and the transformer magnetizing current. In the ideal case (no magnetizing current), the transformer causes $i_{D5}(t)$ and $i_{D6}(t)$ to be equal in magnitude since, if $i_1'(t) = 0$, then $ni_{D5}(t) = ni_{D6}(t)$. But the sum of the two diode currents is equal to the output inductor current:

$$i_{D5}(t) + i_{D6}(t) = i(t) \tag{6.20}$$

Therefore, it must be true that $i_{D5} = i_{D6} = 0.5i$ during the second subinterval. In practice, the diode currents differ slightly from this result, because of the nonzero magnetizing current.

The ideal transformer currents in Fig. 6.18(b) obey

$$i_1'(t) - n i_{D5}(t) + n i_{D6}(t) = 0 \tag{6.21}$$

The node equation at the primary of the ideal transformer is

$$i_1(t) = i_M(t) + i_1'(t) \tag{6.22}$$

Elimination of $i_1'(t)$ from Eqs. (6.21) and (6.22) leads to

$$i_1(t) - n i_{D5}(t) + n i_{D6}(t) = i_M(t) \tag{6.23}$$

Equations (6.23) and (6.20) describe, in the general case, the transformer winding currents during the second subinterval. According to Eq. (6.23), the magnetizing current $i_M(t)$ may flow through the primary winding, through one of the secondary windings, or it may divide between all three of these windings. How the division occurs depends on the i–v characteristics of the conducting transistors and diodes, and on the transformer leakage inductances. In the case where $i_1 = 0$, the solution to Eqs. (6.20) and (6.23) is

$$\begin{aligned} i_{D5}(t) &= \frac{1}{2} i(t) - \frac{1}{2n} i_M(t) \\ i_{D6}(t) &= \frac{1}{2} i(t) + \frac{1}{2n} i_M(t) \end{aligned} \tag{6.24}$$

Provided that $i_M \ll ni$, then i_{D5} and i_{D6} are each approximately $0.5i$.

The next switching period, $T_s < t < 2T_s$, proceeds in a similar manner, except that the transformer is excited with voltage of the opposite polarity. During $T_s < t < (T_s + DT_s)$, transistors Q_2 and Q_3 and diode D_6 conduct. The applied transformer primary voltage is $v_T = -V_g$, which causes the magnetizing current to decrease with slope $-V_g/L_M$. The voltage $v_s(t)$ is equal to nV_g, and the output inductor current $i(t)$ flows through diode D_6. Diodes D_5 and D_6 again both conduct during $(T_s + DT_s) < t < 2T_s$, with operation similar to subinterval 2 described previously. It can be seen that the switching ripple in the output filter elements has frequency $f_s = 1/T_s$. However, the transformer waveforms have frequency $0.5f_s$.

By application of the principle of inductor volt-second balance to the magnetizing inductance, the average value of the transformer voltage $v_T(t)$ must be zero when the converter operates in steady state. During the first switching period, positive volt-seconds are applied to the transformer, approximately equal to

$$\left| V_g - \left(Q_1 \text{ and } Q_4 \text{ forward voltage drops} \right) \right| \left(Q_1 \text{ and } Q_4 \text{ conduction time} \right) \tag{6.25}$$

During the next switching period, negative volt-seconds are applied to the transformer, given by

$$-\left| V_g - \left(Q_2 \text{ and } Q_3 \text{ forward voltage drops} \right) \right| \left(Q_2 \text{ and } Q_3 \text{ conduction time} \right) \tag{6.26}$$

The net volt-seconds, that is, the sum of Eqs. (6.25) and (6.26), should equal zero. While the full bridge scheme causes this to be approximately true, in practice there exist imbalances such as small differences in the transistor forward voltage drops or in the transistor switching times, so that $\langle v_T \rangle$ is small but nonzero. In consequence, during every two switching periods there is a net increase in the magnitude of the magnetizing current. This increase can cause the transistor forward voltage drops to change such that small imbalances are compensated. However, if the imbalances are too large, then the magnetizing current becomes large enough to saturate the transformer.

Transformer saturation under steady-state conditions can be avoided by placing a capacitor in series with the transformer primary. Imbalances then induce a dc voltage component across the capacitor, rather than across the transformer primary. Another solution is the use of current-programmed control, discussed in a later chapter. The series capacitor is omitted when current-programmed control is used.

By application of the principle of volt-second balance to the output filter inductor *L,* the dc load voltage must be equal to the dc component of $v_s(t)$:

$$V = \langle v_s \rangle \tag{6.27}$$

By inspection of the $v_s(t)$ waveform in Fig. 6.19, $\langle v_s \rangle = nDV_g$. Hence,

$$V = nDV_g \tag{6.28}$$

So as in the buck converter, the output voltage can be controlled by variation of the transistor duty cycle *D.* An additional increase or decrease of the voltage can be obtained via the physical transformer turns ratio *n.* Equation (6.28) is valid for operation in the continuous conduction mode; as in the nonisolated buck converter, the full-bridge and half-bridge converters can operate in discontinuous conduction mode at light load. The converter can operate over essentially the entire range of duty cycles $0 \le D < 1$.

Transistors Q_1 and Q_2 must not conduct simultaneously; doing so would short out the dc source V_g, causing a *shoot-through* current spike. This transistor *cross-conduction* condition can lead to low efficiency and transistor failure. Cross conduction can be prevented by introduction of delay between the turn-off of one transistor and the turn-on of the next transistor. Diodes D_1 to D_4 ensure that the peak transistor voltage is limited to the dc input voltage V_g, and also provide a conduction path for the transformer magnetizing current at light load. Details of the switching transitions of the full-bridge circuit are discussed further in a later chapter, in conjunction with zero-voltage switching phenomena.

The full-bridge configuration is typically used in switching power supplies at power levels of approximately 750 W and greater. It is usually not used at lower power levels because of its high parts count—four transistors and their associated drive circuits are required. The utilization of the transformer is good, leading to small transformer size. In particular, the utilization of the transformer core is very good, since the transformer magnetizing current can be both positive and negative. Hence, the entire core *B–H* loop can be used. However, in practice, the flux swing is usually limited by core loss. The transformer primary winding is effectively utilized. But the center-tapped secondary winding is not, since each half of the center-tapped winding transmits power only during alternate switching periods. Also, the secondary winding currents during subinterval 2 lead to winding power loss, but not to transmittal of energy to the load. Design of the transformer of the full-bridge configuration is discussed in detail in a later chapter.

The half-bridge transformer-isolated buck converter is illustrated in Fig. 6.20. Typical waveforms are illustrated in Fig. 6.21. This circuit is similar to the full-bridge of Fig. 6.18(a), except transistors Q_3 and Q_4, and their antiparallel diodes, have been replaced with large-value capacitors C_a and C_b. By volt-second balance of the transformer magnetizing inductance, the dc voltage across capacitor C_b is equal to the dc component of the voltage across transistor Q_2, or $0.5V_g$. The transformer primary voltage

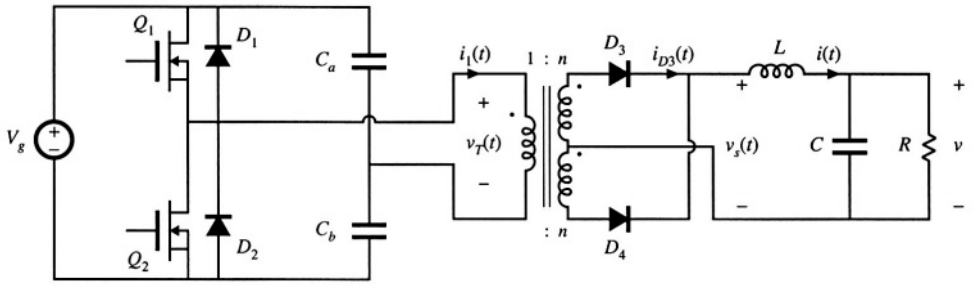

Fig. 6.20 Half-bridge transformer-isolated buck converter.

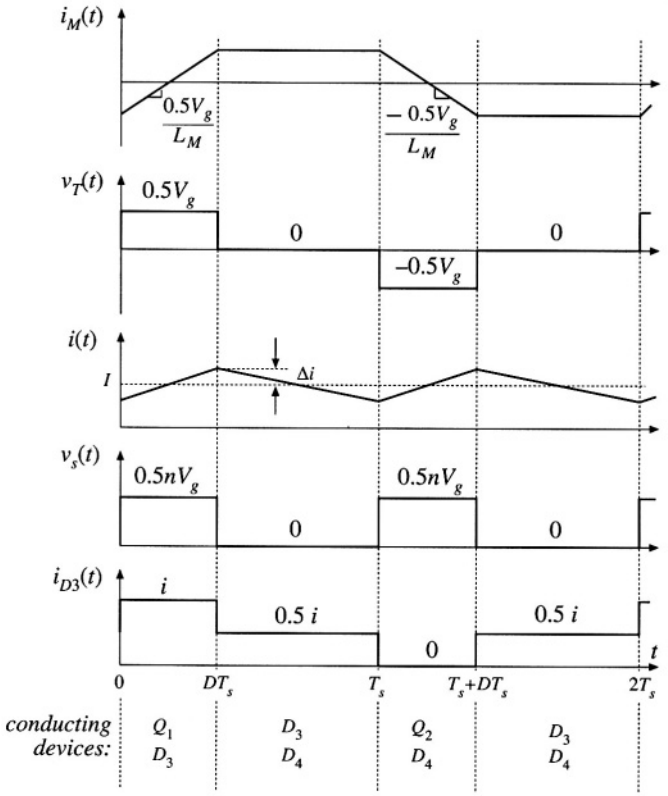

Fig. 6.21 Waveforms of the half-bridge transformer-isolated buck converter.

$v_T(t)$ is then $0.5V_g$ when transistor Q_1 conducts, and $-0.5V_g$ when transistor Q_2 conducts. The magnitude of $v_T(t)$ is half as large as in the full-bridge configuration, with the result that the output voltage is reduced by a factor of 0.5:

$$V = 0.5nDV_g \tag{6.29}$$

The factor of 0.5 can be compensated for by doubling the transformer turns ratio n. However, this causes the transistor currents to double.

So the half-bridge configuration needs only two transistors rather than four, but these two transistors must handle currents that are twice as large as those of the full-bridge circuit. In consequence, the half-bridge configuration finds application at lower power levels, for which transistors with sufficient current rating are readily available, and where low parts count is important. Utilization of the transformer core and windings is essentially the same as in the full-bridge, and the peak transistor voltage is clamped to the dc input voltage V_g by diodes D_1 and D_2. It is possible to omit capacitor C_a if desired. The current-programmed mode generally does not work with half-bridge converters.

6.3.2 Forward Converter

The forward converter is illustrated in Fig. 6.22. This transformer-isolated converter is based on the buck converter. It requires a single transistor, and hence finds application at power levels lower than those commonly encountered in the full-bridge and half-bridge configurations. Its nonpulsating output current, shared with other buck-derived converters, makes the forward converter well suited for applications involving high output currents. The maximum transistor duty cycle is limited in value; for the common choice $n_1 = n_2$, the duty cycle is limited to the range $0 \le D < 0.5$.

The transformer magnetizing current is reset to zero while the transistor is in the off-state. How this occurs can be understood by replacing the three-winding transformer in Fig. 6.22 with the equivalent circuit of Fig. 6.16(b). The resulting circuit is illustrated in Fig. 6.23, and typical waveforms are given in Fig. 6.24. The magnetizing inductance L_M, in conjunction with diode D_1, must operate in the discontinuous conduction mode. The output inductor L, in conjunction with diode D_3, may operate in either continuous or discontinuous conduction mode. The waveforms of Fig. 6.24 are sketched for continuous mode operation of inductor L. During each switching period, three subintervals then occur as illustrated in Fig. 6.25.

During subinterval 1, transistor Q_1 conducts and the circuit of Fig. 6.25(a) is obtained. Diode D_2 becomes forward-biased, while diodes D_1 and D_3 are reverse-biased. Voltage V_g is applied to the transformer primary winding, and hence the transformer magnetizing current $i_M(t)$ increases with a slope of V_g/L_M as illustrated in Fig. 6.24. The voltage across diode D_3 is equal to V_g, multiplied by the turns ratio n_3/n_1.

The second subinterval begins when transistor Q_1 is switched off. The circuit of Fig. 6.25(b) is

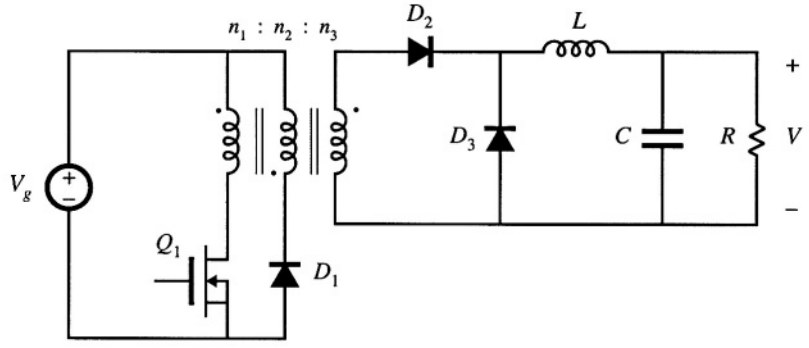

Fig. 6.22 Single-transistor forward converter.

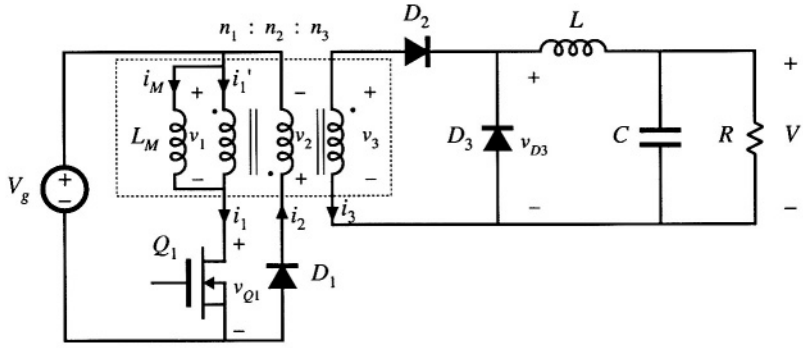

Fig. 6.23 Forward converter, with transformer equivalent circuit model.

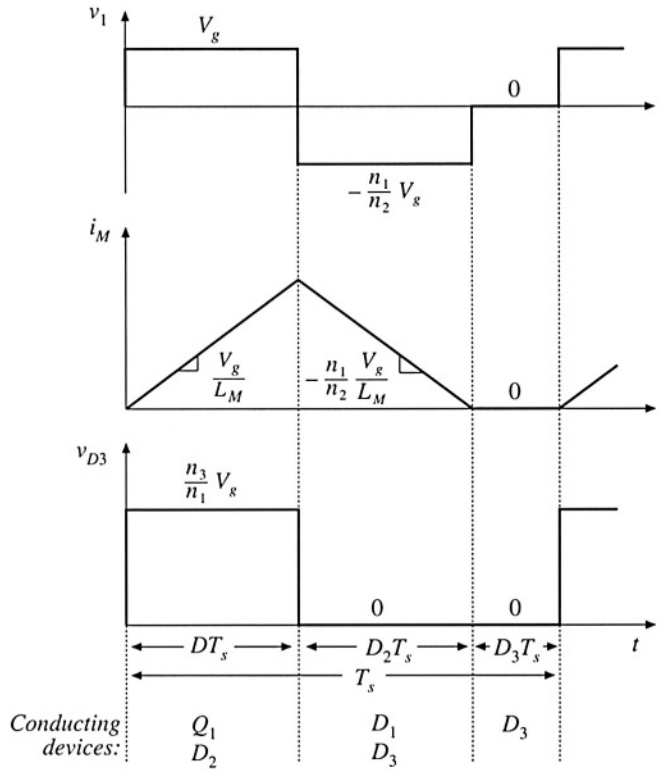

Fig. 6.24 Waveforms of the forward converter.

then obtained. The transformer magnetizing current $i_M(t)$ at this instant is positive, and must continue to flow. Since transistor Q_1 is off, the equivalent circuit model predicts that the magnetizing current must flow into the primary of the ideal transformer. It can be seen that $n_1 i_M$ ampere-turns flow out of the polarity mark of the primary winding. Hence, according to Eq. (6.16), an equal number of total ampere-turns must flow into the polarity marks of the other windings. Diode D_2 prevents current from flowing into the

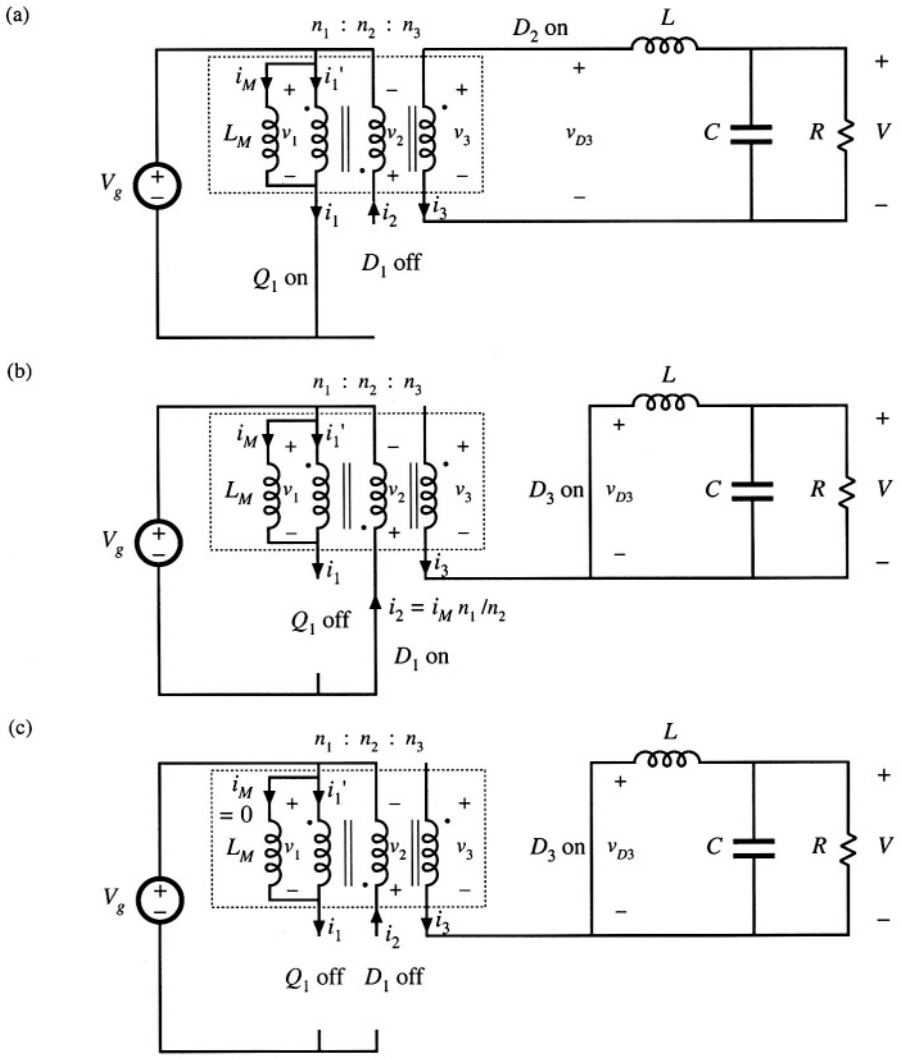

Fig. 6.25 Forward converter circuit: (a) during subinterval 1, (b) during subinterval 2, (c) during subinterval 3.

polarity mark of winding 3. Hence, the current $i_M n_1/n_2$ must flow into the polarity mark of winding 2. So diode D_1 becomes forward-biased, while diode D_2 is reverse-biased. Voltage V_g is applied to winding 2, and hence the voltage across the magnetizing inductance is $-V_g n_1/n_2$, referred to winding 1. This negative voltage causes the magnetizing current to decrease, with a slope of $-V_g n_1/n_2 L_M$. Since diode D_2 is reverse-biased, diode D_3 must turn on to conduct the output inductor current $i(t)$.

When the magnetizing current reaches zero, diode D_1 becomes reverse-biased. Subinterval 3 then begins, and the circuit of Fig. 6.25(c) is obtained. Elements Q_1, D_1, and D_2 operate in the off state, and the magnetizing current remains at zero for the balance of the switching period.

By application of the principle of inductor volt-second balance to the transformer magnetizing

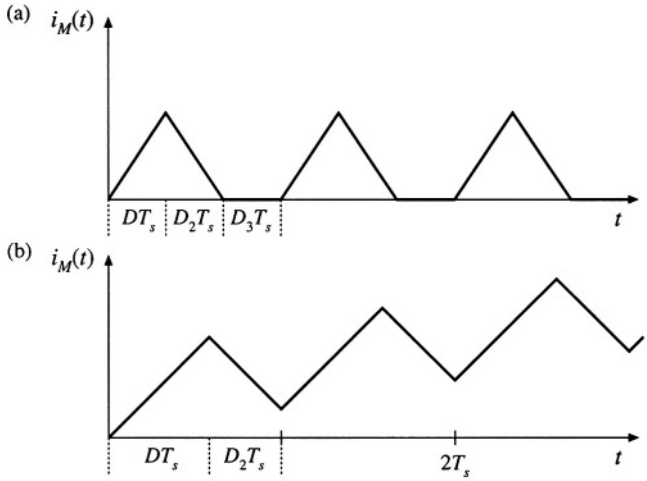

Fig. 6.26 Magnetizing current waveform, forward converter: (a) DCM, $D < 0.5$; (b) CCM, $D > 0.5$.

inductance, the primary winding voltage $v_1(t)$ must have zero average. Referring to Fig. 6.24, the average of $v_1(t)$ is given by

$$\langle v_1 \rangle = D(V_g) + D_2(-V_g n_1/n_2) + D_3(0) = 0 \tag{6.30}$$

Solution for the duty cycle D_2 yields

$$D_2 = \frac{n_2}{n_1} D \tag{6.31}$$

Note that the duty cycle D_3 cannot be negative. But since $D + D_2 + D_3 = 1$, we can write

$$D_3 = 1 - D - D_2 \geq 0 \tag{6.32}$$

Substitution of Eq. (6.31) into Eq. (6.32) leads to

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0 \tag{6.33}$$

Solution for D then yields

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}} \tag{6.34}$$

So the maximum duty cycle is limited. For the common choice $n_1 = n_2$, the limit becomes

$$D \leq \frac{1}{2} \tag{6.35}$$

If this limit is violated, then the transistor off-time is insufficient to reset the transformer magnetizing current to zero before the end of the switching period. Transformer saturation may then occur.

The transformer magnetizing current waveform $i_M(t)$ is illustrated in Fig. 6.26, for the typical

case where $n_1 = n_2$. Figure 6.26(a) illustrates operation with $D \geq 0.5$. The magnetizing inductance, in conjunction with diode D_1, operates in the discontinuous conduction mode, and $i_M(t)$ is reset to zero before the end of each switching period. Figure 6.26(b) illustrates what happens when the transistor duty cycle D is greater than 0.5. There is then no third subinterval, and the magnetizing inductance operates in continuous conduction mode. Furthermore, subinterval 2 is not long enough to reset the magnetizing current to zero. Hence, there is a net increase of $i_M(t)$ over each switching period. Eventually, the magnetizing current will become large enough the saturate the transformer.

The converter output voltage can be found by application of the principle of inductor volt-second balance to inductor L. The voltage across inductor L must have zero dc component, and therefore the dc output voltage V is equal to the dc component of diode D_3 voltage $v_{D3}(t)$. The waveform $v_{D3}(t)$ is illustrated in Fig. 6.24. It has an average value of

$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} D V_g \tag{6.36}$$

This is the solution of the forward converter in the continuous conduction mode. The solution is subject to the constraint given in Eq. (6.34).

It can be seen from Eq. (6.34) that the maximum duty cycle could be increased by decreasing the turns ratio n_2/n_1. This would cause $i_M(t)$ to decrease more quickly during subinterval 2, resetting the transformer faster. Unfortunately, this also increases the voltage stress applied to transistor Q_1. The maximum voltage applied to transistor Q_1 occurs during subinterval 2; solution of the circuit of Fig. 6.25(b) for this voltage yields

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right) \tag{6.37}$$

For the common choice $n_1 = n_2$, the voltage applied to the transistor during subinterval 2 is $2V_g$. In practice, a somewhat higher voltage is observed, due to ringing associated with the transformer leakage inductance. So decreasing the turns ratio n_2/n_1 allows increase of the maximum transistor duty cycle, at the expense of increased transistor blocking voltage.

A two-transistor version of the forward converter is illustrated in Fig. 6.27. Transistors Q_1 and Q_2 are controlled by the same gate drive signal, such that they both conduct during subinterval 1, and are off during subintervals 2 and 3. The secondary side of the converter is identical to the single-transistor forward converter; diode D_3 conducts during subinterval 1, while diode D_4 conducts during subintervals 2 and 3. During subinterval 2, the magnetizing current $i_M(t)$ forward-biases diodes D_1 and D_2. The trans-

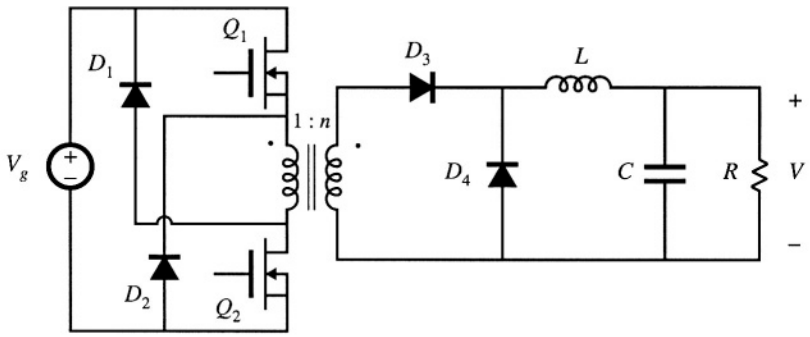

Fig. 6.27 Two-transistor forward converter.

former primary winding is then connected to V_g, with polarity opposite that of subinterval 1. The magnetizing current then decreases, with slope $-V_g/L_M$. When the magnetizing current reaches zero, diodes D_1 and D_2 become reverse-biased. The magnetizing current then remains at zero for the balance of the switching period. So operation of the two-transistor forward converter is similar to the single-transistor forward converter, in which $n_1 = n_2$. The duty cycle is limited to $D < 0.5$. This converter has the advantage that the transistor peak blocking voltage is limited to V_g, and is clamped by diodes D_1 and D_2. Typical power levels of the two-transistor forward converter are similar to those of the half-bridge configuration.

The utilization of the transformer of the forward converter is quite good. Since the transformer magnetizing current cannot be negative, only half of the core *B–H* loop can be used. This would seemingly imply that the transformer cores of forward converters should be twice as large as those of full- or half-bridge converters. However, in modern high-frequency converters, the flux swing is constrained by core loss rather than by the core material saturation flux density. In consequence, the utilization of the transformer core of the forward converter can be as good as in the full- or half-bridge configurations. Utilization of the primary and secondary windings of the transformer is better than in the full-bridge, half-bridge, or push-pull configurations, since the forward converter requires no center-tapped windings. During subinterval 1, all of the available winding copper is used to transmit power to the load. Essentially no unnecessary current flows during subintervals 2 and 3. Typically, the magnetizing current is small compared to the reflected load current, and has negligible effect on the transformer utilization. So the transformer core and windings are effectively utilized in modern forward converters.

6.3.3 Push-Pull Isolated Buck Converter

The push-pull isolated buck converter is illustrated in Fig. 6.28. The secondary-side circuit is identical with the full- and half-bridge converters, with identical waveforms. The primary-side circuit contains a center-tapped winding. Transistor Q_1 conducts for time DT_s during the first switching period. Transistor Q_2 conducts for an identical length of time during the next switching period, such that volt-second balance is maintained across the transformer primary winding. Converter waveforms are illustrated in Fig. 6.29. This converter can operate oven the entire range of duty cycles $0 \le D < 1$. Its conversion ratio is given by

$$V = nDV_g \tag{6.38}$$

This converter is sometimes used in conjunction with low input voltages. It tends to exhibit low primary-

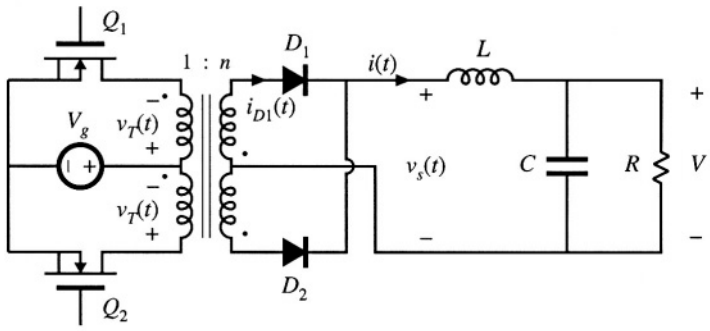

Fig. 6.28 Push-pull isolated buck converter.

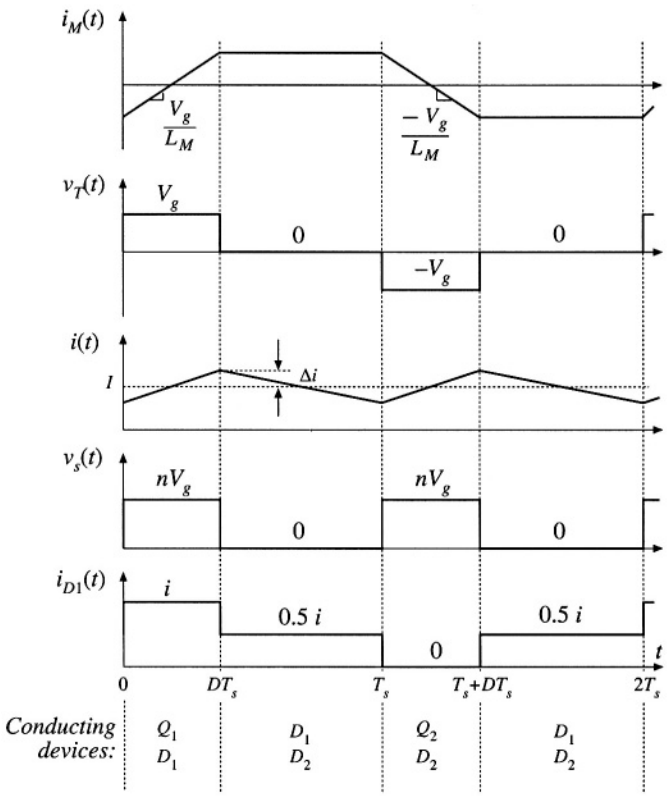

Fig. 6.29 Waveforms of the push-pull isolated buck converter.

side conduction losses, since at any given instant only one transistor is connected in series with the dc source V_g. The ability to operate with transistor duty cycles approaching unity also allows the turns ratio n to be minimized, reducing the transistor currents.

The push-pull configuration is prone to transformer saturation problems. Since it cannot be guaranteed that the forward voltage drops and conduction times of transistors Q_1 and Q_2 are exactly equal, small imbalances can cause the dc component of voltage applied to the transformer primary to be nonzero. In consequence, during every two switching periods there is a net increase in the magnitude of the magnetizing current. If this imbalance continues, then the magnetizing current can eventually become large enough to saturate the transformer.

Current-programmed control can be employed to mitigate the transformer saturation problems. Operation of the push-pull converter using only duty cycle control is not recommended.

Utilization of the transformer core material and secondary winding is similar to that for the full-bridge converter. The flux and magnetizing current can be both positive and negative, and therefore the entire *B–H* loop can be used, if desired. Since the primary and secondary windings are both center-tapped, their utilization is suboptimal.

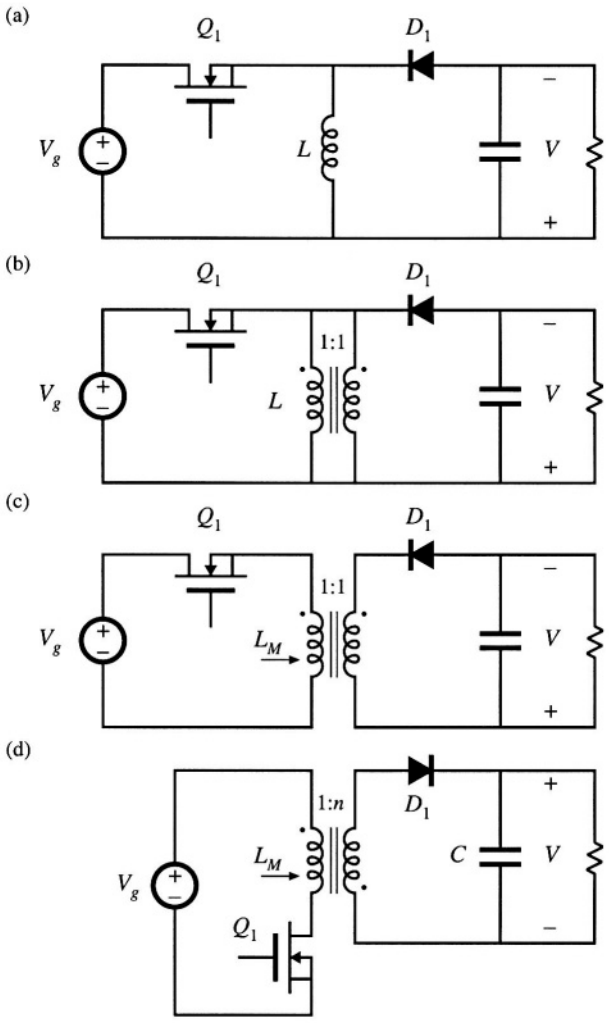

Fig. 6.30 Derivation of the flyback converter: (a) buck–boost converter; (b) inductor L is wound with two parallel wires; (c) inductor windings are isolated, leading to the flyback converter; (d) with a 1:n turns ratio and positive output.

6.3.4 Flyback Converter

The flyback converter is based on the buck–boost converter. Its derivation is illustrated in Fig. 6.30. Figure 6.30(a) depicts the basic buck-boost converter, with the switch realized using a MOSFET and diode. In Fig. 6.30(b), the inductor winding is constructed using two wires, with a 1:1 turns ratio. The basic function of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Fig. 6.30(c), the connections between the two windings are broken. One winding is used while the transistor Q_1 conducts, while the other winding is used when diode D_1 conducts. The total current in the two windings is unchanged from the circuit of Fig. 6.30(b); however, the current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases

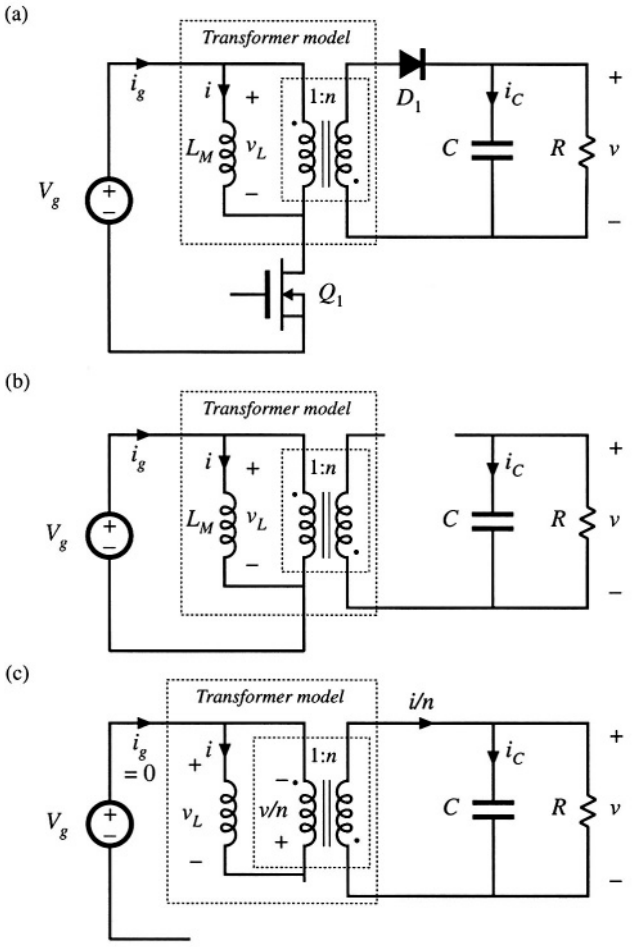

Fig. 6.31 Flyback converter circuit: (a) with transformer equivalent circuit model, (b) during subinterval 1, (c) during subinterval 2.

are identical. Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is "two-winding inductor." This device is sometimes also called a *flyback transformer*. Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. Figure 6.30(d) illustrates the usual configuration of the flyback converter. The MOSFET source is connected to the primary-side ground, simplifying the gate drive circuit. The transformer polarity marks are reversed, to obtain a positive output voltage. A 1:n turns ratio is introduced; this allows better converter optimization.

The flyback converter may be analyzed by insertion of the model of Fig. 6.16(b) in place of the flyback transformer. The circuit of Fig. 6.31(a) is then obtained. The magnetizing inductance L_M functions in the same manner as inductor L of the original buck-boost converter of Fig. 6.30(a). When transistor Q_1 conducts, energy from the dc source V_g is stored in L_M. When diode D_1 conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the 1:n turns ratio.

During subinterval 1, while transistor Q_1 conducts, the converter circuit model reduces to Fig.

6.31(b). The inductor voltage v_L, capacitor current i_C, and dc source current i_g are given by

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{v}{R} \\ i_g &= i \end{aligned} \tag{6.39}$$

With the assumption that the converter operates in the continuous conduction mode, with small inductor current ripple and small capacitor voltage ripple, the magnetizing current i and output capacitor voltage v can be approximated by their dc components, I and V, respectively. Equation (6.39) then becomes

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{V}{R} \\ i_g &= I \end{aligned} \tag{6.40}$$

During the second subinterval, the transistor is in the off-state, and the diode conducts. The equivalent circuit of Fig. 6.31(c) is obtained. The primary-side magnetizing inductance voltage v_L, the capacitor current i_C, and the dc source current i_g for this subinterval are:

$$\begin{aligned} v_L &= -\frac{v}{n} \\ i_C &= \frac{i}{n} - \frac{v}{R} \\ i_g &= 0 \end{aligned} \tag{6.41}$$

It is important to consistently define $v_L(t)$ on the same side of the transformer for all subintervals. Upon making the small-ripple approximation, one obtains

$$\begin{aligned} v_L &= -\frac{V}{n} \\ i_C &= \frac{I}{n} - \frac{V}{R} \\ i_g &= 0 \end{aligned} \tag{6.42}$$

The $v_L(t)$, $i_C(t)$, and $i_g(t)$ waveforms are sketched in Fig. 6.32 for continuous conduction mode operation.

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0 \tag{6.43}$$

Solution for the conversion ratio then leads to

$$M(D) = \frac{V}{V_g} = n\,\frac{D}{D'} \tag{6.44}$$

So the conversion ratio of the flyback converter is similar to that of the buck-boost converter, but contains an added factor of n.

Application of the principle of charge balance to the output capacitor C leads to

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0 \tag{6.45}$$

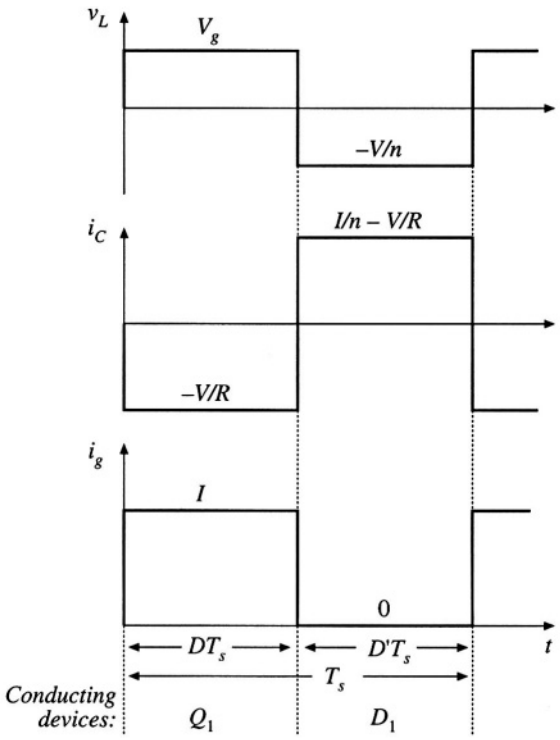

Fig. 6.32 Flyback converter waveforms, continuous conduction mode.

Solution for I yields

$$I = \frac{nV}{D'R} \tag{6.46}$$

This is the dc component of the magnetizing current, referred to the primary. The dc component of the source current i_g is

$$I_g = \langle i_g \rangle = D\langle I \rangle + D'\langle 0 \rangle \tag{6.47}$$

An equivalent circuit that models the dc components of the flyback converter waveforms can now be constructed. Circuits corresponding to the inductor loop equation (6.43) and to node equations (6.45) and (6.47) are illustrated in Fig. 6.33(a). By replacing the dependent sources with ideal dc transformers, one obtains Fig. 6.33(b). This is the dc equivalent circuit of the flyback converter. It contains a 1:D buck-type conversion ratio, followed by a D':1 boost-type conversion ratio, and an added factor of 1:n arising from the flyback transformer turns ratio. By use of the method developed in Chapter 3, the model can be refined to account for losses and to predict the converter efficiency. The flyback converter can also be operated in the discontinuous conduction mode; analysis is left as a homework problem. The results are similar to the DCM buck-boost converter results tabulated in Chapter 5, but are generalized to account for the turns ratio 1:n.

The flyback converter is commonly used at the 50 to 100 W power range, as well as in high-voltage power supplies for televisions and computer monitors. It has the advantage of very low parts

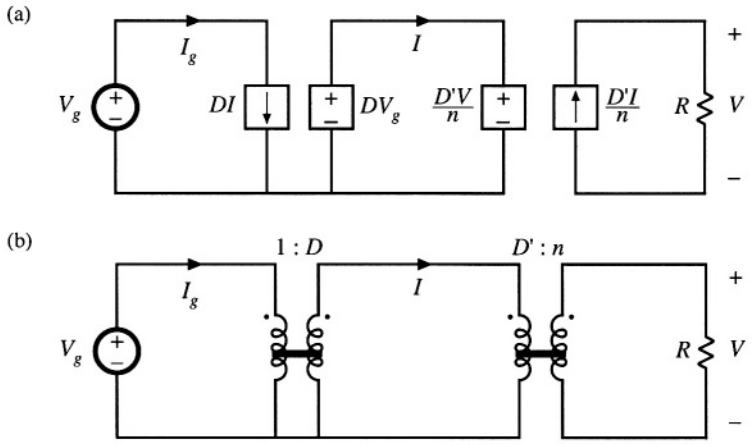

Fig. 6.33 Flyback converter equivalent circuit model, CCM: (a) circuits corresponding to Eqs. (6.43), (6.45), and (6.47); (b) equivalent circuit containing ideal dc transformers.

count. Multiple outputs can be obtained using a minimum number of parts: each additional output requires only an additional winding, diode, and capacitor. However, in comparison with the full-bridge, half-bridge, or two-transistor forward converters, the flyback converter has the disadvantages of high transistor voltage stress and poor cross-regulation. The peak transistor voltage is equal to the dc input voltage V_g plus the reflected load voltage V/n; in practice, additional voltage is observed due to ringing associated with the transformer leakage inductance. Rigorous comparison of the utilization of the flyback transformer with the transformers of buck-derived circuits is difficult because of the different functions performed by these elements. The magnetizing current of the flyback transformer is unipolar, and hence no more than half of the core material B–H loop can be utilized. The magnetizing current must contain a significant dc component. Yet, the size of the flyback transformer is quite small in designs intended to operate in the discontinuous conduction mode. However, DCM operation leads to increased peak currents in the transistor, diode, and filter capacitors. Continuous conduction mode designs require larger values of L_M, and hence larger flyback transformers, but the peak currents in the power stage elements are lower.

6.3.5 Boost-Derived Isolated Converters

Transformer-isolated boost converters can be derived by inversion of the source and load of buck-derived isolated converters. A number of configurations are known, and two of these are briefly discussed here. These converters find some employment in high-voltage power supplies, as well as in low-harmonic rectifier applications.

A full-bridge configuration is diagrammed in Fig. 6.34, and waveforms for the continuous conduction mode are illustrated in Fig. 6.35. The circuit topologies during the first and second subintervals are equivalent to those of the basic nonisolated boost converter, and when the turns ratio is 1:1, the inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to the inductor current and diode current waveforms of the nonisolated boost converter.

During subinterval 1, all four transistors operate in the on state. This connects the inductor L across the dc input source V_g, and causes diodes D_1 and D_2 to be reverse-biased. The inductor current $i(t)$

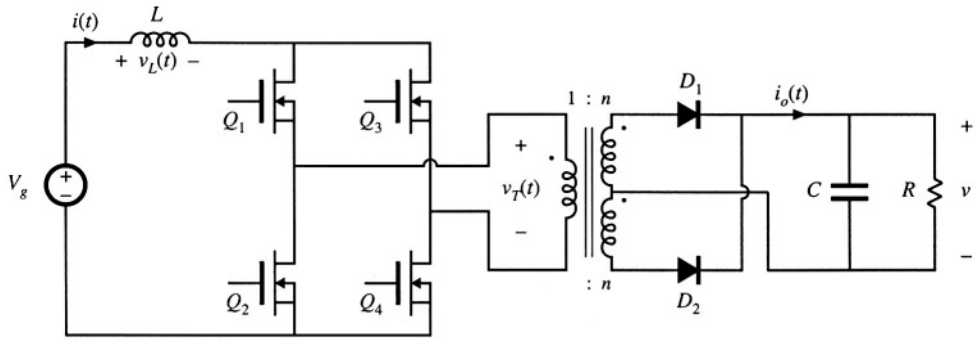

Fig. 6.34 Full-bridge transformer-isolated boost converter.

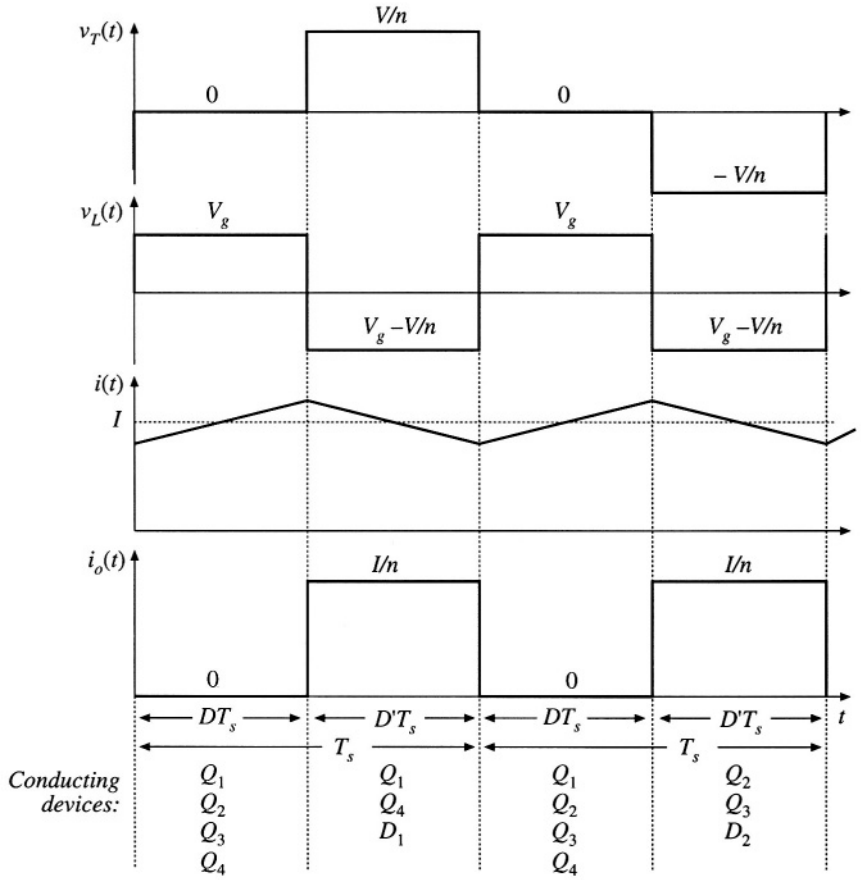

Fig. 6.35 Waveforms of the transformer-isolated full-bridge boost converter, CCM.

increases with slope V_g/L, and energy is transferred from the dc source V_g to inductor L. During the second subinterval, transistors Q_2 and Q_3 operate in the off state, so that inductor L is connected via transistors Q_1 and Q_4 through the transformer and diode D_1 to the dc output. The next switching period is similar, except that during subinterval 2, transistors Q_1 and Q_4 operate in the off state, and inductor L is connected via transistors Q_2 and Q_3 through the transformer and diode D_2 to the dc output. If the transistor off-times and the diode forward drops are identical, then the average transformer voltage is zero, and the net volt-seconds applied to the transformer magnetizing inductance over two switching periods is zero.

Application of the principle of inductor volt-second balance to the inductor voltage waveform $v_L(t)$ yields

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(V_g - \frac{V}{R}\right) = 0 \tag{6.48}$$

Solution for the conversion ratio $M(D)$ then leads to

$$M(D) = \frac{V}{V_g} = \frac{n}{D'} \tag{6.49}$$

This result is similar to the boost converter $M(D)$, with an added factor of n due to the transformer turns ratio.

The transistors must block the reflected load voltage $V/n = V_g/D'$. In practice, additional voltage

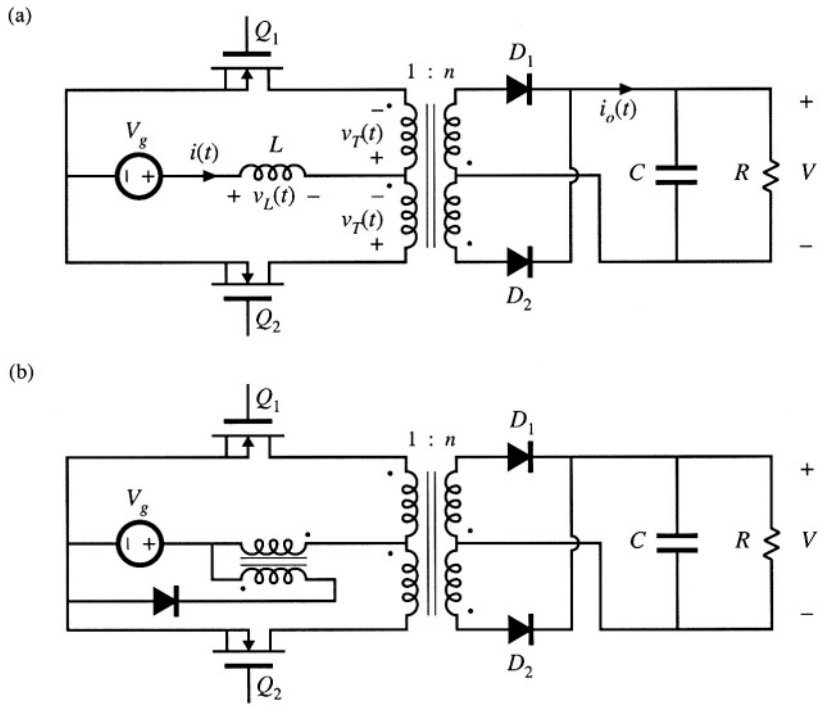

Fig. 6.36 Push-pull isolated converters: (a) based on the boost converter, (b) based on the Watkins-Johnson converter.

is observed due to ringing associated with the transformer leakage inductance. Because the instantaneous transistor current is limited by inductor L, saturation of the transformer due to small imbalances in the semiconductor forward voltage drops or conduction times is not catastrophic. Indeed, control schemes are known in which the transformer is purposely operated in saturation during subinterval 1 [13, 15].

A push-pull configuration is depicted in Fig. 6.36(a). This configuration requires only two transistors, each of which must block voltage $2V/n$. Operation is otherwise similar to that of the full-bridge. During subinterval 1, both transistors conduct. During subinterval 2, one of the transistors operates in the off state, and energy is transferred from the inductor through the transformer and one of the diodes to the output. Transistors conduct during subinterval 2 during alternate switching periods, such that transformer volt-second balance is maintained. A similar push-pull version of the Watkins-Johnson converter, converter 6 of Fig. 6.14, is illustrated in Fig. 6.36(b).

6.3.6 Isolated Versions of the SEPIC and the Ćuk Converter

The artifice used to obtain isolation in the flyback converter can also be applied to the SEPIC and inverse-SEPIC. Referring to Fig. 6.37(a), inductor L_2 can be realized using two windings, leading to the isolated SEPIC of Fig. 6.37(b). An equivalent circuit is given in Fig. 6.37(c). It can be seen that the mag-

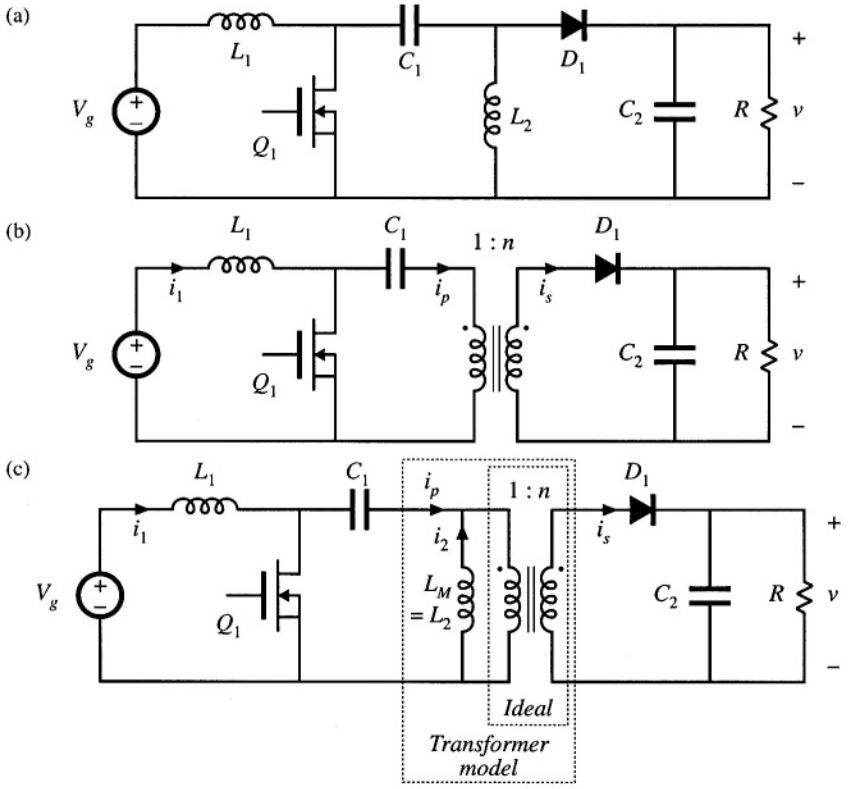

Fig. 6.37 Obtaining isolation in the SEPIC: (a) basic nonisolated converter, (b) isolated SEPIC, (c) with transformer equivalent circuit model.

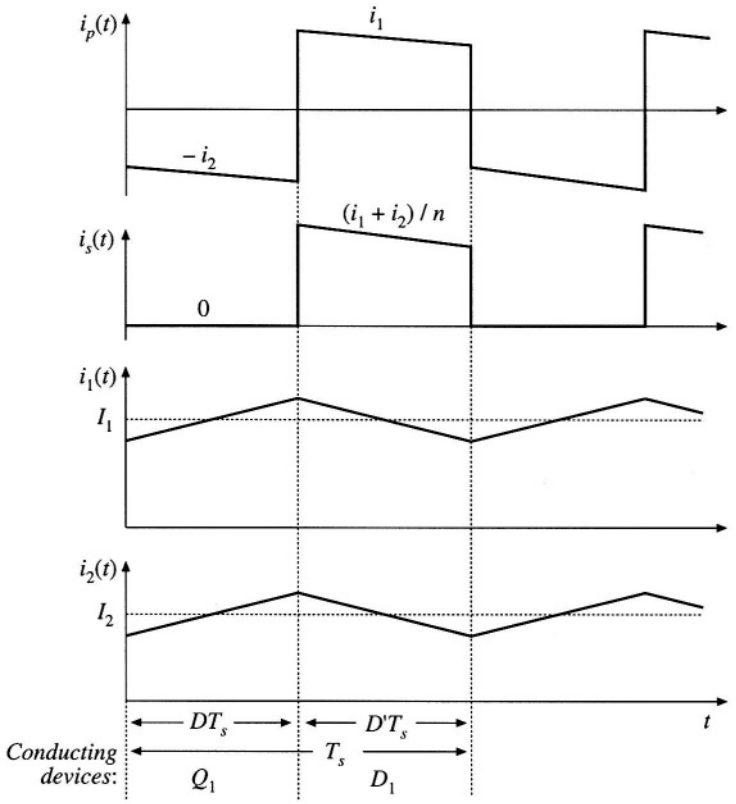

Fig. 6.38 Waveforms of the isolated SEPIC, continuous conduction mode.

netizing inductance performs the energy-storage function of the original inductor L_2. In addition, the ideal transformer provides isolation and a turns ratio.

Typical primary and secondary winding current waveforms $i_p(t)$ and $i_s(t)$ are portrayed in Fig. 6.38, for the continuous conduction mode. The magnetic device must function as both a flyback transformer and also a conventional two-winding transformer. During subinterval 1, while transistor Q_1 conducts, the magnetizing current flows through the primary winding, and the secondary winding current is zero. During subinterval 2, while diode D_1 conducts, the magnetizing current flows through the secondary winding to the load. In addition, the input inductor current i_1 flows through the primary winding. This induces an additional component of secondary current i_1/n, which also flows to the load. So design of the SEPIC transformer is somewhat unusual, and the rms winding currents are larger than those of the flyback transformer.

By application of the principle of volt-second balance to inductors L_1 and L_M, the conversion ratio can be shown to be

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'} \tag{6.50}$$

Ideally, the transistor must block voltage V_g/D'. In practice, additional voltage is observed due to ringing associated with the transformer leakage inductance.

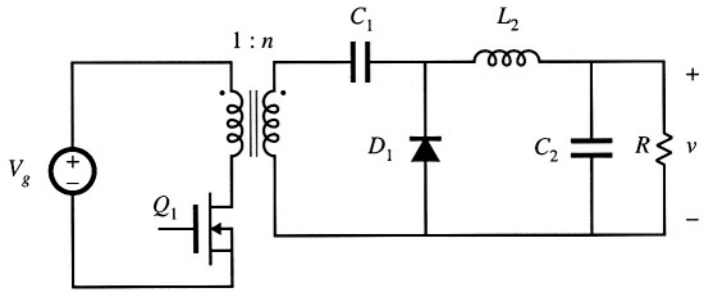

Fig. 6.39 Isolated inverse-SEPIC.

An isolated version of the inverse-SEPIC is shown in Fig. 6.39. Operation and design of the transformer is similar to that of the SEPIC.

Isolation in the Ćuk converter is obtained in a different manner [181. The basic nonisolated Ćuk converter is illustrated in Fig. 6.40(a). In Fig. 6.40(b), capacitor C_1 is split into two series capacitors C_{1a} and C_{1b}. A transformer can now be inserted between these capacitors, as indicated in Fig. 6.40(c). The polarity marks have been reversed, so that a positive output voltage is obtained. Having capacitors in series with the transformer primary and secondary windings ensures that no dc voltage is applied to the transformer. The transformer functions in a conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance.

Utilization of the transformer of the Ćuk converter is quite good. The magnetizing current can

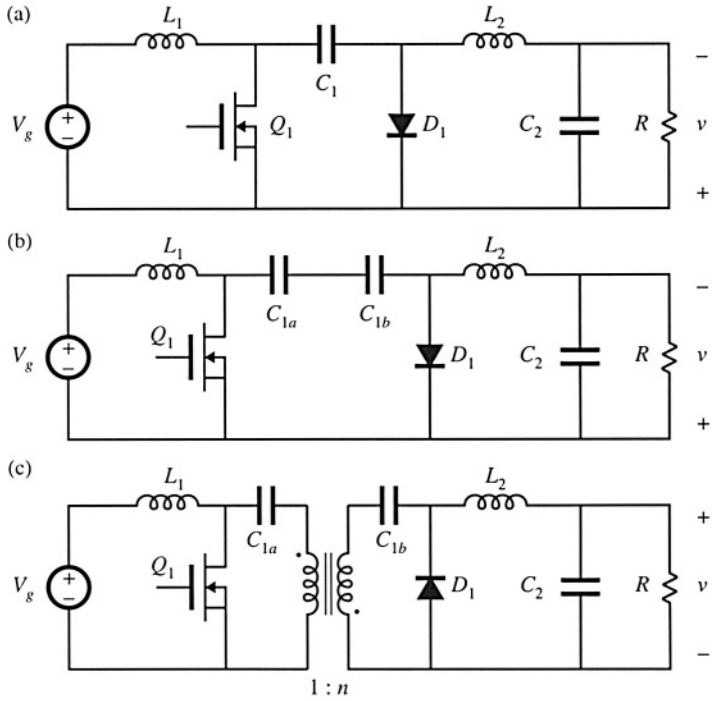

Fig. 6.40 Obtaining isolation in the Ćuk converter: (a) basic nonisolated Ćuk converter, (b) splitting capacitor C_1 into two series capacitors, (c) insertion of transformer between capacitors.

be both positive and negative, and hence the entire core *B–H* loop can be utilized if desired. There are no center-tapped windings, and all of the copper is effectively utilized. The transistor must block voltage V_g/D', plus some additional voltage due to ringing associated with the transformer leakage inductance. The conversion ratio is identical to that of the isolated SEPIC, Eq. (6.50).

The isolated SEPIC and Ćuk converter find application as switching power supplies, typically at power levels of several hundred watts. They are also now finding use as ac–dc low-harmonic rectifiers.

6.4 CONVERTER EVALUATION AND DESIGN

There is no ultimate converter perfectly suited for all possible applications. For a given application, with given specifications, trade studies should be performed to select a converter topology. Several approaches that meet the specifications should be considered, and for each approach important quantities such as worst-case transistor voltage, worst-case transistor rms current, transformer size, etc., should be computed. This type of quantitative comparison can lead to selection of the best approach, while avoiding the personal biases of the engineer.

6.4.1 Switch Stress and Utilization

Often, the largest single cost in a converter is the cost of the active semiconductor devices. Also, the conduction and switching losses associated with the semiconductor devices often dominates the other converter losses. This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices. Minimization of the total switch stresses leads to minimization of the total silicon area required to realize the power devices of the converter.

So it is useful to compare the *total active switch stress* and *active switch utilization* of candidate converter approaches. In a good design, the voltages and currents imposed on the semiconductor devices is minimized, while the load power is maximized. If a converter contains k active semiconductor devices, the total active switch stress S can be defined as

$$S = \sum_{j=1}^{k} V_j I_j \tag{6.51}$$

where V_j is the peak voltage applied to semiconductor switch j, and I_j is the rms current applied to switch j. Peak rather than rms current is sometimes used, with qualitatively similar results. If the converter load power is P_{load}, then the active switch utilization U can be defined as

$$U = \frac{P_{load}}{S} \tag{6.52}$$

The switch utilization is less than one in transformer-isolated converters, and is a quantity to be maximized.

For example, consider the transistor utilization in the CCM flyback converter of Fig. 6.30(d). The peak transistor voltage occurs during subinterval 2, and is equal to the dc input voltage V_g plus the reflected load voltage V/n:

$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'} \tag{6.53}$$

The transistor current waveform coincides with the input current waveform $i_g(t)$, which is sketched in Fig. 6.32. The rms value of this waveform is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}} \tag{6.54}$$

So the total active switch stress is

$$S = V_{Q1,pk} I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right) \tag{6.55}$$

The load power P_{load} can be expressed in terms of V and I by solution of the equivalent circuit model, Fig. 6.33(b). The result is

$$P_{load} = D'V\frac{I}{n} \tag{6.56}$$

Use of Eq. (6.44) to eliminate V_g from Eq. (6.55), and evaluation of Eq. (6.52), leads to

$$U = D'\sqrt{D} \tag{6.57}$$

The transistor utilization U tends to zero at $D = 0$ and at $D = 1$, and reaches a maximum of $U = 0.385$ at $D = 1/3$.

For given values of V_g, V, and the load power, the designer can arbitrarily choose the duty cycle D. The turns ratio is then chosen to satisfy Eq. (6.44), as follows:

$$n = \frac{V}{V_g}\frac{D'}{D} \tag{6.58}$$

At low duty cycle, the transistor rms current becomes large because the transformer turns ratio must be large. At a duty cycle approaching one, the transistor peak voltage is large. So the choice $D = 1/3$ is a good one, which minimizes the product of peak transistor voltage and rms transistor current. In practice, the converter must be optimized to meet a number of different criteria, so a somewhat different duty cycle may be chosen. Also, the converter must usually be designed to operate with some given range of load powers and input voltages; this can lead to a different choice of D, as well as to reduced switch utilization.

For a simple comparison between converters, the switch utilizations of a number of isolated and nonisolated converters are collected in Table 6.1. For simplicity, the formulas assume that the converter is designed to function at a single operating point, that is, with no variations in V_g, V, or P_{load}.

It can be seen that the nonisolated buck and boost converters operate most efficiently when their conversion ratios $M(D)$ are near one. In the case of the boost converter, the switch utilization is greater than one for $D < 0.382$, and approaches infinity as D tends to zero. The reason for this is that, at $D = 0$, the transistor is always off and hence its rms current is zero. But at $D = 0$, $V = V_g$, so the output power is nonzero. All of the load power flows through the diode rather than the transistor. Of course, if it is desired that $V = V_g$, then it would be best to eliminate the boost converter, and directly connect the load to the input voltage. But it is nonetheless true that if the output voltage V is not too much greater than V_g, then a large amount of power can be controlled by a relatively small transistor. Similar arguments apply to the buck converter: all of the load power must flow through the transistor and hence $U \leq 1$, yet converter efficiency and cost per watt are optimized when the output voltage V is not too much smaller than the input voltage.

Table 6.1 Active switch utilizations of some common dc–dc converters, single operating point

Converter	$U(D)$	max $U(D)$	max $U(D)$ occurs at $D =$
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck–boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Ćuk, isolated Ćuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full–bridge, half–bridge, push–pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full–bridge, push–pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Incorporation of an isolation transformer leads to reduced switch utilization. In general, transformer-isolated buck-derived converters should be designed to operate at as large a duty cycle as other considerations will allow. Even so, the switch utilization is reduced to $U \leq 0.353$, meaning that the switch stress is increased by a factor of approximately 2.8 as compared with the nonisolated buck converter at $D = 1$. On the other hand, the transformer turns ratio can be chosen to match the load voltage to the input voltage and better optimize the converter. For example, in a full-bridge buck-derived converter operating with $V_g = 500$ V and V= 5 V, the turns ratio could be chosen to be nearly 100:1, leading to a duty cycle close to one and switch utilization of approximately 0.35. To obtain a 1 kW output power, the total transistor stress would be 1 kW/0.35 = 2.86 kVA. By comparison, the nonisolated buck converter would operate with a duty cycle of 0.01 and a switch utilization of 0.1. Its total switch stress would be 1 kW/0.1 = 10 kVA; transistors with larger rated currents and lower on-resistances would be needed. Similar arguments apply to the transformer-isolated boost-derived converters: these converters are better optimized when they operate at low duty cycles.

The nonisolated buck-boost, nonisolated SEPIC, nonisolated Ćuk converter, and the isolated SEPIC, flyback, and Ćuk converters have similar switch utilizations. In all of these converters, $U \leq 0.385$, which is approximately the same as in the isolated buck-derived converters. So the nonisolated versions of these converters tend to have lower switch utilizations than the buck or boost converters; however, isolation can be obtained with no additional penalty in switch stress. Switch utilization of a single-operating-point design is maximized when the turns ratio is chosen such that $D = 1/3$.

The cost of the active semiconductor devices of a converter approach can be estimated using the converter switch utilization, as follows:

$$\left(\begin{array}{c}\text{semiconductor cost} \\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost} \\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage} \\ \text{derating} \\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current} \\ \text{derating} \\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter} \\ \text{switch} \\ \text{utilization}\end{array}\right)} \tag{6.59}$$

The semiconductor device cost per rated kVA is equal to the cost of a semiconductor device, divided by

the products of its maximum voltage rating and its maximum rms current capability, expressed in $/kVA. This figure depends on a variety of factors, including the device type, packaging, voltage and power levels, and market volume. A typical U.S. value in 2000 is less than $1 /kVA. Voltage and current derating is required to obtain reliable operation of the semiconductor devices. A typical *design guideline* is that the worst-case peak transistor voltage (including transients, voltage spikes due to ringing, and all other anticipated events) should not exceed 75% of the rated transistor voltage, leading to a voltage derating factor of (0.75). Hence, the cost of the active semiconductor switches in a 2000 isolated dc–dc converter is typically in the range $1 to $10 per kW of output power for medium to high-power applications.

6.4.2 Design Using Computer Spreadsheet

Computer spreadsheets are a useful tool for performing converter trade studies and designs. Given specifications regarding the desired output voltage V, the ranges of the input voltage V_g and the load power P_{load}, the desired output voltage ripple Δv, the switching frequency f_s, etc., various design options can be explored. The transformer turns ratio and the inductor current ripple Δi can be taken as design variables, chosen by the engineer. The range of duty cycle variations and the inductor and capacitor component values can then be computed. Worst-case values of the currents and voltages applied to the various power-stage elements can also be evaluated, as well as the sizes of the magnetic elements. By investigating several choices of the design variables, a good compromise between the worst-case voltage stresses and current stresses can be found.

A short spreadsheet example is given in Table 6.2. The converter operates from a dc voltage derived by rectifying a 230 V ± 20% ac source voltage. The converter dc input voltage V_g is therefore $230\sqrt{2}$ V ± 20%. The load voltage is a regulated 15 V dc, with switching ripple Δv no greater than 0.1 V. The load power can vary over the range 20 W to 200 W. It is desired to operate with a switching frequency of f_s = 100 kHz. These values are entered as specifications, at the top of the spreadsheet. The design of a forward converter, Fig. 6.22, and of a flyback converter, Fig. 6.30(d), to meet these specifications is investigated in the spreadsheet. Continuous conduction mode designs are investigated: the inductor current ripple Δi is chosen small enough that the converter operates in CCM at full load power. Depending on the choice of Δi, the converter may operate in either CCM or DCM at minimum load power.

For the single-transistor forward converter, the turns ratios n_2/n_1 and n_3/n_1, as well as the inductor current ripple Δi, can be taken as design variables. For this example, the reset-winding turns ratio n_2/n_1 is chosen to be one, and hence the duty cycle is limited to $D < 0.5$ as given by Eq. (6.35). The maximum duty cycle is computed first. The output voltage of the forward converter, in continuous conduction mode, is given by Eq. (6.36). Solution for the duty cycle D leads to

$$D = \frac{n_1}{n_3}\frac{V}{V_g} \tag{6.60}$$

The maximum value of D occurs at minimum V_g and at full load, and is given in Table 6.2. The minimum CCM value of D, occurring at maximum V_g, is also listed.

The value of the inductance L is computed next. The magnitude of the inductor current ripple Δi can be computed in a manner similar to that used for the nonisolated buck converter to obtain Eq. (2.15). The result is

$$\Delta i = \frac{D'VT_s}{2L} \tag{6.61}$$

Table 6.2 Spreadsheet design example

Specifications			
Maximum input voltage V_g	390 V		
Minimum input voltage V_g	260 V		
Output voltage V	15 V		
Maximum load power P_{load}	200 W		
Minimum load power P_{load}	20 W		
Switching frequency f_s	100 kHz		
Maximum output ripple Δv	0.1 V		
Forward converter design, CCM		***Flyback converter design, CCM***	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Inductance L	26 μH	Inductance L	19 μH ref to sec
Capacitance C	25 μF	Capacitance C	210 μF
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current	1.13 A	Rms transistor current	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

The worst-case maximum ripple occurs in CCM at minimum duty cycle. Solution for L yields

$$L = \frac{D'VT_s}{2\Delta i} \tag{6.62}$$

This equation is used to select L such that the worst-case ripple is equal to the specified value of Δi. The required value of L is listed in Table 6.2. The required value of C that leads to the specified voltage ripple Δv is also computed, using Eq. (2.60). Since Eq. (2.60) neglects capacitor esr, a larger value of C may be required in practice.

If the converter operates in the discontinuous conduction mode at light load, then the controller must reduce the duty cycle D to maintain the required output voltage V. The conversion ratio $M(D, K)$ of the DCM forward converter can be found analytically, using the method developed in the previous chapter. Alternatively, the nonisolated buck converter solution, Eq. (5.29), can be applied directly if all element values are referred to the transformer secondary side. Hence, the output voltage in DCM is given by

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}} \tag{6.63}$$

with $K = 2L/RT_s$, and $R = V^2/P_{load}$. Solution for the duty cycle D yields

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \tag{6.64}$$

The actual duty cycle is the smaller of Eqs. (6.60) and (6.64). The minimum duty cycle occurs at minimum load power and maximum V_g, and is given in Table 6.2.

Worst-case component stresses can now be evaluated. The peak transistor voltage is given by Eq. (6.37). The rms transistor current is calculated with the help of Appendix 1. With the assumption that the transformer magnetizing current can be neglected, the transistor current is equal to the reflected inductor current $i(t)n_3/n_1$ during subinterval 1, and is equal to zero during subintervals 2 and 3. The rms transistor current is therefore

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{(\Delta i)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I \tag{6.65}$$

where $I = P_{load}/V$. The worst-case value of $I_{Q1\text{-}rms}$ occurs at maximum load power and at maximum duty cycle. Expressions for the worst-case stresses in the diodes and output capacitor, as well as for the flyback converter, are found in a similar manner. Their derivation is left as an exercise for the student.

The designs of Table 6.2 are good ones which illustrate the tradeoffs inherent in selection of an isolated converter topology, although some additional design optimization is possible and is left as a homework problem. Both designs utilize a turns ratio of 8:1. The rms transistor current is 22% higher in the flyback converter. This current could be reduced, at the expense of increased transistor voltage. The flyback converter imposes only 510 V on the transistor. A transistor rated at 800 V or 1000 V could be used, with an adequate voltage derating factor and some margin for voltage ringing due to transformer leakage inductance. The 780 V imposed on the transistor of the forward converter is 53% higher than in the flyback converter. Power MOSFETs with voltage ratings greater than 1000 V are not available in 1997; hence, when voltage ringing due to transformer leakage inductance is accounted for, this design will have an inadequate voltage design margin. This problem could be overcome by changing the reset winding turns ratio n_2/n_1, or by using a two-transistor forward converter. It can be concluded that the transformer reset mechanism of the flyback converter is better than that of the conventional forward converter.

Because of the pulsating nature of the secondary-side currents in the flyback converter, the rms and peak secondary currents are significantly higher than in the forward converter. The flyback converter diode must conduct an rms current that is 47% greater than that of forward converter diode D_3, and 80% greater than the current in forward converter diode D_2. The secondary winding of the flyback transformer must also conduct this current. Furthermore, the output capacitor of the flyback converter must be rated to conduct an rms current of 9.1 A. This capacitor will be much more expensive than its counterpart in the forward converter. It can be concluded that the nonpulsating output current property of the forward converter is superior to the pulsating output current of the flyback. For these reasons, flyback converters and other converters having pulsating output currents are usually avoided when the application calls for a high-current output.

6.5 SUMMARY OF KEY POINTS

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Ćuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.
2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.
3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.
4. In the full–bridge, half–bridge, and push–pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.
5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck–boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.

REFERENCES

[1] S. ĆUK, "Modeling, Analysis, and Design of Switching Converters," Ph.D. thesis, California Institute of Technology, November 1976.

[2] S. ĆUK and R. D. MIDDLEBROOK, "A New Optimum Topology Switching Dc-to-Dc Converter," *IEEE Power Electronics Specialists Conference,* 1977 Record, pp. 160-179, June 1977.

[3] E. LANDSMAN, "A Unifying Derivation of Switching Dc-Dc Converter Topologies," *IEEE Power Electronics Specialists Conference,* 1979 Record, pp. 239-243, June 1979.

[4] R. TYMERSKI and V. VORPERIAN, "Generation, Classification, and Analysis of Switched-Mode Dc-to-Dc Converters by the Use of Converter Cells," *Proceedings International Telecommunications Energy Conference,* pp. 181-195, October 1986.

[5] S. ĆUK and R. ERICKSON, "A Conceptually New High-Frequency Switched-Mode Amplifier Technique Eliminates Current Ripple," *Proceedings Fifth National Solid-State Power Conversion Conference* (Powercon 5), pp. G3.1-G3.22, May 1978.

[6] F. BARZEGAR and S. Ćuk, "A New Switched-Mode Amplifier Produces Clean Three-Phase Power," *Proceedings Ninth International Solid-State Power Conversion Conference* (Powercon 9), pp. E3.1-E3.15, July 1982.

[7] K. D. T. NGO, S. ĆUK, and R. D. MIDDLEBROOK, "A New Flyback Dc-to-Three-Phase Converter with Sinusoidal Outputs," *IEEE Power Electronics Specialists Conference,* 1983 Record, pp. 377-388.

[8] R. W. ERICKSON, "Synthesis of Switched-Mode Converters," *IEEE Power Electronics Specialists Conference,* 1983 Record, pp. 9-22, June 1983.

[9] D. MAKSIMOVIĆ and S. ĆUK, "General Properties and Synthesis of PWM Dc-Dc Converters," *IEEE Power Electronics Specialists Conference,* 1989 Record, pp. 515-525, June 1989.

[10] M. S. MAKOWSKI, "On Topological Assumptions on PWM Converters—A Reexamination," *IEEE Power Electronics Specialists Conference,* 1993 Record, pp. 141-147, June 1993.

[11] B. ISRAELSEN, J. MARTIN, C. REEVE, and V. SCOWN, "A 2.5 kV High Reliability TWT Power Supply: Design Techniques for High Efficiency and Low Ripple," *IEEE Power Electronics Specialists Conference,* 1977 Record, pp. 109-130, June 1977.

[12] R. SEVERNS, "A New Current-Fed Converter Topology," *IEEE Power Electronics Specialists Conference,* 1979 Record, pp. 277-283, June 1979.

[13] V. J. THOTTUVELIL, T. G. WILSON, and H. A. OWEN, "Analysis and Design of a Push-Pull Current-Fed *Converter*," *IEEE Power Electronics Specialists Conference,* 1981 Record, pp. 192-203, June 1981.

[14] R. REDL AND N. SOKAL, "Push–Pull Current-Fed Multiple-Output Dc–Dc Power Converter with Only One Inductor and with 0–100% Switch Duty Ratio," *IEEE Power Electronics Specialists Conference,* 1980 Record, pp. 341-345, June 1982.

[15] P. W. CLARKE, "Converter Regulation by Controlled Conduction Overlap," U. S. Patent 3,938,024, February 10, 1976.

[16] R. P. MASSEY and E. C. SNYDER, "High-Voltage Single-Ended Dc-Dc Converter," *IEEE Power Electronics Specialists Conference,* 1977 Record, pp. 156-159, June 1977.

[17] D. MAKSIMOVIĆ and S. ĆUK, "Switching Converters with Wide DC Conversion Range," *IEEE Transactions on Power Electronics,* Vol. 6, No. 1, pp. 151-157, January 1991.

[18] R. D. MIDDLEBROOK and S. ĆUK, "Isolation and Multiple Outputs of a New Optimum Topology Switching Dc-to-Dc Converter," *IEEE Power Electronics Specialists Conference,* 1978 Record, pp. 256-264, June 13-15, 1978.

[19] T. G. WILSON, "Cross Regulation in an Energy-Storage Dc-to-Dc Converter with Two Regulated Outputs," *IEEE Power Electronics Specialists Conference,* 1977 Record, pp. 190-199, June 1977.

[20] H. MATSUO, "Comparison of Multiple-Output Dc-Dc Converters Using Cross Regulation," *IEEE Power Electronics Specialists Conference,* 1979 Record, pp. 169-185, June 1979.

[21] K. HARADA, T. NABESHIMA, and K. HISANAGA, "State-Space Analysis of the Cross-Regulation," *IEEE Power Electronics Specialists Conference,* 1979 Record, pp. 186-192, June 1979.

[22] J. N. PARK and T. R. ZALOUM, "A Dual Mode Forward/Flyback Converter," *IEEE Power Electronics Specialists Conference,* 1982 Record, pp. 3-13, June 1982.

[23] S. ĆUK, "General Topological Properties of Switching Structures," *IEEE Power Electronics Specialists Conference,* 1979 Record, pp. 109-130, June 1979.

[24] R. SEVERNS and G. BLOOM, *Modern Dc–to–Dc Switchmode Power Converter Circuits,* New York: Van Nostrand Reinhold, 1985.

[25] N. MOHAN, T. UNDELAND, and W. ROBBINS, *Power Electronics: Converters, Applications, and Design,* 2nd edit., New York: John Wiley & Sons, 1995.

[26] J. KASSAKIAN, M. SCHLECHT, and G. VERGHESE, *Principles of Power Electronics,* Reading, MA: Addison-Wesley, 1991.

[27] D. MITCHELL, *Dc–Dc Switching Regulator Analysis,* New York: McGraw-Hill, 1988.

[28] K. KIT SUM, *Switch Mode Power Conversion: Basic Theory and Design,* New York: Marcel Dekker, 1984.

[29] R. E. TARTER, *Solid-State Power Conversion Handbook,* New York: John Wiley & Sons, 1993.

[30] Q. CHEN, F. C. LEE, and M. M. JOVANOVIĆ, "DC Analysis and Design of Multiple-Output Forward Converters with Weighted Voltage-Mode Control," *IEEE Applied Power Electronics Conference,* 1993 Record, pp. 449-455, March 1993.

PROBLEMS

6.1 Tapped-inductor boost converter. The boost converter is sometimes modified as illustrated in Fig. 6.41, to obtain a larger conversion ratio than would otherwise occur. The inductor winding contains a total of $(n_1 + n_2)$ turns. The transistor is connected to a tap placed n_1 turns from the left side of the inductor, as shown. The tapped inductor can be viewed as a two-winding $(n_1 : n_2)$ transformer, in which the two windings are connected in series. The inductance of the entire $(n_1 + n_2)$ turn winding is L.

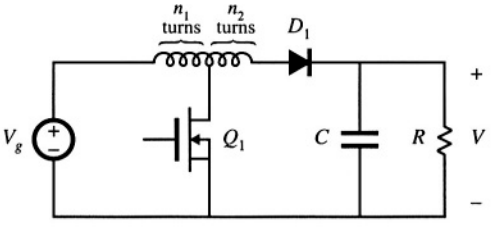

Fig. 6.41 Tapped-inductor boost converter, Problem 6.1

(a) Sketch an equivalent circuit model for the tapped inductor, which includes a magnetizing inductance and an ideal transformer. Label the values of the magnetizing inductance and turns ratio.

(b) Determine an analytical expression for the conversion ratio $M = V/V_g$. You may assume that the transistor, diode, tapped inductor, and capacitor are lossless. You may also assume that the converter operates in continuous conduction mode.

(c) Sketch $M(D)$ vs. D for $n_1 = n_2$, and compare to the nontapped $(n_2 = 0)$ case.

6.2 Analysis of the DCM flyback converter. The flyback converter of Fig. 6.30(d) operates in the discontinuous conduction mode.

(a) Model the flyback transformer as a magnetizing inductance in parallel with an ideal transformer,

and sketch the converter circuits during the three subintervals.

(b) Derive the conditions for operation in discontinuous conduction mode.

(c) Solve the converter: derive expressions for the steady-state output voltage V and subinterval 2 (diode conduction interval) duty cycle D_2.

6.3 Analysis of the isolated inverse–SEPIC of Fig. 6.39. You may assume that the converter operates in the continuous conduction mode, and that all inductor current ripples and capacitor voltage ripples are small.

(a) Derive expressions for the dc components of the magnetizing current, inductor current, and capacitor voltages.

(b) Derive analytical expressions for the rms values of the primary and secondary winding currents. Note that these quantities do not simply scale by the turns ratio.

6.4 The two–transistor flyback converter. The converter of Fig. 6.42 is sometimes used when the dc input voltage is high. Transistors Q_1 and Q_2 are driven with the same gating signal, such that they turn on and off simultaneously with the same duty cycle D. Diodes D_1 and D_2 ensure that the off state voltages of the transistors do not exceed V_g. The converter operates in discontinuous conduction mode. The magnetizing inductance, referred to the primary side, is L_M.

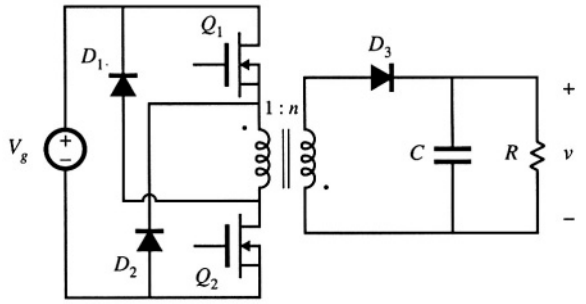

Fig. 6.42 Two-transistor flyback converter, Problem 6.4.

(a) Determine an analytical expression for the steady-state output voltage V.

(b) Over what range of duty cycles does the transformer reset properly? Explain.

6.5 A nonideal flyback converter. The flyback converter shown in Fig. 6.30(d) operates in the continuous conduction mode. The MOSFET has on-resistance R_{on}, and the diode has a constant forward voltage drop V_D. The flyback transformer has primary winding resistance R_p and secondary winding resistance R_s.

(a) Derive a complete steady-state equivalent circuit model, which is valid in the continuous conduction mode, and which correctly models the loss elements listed above as well as the converter input and output ports. Sketch your equivalent circuit.

(b) Derive an analytical expression for the converter efficiency.

6.6 A low-voltage computer power supply with synchronous rectification. The trend in digital integrated circuits is towards lower power supply voltages. It is difficult to construct a high-efficiency low-voltage power supply, because the conduction loss arising in the secondary-side diodes becomes very large. The objective of this problem is to estimate how the efficiency of a forward converter varies as the output voltage is reduced, and to investigate the use of synchronous rectifiers.

The forward converter of Fig. 6.22 operates from a dc input of $V_g = 325$ V, and supplies 20 A to its dc load. Consider three cases: (*i*) $V = 5$ V, (*ii*) $V = 3.3$ V, and (*iii*) $V = 1.5$V. For each case, the turns ratio n_3/n_1 is chosen such that the converter produces the required output voltage at a transistor duty cycle of $D = 0.4$. The MOSFET has on-resistance $R_{on} = 5\ \Omega$. The secondary-side schottky diodes have

forward voltage drops of $V_F = 0.5$ V. All other elements can be considered ideal.

(a) Derive an equivalent circuit for the forward converter, which models the semiconductor conduction losses described above.

(b) Solve your model for cases (*i*), (*ii*), and (*iii*) described above. For each case, determine numerical values of the turns ratio n_3/n_1 and for the efficiency η.

(c) The secondary-side Schottky diodes are replaced by MOSFETs operating as synchronous rectifiers. The MOSFETs each have an on-resistance of 4 mΩ. Determine the new numerical values of the turns ratio n_3/n_1 and the efficiency η, forcases (*i*), (*ii*), and (*iii*).

6.7 Rotation of switching cells. A network containing switches and reactive elements has terminals *a, b,* and *c*, as illustrated in Fig. 6.43(a). You are given that the relationship between the terminal voltages is $V_{bc}/V_{ac} = \mu(D)$.

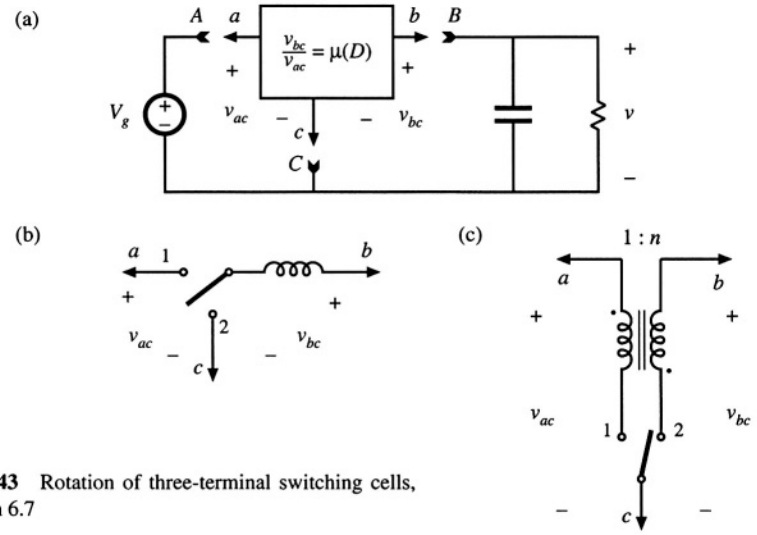

Fig. 6.43 Rotation of three-terminal switching cells, Problem 6.7

(a) Derive expressions for the source-to-load conversion ratio $V/V_g = M(D)$, in terms of $\mu(D)$, for the following three connection schemes:

(i) *a-A b-B c-C*

(*ii*) *a-B b-C c-A*

(*iii*) *a-C b-A c-B*

(b) Consider the three-terminal network of Fig. 6.43(b). Determine $\mu(D)$ for this network. Plug your answer into your results from part (a), to verify that the buck, boost, and buck–boost converters are generated.

(c) Consider the three-terminal network of Fig. 6.43(c). Determine $\mu(D)$ for this network. Plug your answer into your results from part (a). What converters are generated?

6.8 Transformer-isolated current-sense circuit. It is often required that the current flowing in a power transistor be sensed. A noninductive resistor *R* placed in series with the transistor will produce a voltage $v(t)$ that is proportional to the transistor drain current $i_D(t)$. Use of a transformer allows isolation between the power transistor and the control circuit. The transformer turns ratio also allows reduction of the current and power loss and increase of the voltage of the resistor. This problem is concerned with design of the transformer-isolated current-sense circuit of Fig. 6.44.

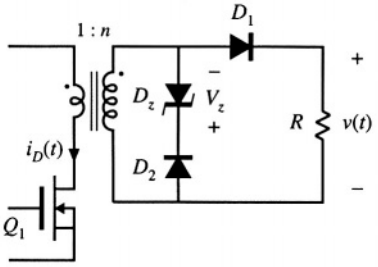

Fig. 6.44 Transformer-isolated circuit for sensing the transistor switch current, Problem 6.8

The transformer has a single-turn primary and an n-turn secondary winding. The transistor switches on and off with duty cycle D and switching frequency f_s. While the transistor conducts, its current is essentially constant and is equal to I. Diodes D_1 and D_2 are conventional silicon diodes having forward voltage drop V_D. Diode D_Z is a zener diode, which can be modeled as a voltage source of value V_Z, with the polarity indicated in the figure. For a proper design, the circuit elements should be chosen such that the transformer magnetizing current, in conjunction with diode D_2, operates in discontinuous conduction mode. In a good design, the magnetizing current is much smaller than the transistor current. Three subintervals occur during each switching period; subinterval 1, in which Q_1 and D_1 conduct; subinterval 2, in which D_2 and D_Z conduct; subinterval 3, in which Q_1, D_1 and D_2 are off.

(a) Sketch the current sense circuit, replacing the transformer and zener diode by their equivalent circuits.

(b) Sketch the waveforms of the transistor current $i_D(t)$, the transformer magnetizing current $i_M(t)$, the primary winding voltage, and the voltage $v(t)$. Label salient features.

(c) Determine the conditions on the zener voltage V_Z that ensure that the transformer magnetizing current is reset to zero before the end of the switching period.

(d) You are given the following specifications:

Switching frequency	$f_s = 100$ kHz
Transistor duty cycle	$D \le 0.75$
Transistor peak current	max $i_D(t) \le 25$ A

The output voltage $v(t)$ should equal 5 V when the transistor current is 25 A. To avoid saturating the transformer core, the volt-seconds applied to the single-turn primary winding while the transistor conducts should be no greater than 2 volt-μsec. The silicon diode forward voltage drops are $V_D = 0.7$ V.

Design the circuit: select values of R, n, and V_Z.

6.9 Optimal reset of the forward converter transformer. As illustrated in Fig. 6.45, it is possible to reset the transformer of the forward converter using a voltage source other than the dc input V_g; several such schemes appear in the literature. By optimally choosing the value of the reset voltage V_r, the peak voltage stresses imposed on transistor Q_1 and diode D_2 can be reduced. The maximum duty cycle can also be increased, leading to a lower transformer turns ratio and lower transistor current. The resulting improvement in converter cost and efficiency can be significant when the dc input voltage varies over a wide range.

(a) As a function of V_g, the transistor duty cycle D, and the transformer turns ratios, what is the minimum value of V_r that causes the transformer magnetizing current to be reset to zero by the end of the switching period?

(b) For your choice of V_r from part (a), what is the peak voltage imposed on transistor Q_1?

This converter is to be used in a universal-input off-line application, with the following specifications. The input voltage V_g can vary between 127 and 380 V. The load voltage is regulated by variation of the

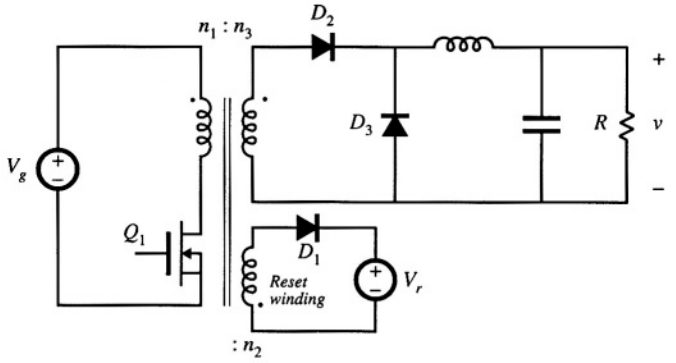

Fig. 6.45 Forward converter with auxiliary reset winding, Problem 6.9

duty cycle, and is equal to 12 V. The load power is 480 W.

(c) Choose the turns ratio n_3/n_1 such that the total active switch stress is minimized. For your choice of n_3/n_1, over what range will the duty cycle vary? What is the peak transistor current?

(d) Compare your design of Part (c) with the conventional scheme in which $n_1 = n_2$ and $V_r = V_g$. Compare the worst-case peak transistor voltage and peak transistor current.

(e) Suggest a way to implement the voltage source V_r. Give a schematic of the power-stage components of your implementation. Use a few sentences to describe the control-circuit functions required by your implementation, if any.

6.10 Design of a multiple-output dc-dc flyback converter. For this problem, you may neglect all losses and transformer leakage inductances. It is desired that the three-output flyback converter shown in Fig. 6.46 operates in the discontinuous conduction mode, with a switching frequency of $f_s = 100$ kHz. The nominal operating conditions are given in the diagram, and you may that there are no variations in the input voltage or the load currents. Select $D_3 = 0.1$ (the duty cycle of subinterval 3, in which all semiconductors are off). The objective of this problem is to find a good steady-state design, in which the semiconductor peak blocking voltages and peak currents are reasonably low.

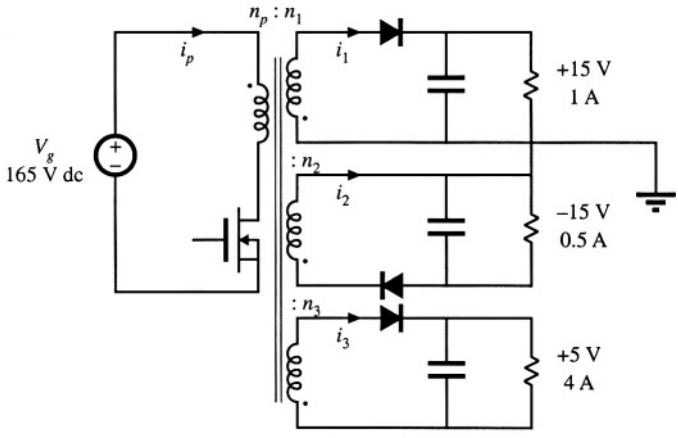

Fig. 6.46 Three-output flyback converter design, Problem 6.10.

(a) It is possible to find a design in which the transistor peak blocking voltage is less than 300 V, and the peak diode blocking voltages are all less than 35 V, under steady-state conditions. Design the converter such that this is true. Specify: (*i*) the transistor duty cycle *D,* (*ii*) the magnetizing inductance L_M, referred to the primary, (*iii*) the turns ratios n_1/n_p and n_3/n_p.

(b) For your design of part (a), determine the rms currents of the four windings. Note that they don't simply scale by the turns ratios.

6.11 Spreadsheet design.

(a) Develop the analytical expressions for the "Results" and "Worst-case stresses" of the forward converter spreadsheet design example of Table 6.2.

(b) Enter the formulas you developed in part (a) into a computer spreadsheet, and verify that your computed values agree with those of Table 6.2.

(c) It is desired to reduce the forward converter peak transistor voltage to a value no greater than 650 V. Modify the design numbers to accomplish this, and briefly discuss the effect on the other component stresses.

(d) For these specifications, what is the largest possible value of the transistor utilization of the CCM forward converter? How should the spreadsheet design variables be chosen to attain the maximum transistor utilization?

6.12 Spreadsheet design of an isolated Ćuk converter. The isolated Ćuk converter of Fig. 6.40(c) is to be designed to meet the specifications listed in Table 6.2. The converter is to be designed such that it operates in continuous conduction mode at full load.

(a) Develop analytical expressions for the following quantities:

- The maximum and minimum duty cycles, for CCM operation
- The peak voltages and rms currents of both semiconductor devices
- The ripple magnitudes of the capacitor voltages and inductor currents
- The rms capacitor currents
- The transistor utilization *U*

(b) Enter the formulas you developed in part (a) into a computer spreadsheet. What are the design variables?

(c) For the specifications listed in Table 6.2, select the design variables to attain what you believe is the best design. Compare the performance of your design with the flyback and forward converter designs of Table 6.2.