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Modeling, Design and Control of a Solar Array Simulator Based on Two-Stage Converters

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Abstract Power inverters for photovoltaic (PV) applications must be tested according to standards in order to be certified and commercialized. A common practice to test PV inverters is the utilization of solar array simulators (SAS). This paper presents a SAS topology based on a double-stage structure: The first stage is based on a three-phase PWM rectifier, and the second stage is based on a bidirectional buck converter. This structure is responsible to emulate the photovoltaic array behavior. A methodology to design the SAS components and control system parameters is presented. This methodology considers a range of operation points of the SAS. Additionally, it is verified that the dc-link capacitance of the inverter under test can affect the SAS dynamic behavior and its output current ripple. The results are divided into two parts: resistive loads and commercial inverters. Firstly, the SAS steady-state operation following the solar array I–V curve is demonstrated through simulation and experimental results, using resistive loads. In the second part, two commercial inverters with different nominal power and dc-link capacitance are considered. Using the proposed design methodology, the SAS topology operates correctly and the maximum power point tracker of the inverter under test is not affected if its input capacitance is within the design limits.

Keywords Solar array simulator · Certification of photovoltaic inverters · Dc/dc converter control

1 Introduction

Grid-connected photovoltaic (PV) systems have grown considerably in recent years. The fundamental element of grid-connected PV system is the inverter, which injects the generated power into the electrical grid. Power inverters for PV applications must be tested and certified according to the present standards, before being commercialized (Camino-Villacorta et al. 2012).

Nowadays, the test and certification of inverters for photovoltaic applications are based on international standards. The use of photovoltaic arrays in the test is a methodology few flexible, since the weather conditions are not controlled and the array needs to be reconfigured in order to test inverters with different rated power. In view of this problem, IEC 61683 suggests the use of a device known as solar array simulator (SAS) in the certification tests. This device is a power source which reproduces I–V (current–voltage) characteristics similar to a PV array (IEC 1999). SAS can emulate the solar array behavior for a set of weather conditions (irradiance and temperature variations) and partial shadowing. Furthermore, this device can operate with different power levels and can be used to test inverters with different rated power.

Most commercial inverters control the solar array output voltage in order to track the maximum power point (Piazza et al. 2010). Therefore, the SAS output voltage is controlled

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by the inverter under test. Since the purpose of the SAS is to reproduce the I–V characteristic of a solar array, its output current must be controlled.

Several SAS topologies for low-power applications are presented in the literature. For example, in Mukerjee and Dasgupta (2007) is proposed a low-cost option to a SAS based on a variable dc power supply. However, this topology uses a series resistor that increases the system losses. In Nagayoshi (2004) is proposed a magnifier circuit applied to a pn photosensor that obtains characteristics of a solar array. Finally, in Gadelovits et al. (2014) is proposed an adaptation in a commercial dc power supply in order to build a SAS. Basically, the output current is sensed, processed by a microcontroller which defines the dc power supply voltage reference.

Generally, the SAS topologies present two stages: a rectifier stage based on diodes and a dc/dc converter. The dc/dc buck converter is the most employed in the literature (Ollila 1995; Matsukawa et al. 2003; Gonzalez et al. 2010; Bun et al. 2011; Piao et al. 2013; Piazza et al. 2010; Koran et al. 2010). A low-cost SAS based on buck converter is proposed in Vijayakumari et al. (2012). However, the converter design considers only the nominal operation point of the converter and the experimental results considered only resistive loads connected to the SAS output.

Other converter topologies are proposed by Chang et al. (2013); Jike and Shengtie (2012); Koran et al. (2014). For example, a LLC-resonant dc–dc converter-based SAS is presented in Chang et al. (2013). The experimental results for a commercial inverter were also presented. The main drawback of this structure is the complexity of the converter topology. Furthermore, even with a complex design methodology, it considers only the operation at the nominal operation point, as detailed in Chang et al. (2014).

Koran et al. (2014) proposes a SAS based on a three-phase ac–dc dual boost rectifier cascaded with a three-phase dc–dc interleaved buck converter. The experimental results for resistive loads and for a commercial inverter are presented. Again, the converter topology is complex and its design considered only the nominal operation point.

In Sanchis et al. (2005) is proposed a SAS with two control modes: Firstly, the SAS measures the real evolution of the I–V characteristic curves of solar array and physically emulates in real time these curves to test photovoltaic inverters. The structure is based on a bidirectional converter. Tests for this topology considering commercial inverters were presented later in Sanchis et al. (2007). However, no details about the SAS start-up and design are discussed.

In fact, rectifiers based on diodes have grid current with higher harmonic distortion and their output voltage is not controllable. Therefore, the maximum SAS output voltage is limited to the peak of the line voltage. Furthermore, the traditional dc/dc buck converter is difficult to be controlled

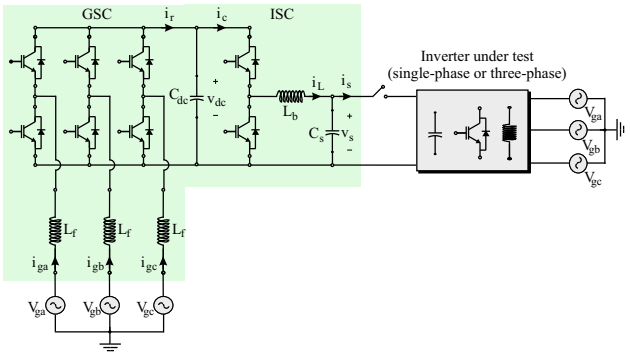


Fig. 1 Proposed structure of solar array simulator

when unloaded. Therefore, the solar array open-circuit point is not emulated if this converter topology is employed (Jike and Shengtie 2012). These drawbacks of the traditional SAS structure are barely related in the literature.

Most works in the literature design the dc/dc power stage considering only the nominal operation point. This approach is widely used for applications in which the converter works with a constant output voltage (Robert and Maksimovic 2004; Mohan et al. 2002). However, due to variations in the operation point on the solar array curve, the converter design needs to include an analysis in other operation points.

Based on the mentioned limitations, an improved SAS structure is presented in Cupertino et al. (2015a, b), which is used in this work. The proposed topology is shown in Fig. 1 and consists of two stages: The first one is based on a PWM voltage source rectifier, and the second consists of a bidirectional converter. These stages are referred in this work as GSC (grid side converter) and ISC (inverter side converter), respectively.

The GSC guarantees high power factor in the grid and currents with low harmonic distortion. This converter controls the first-stage dc-link voltage. Furthermore, the GSC can increase the dc-link, if necessary, which results in a SAS able to test commercial inverters with a wide range of input voltage.

The ISC allows a stable operation at the open-circuit point due to its bidirectional characteristic. The open-circuit voltage control is important because most commercial inverters start their operation when open-circuit voltage reaches a minimum value. Therefore, the possibility of controlling the open-circuit voltage is interesting for the system start-up and for evaluating the voltage threshold of the commercial inverter under test.

The main contributions of this paper are given as:

1. *Flexible structure* the proposed topology is able to emulate many levels of solar irradiance and temperature. Furthermore, the double-stage structure permits emulating solar arrays with different output voltage levels;

2. The dc/dc stage is bidirectional and allows the proposed SAS control even if the SAS is unloaded;
3. The design of dc/dc stage considers the full operation area of the solar array;
4. Analysis of the SAS output current ripple as function of the dc-link capacitance of the inverter under test.

The present work is organized as follows. The modeling and control for both GSC and ISC are detailed in Sect. 2. The design of ISC components and the effect of dc-link capacitance of the inverter under test are also analyzed in this section. Simulation results are presented in Sect. 3 in order to demonstrate the dynamic behavior of the proposed SAS topology. Experimental results with resistive loads and two commercial inverters of 3,1 and 1,5 kW are addressed in Sect. 4. Finally, conclusions are stated in Sect. 5.

2 Modeling of the Solar Array Simulator

2.1 Ac/Dc Stage

The SAS rectifier stage is based on a three-phase PWM converter. An inductive filter interfaces the SAS with the ac-grid in order to reduce the harmonic content generated by the IGBTs switching. The design of this filter is presented in Ponnaluri et al. (2000).

It was employed the classical control structure based on proportional-integral controllers in synchronous reference frame (dq). This strategy consists in two cascade loops: internal loops controlling the direct and quadrature components of grid currents and the external loops regulating the dc-link voltage and the reactive power injected into the grid (Liserre et al. 2005). The control structure of the PWM rectifier is presented in Fig. 2a.

The synchronization of the converter with the grid voltage is based on a decoupled double synchronous reference frame phase-locked loop (DDSRF-PLL), proposed by Rodriguez et al. (2007). This PLL performs well during voltage unbalances and voltage harmonics.

The modulation strategy implemented is the space vector PWM (SVPWM) technique. The control digital implementation uses a sample time equals twice the switching frequency. The gains are adjusted according to the procedures described in Suul et al. (2008). The parameters of the PWM rectifier are presented in Table 1.

The controllers gains used in the simulation and experimental setup are presented in Table 2.

2.2 Dc/Dc Stage

The dc/dc stage has two operational modes:

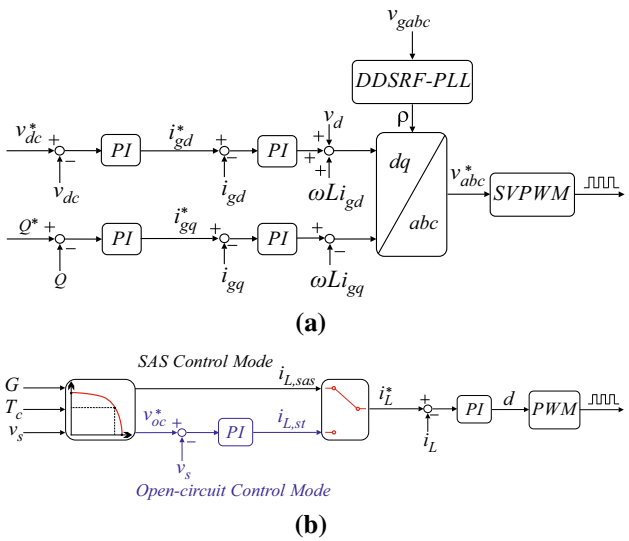


Fig. 2 SAS control structures: **a** complete control structure of PWM rectifier; **b** complete control structure of dc/dc converter

Table 1 Ac/dc stage parameters

Parameter	Symbol	Value
Maximum power	P_{max}	10 kW
Grid voltage	V_g	220 V
Grid frequency	f_n	60 Hz
Dc-link Voltage	V_{dc}	450 V
Switching frequency	f_s	6 kHz
Filter inductance	L_f	4 mH
Filter resistance	R_f	50 $m\Omega$
Dc-link capacitance	C_{dc}	3.06 mF

Table 2 Ac/dc stage controller gains

Parameter	Symbol	Value
Prop. gain of grid current loop	$K_{p,i_{dq}}$	6
Int. gain of grid current loop	$K_{i,i_{dq}}$	75
Prop. gain of dc-link voltage loop	$K_{p,v_{dc}}$	1.4
Int. gain of dc-link voltage loop	$K_{i,v_{dc}}$	32
Prop. gain of reactive power loop	$K_{p,Q}$	0.0004
Int. gain of reactive power loop	$K_{i,Q}$	0.1

– *Open-circuit control mode* It is responsible for starting the converter switching operation and controlling the output voltage when the simulator is unloaded (the inverter under test is not operating). In this operation mode, the voltage output reference is the solar array open-circuit voltage;
– *Solar array simulator control mode* The current reference is obtained based on the I–V characteristic curve. The output voltage is controlled by the inverter under test.

The dc/dc control strategy is shown in Fig. 2b. For each operation mode, a different form to calculate the inductor current reference is employed. In open-circuit control mode, it is used a cascade control loop: The external loop regulates the output voltage to the open-circuit value, and the internal loop regulates the inductor current.

On the other hand, the SAS control mode is based on a look-up table of I–V curves (Piazza et al. (2010)). This method consists in the following steps: Firstly, a table with values of I–V curve is chosen for given values of solar irradiance G and temperature T_c (defined by the user). Then, the output voltage measurement is interpolated in this table. Therefore, for a given value of output voltage, the inductor current reference is calculated following the I–V curve. This interpolation is dynamic and allows the SAS to emulate the behavior of a solar array under different climatic conditions (Matsukawa et al. (2003)). The solar array curves used in the experimental tests result from a series and parallel connection of SM48KSM modules, manufactured by Kyocera.

It is important to highlight that some MPPT algorithms are based on measurements from the solar array short-circuit current (Bhatnagar and Nema 2013). However, it is not necessary to include a new operation mode, since this condition is intrinsically included in the solar array simulator control mode. In fact, when the output voltage is zero (during a short circuit, for example), the SAS output current is controlled to the short-circuit current of the I–V curve. This condition is possible since the dc/dc stage is current controlled.

The following aspects were considered in the dc/dc converter modeling:

- The dc-link voltage of the PWM rectifier is constant;
- Only resistive losses in the inductor are considered;
- The inverter under test is modeled as a resistive load connected to the SAS output.

Therefore, a transfer function which relates inductor current and converter duty cycle is given by Robert and Maksimovic (2004):

$$G_{id}(s) = \frac{(R_s C_s + 1)V_{dc}}{R_s L_b C_s s^2 + (L_b + R_{Lb} R_s C_s)s + (R_s + R_{Lb})}. \tag{1}$$

where $R_s = \frac{v_s^2}{P_s}$ is the equivalent output resistance. This variable represents the power P_s delivered to the inverter under test.

The transfer function that relates the inductor current and the dc-link voltage, considering the SAS unloaded, is given by:

$$G_{vi}(s) = \frac{1}{C_s s}. \tag{2}$$

The current control loop is based on a PI controller, which is also used in the voltage control loop. The digital implementation of the control uses a sample time equals to the switching frequency, and the gains are adjusted according to the procedures described in Robert and Maksimovic (2004). The components design for the dc/dc stage is presented in the following subsection.

2.3 Dc/Dc Stage Design

Due to the variety of types of inverters that can be tested, a SAS generally does not process the rated power. Furthermore, the operation points of the ISC are defined by the I–V curves which will be emulated. Therefore, in order to determine the dc/dc converter inductance and capacitance, it is necessary to analyze not only the current and voltage ripple at rated power, but also its behavior at different operation points on the I–V curves.

For the sake of simplicity, considering the inverter under test as a resistive load connected to the SAS output, the minimum value for the converter inductance $L_{b,min}$ is given by Mohan et al. (2002):

$$L_{b,min} = \frac{v_s(1-d)}{f_{sb}\Delta i_L(\%) i_L} \tag{3}$$

where $\Delta i_L(\%)$ is the maximum admissible current ripple, d is the converter duty cycle, f_s is the switching frequency and i_L is the inductor current.

In order to define the inductance of the converter, it is necessary to evaluate, for a given value of $\Delta i_L(\%)$, the minimum necessary inductance. This value can be obtained by calculating the minimum necessary inductance for all operation points of the converter.

The operation points of the converter are determined by the reference I–V curve. The inductor current, output voltage and duty cycle can be determined for each operation point. In the present case study, the dc/dc stage maximum output current is 32 A and the maximum output voltage is 400 V. The use of a solar array with 18 modules and 11 strings connected in parallel allows obtaining (for 1000 W/m^2 and 25 °C) an open-circuit voltage and short-circuit current close to the converter limits. This equivalent solar array presents a maximum power of 10 kW.

Thus, considering this case study and a constant ripple of 30% (Hauke 2015), the inductance value can be obtained for various levels of solar irradiance, as shown in Fig 3a. As can be observed, when the power processed by the converter decreases, the minimum inductance value increases. Using $L_b = 5$ mH, the ripple remains less then 30% in all operation points above 10% of the rated power (Fig. 3a).

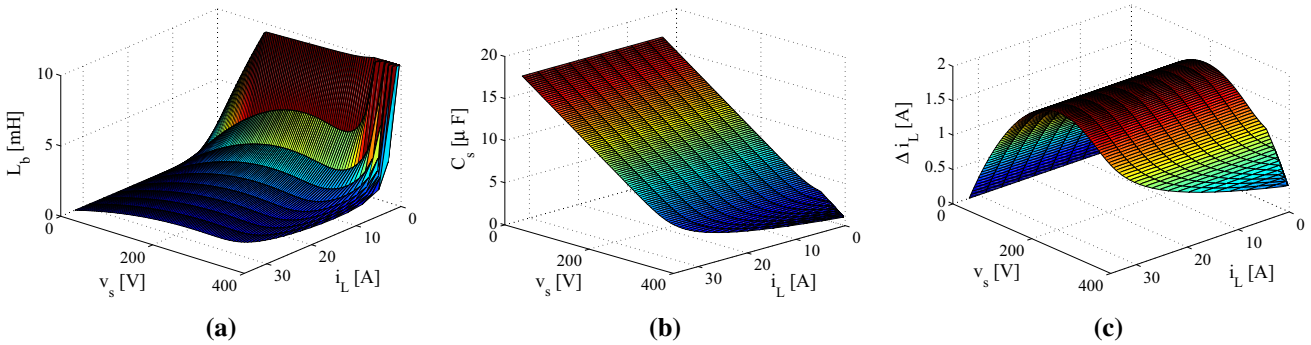


Fig. 3 Specifications of dc/dc converter passive elements: **a** minimum value of dc/dc converter inductance as function of the SAS operation point for 30% of current ripple; **b** minimum value of dc/dc converter capacitance as function of the SAS operation point for 1% of output voltage ripple; **c** inductor current ripple for $L_b = 5$ mH as function of the SAS operation point

The inductance and the voltage ripple needs to be known in order to specify the output capacitor. The minimum output capacitance can be calculated by Mohan et al. (2002):

$$C_{s,min} = \frac{(1-d)}{8 L_b f_{sb}{}^2 \Delta v_s(\%)} \tag{4}$$

where $\Delta v_s(\%)$ is the maximum admissible voltage ripple and v_s is the SAS output voltage.

Using 5 mH for the inductor and 1% of voltage ripple, it is possible to obtain the surface of Fig. 3b. Therefore, the minimum capacitor value is close to $20\,\mu F$.

In order to guarantee a suitable current in the load, the capacitor needs to absorb all inductor current ripple. The value of maximum current ripple can be obtained considering $L_b = 5$ mH in (3), as presented in Fig. 3c. It can be observed that the maximum current ripple is less than 2 A. Therefore, the minimum capacitor current capability is 2 A.

However, the output capacitance value design presents another constraint. When a commercial inverter is connected to the SAS output, the inductor ripple is divided by two capacitances: the SAS output capacitance and the inverter dc-link capacitance. Thus, the model presented in Fig. 4a is considered in the analysis of the output current ripple . The ripple is determined by the current divisor between the SAS output capacitance C_s and the inverter dc-link capacitance C_i. Considering this circuit, it is possible to obtain:

$$K = \frac{I_{s,h}(s)}{I_{L,h}(s)} = \frac{C_i}{C_i + C_s} \tag{5}$$

where K is the ripple relation. $I_{s,h}(s)$ and $I_{L,h}(s)$ are the Laplace's transform of SAS output and inductor currents of harmonic order h, respectively.

By using (5), Fig. 4b shows the relation between the inverter dc-link capacitance in pu (base value is the SAS output capacitance) and ripple relation K. As observed, when the inverter dc-link capacitance increases, the output current

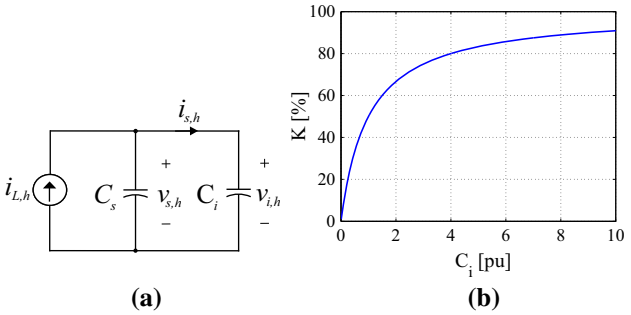


Fig. 4 Effect of the inverter dc-link capacitance: **a** Equivalent model for calculation of steady-state ripple of the SAS output current; **b** effect of inverter dc-link capacitance variation in the SAS output current ripple

ripple also increases. This fact must be considered, since the inverter under test generally measures this variable in order to reach the maximum power point of the solar array. Therefore, high values of output current ripple can affect the performance of the inverter MPPT.

Applying (5), if the SAS output capacitance is 10 times the inverter dc-link capacitance, K is approximately 0.09. Therefore, 9% of inductor current ripple will flow to the inverter. In the present study, the maximum inverter dc-link capacitance is defined 100 μF. In this situation, a SAS output capacitance of 1 mF (10 times higher) is used in this work. It is important to highlight that if larger values of capacitance are employed, the performance in terms of output current ripple is improved. However, the time response and the cost of the SAS will be affected.

Finally, the parameters ISC are presented in Table 3. The controllers gains used in the simulation and experimental setup are presented in Table 4.

2.4 Effect of Parametric Variation in Current Control Performance

In this section, the effect of parametric variation in the dc/dc current control is presented. This analysis is justified by two

Table 3 Dc/dc stage parameters

Parameter	Symbol	Value
Switching frequency	f_{sb}	12 kHz
Inductance	L_b	5 mH
Inductor resistance	R_{L_b}	62.5 $m\Omega$
Capacitance	C_s	1 mF

Table 4 Dc/dc stage controller gains

Parameter	Value	Value
Prop. gain of current loop	K_{p,i_L}	0.03
Int. gain of current loop	K_{i,i_L}	78.3
Prop. gain of voltage loop	K_{p,v_s}	0.18
Int. gain of voltage loop	K_{i,v_s}	2.5

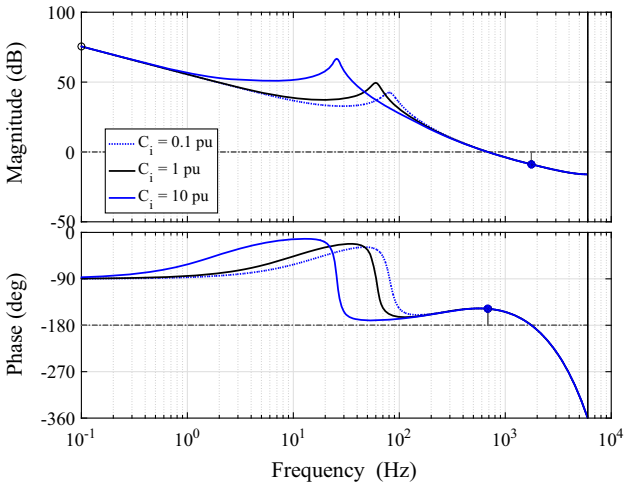
factors. Firstly, when an inverter is connected to the solar array simulator output, the SAS output capacitance C_s and the inverter input capacitance C_i are connected in parallel. Therefore, the equivalent system presents variations in the capacitance value. Furthermore, the current controller is designed considering a determined value of output power (nominal, for example). Thereby, a fixed value for R_s is employed. Nevertheless, the output power is dependent of the inverter under test and variations in this parameter are possible. Therefore, the effect of parametric variations in C_i and R_s needs to be analyzed.

The stability analysis presented in this work is accomplished in discrete-time domain. It considers the following points (Peña-Alzola et al. 2014):

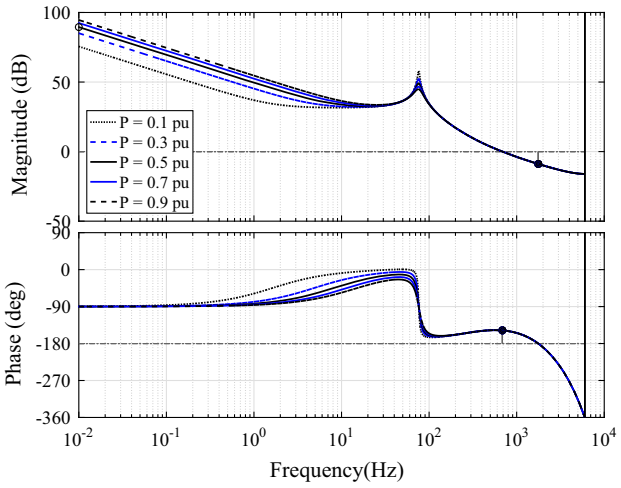
- Zero-order hold, necessary to sample the current signal;
- Delay of one cycle generated by PWM algorithm;
- PI controllers are discretized by trapezoidal method;
- Sampling frequency used is equal to the switching frequency of dc/dc stage.

The effect of the inverter dc-link capacitance C_i is included in (1) replacing the term C_b by $C_b + C_i$. Figure 5a presents the Bode diagrams considering the inverter dc-link capacitance from 0.1 to 10 pu in the SAS output capacitance base. It can be observed that this capacitance influences the resonant frequency of the open-loop transfer function. Nevertheless, this variation increases the closed-loop step response overshoot less than 1%. Furthermore, the phase and gain margins are few affected. For this reason, the dynamic of current control stability is almost unaffected by the inverter dc-link capacitance variation.

The effect of the SAS output power is presented in Fig. 5 (b). The output resistance R_s is calculated considering the a duty cycle of 75%, resulting in an output voltage $v_s = 337.5V$. It can be observed that the resistance influences in the gain at low frequencies and therefore in the steady-state error. However, the variations in the steady-state error are less than 0.5%. Again, the phase and gain margins are slightly affected. Therefore, the controller parameters are considered adequate for this application.



(a)



(b)

Fig. 5 Effect of parametric variation in current control performance: **a** effect of the inverter input capacitance C_i; **b** effect of the output power (equivalent to variations in R_s)

3 Simulation Results

In this section, the simulation results of the proposed SAS structure are presented and analyzed. Simulations were implemented in *Matlab/Simulink* environment. In order to analyze variations of the SAS input and output powers, the solar irradiance and the load are changed according to Fig. 6a.

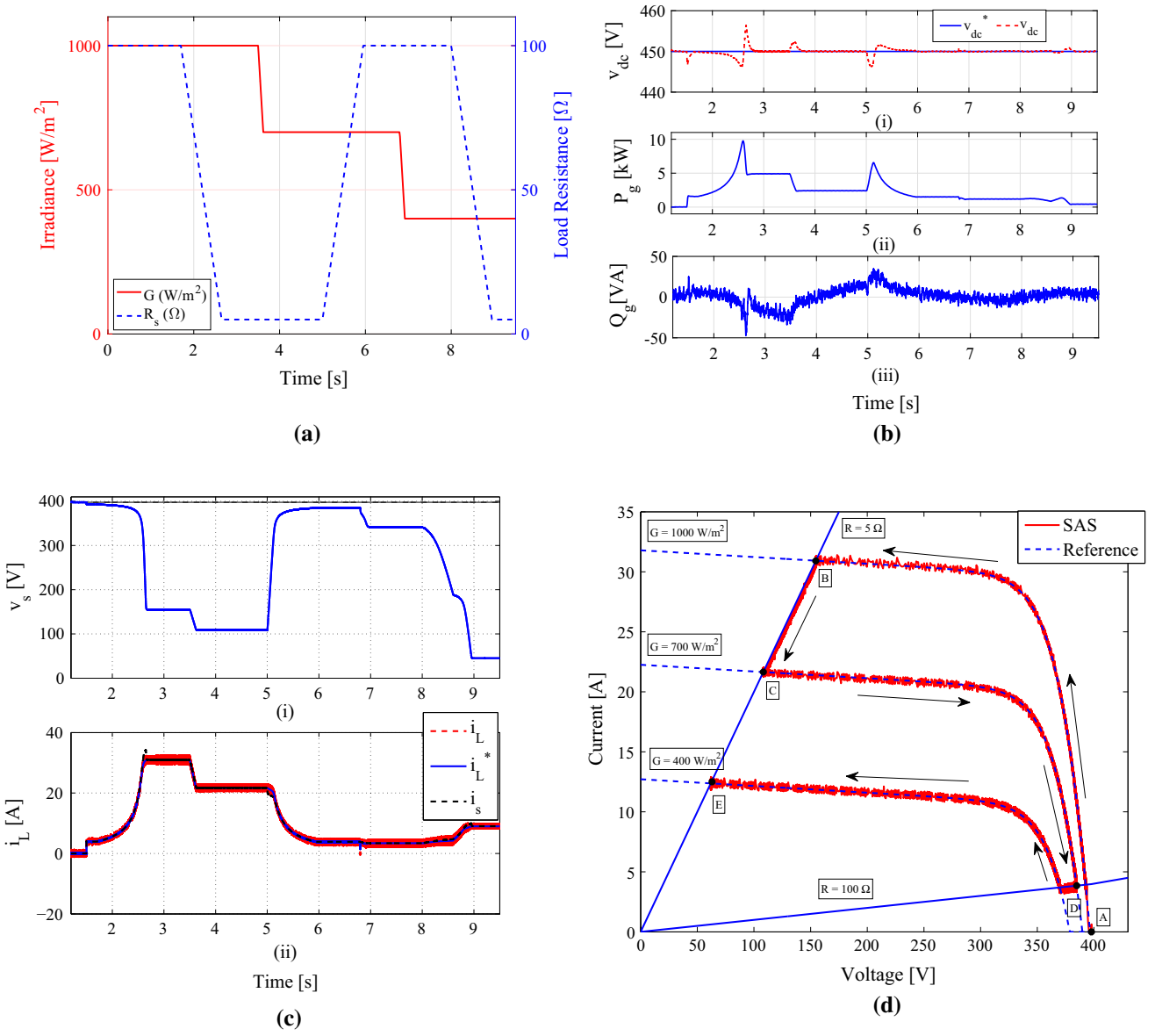


Fig. 6 Simulation results for SAS: **a** simulated solar irradiance and load resistance profiles; **b** dynamic behavior of PWM rectifier during SAS operation with resistive load: *i* dc-link voltage; *ii* Active power supplied by electrical grid; *iii* Reactive power supplied by electrical grid; **c** dynamic behavior of the dc/dc converter during the SAS operation with resistive load: *i* output voltage; *ii* inductor and output currents; **d** SAS paths in I–V plane with resistive load

The operation in various points on the I–V curve is tested using a variable resistance.

Figure 6b presents the GSC dynamic behavior. As observed in Fig. 6b–i, load variations generate disturbances in the rectifier dc-link voltage. Voltage variations are smaller than 2% of the rated value, which results in a well regulated dc-link voltage. Figure 6b-ii presents the grid active power. As observed in Fig. 6b-iii, the reactive power controlled in zero results in a power factor close to unitary.

Figure 6c presents the ISC behavior, showing that the output current i_s follows the reference i_L^*. Load variations results in changes in the operation point. The inductor current i_L presents a ripple, which is filtered by means of the output capacitor. Therefore, the SAS output current presents smaller ripple, but its dynamic behavior changes in terms of overshoot.

Figure 6d presents the SAS path in I–V plane. These paths illustrate the inductor current variation that follows the I–V reference curves. The system starts at point A (open-circuit voltage), changes to point B (load variation with constant irradiance), C (irradiance variation with constant load), D (load variation with constant irradiance) and

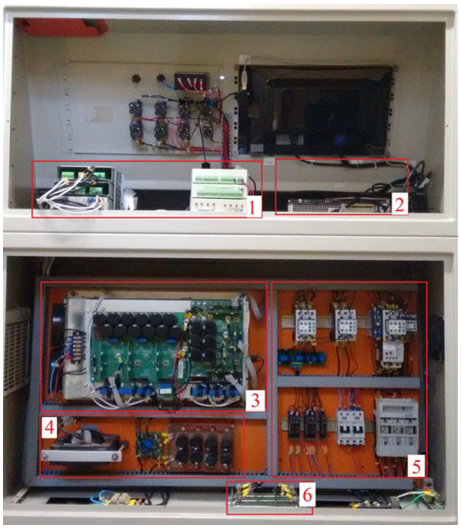


Fig. 7 Implemented test bench: *1* control and signal conditioner boards; *2* computer (monitoring and data acquisition); *3* power modules; *4* LC filter of dc/dc converter; *5* command circuit; *6* Pre-charge resistors

finishes at point E (constant irradiance with load variation).

4 Experimental Results

A test bench was built in order to evaluate the behavior of the proposed topology. All control algorithms were implemented in F28335 floating point DSP from Texas Instruments. The complete view of the prototype and its main components are shown in Fig. 7.

4.1 Start-up and Ac/Dc Control Stage

The start-up of the converter consists in the following steps:

- Connection of GSC to the grid by means of pre-charge resistors. In this step, the dc-link voltage reaches a value close to 310 V;
- Start of GSC switching: the GSC control is enabled and the dc-link voltage reaches the reference (420 V);
- Start of ISC switching: the ISC control is enabled and set to mode 1. Thus, the output voltage reaches the solar array open-circuit voltage;
- After the previous steps, the inverter which will be tested can be connected to the SAS output and the control strategy is switched to mode 2. In this situation, the ISC will follow the solar array characteristics defined by the user.

As observed in Fig. 8a, at the time 6.2 s, the GSC dc-link voltage follows the reference without significant transients.

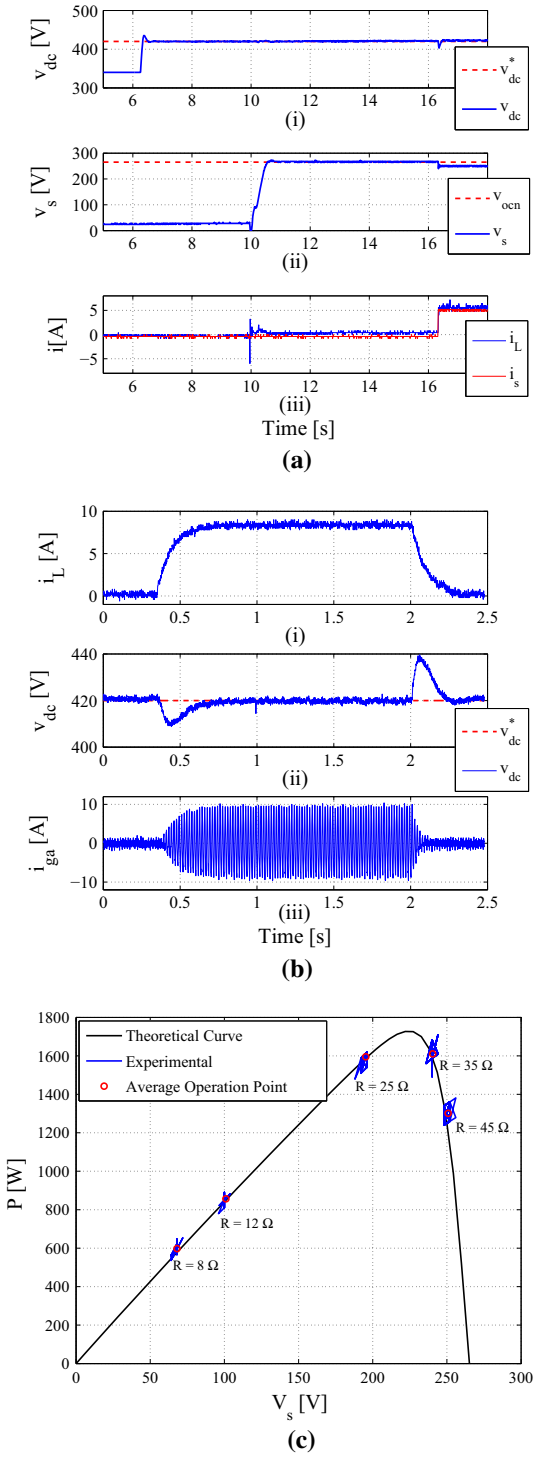


Fig. 8 Experimental results for the proposed SAS topology: **a** experimental result of the system start-up: *i* GSC dc-link voltage; *ii* SAS output voltage; *iii* SAS inductor and output currents; **b** experimental result of the GSC control strategy: *i* ISC inductor current (disturbance); *ii* GSC dc-link voltage; *iii* phase A grid current; **c** steady-state operation points of SAS with resistive load

At the time 10 s, the ISC control is enabled and the SAS output voltage reaches the open-circuit voltage value. An average value of inductor current close to 0.3 A is necessary

to maintain the capacitor charged. The output current is zero because no load is connected before the start-up.

Finally, in order to verify the SAS dynamic behavior during the change of ISC control mode, at the time 16.2 s a resistive load of 50 ohms is connected to the ISC output and the control strategy is switched to mode 2. In this situation, the ISC follows the reference solar array characteristic curve. No significant transient is observed during the change in the ISC control mode.

The GSC dynamic behavior is evaluated by means of load disturbances. The results for load disturbance are presented in Fig. 8b considering again a resistive load connected to the SAS output. The ISC inductor current behavior is shown in Fig. 8b–i. The dc-link voltage can follow the reference with a transient response close to 250 ms, as shown in Fig. 8b-ii. Finally, the load insertion increases the grid current, as shown in Fig. 8b-iii. Considering this operation point, the efficiency obtained is 87.8%.

4.2 Operation with Resistive Load

A test widely presented in the literature involves the connection of resistive loads at the SAS output in order to evaluate whether the device is able to represent the solar array operation points. This test is useful to assessing the steady-state operation points, but the dynamic behavior of the inverter under test cannot be represented.

The results obtained by using resistive loads are shown in Fig. 8c. The oscillations observed in the measured data are justified by the SAS output current ripple. The average operation points in steady state are under the theoretical curve. Furthermore, the SAS is able to operate in points below and above the maximum power point as expected.

4.3 Operation with PV Inverter

Two tests are conducted in this section with two commercial PV inverters connected to the proposed SAS. The main parameters of the inverters are presented in Table 5. The first inverter has a dc-link capacitance of 5 mF, while the second has a dc-link capacitance of $100\,\mu F$. These results show the effect of an inverter with high dc-link capacitance connected in the SAS output, increasing the current ripple.

Table 5 Main parameters of commercial inverters

Parameter	Inverter 1	Inverter 2
P_{max}	3.1 kW	1.6 kW
V_g	220 V	220 V
$V_{dc,max}$	650 V	500 V
C_i	5 mF	0.1 mF

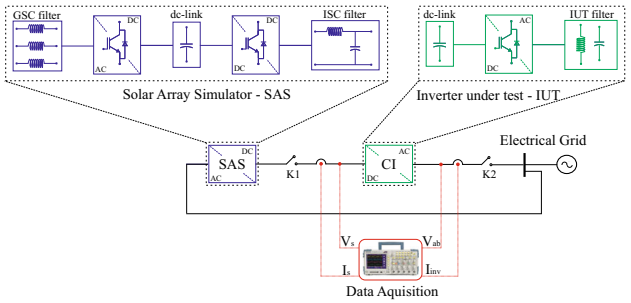


Fig. 9 Experimental setup for performance evaluation of the proposed SAS topology connected to commercial inverters

This setup was implemented according to Fig. 9. The commercial inverter ac circuit is connected to the grid by means of contactor $K2$, while the dc circuit is connected to the SAS output by means of the contactor $K1$. In this setup, the power supplied by the electrical grid refers only to the losses in the SAS and in the commercial inverter.

It was considered a solar array with 309 V of open-circuit voltage and 2.7 kW in the tests conducted with the inverter 1. The waveforms obtained in steady state for $1000\,W/m^2$ are presented in Fig. 10a. Figure 10a–i shows the voltage and current at the output of the inverter 1. These waveforms are shifted by 180 degrees, which indicates the injection of active power. The SAS output voltage and output current are presented in Fig. 10a-ii and a-iii, respectively. The SAS output current presents a high ripple, which reaches 5 A. Furthermore, the current injected by the inverter under test is highly distorted. The current THD for inverter 1 is 10.93%, which is not in accordance with the distortion informed by the manufacturer ($\leq$5%).

For the tests conducted with the inverter 2, it was programmed a solar array with 245 V of open-circuit voltage and 1.55 kW. Figure 10b–i shows the grid voltage and current for the test of inverter 2 . The SAS output voltage and current are presented in Fig.10b-ii and b-iii, respectively. A low distortion level is observed in the current waveform. The current THD for inverter 2 is 3.67%, which is in accordance with the values informed by the manufacturer ($\leq$5%).

The harmonic spectra of the output current for inverter 1 and 2 are presented in Fig. 11. The distortion in the grid current for the first inverter can be justified by the interaction between its dc-link capacitance and the SAS output capacitance. In fact, the capacitance of inverter 1 is out the range considered in the SAS design. Therefore, a high ripple is observed in the SAS output current. Consequently, this ripple generates oscillations in the inverter control system, thus affecting the inverter output current (low-order harmonics are injected into the grid). For the second inverter tested, the dc-link capacitance is in accordance with the design constraints proposed in this work, since the inverter 2 dc-link capaci-

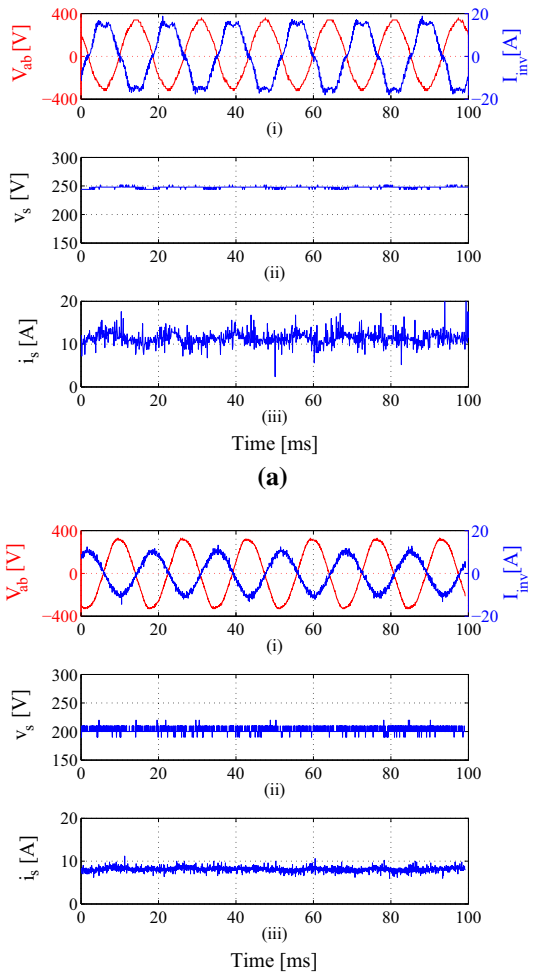


Fig. 10 Experimental results in steady state for both inverters: **a** steady-state waveforms of the proposed SAS operating with the inverter 1 for an irradiance level equal to 1000 W/m^2: *i* grid voltage and injected current; *ii* SAS output voltage; *iii* SAS output current; **b** steady-state waveforms of the proposed SAS operating with the inverter 2 for an irradiance level equal to 1000 W/m^2: *i* grid voltage and injected current; *ii* SAS output voltage; *iii* SAS output current

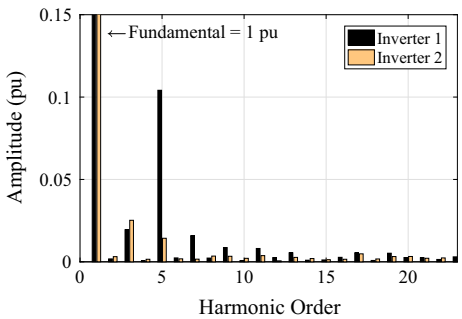


Fig. 11 Current harmonic spectra for the current at the inverters output

tance is 10 times smaller than the SAS output capacitance. Thereby, according to equation (5), more than 90% of the current ripple will flow through the capacitor C_s and a small

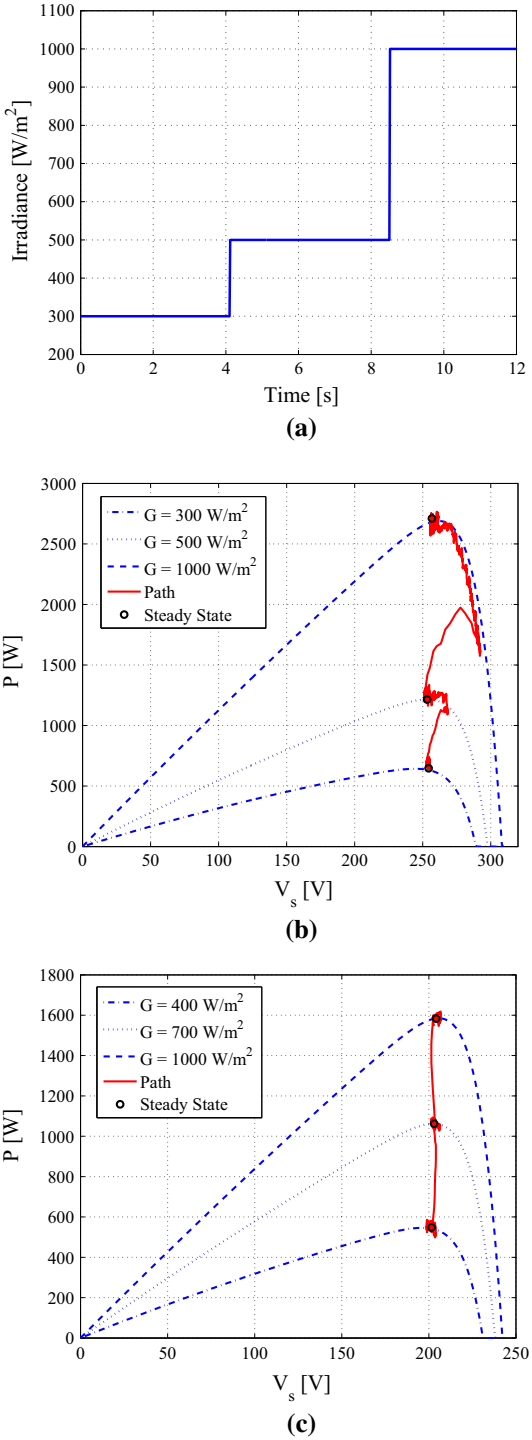


Fig. 12 Experimental results in the dynamic test for both inverters: **a** Irradiance profile used in the results with the inverters 1 and 2; **b** dynamic behavior of SAS in P–V plane for inverter 1; **c** dynamic behavior of SAS in P–V plane for inverter 2

ripple will be observed in SAS output current for the second inverter.

The dynamic behavior of the inverters maximum power point tracker is evaluated by means of the solar irradiance profile shown in Fig. 12a. The SAS output current ripple

also affects the maximum power point tracker of the inverter under test, as shown in Fig. 12b. Furthermore, the transient response of the SAS does not follow the reference. Generally, the inverter control system measures the SAS output current in order to follow the maximum power point of the solar array. In this situation, the larger ripple in the SAS output current generates oscillations in the maximum power point tracker algorithm, affecting the dynamic performance of the tested inverter. Applying the same irradiance profile in inverter 2, Fig. 12c is obtained. In this case, the SAS output current ripple is small and the maximum power point tracker of the inverter is slight affected.

5 Conclusion

This paper proposed a flexible SAS topology. The dynamic modeling of the system and the effect of inverter dc-link capacitance were discussed. A design methodology exploring all operation points of the converter was presented.

Simulation results considering resistive loads show that the system is able to emulate the solar array $P \times V$ curve for different irradiances. Experimental results using resistive loads also demonstrate the SAS steady-state operation.

Finally, experimental results for two commercial inverters show the SAS dynamic behavior. The results for the first commercial inverter, which presents a high dc-link capacitance value, show a high level of ripple in the SAS output current. This ripple affects the inverter maximum power point tracker and the ISC control strategy. In this case, the injected grid current is highly distorted.

For the second commercial inverter with lower dc-link capacitance, the ISC control operates correctly and the maximum power point of the inverter under test was not affected.

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