High-Power High-Dynamic-Performance Space Solar Array Simulator Using Step-Wave Tracking Output Voltage Approach

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***Abstract*—With the power of high-orbit satellites now reaching dozens of kilowatts, solar energy sources play an important role in nonterrestrial applications. However, most of the existing high-power solar array simulators (SASs) are designed for simulating energy sources in terrestrial applications, and may not have suitable dynamic performance for nonterrestrial applications. This paper proposes a design for a high-power high-dynamic-performance space solar array simulator (SSAS) system, which combines a linear power stage unit and a multilevel bus tracking converter unit, in order to achieve a fast step-switching capability and high-power-handling capacity. In this paper, we consider the SSAS power system as two separate parts: the I–V power curve simulator that uses a linear power stage with 20 linear voltage-controlled current paths in parallel; and the multilevel bus tracking converter unit that provides the variable voltage levels tracking the SSAS output voltage, in order to decrease the power dissipation in the linear power stage. This paper establishes a mathematical model for the multilevel converter under this particular system architecture, and presents the application qualification conditions and system design principles. The proposed 2.4-kW SSAS can react quickly to a load step between the short-circuit and open-circuit states, which are the most challenging working conditions, at a stepping frequency of 3 kHz; this is a superior dynamic performance compared to other similar devices. The experimental results of testing the spacecraft power supply with a shunt regulator architecture demonstrating better performance, when compared to the results from four SAS modular products in parallel.**

***Index Terms*—High-dynamic performance, I–V curve, linear power stage, multilevel tracking converter, solar array simulator (SAS).**

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I. Introduction

SOLAR energy is the main power source for a spacecraft; therefore, the power-conditioning unit is the most critical part in the entire spacecraft. The supply voltage and power of high-orbit satellites are considerably higher than those of the low-orbit satellites, with the power of high-orbit satellites currently reaching dozens of kilowatts. Hence, to improve the performance and reliability of space power systems, it is important to test the output characteristics of the space solar array in testing and evaluation environments close to those found in space. Space satellites suffer from challenging and complex working conditions, with a large range of temperature variations, and rapidly changing sunlight conditions. In addition, the space solar panels experience high-energy particle radiation [1]. Therefore, it is impossible to use typical terrestrial solar simulators to reproduce the working conditions of a space orbit satellite [2]. To perform this task in a better manner, we require a space solar array simulator (SSAS) to simulate the working conditions in space during the terrestrial testing of satellite power systems [3]. Solar panels in space can experience different solar radiation intensities, different temperatures, partial shading, or even partial destructive damage, which will cause a nonregular I–V characteristic output, with a nonlinearity that is difficult to produce with an SSAS. Thus, the data points of the nonregular I–V curves must be imported into the SSAS, in order that the SSAS output is consistent with the given I–V curve shape. The SSAS can be thought of as equivalent to a power amplifier with a high-dynamic performance, which can better meet the testing requirements of spacecraft power supplies during the terrestrial testing period.

Currently, most spacecraft power systems use the sequential switching shunt regulator (S3R) architecture, as shown in Fig. 1, which was introduced by the European Space Agency in the 1970s because of its high efficiency, low mass, simplicity, and high reliability [4]. The main feature of this topology, when used as a load for the SSAS, is the production of a step voltage with a high frequency, with the main bus voltage of the S3R being always regulated [5]. The dynamic response of the SSAS should be sufficiently fast to meet the power demands of the shunt regulator (SR), implying that the solar array simulator (SAS) should have a current-output-type framework. Essentially, the solar array panel output is also a current output.

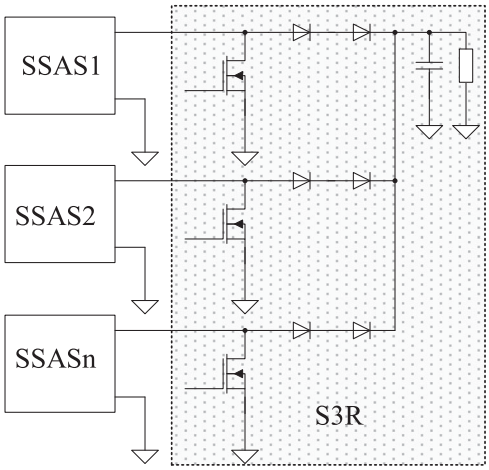

Fig. 1. S3R with the SSAS as a power source.

From the early articles on SASs using linear topologies, an approximate classification of the SASs can be made, based on their hardware structure and the power amplifiers used. One of the earliest contributions to SASs was made by Baert [6], which had the effect of virtually increasing the area of a small reference solar cell. A similar approach was followed by Nagayoshi [7] who proposed a multi I–V magnifier circuit with an elementary unit based on a dc linear amplifier. The circuit used a small photovoltaic (PV) cell as an I–V generator and provided separate amplifications for the voltage and current to realize a PV simulator. To overcome the limited flexibility of the common PV emulation methods to simulate the influence of the weather and PV source parameters, Easwarakhanthan *et al.* proposed a microcomputer controller simulator based on a programmable dc voltage source, a programmable multimeter, and a power amplifier [8].

However, these linear power stage solutions could not provide the high voltage, current, and power required for high-power testing applications. To improve the power level of the SAS, Lloyd *et al.* used a combination of a class A regulator and several dc supplies that could be connected to the regulator using switches [9], similar to an envelope-tracking power amplifier [10]. In particular, a modular design was utilized to setup a PV source simulator with a single power unit capable of delivering a maximum power of 400 W.

To meet the requirements of high-power system testing, a circuit based on switching converters is the mainstream plan. However, the switching solutions generally used in terrestrial applications cannot provide the high dynamic performance required for the extreme conditions encountered in nonterrestrial applications [11]. Specific system operation modes such as frequent load steps between the nominal and short-circuit states [5], [12], and load steps between the nominal and open-circuit states are usually adopted in nonterrestrial applications. These modes demand a faster dynamic response than for terrestrial applications. Nguyen-Duy *et al.* [13] proposed a highly dynamic nonlinear PV simulator consisting of a fourth-order output filter buck converter [14] and a novel nonlinear small-signal reference generator, with a rapid settling time of 10 μs. This switching solution could respond to a step-changing load from the nominal state to the open-circuit state, at 1 kHz, with a maximum output power of 200 W. However, this was not suitable for the SR structures of space power systems and the dynamic characteristics were not sufficiently fast to test SR power systems.

In addition to the PV simulators described in the literature, manufacturers have proposed different solutions for PV source simulation. Their customized turnkey approaches usually adopt a modular concept with programmable dc power supplies, which can be operated as individual equipment, or in multichannel configurations to meet higher power rating requirements [15]. Two SAS systems proposed by Elgar (Ametek) [16], [17] and Keysight (Agilent) [18] are described here. These two SAS systems are usually used for testing space power systems, and use linear topologies to simulate the I–V output curve with high-dynamic performances suitable for aerospace applications.

The proposed high-power SSAS adopts a switching linear hybrid architecture to improve the system efficiency and achieve both higher power output capacity and better dynamic performance than the SAS modular products on the market that require four modules in parallel to output the same power level. The SSAS output I–V power curves are closer to those of a real solar array panel, and hence the SSAS can more reliably test space power systems.

In this paper, we consider the SSAS power system as two separate parts: the I–V power curve simulator that uses a linear power stage with 20 linear voltage-controlled current paths in parallel; and the multilevel bus tracking converter unit that provides the variable voltage levels that track the SSAS output voltage in order to decrease the power dissipation in the linear power stage. Unlike the traditional applications of envelope-tracking power systems, the multilevel bus tracking converter of the SSAS that tracks the output voltage of the SSAS should be designed first, in order that the bus voltage can correctly step change the voltage levels. However, the output voltage of the SSAS first needs the bus voltage to be set; it then changes its voltage arbitrarily without distortion. This contradictory tracking logic requires the establishment of an accurate system model to facilitate detailed analysis to establish reasonable design principles. This paper establishes a correlation analysis model and presents the relevant system design considerations.

II. Proposed SSAS

A. Proposed System Configuration

The proposed system configuration is shown in Fig. 2. It includes three parts: the multilevel bus tracking converter unit, the linear power stage, and the field-programmable gate array (FPGA) digital controller [19]. The load Z_L connected to the SSAS output terminal is unknown, and is usually the tested power supply device.

The output voltage sample circuit should sample the SSAS output voltage into the low-voltage sampling signal U_{sas_sa}, and then send it to the multilevel bus tracking converter unit and FPGA digital controller. The multilevel bus tracking converter must produce the corresponding switching control instructions based on the given U_{sas_sa} signal, so that an appropriate bus

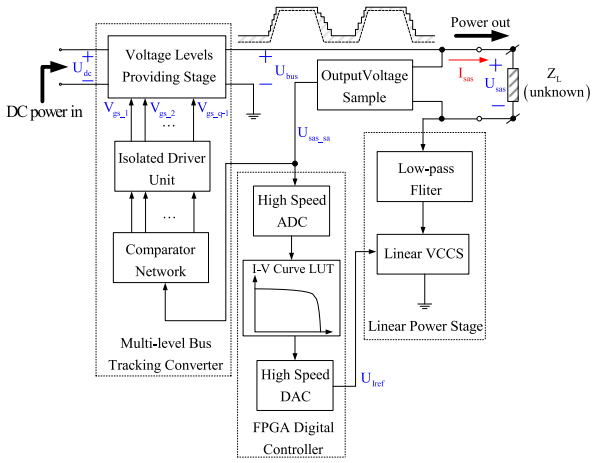

Fig. 2. Proposed SSAS configuration.

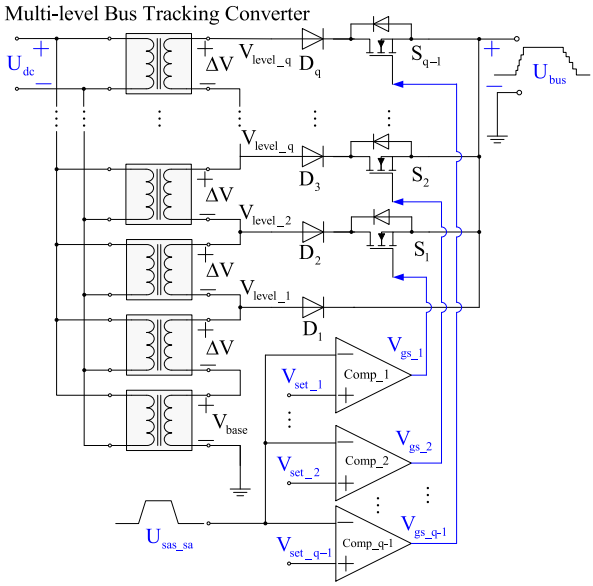

Fig. 3. Schematic diagram of the step-wave approach.

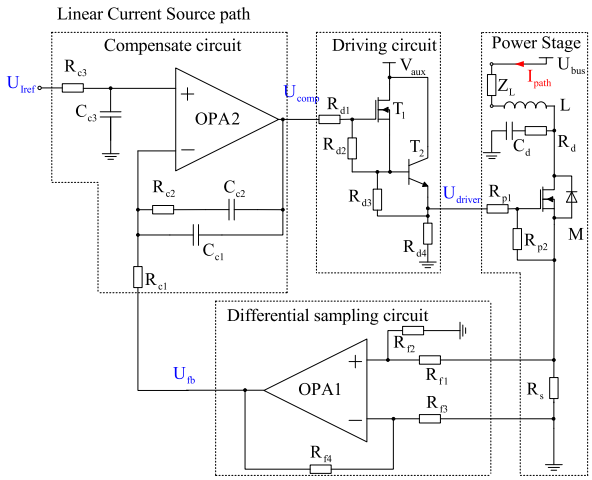

Fig. 4. Schematic of a single linear current path.

voltage level can be established. The FPGA digital controller is used to output the reference controlling voltage U_{Iref} of the linear voltage-controlled current source (VCCS) to control the expected SSAS output power current, which is one operating point of the set I–V power curve. The certain U_{Iref} is dependent on the given U_{sas_sa} through the I–V lookup table [20] that is prestored in the RAM of the digital controller.

B. Structure of Multilevel Bus Tracking Converter Unit

The multilevel bus tracking converter aims to decrease the linear power dissipation by using the envelope-tracking power supply architecture in order that the whole SSAS system has an improved power processing capacity. The key point is that the multilevel bus tracking converter should be switched fast enough to track the SSAS output voltage in a timely fashion [21]. However, unlike the envelope-tracking power supplies, the tracking envelope signal is not known in advance. The bus tracking converter will never know which voltage level should be generated unless the SSAS output voltage is already being produced, which means that the multilevel bus tracking level U_{bus} will always lag behind the output voltage U_{sas}. Thus, this part must be designed based on detailed analysis of the SSAS system, as introduced in Section III. The schematic diagram of the step-wave approach is shown in Fig. 3.

The level provider cell is made up of multiple isolated dc–dc modules connected in series to provide different levels, and the number of levels is q. These isolated dc–dc modules have the same input dc power voltage U_{dc} and output the same voltage ΔV, except for the first one that produces a voltage V_{base} to meet the saturation voltage requirements of the linear power stage. The control voltage U_{sas_sa} is compared with the setting levels V_{set_1} to $V_{set\_q\text{-}1}$ ($V_{set\_1} < V_{set\_2} < \ldots < V_{set\_q\text{-}1}$) using the comparators Comp_1 to Comp_q-1. The drive signals S_1–$S_{q\text{-}1}$ control the ON/OFF state of each gating switch. Therefore, a step wave is constituted by the corresponding voltage levels ($V_{level\_1} < V_{level\_2} < \ldots < V_{level\_q}$), which are converted from the same input voltage U_{dc}. If the provided voltage levels are sufficient, the shape of U_{bus} can be very close to that of U_{sas}.

III. Design of High-Power SSAS Control System and Small-Signal Model Analysis

A. Modeling, Control, and Design of the Multi-Parallel-Path Linear Power Stage

The schematic of a single linear current path is shown in Fig. 4. The circuit and mathematical model were analyzed in a previous article [22]. Some parameters have been fixed at values suitable for high-power SSAS applications, and are shown in Tables I and II.

Using the known small-signal modeling procedures [23], the frequency response of the proposed linear current source can be analyzed. The small-signal dynamic characteristics of the proposed linear current source can be obtained using a network frequency analyzer [24]. From the frequency analysis simulation of the small-signal model of the proposed linear current source, the open-loop frequency response curve is obtained as shown

TABLE I
PARAMETERS OF THE LINEAR CURRENT SOURCE

Parameter	Value	Parameter	Value
R_{d1}	4.7 Ω	R_{f1}	10 kΩ
R_{d2}	10 kΩ	R_{f2}	100 kΩ
R_{d3}	2 kΩ	R_{f3}	10 kΩ
R_{d4}	300 Ω	R_{f4}	100 kΩ
R_{p1}	4.6 Ω	R_{c1}	30 kΩ
R_{p2}	10 kΩ	C_{c1}	22 pF
R_s	0.2 Ω	R_{c2}	1 kΩ
OPA 1, 2	LM6172	C_{c2}	100 pF
G_{BW_opa}	86 dB	R_{c3}	1 kΩ
R_{o_opa}	14 Ω	C_{c3}	100 pF

TABLE II
ELECTRICAL PARAMETERS OF SiC-MOS TRANSISTOR C2M0080120D

Parameters of SiC-MOS Transistor (C2M0080120D)	Value	Unit
g_{fs} [1)]	0.7	S
C_{iss}	950	pF
C_{rss}	6.5	pF
C_{oss}	80	pF
R_G	4.6	Ω

Note: 1) A valid g_{fs} is dependent on the transfer characteristic curve in the datasheet.

in Fig. 5(a). From the small-signal model open-loop simulation frequency Bode response, it can be seen that the phase margin is 87.94° and the cut-roll frequency is 51.765 kHz.

A prototype was built to demonstrate the actual open loop response using the frequency response analyzer FRA5097 under the same working conditions. The swept-frequency open-loop Bode responses of a single linear current path is shown in Fig. 5(b); each path has a phase margin $\Delta\varphi$ of 82.12° and a cut-roll frequency f_{cr} of 47.58 kHz, which are close to the simulated Bode results from the proposed small-signal model.

However, in the case of an SSAS with combined analog hardware systems and digital controller systems, considering the issue of delay margin is significantly more important, because a satisfactory phase margin does not guarantee a satisfactory delay margin [25], especially in systems with high bandwidths and high-dynamic response requirements. From the measured open-loop Bode plot, the cutoff frequency ω_{cr} is

$$\omega_{cr} = 2\pi f_{cr} = 2.99 \times 10^5 \text{ rad/s}. \tag{1}$$

The phase margin $\Delta\Phi$ is

$$\Delta\Phi = (\Delta\varphi/360^\circ) \times 2\pi = 1.443 \text{ rad}. \tag{2}$$

The delay margin $\Delta\tau_{dm}$ can be calculated from the phase margin $\Delta\Phi$ and cutoff frequency ω_{cr} as follows:

$$\Delta\tau_{dm} = \frac{\Delta\Phi}{\omega_{cr}} = 4.83\ \mu\text{s}. \tag{3}$$

The FPGA digital controller uses a 40-MHz clock for the analog-to-digital and digital-to-analog converters, and provides the U_{Iref} from the I–V lookup table. The total delay time T_s can be calculated to be 600 ns, that is

$$\Delta\tau_{dm} > T_s = 0.6\ \mu\text{s}. \tag{4}$$

The index of selecting the delay margin for system designing is

$$\Delta\tau_{dm} \geq T_s\ [\min : 0.75T_s]. \tag{5}$$

Therefore, the phase margin and delay margin of the linear power stage are satisfactory for use in high-dynamic-performance SSAS applications.

B. Small-Signal Model for Analyzing the Influence of Stepping Voltage on the Linear Current Source

The linear current source path uses a power MOSFET working in the saturation region to output a constant current that is proportional to the reference voltage U_{Iref}, irrespective of the state of U_{ds}, where U_{ds} is the voltage between the drain and source of the power MOSFET. The corresponding mathematical model relationship can be obtained by considering the small-signal model of the power MOSFET alone. Fig. 6 shows the related small-signal circuit equivalent model [26].

Based on Fig. 6(a), we can obtain (6)–(8) from the three nodes I– III according to KVL and KCL

$$I_d(s) = g_{fs}U_{gs\_inner}(s) + sC_{gd}U_{dg}(s) + sC_{ds}U_{ds}(s) \tag{6}$$

$$I_s(s) = g_{fs}U_{gs\_inner}(s) + I_{Cgs}(s) + sC_{ds}U_{ds}(s) \tag{7}$$

$$\frac{U_{gs\_outer}(s) - U_{gs\_inner}(s)}{R_g} + sC_{gd}U_{dg}(s) = I_{Cgs}(s). \tag{8}$$

By simplifying, we can derive the following equation:

$$\frac{U_{gs\_outer}(s) - U_{gs\_inner}(s)}{R_g} = sC_{gs}U_{gs\_inner}(s) - sC_{gd}U_{dg}(s). \tag{9}$$

The mathematical relationship between $I_d(s)$ and $U_{ds}(s)$ can be deduced from G_{PSRR_id}, which can accurately analyze the effect of the step $U_{ds}(s)$ on the drain current of the linear current source, as per

$$G_{PSRR\_id} = \frac{I_d(s)}{U_{ds}(s)} = \frac{a_1 s^2 + a_2 s}{b_1 s + 1} \tag{10}$$

where there are

$$a_1 = R_g C_{ds}(2C_{gs} + C_{gd}) \tag{11}$$

$$a_2 = (g_{fs}R_g + 1)C_{gd} + C_{ds} \tag{12}$$

$$b_1 = R_g(C_{gs} + C_{gd}). \tag{13}$$

The G_{PSRR_id} of (10) is analyzed with two zero points and one pole, which is equivalent to a differential characteristic. To reduce the peak current output from the SSAS, a damping *LC* filter is added to the linear VCCS [27], as shown in Fig. 6(b). The mathematical model G_{PSRR_iin} between $I_{in}(s)$ and $U_d(s)$ is given by

$$G_{PSRR\_iin} = \frac{I_{in}(s)}{U_d(s)} = \frac{z_1 s + z_2}{p_1 s^2 + p_2 s + p_3} \tag{14}$$

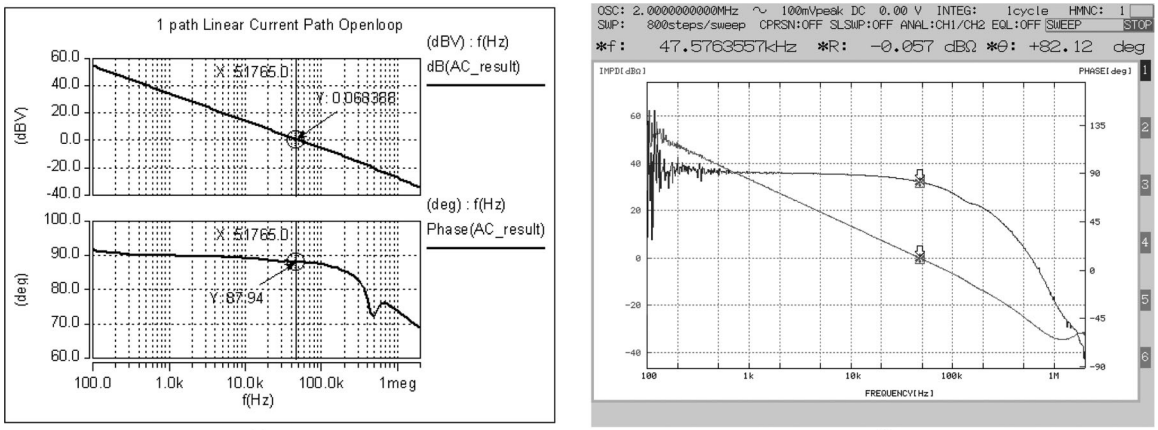

Fig. 5. Bode response results for the proposed single path linear current source system: (a) open-loop Bode response simulation results to evaluate the stability margin and (b) measured open-loop Bode plot.

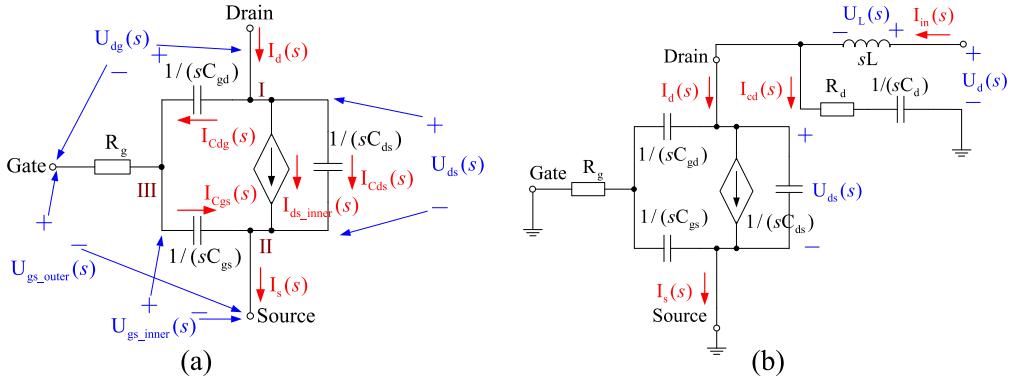

Fig. 6. Related small-signal circuit equivalent model: (a) equivalent circuit model to analyze the relationship between $I_d(s)$ and $U_{ds}(s)$ and (b) equivalent circuit model to analyze the relationship between $I_{in}(s)$ and $U_d(s)$.

where there are

$$z_1 = 1 + R_d G_{\text{PSRR\_id}})C_d \tag{15}$$

$$z_2 = G_{\text{PSRR\_id}} \tag{16}$$

$$p_1 = (1 + R_d G_{\text{PSRR\_id}})LC_d \tag{17}$$

$$p_2 = R_d C_d + LG_{\text{PSRR\_id}} \tag{18}$$

$$p_3 = 1. \tag{19}$$

The damped *LC* low-pass filter is used to inhibit the high-frequency components of the step-up change in $U_d(s)$, thereby reducing the $U_{ds}(s)$ variations to reduce the effect of the step changing $U_d(s)$ on $I_d(s)$. From Fig. 6, we can see that the mathematical model of $U_d(s)$ to $U_{ds}(s)$ is G_{LPF}

$$G_{\text{LPF}} = \frac{U_{ds}(s)}{U_d(s)} = \frac{R_d C_d s + 1}{LC_d s^2 + R_d C_d s + 1}. \tag{20}$$

The mathematical expression $G_{PSRR\_id\_LP}$ of the effect of the step change of $U_d(s)$ on $I_d(s)$ is

$$G_{\text{PSRR\_id\_LP}} = \frac{I_d(s)}{U_d(s)} = G_{\text{LPF}} \cdot G_{\text{PSRR\_id}}. \tag{21}$$

By analysis of the design, a reasonable choice of the parameters gives $L = 100\ \mu H$, $C_d = 1\ \mu F$, and $R_d = 20\ \Omega$. The frequency-domain characteristic curves of G_{PSRR_id}, G_{LPF}, and $G_{PSRR\_id\_LP}$ and are obtained as shown in Fig. 7(a) and (b).

From Fig. 7, it can be seen that the system during the $U_d(s)$ suppression effect is almost maintained at -100 dB by adding the designed damped LC low-pass filter. However, Fig. 6(b) shows that the SSAS output current I_{sas} is equal to I_{in}; therefore, it is necessary to derive the influence of the stepping $U_d(s)$ on $I_{in}(s)$ after adding the LPF. According to the above-obtained $I_{in}(s)$ and $U_d(s)$ mathematical model G_{PSRR_iin}, the corresponding frequency-domain characteristic curve can be obtained as shown in Fig. 7(b). By adding the designed LPF, the high-frequency noise of $U_d(s)$ can be suppressed adequately, which validates the rationality of the filter parameter design.

C. Modeling, Control, and Design of the Multi-Level Bus Tracking Converter

The mathematical model $G_{Linear\_N\,path}$ of the linear VCCS, from the reference voltage $U_{Iref}(s)$ to the output current $I_{Lin}(s)$ is known from a previous article. In addition, the entire SSAS system structure can be deduced from the aforesaid analysis, and is shown in Fig. 8.

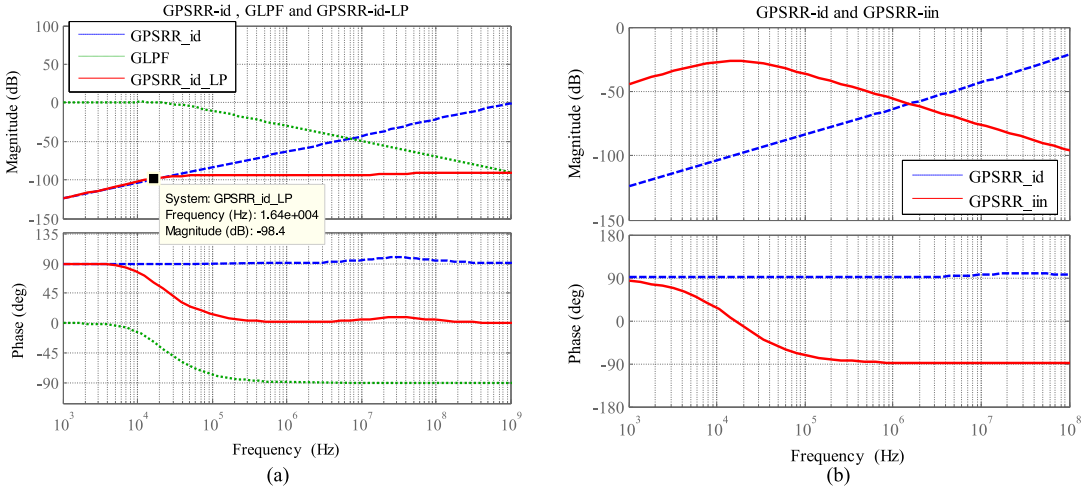

Fig. 7. Comparison of frequency-domain responses of mathematical model with damping *LC* filter: (a) frequency domain characteristic curve of $G_{PSRR\_id\_LP}$ and (b) frequency domain characteristic curve of G_{PSRR_iin}.

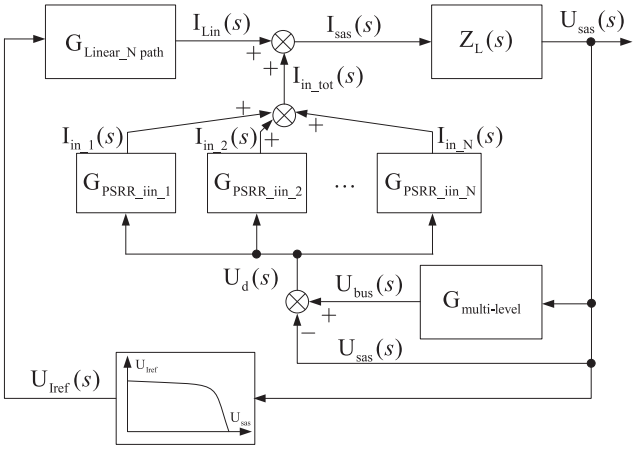

Fig. 8. Entire SSAS system structure block diagram.

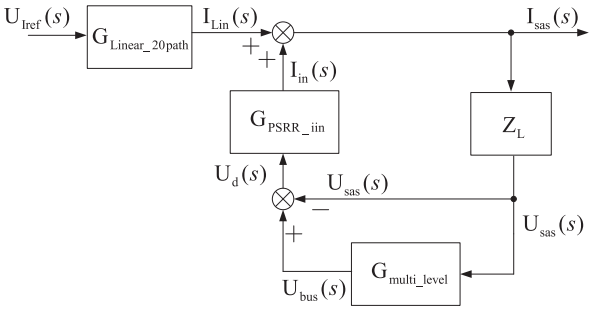

Fig. 9. Block diagram of the multilevel bus tracking converter.

When the SSAS is working at a fixed operating point on the set I–V curve, the multilevel bus tracking converter operates as per the block diagram shown in Fig. 9.

Because there are

$$U_{\text{sas}}(s) = I_{\text{sas}}(s) \cdot Z_L \tag{22}$$

$$U_{\text{bus}}(s) = U_{\text{sas}}(s) \cdot G_{\text{multi\_level}} \tag{23}$$

$$U_{\text{d}}(s) = U_{\text{bus}}(s) - U_{\text{sas}}(s) = (G_{\text{multi\_level}} - 1) \cdot U_{\text{sas}}(s). \tag{24}$$

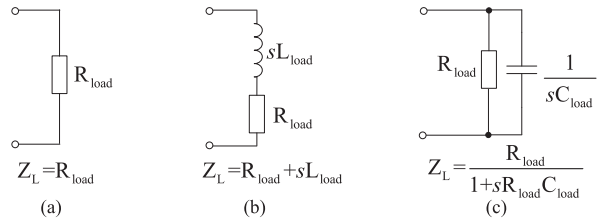

Fig. 10. Equivalent model expressions for different load types: (a) Z_L is a resistive load; (b) Z_L is an inductive load; and (c) Z_L is a capacitive load.

Let $U_{\text{Iref}}(s)$ be 0, then $I_{\text{Lin}}(s)$ is 0, and we can obtain the mathematical model $G_{\text{multi\_level}}$ between $U_{\text{bus}}(s)$ and $U_{\text{sas}}(s)$ as follows:

$$G_{\text{multi\_level}} = \frac{U_{\text{bus}}(s)}{U_{\text{sas}}(s)} = \frac{1 + Z_L G_{\text{PSRR\_iin}}}{Z_L G_{\text{PSRR\_iin}}}. \tag{25}$$

The mathematical model $G_{\text{multi\_level}}$ derived from the aforesaid equation is related to the load Z_L of the connected SSAS. In order to study the effect of Z_L on $G_{\text{multi\_level}}$, Z_L is divided into three kinds of load conditions, as shown in Fig. 10. We can use MATLAB to obtain the frequency-domain characteristics of $G_{\text{multi\_level}}$ for the different load types of Z_L with appropriate load parameters, as shown in Fig. 11.

It can be seen from the frequency-domain simulation waveforms of different load types in Fig. 11 that, when Z_L is resistive or inductive, U_{bus} always lags behind U_{sas} in the low-frequency band, with 90° phase difference, i.e., the U_{bus} under resistive and inductive load conditions. The tracking waveform always lags behind the U_{sas} waveform. This conclusion means that it is impossible to track the output voltage U_{sas} for U_{bus} without distortion under resistive and inductive load conditions.

When Z_L is a capacitive load, the phase difference between U_{bus} and U_{sas} in the low-frequency band is almost 0°, and C_{load} cannot be too small that U_{bus} can track U_{sas} with less distortion of U_{sas}, which means the tracking bandwidth has some limitations.

Fortunately, the proposed SSAS is used in spacecraft power supply test applications with SR structures, which are ideal

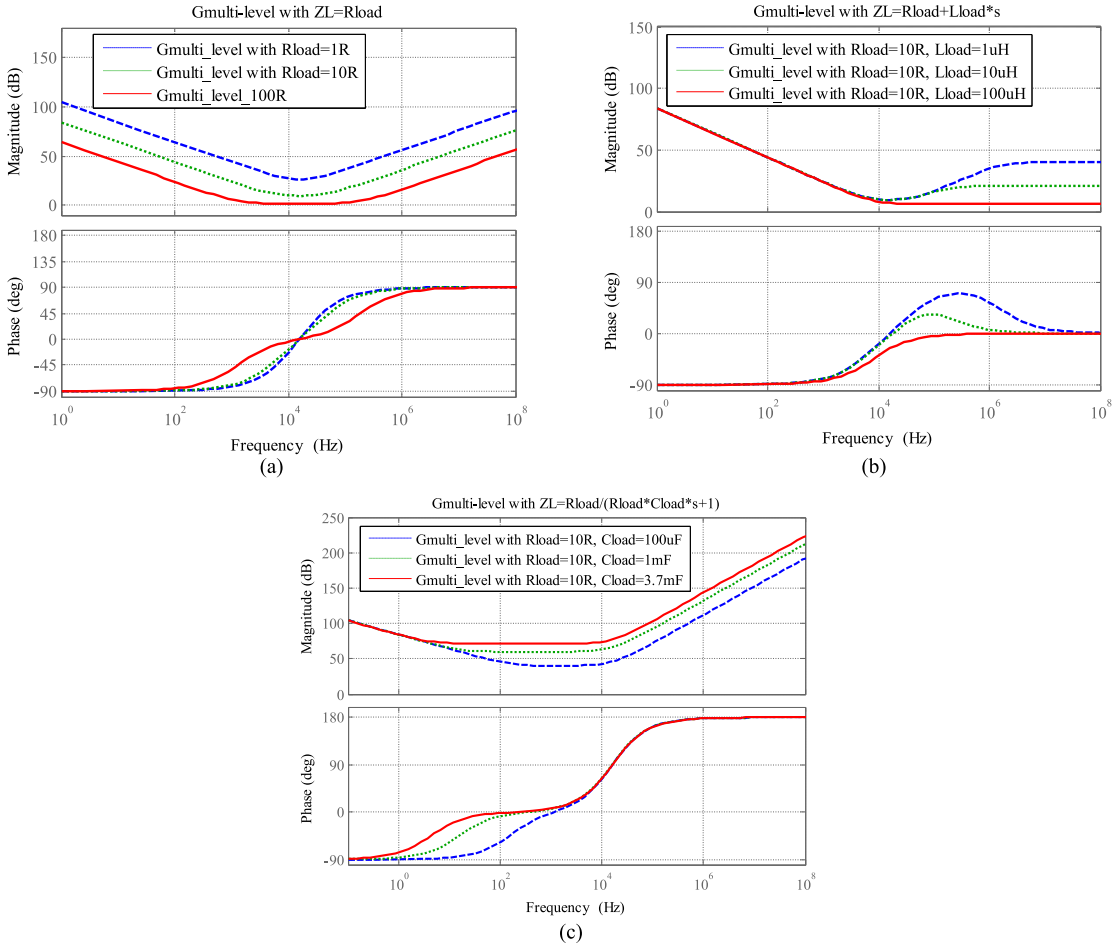

Fig. 11. Frequency response curve of G_{multi_level} for different types of Z_L. (a) Z_L is a resistive load; (b) Z_L is an inductive load; and (c) Z_L is a capacitive load.

capacitive loads. Therefore, the proposed SSAS can perform adequately in these conditions.

D. Considerations for Parameter Design of the Multilevel Bus Tracking Converter

The multilevel converter used here is made up of common isolation dc–dc power supply modules in series. According to the high-power SSAS index requirements, the minimum output power current of the selected isolated dc–dc converter is 20 A. According to the demanded power level and the size of the dc–dc module, the common 12-V output isolated dc–dc module is used to provide the multilevel converter unit level voltage. The power index requirements for high-power SSAS are shown in Table V.

From Table V, it can be seen that the maximum SSAS output voltage U_{sas_max} is 120 V, and if the selected level voltage ΔV is 12 V, then the required level q of the multilevel converter is 10. That is, the number of levels required for the multilevel converter is at least 10. Since the linear VCCS requires a predetermined U_{ds} voltage to ensure that the power MOSFET operates reliably in the saturated region, a base voltage V_{base} is required; the base voltage is chosen to be 5 V. It is possible to introduce the first-level voltage V_{level_1} of the multilevel converter as $(V_{base} + \Delta V)$. It is also possible to derive the relationship between the SSAS output voltage $U_{sas}(t)$ and the set inversion levels $V_{set\_1}, V_{set\_2}, \ldots, V_{set\_q\text{-}1}$, and the corresponding bus voltages $U_{bus}(t)$, $V_{level\_1}, V_{level\_2}, \ldots, V_{level\_q}$, are shown in Table III.

The time-domain expression for the bus voltage can be obtained as follows:

$$U_{bus}(t) = V_{base} + \Delta V + \text{ceil}\left[\frac{q-1}{U_{sas\_max}} \cdot U_{sas}(t) - \lambda + 1\right] \cdot \Delta V \tag{26}$$

where ceil is the rounding function. From the aforementioned thermal analysis and the time-domain mathematical expression of the multilevel converter tracking bus voltage, it can be seen that the chosen value of λ should be guaranteed such that the U_{bus} (t) can track the SSAS output voltage U_{sas} (t) satisfactorily.

It can be seen that the larger the λ is, the greater the delay margin τ will be, but the maximum power dissipation of a single power MOSFET, P_{tot} will be 26 W due to the thermal loss in the linear current source, and the maximum current of a single linear path will be 1 A; thus, the permissible U_{ds_max} will be 26 V. When $U_{sas}(t)$ increases to V_{set_1}, $U_{bus}(t)$ will be flipped from V_{level_1} to V_{level_2}, where the power MOSFET has the maximum power dissipation. The following inequalities hold true:

$$U_{ds\_max} = U_{bus}(t) - U_{sas}(t) \leq 26 \text{ V}. \tag{27}$$

TABLE III
LOGICAL RELATIONS BETWEEN LEVEL PARAMETERS OF MULTILEVEL BUS TRACKING CONVERTER

The range of tracked voltage $U_{sas}(t)$ / V	The setting flipping voltage $V_{set\_i}(i = 1, 2, \ldots, q\text{-}1)$	Value (V)	Bus level voltage $U_{bus}(t)$ (V_{level_i+1})	Value (V)
$[0, V_{set\_1})$	–	–	V_{level_1}	$V_{base} + \Delta V$
$[V_{set\_1}, V_{set\_2})$	V_{set_1}	$\lambda.U_{sas\_max}/(q\text{-}1)$	V_{level_2}	$V_{base} + 2.\Delta V$
$[V_{set\_2}, V_{set\_2})$	V_{set_2}	$(\lambda + 1).U_{sas\_max}/(q\text{-}1)$	V_{level_3}	$V_{base} + 3.\Delta V$
...	...	...	...	...
$[V_{set\_i\text{-}1}, V_{set\_i})$	V_{set_3}	$(\lambda + i\text{-}1).U_{sas\_max}/(q\text{-}1)$	V_{level_4}	$V_{base} + i.\Delta V$
...	...	...	...	...
$[V_{set\_q\text{-}1}, U_{sas\_max})$	$V_{set\_q\text{-}1}$	$(\lambda + q\text{-}2).U_{sas\_max}/(q\text{-}1)$	V_{level_10}	$V_{base} + (q\text{-}1).\Delta V$

Note: λ is the proportion weight of V_{set_1} in U_{sas_max} divided by $(q - 1)$, and the proportion weight of each flip level is the same.

TABLE IV
MULTILEVEL BUS TRACKING CONVERTER DESIGN PARAMETER VALUES

Therange of tracked voltage $U_{sas}(t)$ / V	The setting flipping voltage V_{set_i} $(i = 1, 2, \ldots, q\text{-}1)$	Value (V)	Bus level voltage $U_{bus}(t)$ $(V_{level_{i+1}})$	Value (V)
[0.00, 3.00)	–	–	V_{level_1}	17.00
[3.00, 16.33)	V_{set_1}	3.00	V_{level_2}	29.00
[16.33, 29.67)	V_{set_2}	16.33	V_{level_3}	41.00
[29.67, 43.00)	V_{set_3}	29.67	V_{level_4}	53.00
[43.00, 56.33)	V_{set_4}	43.00	V_{level_5}	65.00
[56.33, 69.67)	V_{set_5}	56.33	V_{level_6}	77.00
[69.67, 83.00)	V_{set_6}	69.67	V_{level_7}	89.00
[83.00, 96.33)	V_{set_7}	83.00	V_{level_8}	101.00
[96.33, 109.67)	V_{set_8}	96.33	V_{level_9}	113.00
[109.67, 120.00]	V_{set_9}	109.67	V_{level_10}	125.00

TABLE V
I–V CURVES SETTING FOR THE EXPERIMENT

Setting parameters	The setting I–V Curve for steady I–V and shunt switching testing	The setting I–V Curve for SR testing
Open-circuit voltage (U_{oc})	120 V	120 V
Short-circuit current (I_{sc})	20 A	18 A
The maximum power point voltage (U_{mp})	105 V	95 V
The maximum power point current (I_{mp})	18 A	15 A

The existence inequality

$$29\,\mathrm{V} - \lambda \cdot (120\,\mathrm{V}/9\,\mathrm{V}) \leq 26\,\mathrm{V} \tag{28}$$

can be solved by

$$\lambda \geq 0.225. \tag{29}$$

When λ is 0.225, $U_{bus}(t)$ can guarantee the ability to track $U_{sas}(t)$ more quickly, and the thermal power consumption of the linear power stage can meet the design requirements. The values of the set voltage V_{set_i}, bus voltage $U_{bus}(t)$, and SSAS output voltage $U_{sas}(t)$ can be calculated as shown in Table IV.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed high-power SSAS is tested under three typical operating conditions usually encountered in nonterrestrial applications, including the steady-state response along the static I–V curve and the step change of output load between the short-circuit and open-circuit states, which are the most extreme working conditions of an SAS, at different stepping frequencies. In addition, the SSAS is tested using a SR structure. As high power is used in space power systems, the characteristics of the SSAS should be better than that of the commonly used SAS modular products, in terms of both electrical performance and volume.

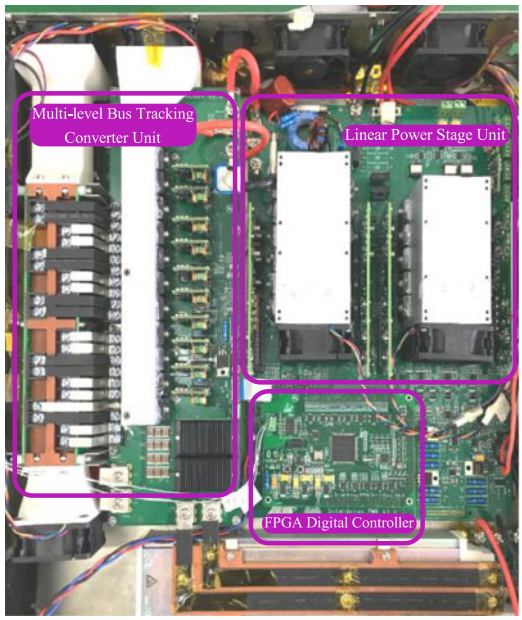

Fig. 12. Photograph of the prototype.

As the proposed circuit is of the current-output type, it unfortunately suffers from an undersigned open-circuit voltage output. Hence, the problem of load step between the nominal and the open-circuit states of the voltage-controlled current SSAS will not be addressed in this paper. A photograph of the prototype is depicted in Fig. 12. The proposed high-power and high dynamic performance SSAS can also simulate different nonregular I–V curves including those representing different solar radiation intensities, different temperatures, partial shading, or even partial destructive damage because of the fast response to the changing working points of the set table curves of these nonlinear I–V curves.

The 20 linear VCCSs are connected in parallel to provide a maximum current output of 20 A. Four dc fans operating at their highest speeds are installed at both ends of the radiator to extract

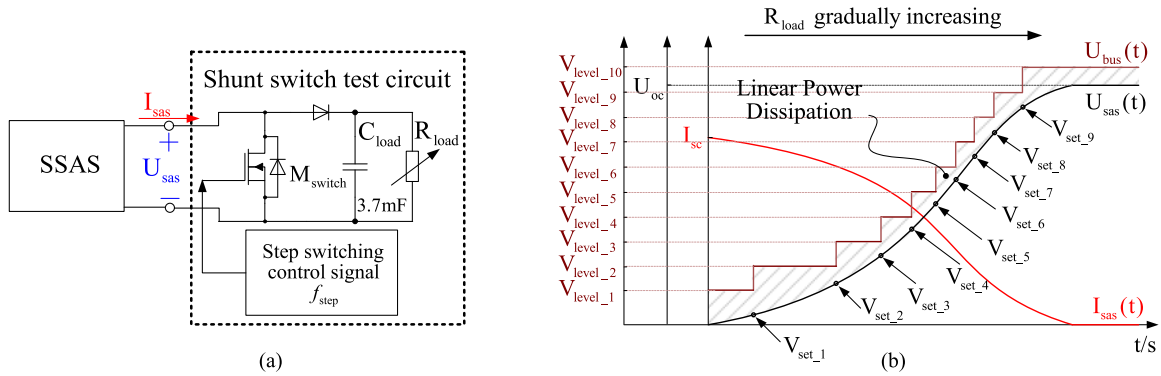

Fig. 13. Testing circuit and expectation steady waveform diagram. (a) Testing circuit for steady response experiment with M_{switch} in the off state and (b) Illustration of multilevel bus voltage $U_{bus}(t)$ and output current $I_{asa}(t)$ changes with $U_{sas}(s)$ increase.

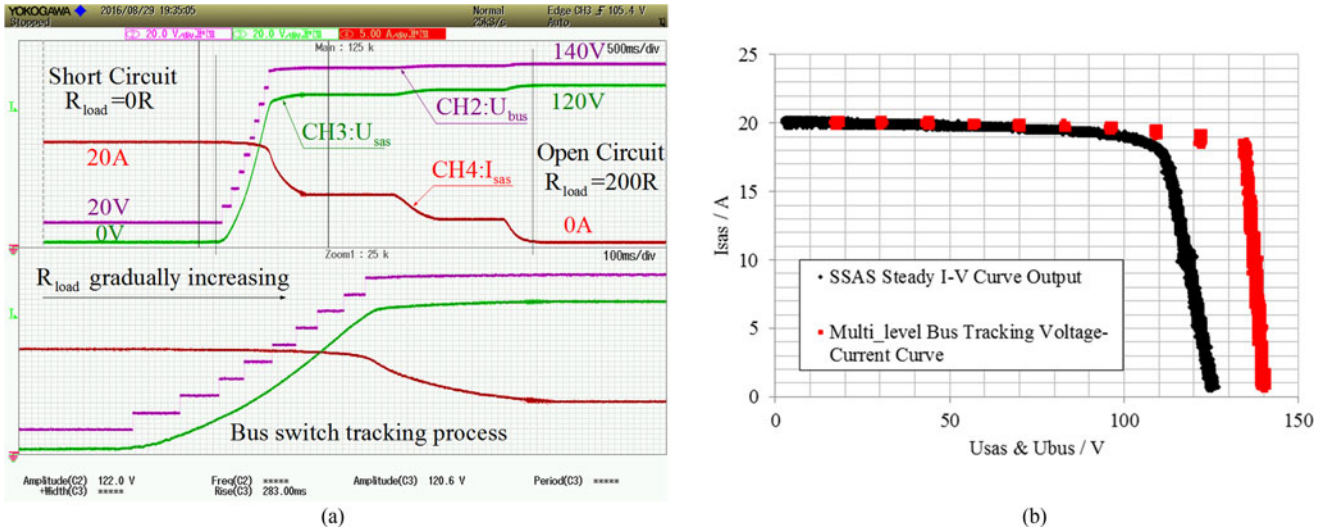

Fig. 14. Steady-state output current and voltage of the proposed SSAS. (a) Time-domain waveforms of the SSAS output voltage U_{sas} and output current I_{sas}; and (b) I–V curve output of the experimental data from the oscilloscope.

heat. The sealed air passage is removed in Fig. 12 in order to show the hardware circuit structure clearly.

The setting of the I–V power curves is different under different testing conditions, as shown in Table V. The experiments on steady-state response and shunt switching with different operating points use the maximum output capability of the I–V curve. However, the tested SR should be tested with a relatively small I–V power curve. Both setting curves have a maximum open-circuit voltage U_{oc} of 120 V.

A. Steady-State Response

To examine the steady-state response of the SSAS, the output voltage U_{sas} and output current I_{sas} are tested by gradually increasing the resistance of the connected R_{load}. The I–V curve specifications for the experiment are shown in Table V. The testing circuit is shown in Fig. 13(a) with the switching MOSFET M_{switch} kept in the off state so that the SSAS output terminal is connected with a capacitive load. Fig. 13(b) shows the expected steady-state waveform. $U_{bus}(t)$ will always track the output voltage $U_{sas}(t)$, and will flip to the next adjacent level when $U_{sas}(t)$ reaches the corresponding set voltage V_{set_i}. The output current $I_{sas}(t)$ will decrease gradually owing to the working logic of the set of I–V curves. The partial area of shadows is the linear power dissipation P_{dis_lin}; P_{dis_lin} can be controlled by reasonable design of the multilevel converter parameters.

Fig. 14 shows the steady-state response of the SSAS. Fig. 14(a) depicts the time-domain output voltage U_{sas} and the output current I_{sas}. The operating point of the I–V curve is from the short-circuit region to an approximate open-circuit region, with a gradual change in the resistance of the sliding rheostat connected to the output terminal of the SSAS. The bottom half of Fig. 14(a) shows an expanded view of its middle part, in order to observe the bus tracking process more clearly. Fig. 14(b) shows the experimental data of U_{sas} and I_{sas}, recorded by an oscilloscope; the data are plotted in the second coordinate, with U_{sas} on the horizontal axis and I_{sas} on the vertical axis. The scatter plots of U_{bus} and U_{sas} are also shown in Fig. 14(b).

From the results of the steady-state experiment, it can be seen that the output I–V curve of the SSAS is the setting I–V curve, and the multilevel bus tracking converter can track U_{sas} satisfactorily. Thus, the proposed SSAS can satisfactorily simulate a normal steady-state I–V curve.

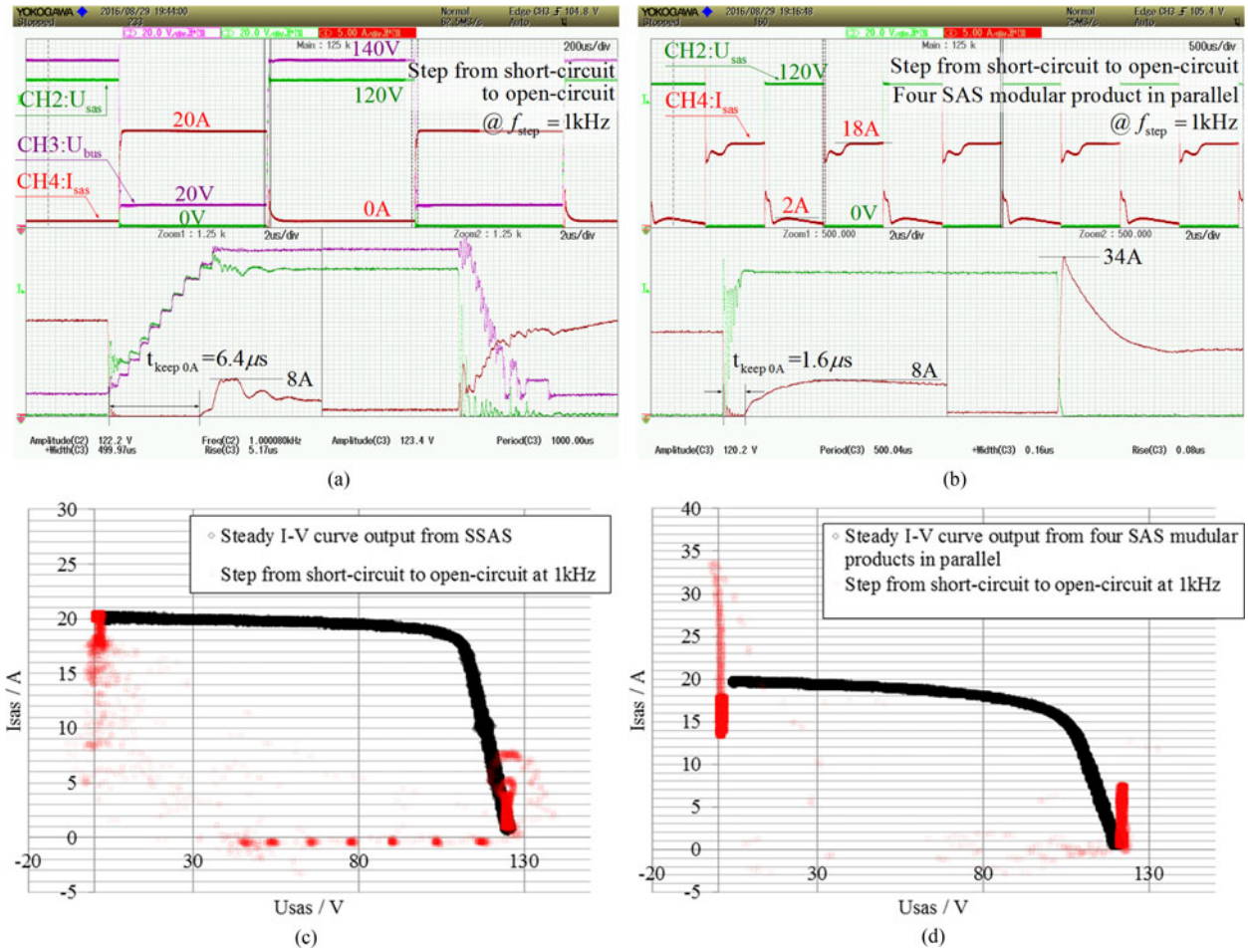

Fig. 15. Step working point between the short-circuit and the open-circuit stages at $f_{step} = 1$ kHz: (a) time-domain waveform of the SSAS; (b) time-domain waveform of the four SAS modules in parallel; (c) distribution of step switching data in the output steady I–V curve of SSAS; and (d) distribution of step switching data in the output steady I–V curve of SAS modular products.

B. Shunt-Switching Regulation

The shunt-switching regulation experiment analyses the step from a short-circuit to an open-circuit, which is the harshest working condition for an SAS. Measured data from the SSAS and the four SAS modular products in parallel, during the step between the short-circuit and the open-circuit at a 1-kHz stepping frequency, are shown in Fig. 15.

The experimental data are mainly focused on the setting I–V power curve at the short-circuit and open-circuit operating points. The data points of the switching transition process are scattered at the lower end of the setting I–V curve because of the influence from the multilevel bus tracking process, which cannot guarantee an undistorted U_{sas} under high-output power conditions. During the process of switching, the rising edges of U_{bus} and U_{sas} are so close that the linear current source cannot work in the saturated area; therefore, the process I_{sas} will be zero. From Fig. 15(a), we can find that the duration when I_{sas} is maintained at 0 A, t_{keep_0A} is approximately 6.4 μs, which will not influence the tested power supply that acts equivalent to the capacitive load.

However, the four SAS modular products in parallel do not operate well in this working condition and the time-domain waveform has considerable distortion. Fig. 15(d) shows that the experimental data are not mainly focused on the setting I–V power curve at the short-circuit and open-circuit operating points. Moreover, it can be observed from Fig. 15(b) that there is a huge peak current reaching 34 A, which would have a great influence on the tested power supply that acts equivalent to the capacitive load. We can find a common phenomenon in Fig. 15(a) and (b): both I_{sas} will reach approximately 8 A after remaining at 0 A for a short period because the speed of switching is too fast. The results show that the SSAS demonstrates excellent dynamic characteristics.

In order to better examine the limited dynamic characteristics, the stepping test frequency was increased to 3 kHz. Fig. 16 shows the experimental results for the SSAS and the four SAS modular products in parallel at an f_{step} of 3 kHz.

As shown in Fig. 16 (a) and (c), the proposed SSAS can still operate satisfactorily at a 3-kHz stepping frequency between the short-circuit and open-circuit states, without any current spikes, and the two operating points can be steadily reached from the distributed experimental data. However, the time-domain waveforms of the four parallel SAS modular products have considerable distortions, such that the designated working points are

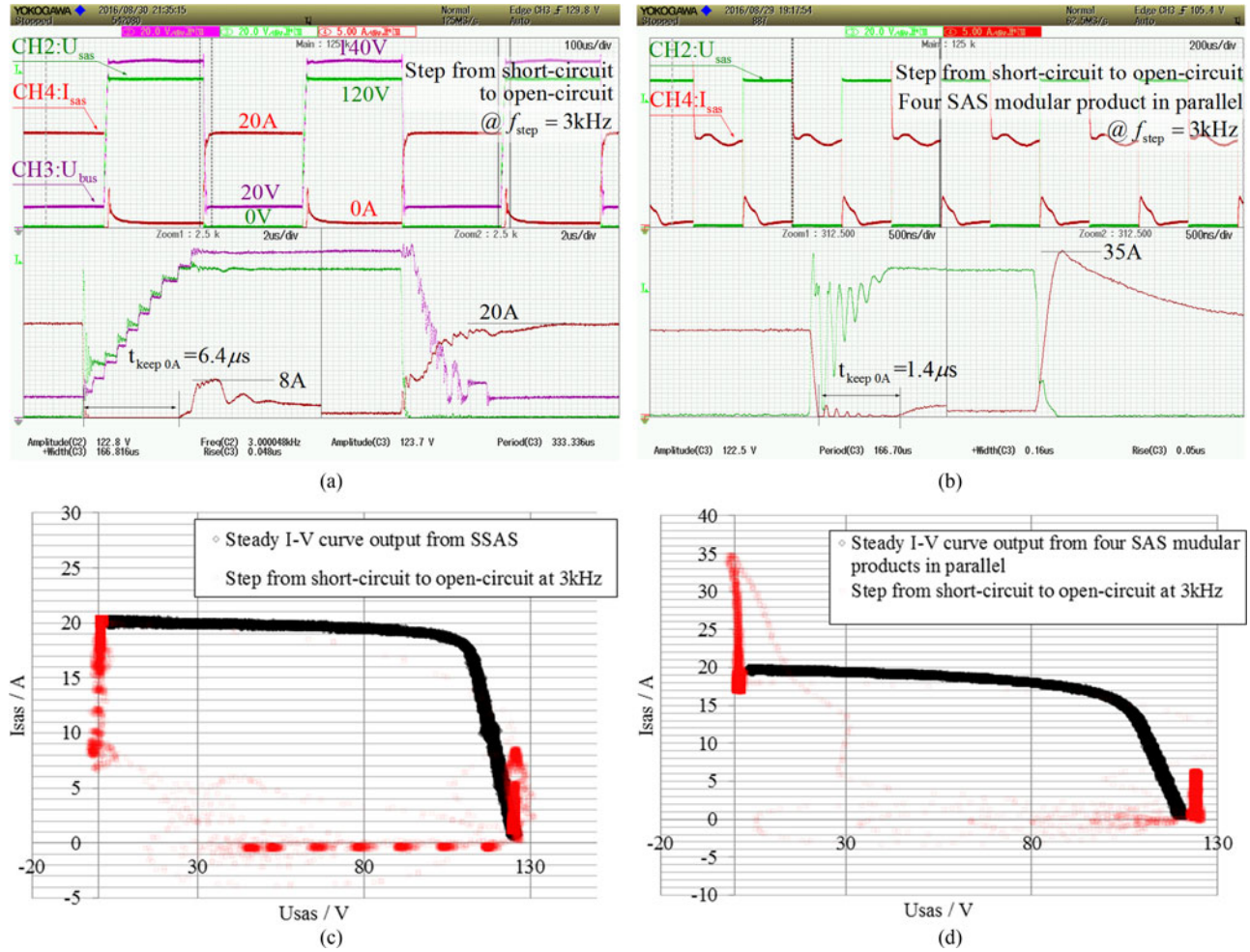

Fig. 16. Step working point between the short-circuit and open-circuit at $f_{step} = 3$ kHz: (a) time-domain waveform of the SSAS; (b) time-domain waveform of the four SAS modules in parallel; (c) distribution of step switching data in the output steady I–V curve of SSAS; and (d) distribution of step switching data in the output steady I–V curve of SAS modular products.

hardly reached. Similarly to the SSAS, there is a 35-A current peak output.

C. Testing and Evaluation of SR Regulator

However, our final goal is to test the space power system. The SSAS and the four SAS modular products in parallel were tested using a shunt switching regulator, with the results given in Fig. 17. Because there are voltage and current limits for the tested shunt regulator, the set I–V curve is changed as shown in Table V. The test result waveforms from the SSAS are shown in Fig. 17(a) and (c). U_{bus} is the SSAS multilevel bus tracking voltage and U_{sas} and I_{sas} are the SSAS output voltage and current, respectively. For better clarity, comparisons of the test results from the four parallel SAS modular products are shown in Fig. 17(b) and (d).

In fact, the test with SR is equivalent to step switching from the short-circuit to a nominal load, and this working condition is relatively easy to complete well for both type of SAS. Fig. 17(a) shows the time-domain waveform of the SSAS and (see Fig. 17c) is the data distribution; the SSAS can reach the two operating points, (0 V, 19 A) and (100 V, 13 A), very steadily and react fast. There are some unaltered data points distributed around the set I–V curve because of the influence from the multilevel tracking switching. However, it should be noted that the expected working points are (0 V, 18 A) and (100 V, 13.67 A). The current difference is dependent on the control accuracy of the 20 paths of parallel linear current sources; it is difficult to achieve a high current control accuracy without additional current calibration compensation methods. However, adding a common external current loop to ensure an accurate output load current would sacrifice the high-dynamic response of the linear power stage; thus, using a current calibration compensation method would be more suitable in the SSAS application.

However, from the testing results from the four parallel SAS modular products, we can find that the nominal working point (100 V, 12 A) cannot be reached adequately because of the relatively slow dynamic response capability. A current spike always exists during the switching period, and can reach 22.4 A, which is much larger than the set short-circuit current I_{sc}. This indicates that the proposed SSAS is more suitable for high-power space power supply testing applications.

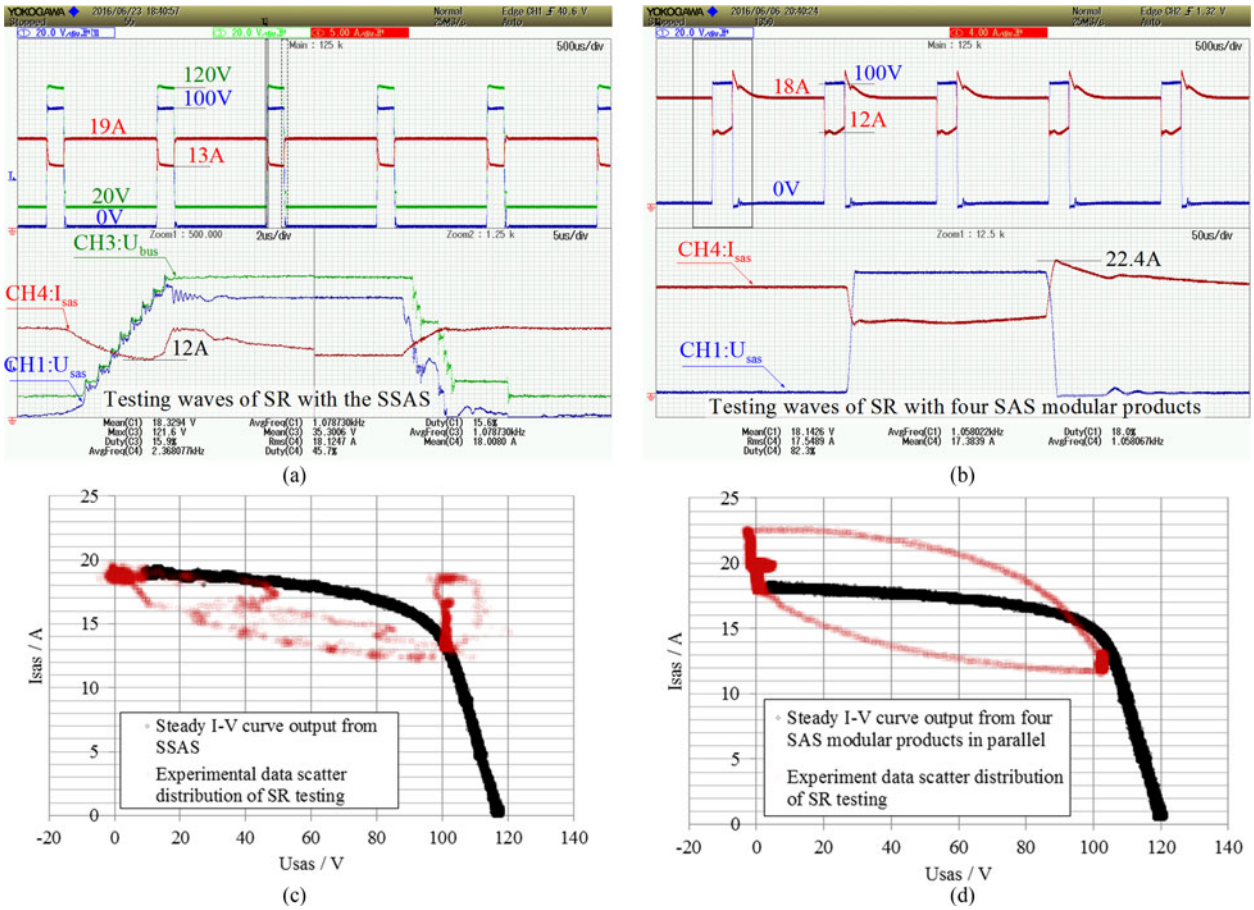

Fig. 17. Experimental results with a shunt switching regulator: (a) time-domain waveform of the SSAS; (b) time-domain waveform of the four SAS modules in parallel; (c) distribution of step switching data in the output steady I-V curve of SSAS; and (d) distribution of step switching data in the output steady I–V curve of SAS modular products.

V. Conclusion

This paper proposed and demonstrated an SSAS system with high-power output capability and high-dynamic performance. The 2.4-kW SSAS could undergo a shunt-switching test from the short-circuit state to the open-circuit state at a stepping frequency of 3 kHz with perfect results; this is the harshest possible working condition for an SAS. Four parallel SAS modular products were also tested under the same working conditions for comparison. The experimental results showed that the proposed SSAS showed better dynamic performance than the SAS modular products. This paper, therefore, provides a state-of-the-art solution for simulating different types of nonlinear I–V curves for both nonterrestrial and territorial applications.

However, it must be acknowledged that the proposed method has several limitations. The first issue is the configuration of the high-power SSAS in a manner suitable for capacitive load applications alone. The bus voltage should track the output voltage of the SSAS, which needs the bus voltage to be sufficiently high to prevent distortion. The second issue is that the actual output I–V curves do not accurately follow the designed I–V curves because of the linear power stage response of the output current. The linear power stage, which consists of 20 current paths used to control the current of the SSAS using a reference voltage, cannot obtain very high control accuracy due to the differences between the different linear current paths. This issue will become increasingly obvious under low-current output conditions. The approaches to realize high accuracy involve adding calibration parameters with the FPGA digital controller and dynamically controlling the number of available linear current paths at different power current outputs. In future studies, we propose to address these issues to enable the SSAS to attain all the properties of an actual solar array panel.

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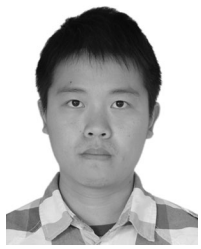

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