17
Line-Commutated Rectifiers

Conventional diode peak-detection rectifiers are inexpensive, reliable, and in widespread use. Their shortcomings are the high harmonic content of their ac line currents, and their low power factors. In this chapter, the basic operation and ac line current waveforms of several of the most common single-phase and three-phase diode rectifiers are summarized. Also introduced are phase-controlled three-phase rectifiers and inverters, and passive harmonic mitigation techniques. Several of the many references in this area are listed at the end of this chapter [1–15].

Rigorous analytical design of line-commutated rectifier and filter circuits is unfeasible for all but the simplest of circuits. Typical peak-detection rectifiers are numerically ill-conditioned, because small changes in the dc-side ripple voltage lead to large changes in the ac line current waveforms. Therefore, the discussions of this chapter are confined to mostly qualitative arguments, with the objective of giving the reader some insight into the physical operation of rectifier/filter circuits. Waveforms, harmonic magnitudes, and power factors are best determined by measurement or computer simulation.

17.1 THE SINGLE-PHASE FULL-WAVE RECTIFIER

A single-phase full-wave rectifier, with uncontrolled diode rectifiers, is shown in Fig. 17.1. The circuit includes a dc-side L–C filter. There are two conventional uses for this circuit. In the traditional full-wave rectifier, the output capacitor is large in value, and the dc output voltage $v(t)$ has negligible ripple at the second harmonic of the ac line frequency. Inductor L is most often small or absent. Additional small inductance may be in series with the ac source $v_g(t)$. A second conventional use of this circuit is in the low-harmonic rectifiers discussed in the next chapter. In this case, the resistive load is replaced by a dc-dc converter that is controlled such that its power input port obeys Ohm's law. For the purposes of understanding the rectifier waveforms, the converter can be modeled by an effective resistance R, as in the cir-

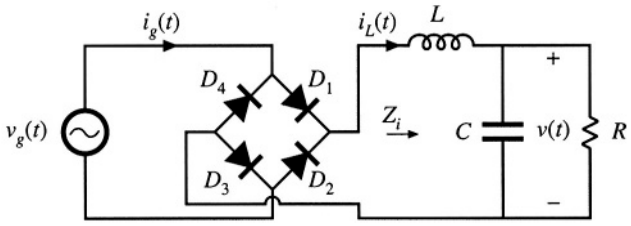

Fig. 17.1 Conventional single-phase full-wave rectifier, with dc-side *L–C* filter

cuit of Fig. 17.1. In this application, the *L–C* filter is required to filter the conducted electromagnetic interference (EMI) generated by the converter. The inductor and capacitor element values are typically small in value, and $v(t)$ is approximately a rectified sinusoid. More generally, there may be several sections of *L–C* filter networks, connected to both the dc and ac sides of the diode rectifier, which filter EMI, smooth the dc output voltage, and reduce the ac line current harmonics.

The presence of any filter degrades the ac current waveform of the rectifier. With no reactive elements ($L = 0$ and $C = 0$), the rectifier presents a purely resistive load to the ac input. The output voltage $v(t)$ is then a rectified sinusoid, there are no ac line current harmonics, and the power factor is unity. Addition of reactive elements between the rectifier diodes and the load leads in general to ac line current harmonics. Given that such a filter is necessary, one might ask what can be done to keep these harmonics as small as possible. In this section, the dependence of the ac line current total harmonic distortion on the filter parameters is described.

The circuit of Fig. 17.1 generates odd harmonics of the ac line voltage in the ac line current. The dc output voltage contains dc and even harmonics of the ac line voltage. The circuit exhibits several modes of operation, depending on the relative values of *L, C,* and *R.* It is easiest to understand these modes by considering the limiting cases, as follows.

17.1.1 Continuous Conduction Mode

When the inductor L is very large, then the inductor current $i_L(t)$ is essentially constant. This follows from the inductor definition $v_L(t) = L di_L(t)/dt$. For a given applied inductor voltage waveform $v_L(t)$, the slope $di_L(t)/dt$ can be made arbitrarily small by making L sufficiently large. In the limiting case where L is infinite, the slope $di_L(t)/dt$ becomes zero, and the inductor current is constant dc. To provide a path for the constant inductor to flow, at least two of the rectifier diodes must conduct at any given instant in time. For the circuit of Fig. 17.1, diodes D_1 and D_3 conduct when the ac line voltage $v_g(t)$ is positive, and D_2 and D_4 conduct when $v_g(t)$ is negative. The ac line current waveform is therefore a square wave, with $i_g(t) = i_L(t)$ when $v_g(t)$ is positive, and $i_g(t) = -i_L(t)$ when $v_g(t)$ is negative. The diode conduction angle β, defined as the angle through which one of the diodes conducts, is equal to 180° in CCM.

The rms value of a square wave is equal to its peak value I_{pk}, in this case the dc load current. The fundamental component of a square wave is equal to $4I_{pk}/\pi$, The square-wave contains odd harmonics which vary as $1/n$. The distortion factor is therefore

$$\text{distortion factor} = \frac{I_{1,rms}}{I_{rms}} = \frac{4}{\pi\sqrt{2}} = 90.0\% \qquad (17.1)$$

The total harmonic distortion is

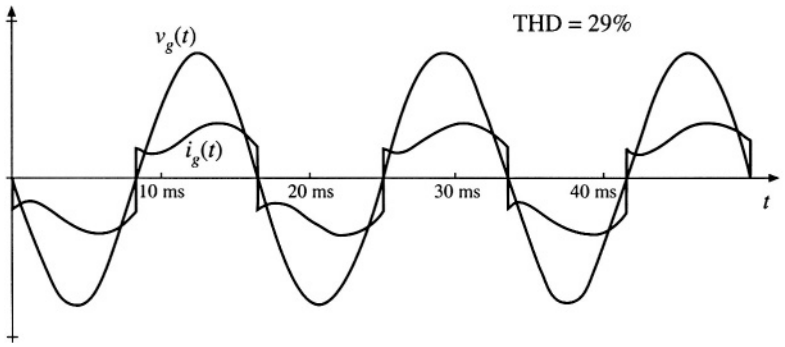

Fig. 17.2 Typical ac line current and voltage waveforms, continuous conduction mode. $f_0/f_L = 5$, $Q = 0.25$.

$$\text{THD} = \sqrt{\left(\frac{1}{\text{distortion factor}}\right)^2 - 1} = 48.3\% \tag{17.2}$$

So the limiting case of the large inductor leads to some significant harmonic distortion, although it is not as bad as the peak detection rectifier case. Since the square wave is in phase with the ac input voltage, the displacement factor is unity, and hence the power factor is equal to the distortion factor.

Whenever the inductor is sufficiently large, the rectifier diodes conduct continuously (i.e., there is no time interval in which all four diodes are reverse-biased). This is called the continuous conduction mode (CCM). A typical ac line current waveform is plotted in Fig. 17.2 for a finite but large value of L. It can be seen that the ac line current is discontinuous at the ac line voltage zero crossing, as in the square-wave limiting case. Some ringing is also present. This waveform contains a total harmonic distortion of approximately 29%.

17.1.2 Discontinuous Conduction Mode

The opposite case occurs when the inductor is very small and the capacitor C is very large. This is the peak detector circuit. In the limit as L goes to zero and C goes to infinity, the ac line current approaches a string of delta (impulse) functions that coincide with the peaks of the sinusoidal input voltage waveform. It can be shown that, in this limiting case, the THD becomes infinite while the distortion factor and power factor become zero. Of course, in the practical case the current is not infinite; nonetheless, large THD with low power factor is quite possible. The diodes conduct for less than one-half of the ac line period, and hence $\beta < 180^\circ$ in DCM.

Whenever the capacitor is large and the inductor is small, the rectifier tends to "peak detect," and the rectifier operates in the discontinuous conduction mode (DCM). There exist time intervals of nonzero length where all four rectifier diodes are reverse-biased. A typical set of waveforms is plotted in Fig. 17.3, where the capacitor is large but finite, and the inductor is small but nonzero. The ac line voltage and the value of the load resistance are the same as in Fig. 17.2, yet the peak current is substantially larger. The THD for this waveform is 145%, and the distortion factor is 57%.

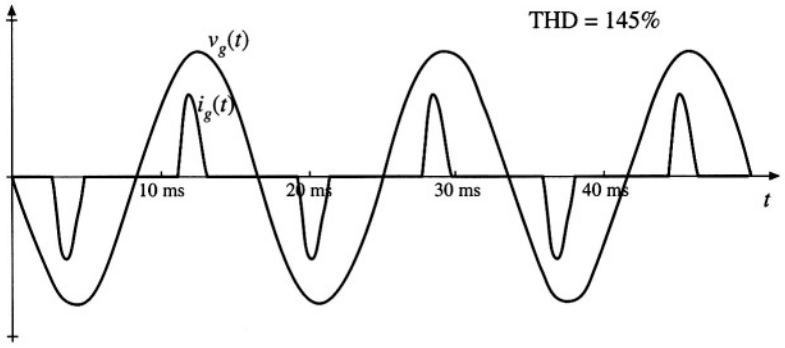

Fig. 17.3 Typical ac line current and voltage waveforms, discontinuous conduction mode. $f_0/f_L = 8.4$, $Q = 121$.

17.1.3 Behavior When *C* is Large

A variety of authors have discussed the solution of passive rectifier circuits; several works are listed in the references [8–15]. Analysis of even the simple circuit of Fig. 17.1 is surprisingly complex. For the case when *C* is infinite, it was shown in [8] that the rectifier waveshapes can be expressed as a function of a single dimensionless parameter K_L, defined as

$$K_L = \frac{2L}{RT_L} \tag{17.3}$$

where $T_L = 1/f_L$ is the ac line period. Equation (17.3) is of the same form as Eq. (5.6), used to define the dimensionless parameter *K* which governs the DCM behavior of PWM converters. Figure 17.4 illustrates the behavior of the single-phase rectifier circuit of Fig. 17.1, as a function of K_L and for infinite *C* [8]. When K_L is greater than approximately 0.1, the rectifier operates in CCM, with waveforms similar to those in Fig. 17.2.

The voltage conversion ratio *M* is defined as

$$M = \frac{V}{V_m} \tag{17.4}$$

where V_m is the peak value of the sinusoidal ac input voltage. In CCM, the output voltage is ideally independent of load, with $M = 2/\pi$. Addition of ac-side inductance can cause the output voltage to exhibit a dependence on load current. The total harmonic distortion in CCM is nearly constant and equal to the value given by Eq. (17.2).

Near the boundary between CCM and DCM, the fundamental component of the line current significantly lags the line voltage. The displacement factor reaches a minimum value slightly less than 80%, and power factors between 70% and 80% are observed.

For $K_L \ll 0.1$, the rectifier operates heavily in DCM, as a peak-detection rectifier. As K_L is decreased, the displacement factor approaches unity, while the THD increases rapidly. The power factor is dominated by the distortion factor. The output voltage becomes dependent on the load, and hence the rectifier exhibits a small but nonzero output impedance.

For K_L less than approximately 0.05, the waveforms are unchanged when some or all of the inductance is shifted to the ac side of the diode bridge. Figure 17.4 therefore applies to rectifiers contain-

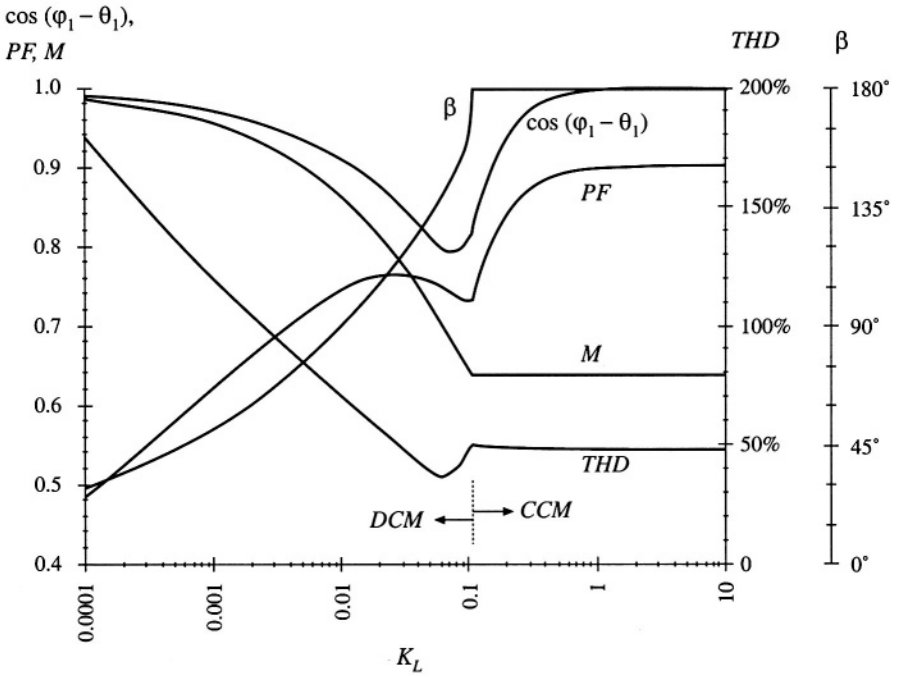

Fig. 17.4 Diode conduction angle β, displacement factor, power factor, conversion ratio, and total harmonic distortion of the rectifier circuit of Fig. 17.1, with infinite capacitance.

ing both ac-side and dc-side inductance, provided that the circuit operates sufficiently deeply in DCM. The parameter K_L is computed according to Eq. (17.3), with L taken to be the total ac-side plus dc-side inductance. A common example is the case where the circuit contains no physical discrete inductor; the performance is then determined by parasitic elements such as the capacitor equivalent series inductance, the inductance of the utility distribution wiring, and transformer leakage inductances.

17.1.4 Minimizing THD When *C* is Small

Let us now consider the performance of the second case, in which the inductor and capacitor are small and are intended solely to prevent load-generated EMI from reaching the ac line. In this case, dc-side filtering of the low-frequency even voltage harmonics of the ac line frequency is not necessary. The filter can be characterized by a corner frequency f_0, characteristic impedance R_0, and Q-factor, where

$$\begin{aligned} f_0 &= \frac{1}{2\pi\sqrt{LC}} \\ R_0 &= \sqrt{\frac{L}{C}} \\ Q &= \frac{R}{R_0} \\ f_p &= \frac{1}{2\pi RC} = \frac{f_0}{Q} \end{aligned} \tag{17.5}$$

To obtain good filtering of the EMI, the corner frequency f_0 should be selected to be sufficiently low. However, as can be seen from Eq. (17.5), reducing the value of f_0 requires increasing the values of L and/or C. As described above, it is undesirable to choose either element value too large, because large distortion results. So f_0 should not be too low, and there is a limit to the amount of filtering that can be obtained without significantly distorting the ac line current waveform.

How low can f_0 be? Once f_0 is chosen, how should L and C be chosen such that THD is minimized? We might expect that THD is increased when the phase of the filter input impedance $-Z_i(j\omega)$, evaluated at the second harmonic of the line frequency or $2f_L$, differs significantly from 0°. When the zero crossings of the voltage and current waveforms do not coincide, then diode switching distorts the current waveform. To a lesser extent, input impedance phase shift at the higher-order even harmonic frequencies of the ac line frequency should also affect the THD. The input impedance $Z_i(s)$ contains two zeroes at frequency f_0, and a pole at frequency $f_p = f_0/Q$. To obtain small phase shift at low frequency, f_0 must be sufficiently large. In addition, Q must be neither too small nor too large: small Q causes the zeroes at f_0 to introduce low-frequency phase shift, while large Q causes the pole at f_p to occur at low frequency.

An approximate plot of THD vs. the choice of f_0 and Q is given in Fig. 17.5. It can be seen that there is an optimum choice for Q: minimum THD occurs when Q lies in the range 0.5 to 1. A typical waveform is plotted for the choice $f_0/f_L = 10$, $Q = 1$, in Fig. 17.6. The THD for this waveform is 3.6%, and the distortion factor is 99.97%.

Small Q corresponds to CCM operation, with large L and small C. In the extreme case as $Q \to 0$, the ac line current tends to a square wave with THD = 48%. Large Q corresponds to DCM operation, with small L and large C. In the extreme case as $Q \to \infty$, the ac line current tends to a string of delta functions with $\text{THD} \to \infty$. The optimum choice of Q leads to operation near the CCM-DCM boundary, such that the ac line current waveform contains neither step changes nor subintervals of zero current.

In the case when the load resistance R varies over a wide range of values, it may be difficult to optimize the circuit such that low THD is always obtained. It can be seen that increasing f_0/f_L leads to low THD for a wider range of load resistance. For example, when $f_0 = 5f_L$, $\text{THD} \leq 10\%$ can be obtained only for Q between approximately 0.6 and 1.5, which is a 2.5:1 range of load resistance variations. If the

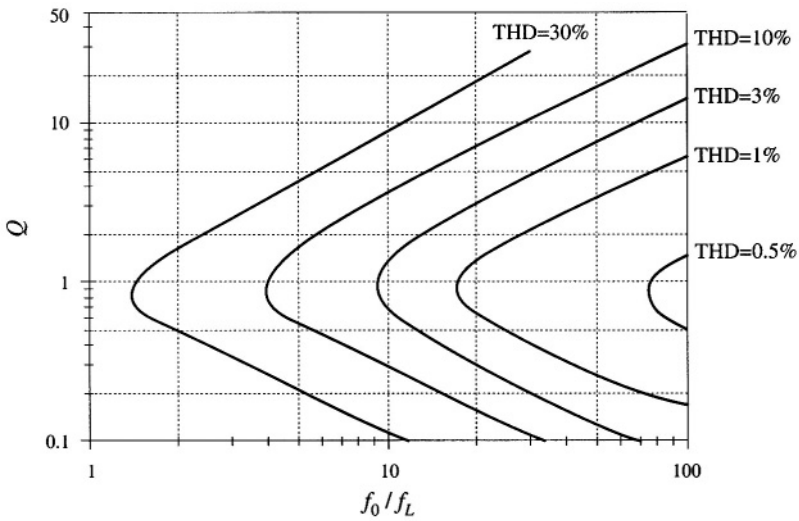

Fig. 17.5 Approximate total harmonic distortion of the single-phase diode rectifier with dc-side L–C filter.

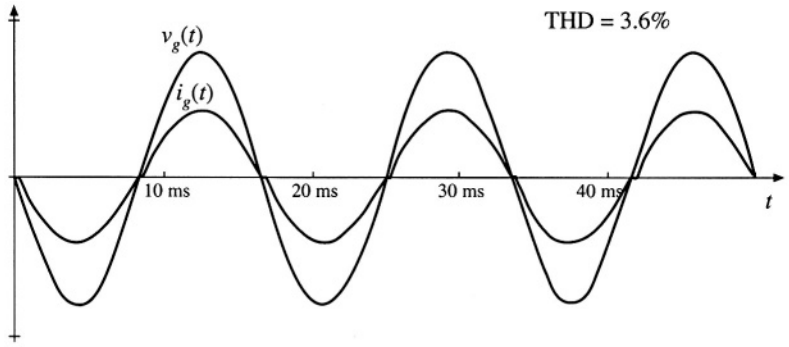

Fig. 17.6 Typical ac line current and voltage waveforms, near the boundary between continuous and discontinuous modes and with small dc filter capacitor. $f_0/f_L = 10$, $Q = 1$.

filter cutoff frequency f_0 is increased to $20f_L$, then THD $\leq 10\%$ is obtained for Q between approximately 0.15 and 7, or nearly a 50:1 range of resistance variations. In most cases, maximum harmonic limits are enforced only at full load, and hence it is possible to design with relatively low values of f_0/f_L if desired.

17.2 THE THREE-PHASE BRIDGE RECTIFIER

A basic full-wave three-phase uncontrolled rectifier with LC output filter is shown in Fig. 17.7. Its behavior is similar to the single-phase case, in that it exhibits both continuous and discontinuous conduction modes, depending on the values of L and C. The rectifier generates odd non-triplen harmonics in the ac line current. So the ac line current may contain 1^{st}, 5^{th}, 7^{th}, 11^{th}, 13^{th}, etc. harmonics. The dc output may contain dc and even triplen harmonics: 0, 6, 12, 18, etc.

In the basic circuit of Fig. 17.7, no more than two of the six diodes can conduct during each interval, and hence the line current waveforms must contain intervals of nonzero length during which the current is zero. Unlike the single-phase case, the ac line current waveform must contain distortion even when the filter elements are removed.

17.2.1 Continuous Conduction Mode

In the continuous conduction mode, each ac line current is nonzero for 120 degrees out of each line half-cycle. For the remaining 60 degrees, the current is zero. This mode occurs when the inductance L is suf-

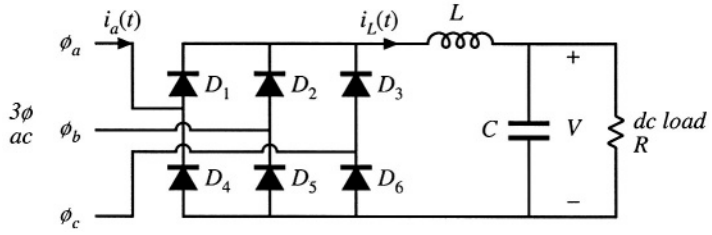

Fig. 17.7 Basic uncontrolled 3ø bridge rectifier circuit, with dc-side L–C filter.

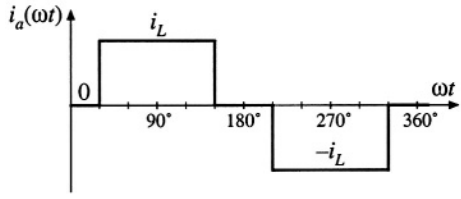

Fig. 17.8 Ac line current waveform $i_a(t)$, for the case when inductor L is large. The phase is drawn with respect to the zero crossing of the line-to-neutral voltage $v_{an}(t)$.

ficiently large, as well as when the filter elements L and C are removed entirely.

In the limit, when L is very large, then the current $i_L(t)$ is essentially constant. The current in phase a, $i_a(t)$, is then as shown in Fig. 17.8. It can be shown that the Fourier series for this waveform is

$$i_a(t) = \sum_{n=1,5,7,11,\ldots}^{\infty} \frac{4}{n\pi} I_L \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \sin(n\omega t) \tag{17.6}$$

which is similar to the spectrum of the square wave of the single-phase case, but with the triplen harmonics missing. The THD of this waveform is 31%, and the distortion factor is $3/\pi = 95.5\%$. As in the case of the square wave, the amplitude of the odd nontriplen n^{th} harmonic is $(1/n)$ times the fundamental amplitude. So this waveform contains 20% fifth harmonic, 14% seventh harmonic, 9% eleventh harmonic, etc. It is interesting that, in comparison with the square-wave single-phase case, the missing 60° in the three-phase case improves the THD and power factor, by removing the triplen harmonics.

With a less-than-infinite value of inductance, the output ripple causes the ac line currents to be rounded, as in the typical waveform of Fig. 17.9. This waveform has a 31.9% THD, with a distortion factor that is not much different from the waveform of Fig. 17.8.

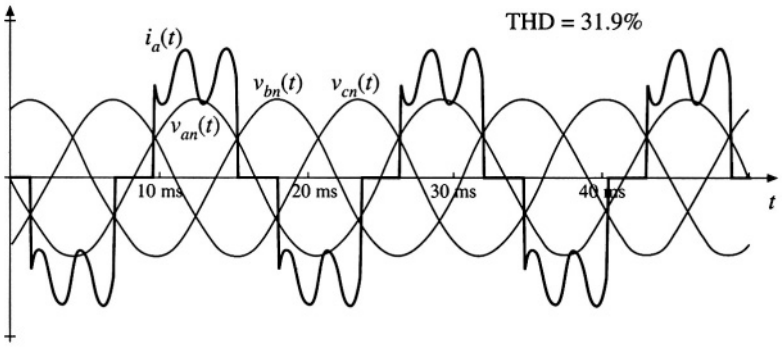

Fig. 17.9 Continuous conduction mode ac line-neutral voltages and phase a current, for a moderate value of inductance.

17.2.2 Discontinuous Conduction Mode

If the inductance is further reduced, then the three-phase rectifier enters the discontinuous conduction mode. The rectifier then begins to peak-detect, and the current waveforms become narrow pulses of high amplitude, occurring near the peaks of the line-line voltages. The phase a line current $i_a(t)$ contains two positive and two negative pulses, at the positive and negative peaks of the line-line voltages $v_{ab}(t)$ and $v_{ac}(t)$. As in the single-phase case, the total harmonic distortion becomes quite large in this case, and the

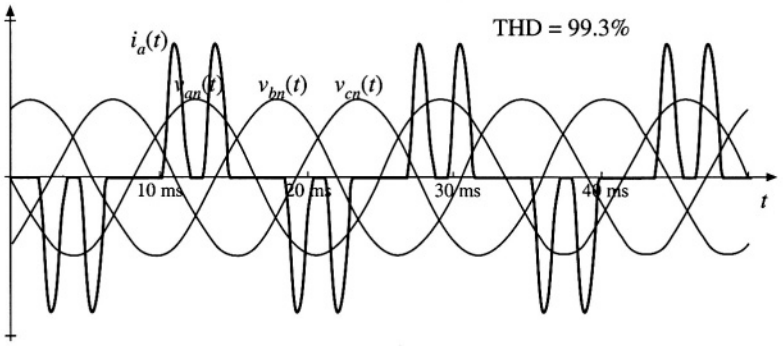

Fig. 17.10 Discontinuous conduction mode ac line-neutral voltages and phase *a* current.

power factor can be significantly degraded.

A typical waveform is given in Fig. 17.10. This waveform has a THD of 99.3%, and a distortion factor of 71%. This would be considered unacceptable in high-power applications, except perhaps at light load.

17.3 PHASE CONTROL

There are a wide variety of schemes for controlling the dc output of a 3ø rectifier using thyristors [1,2]. The most common one is shown in Fig. 17.11, in which the six diodes of Fig. 17.7 are replaced by silicon controlled rectifiers (SCRs). Typical waveforms are given in Fig. 17.12, for large dc-side filter inductance.

If Q_1 were an uncontrolled diode, it would conduct whenever the line-to-line voltage v_{ab} or v_{ac} is the largest in magnitude of the six line-line voltages v_{ab}, v_{bc}, v_{ca}, v_{ba}, v_{cb}, and v_{ca}. This occurs for 120° of each cycle, beginning at the point where $v_{ab} = v_{cb}$. In Fig. 17.12, this occurs at $\omega t = 60°$. The output voltage of the controlled rectifier is controlled by delaying the firing of Q_1 by an angle α, such that Q_1 begins conducting at $\omega t = 60° + \alpha$. This has the effect of reducing the dc output voltage.

There can be no dc component of voltage across inductor *L*. Hence, in steady-state, the dc component of the rectifier output voltage $v_R(t)$ must equal the dc load voltage *V*. But $v_R(t)$ is periodic, with period equal to six times the ac line period (or 60°). So the dc component of $v_R(t)$ can be found by Fourier analysis, and is equal to the average value of $v_R(t)$. Over one 60° interval, for example $(60° + \alpha) \le \omega t \le (120° + \alpha)$, $v_R(t)$ follows the line-line voltage $v_{ab}(t) = 3V_m \sin(\omega t + 30°)$. The average is therefore

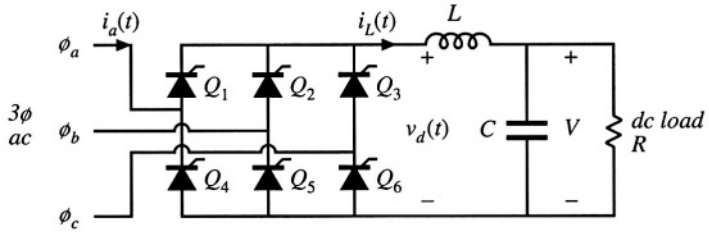

Fig. 17.11 Basic controlled 3ø bridge rectifier circuit, with dc-side *L–C* filter.

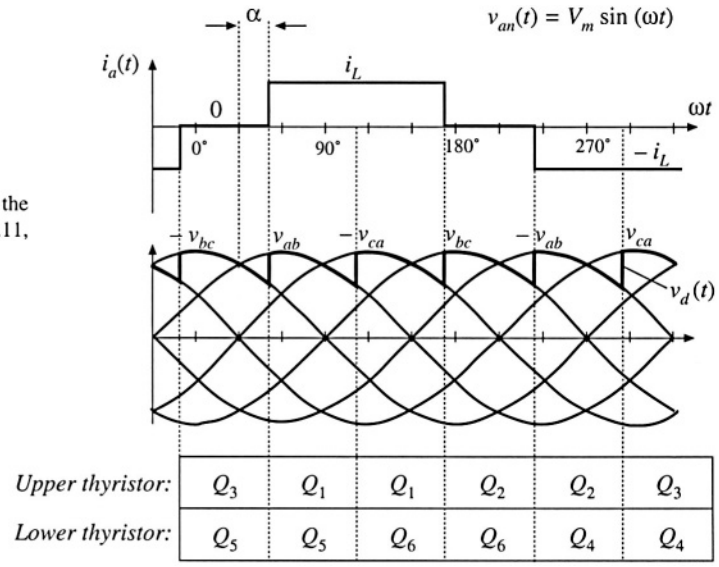

Fig. 17.12 Waveforms for the controlled rectifier of Fig. 17.11, with large dc filter inductance.

$$V = \frac{3}{\pi}\int_{30^\circ+\alpha}^{90^\circ+\alpha} \sqrt{3}\, V_m \sin(\theta + 30^\circ)\, d\theta$$
$$= \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \cos\alpha \qquad (17.7)$$

where $V_{L\text{-}L,\,rms}$ is the rms line-to-line voltage. This equation is plotted in Fig. 17.13. It can be seen that, if it is necessary to reduce the dc output voltage to values close to zero, then the delay angle α must be

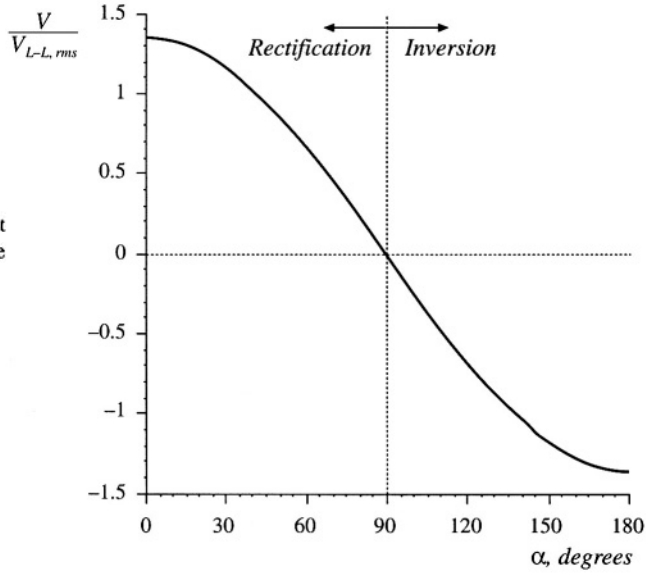

Fig. 17.13 Variation of the dc output voltage V with delay angle α, for the phase-controlled circuit of Fig. 17.11.

increased to close to 90°. With a small inductance, the controlled rectifier can also operate in discontinuous conduction mode, with modified output voltage characteristics.

17.3.1 Inverter Mode

If the dc load is capable of supplying power, then it is possible for the direction of power flow to reverse. For example, consider the three-phase controlled rectifier circuit of Fig. 17.14. The resistive load is replaced by a voltage source and thevenin-equivalent resistance, capable of either supplying or consuming power. The dc load power is equal to VI_L, which is positive (rectifier mode) when both V and I_L are positive. The thyristor is a unidirectional-current switch, which cannot conduct negative current, and hence I_L must always be positive. However, it is possible to cause the output voltage V to be negative, by increasing the delay angle α. The dc load power VI_L then becomes a negative quantity (inverter mode), meaning that power flows from the dc load into the 3øac system.

Provided that the dc-side filter inductance L is sufficiently large, then Eq. (17.7) is valid even when the delay angle α is greater than 90°. It can be seen in Fig. 17.13 that the dc output voltage V becomes negative for $\alpha > 90^\circ$, and hence the power flow indeed reverses. Delay angles approaching 180° are possible, with the maximum angle limited by commutation of the thyristor devices.

17.3.2 Harmonics and Power Factor

Let us next consider the harmonic content and power factor of the phase-controlled rectifier with large inductance. Comparison of the line current waveform of Fig. 17.12 with that of the uncontrolled rectifier (Fig. 17.8) reveals that the waveshapes are identical. The only difference is the phase lag α present in the phase-controlled rectifier. This has the effect of shifting the fundamental component of current (and the harmonics as well) by angle α. The Fourier series is therefore

$$i_a(t) = \sum_{n=1,5,7,11,\ldots}^{\infty} \frac{4}{n\pi} I_L \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \sin\left(n\omega t - n\alpha\right) \tag{17.8}$$

Hence the harmonic amplitudes are the same (the fifth harmonic amplitude is 20% of the fundamental, etc.), the THD is again 31%, and the distortion factor is again 95.5%. But there is phase lag in the fundamental component of current, which leads to a displacement factor of $\cos(\alpha)$. The power factor is therefore

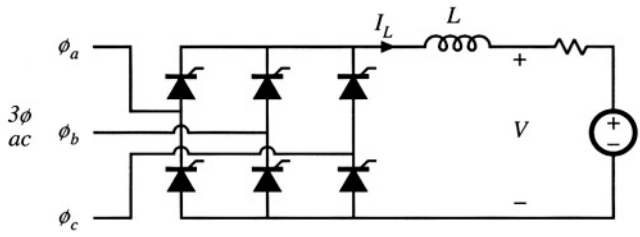

Fig. 17.14 If the load is capable of supplying power, then the 3ø bridge circuit functions as an inverter for $V < 0$ and $\alpha > 90^\circ$.

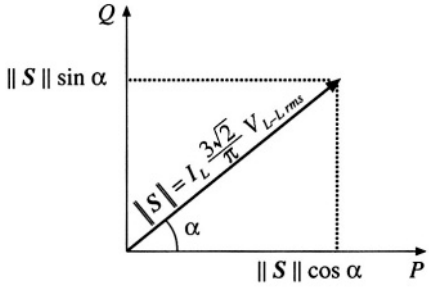

Fig. 17.15 Fundamental component complex power diagram for the 3ø bridge circuit operating in rectifier mode.

$$\text{power factor} = 0.955\,|\cos(\alpha)| \tag{17.9}$$

which can be quite low when the dc output voltage V is low.

It is at first somewhat puzzling that the introduction of phase control can cause the fundamental current to lag the voltage. Apparently, the rectifier consumes reactive power equal to

$$Q = \sqrt{3}\, I_{a,\,rms} V_{L\text{-}L,\,rms} \sin\alpha = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \sin\alpha \tag{17.10}$$

We normally associate lagging current and the consumption of reactive power with inductive energy storage. But this is not what is happening in the rectifier; indeed, the inductor and capacitor can be removed entirely from the rectifier circuit, and a lagging fundamental current is still obtained by phase control. It is simply the delay of the switching of the rectifiers that causes the current to lag, and no energy storage is involved. So two mechanisms cause the phase-controlled rectifier to operate with low power factor: the lagging fundamental component of current, and the generation of current harmonics.

Equation (17.10) can be further interpreted. Note that the dc output power P is equal to the dc inductor current I_L times the dc output voltage V. By use of Eq. (17.7), this can be written

$$P = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \cos\alpha \tag{17.11}$$

Comparison of Eqs. (17.10) and (17.11) reveals that the rectifier fundamental volt-amperes can be expressed using the conventional concepts of complex power $S = P + jQ$, where P is the real (average) power consumed and Q is the fundamental reactive power consumed. The complex power phasor diagram, treating the fundamental components only, is illustrated in Fig. 17.15.

17.3.3 Commutation

Let's consider next what happens during the switching transitions. In the phase-controlled rectifier circuit of Fig. 17.16, the dc-side inductor L_d is large in value, such that its current ripple is negligible. Inductors L_a, L_b, and L_c are also present in the ac lines; these may be physical inductors of the rectifier circuit, or they may represent the source impedance of the power system, typically the leakage inductances of a nearby transformer. These inductors are relatively small in value.

Consider the switching transition illustrated in Fig. 17.17. Thyristors Q_3 and Q_5 initially conduct. At time t_{c1}, thyristor Q_1 is gated on, and the dc current i_L begins to shift from Q_3 to Q_1. The ac line currents $i_a(t)$ and $i_c(t)$ cannot be discontinuous, since inductors L_a and L_c are present in the lines. So dur-

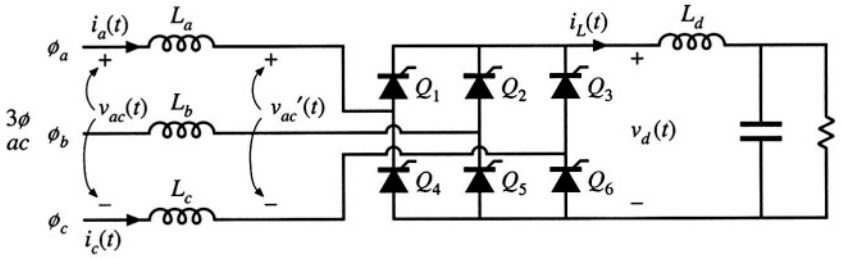

Fig. 17.16 Controlled 3ø rectifier circuit, with small ac-side inductances.

ing the interval $t_{c1} < t < t_{c2}$, thyristors Q_1 and Q_3 both conduct, and the voltage v_{ac}' is zero. Voltage is applied across inductors L_a and L_c, causing their currents to change; for successful commutation, sufficient volt-seconds must be applied to cause the currents to change from i_L to zero, and vice versa. Any stored charge that remains in thyristor Q_3 when current $i_c(t)$ reaches zero must also be removed, and hence $i_c(t)$ actually continues negative as discussed in Chapter 4. When the reverse recovery process of Q_3 is complete, then Q_3 is finally in the off-state, and the next subinterval begins with the conduction of thyristors Q_1 and Q_5.

The commutation process described above has several effects on the converter behavior. First, it can be seen that the thyristor bridge dc-side voltage $v_d(t)$ is reduced in value during the commutation interval. Hence, its average value $\langle v_d \rangle$ and the dc output voltage V are reduced. The amount of reduction is dependent on the dc load current: a larger dc load current leads to a longer commutation interval, and hence to a greater reduction in $\langle v_d \rangle$. So the rectifier has an effective output resistance. Second, the maximum value of the delay angle α is limited to some value less than 180°. If α exceeds this limit, then insufficient volt-seconds are available to change inductor current $i_c(t)$ from i_L to zero, leading to *commutation failure*. Third, when the rectifier ac-side inductors are small or zero, so that L_a, L_b, and L_c represent

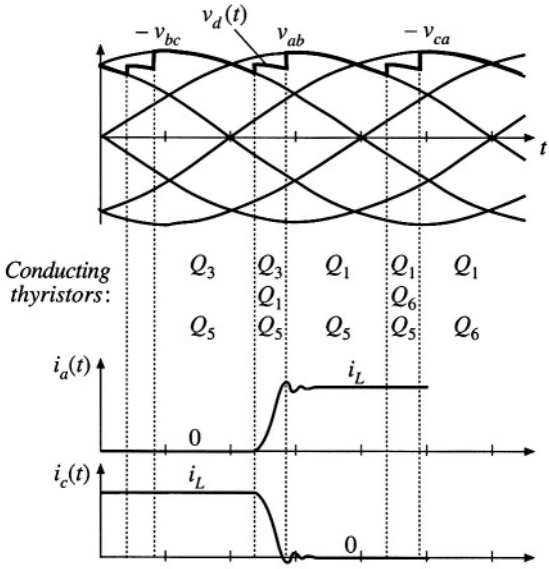

Fig. 17.17 Switching transition waveforms, for the rectifier of Fig. 17.16.

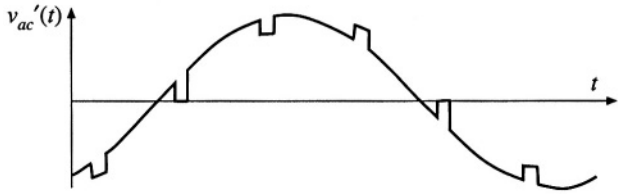

Fig. 17.18 Notching of the ac line-line voltage waveforms during the commutation intervals.

essentially only the power system source impedance, then commutation causes significant notching of the ac voltage waveforms (Fig. 17.18) at the point of common coupling of the rectifier to the power system. Other elements connected locally to the power system will experience voltage distortion. Limits for the areas of these notches are suggested in IEEE/ANSI standard 519.

17.4 HARMONIC TRAP FILTERS

Passive filters are often employed to reduce the current harmonics generated by rectifiers, such that harmonic limits are met. The filter network is designed to pass the fundamental and to attenuate the significant harmonics such as the fifth, seventh, and perhaps several higher-order odd nontriplen harmonics. Such filters are constructed using resonant tank circuits tuned to the harmonic frequencies. These networks are most commonly employed in balanced three-phase systems. A schematic diagram of one phase of the filter is given in Fig. 17.19.

The ac power system is modeled by the thevenin-equivalent network containing voltage source v_s and impedance Z_s'. Impedance Z_s' is usually inductive in nature, although resonances may occur due to nearby power-factor-correction capacitors. In most filter networks, a series inductor L_s' is employed; the filter is then called a harmonic trap filter. For purposes of analysis, the series inductor L_s' can be lumped into Z_s', as follows:

$$Z_s(s) = Z_s'(s) + sL_s' \tag{17.12}$$

The rectifier and its current harmonics are modeled by current source i_r. Shunt impedances $Z_1, Z_2, \ldots$ are

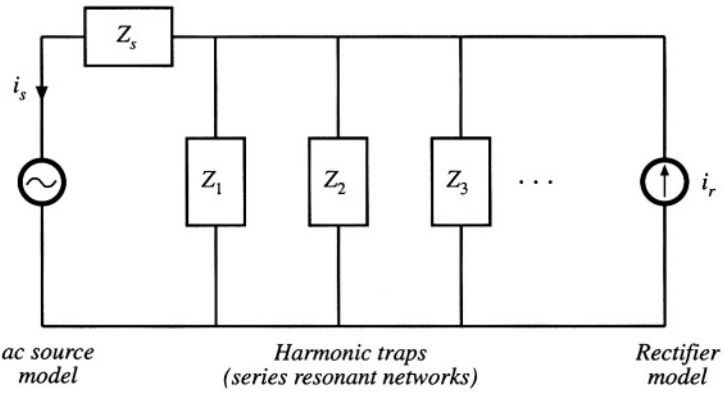

Fig. 17.19 A harmonic trap filter. One phase is illustrated, on a line-to-neutral basis.

tuned such that they have low impedance at the harmonic frequencies, and hence the harmonic currents tend to flow through the shunt impedances rather than into the ac power system.

The approximate algebra-on-the-graph method described in Chapter 8 is used here to construct the filter transfer function, in terms of impedance Z_s and the shunt impedances $Z_1, Z_2, \ldots$. This approach yields a simple intuitive understanding of how the filter operates. Since the harmonic frequencies are close in value, the pole and zero frequencies of the filter are never well separated in value. So the approximate algebra-on-the-graph method is, in general, not sufficiently accurate for the complete design of these filters, and the pole frequencies must be found by numerical methods. A typical design approach might involve estimating element values using the algebra-on-the-graph method, then refining the values using a computer simulation package.

The filter transfer function $H(s)$ is given by the current divider ratio

$$H(s) = \frac{i_s(s)}{i_r(s)} = \frac{Z_1 \parallel Z_2 \parallel \cdots}{Z_s + Z_1 \parallel Z_2 \parallel \cdots} \tag{17.13}$$

As discussed in Chapter 8, another way to write this transfer function is

$$H(s) = \frac{i_s(s)}{i_r(s)} = \frac{Z_s \parallel Z_1 \parallel Z_2 \parallel \cdots}{Z_s} \tag{17.14}$$

So we can construct $H(s)$ by first constructing the parallel combination $Z_s \parallel Z_1 \parallel Z_2 \parallel \ldots$, then dividing by the total line impedance Z_s. It can be shown that, if $Z_s(s)$ contains no poles, then the numerator of $H(s)$ is the product of the zeroes of the shunt impedances $Z_1, Z_2, \ldots$. So this graphical method yields the exact zeroes of $H(s)$, which coincide with the series resonances of the shunt impedances. But the poles of $H(s)$, which arise from parallel resonances in the filter, require more work to compute.

Let us first consider the simple case illustrated in Fig. 17.20, where Z_1 consists of a series resonant circuit tuned to eliminate the fifth harmonic, and Z_s is composed of a single inductor L_s. Construction of the impedance of a series resonant network is described in Chapter 8. The $\parallel Z_1 \parallel$ asymptotes follow the capacitor impedance magnitude $1/\omega C_1$ at low frequency, and the inductor impedance magnitude ωL_1 at high frequency. At the resonant frequency, $\parallel Z_1 \parallel$ is equal to R_1. The asymptotes for $\parallel Z_1 \parallel$ are constructed in Fig. 17.21 (a).

Figure 17.21 (a) also illustrates the impedance magnitude $\parallel Z_s \parallel = \omega L_s$, as well as construction of

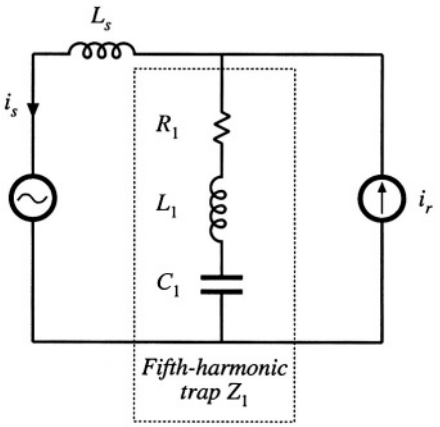

Fig. 17.20 Simple harmonic trap filter example, containing a series resonant trap tuned to the fifth harmonic, and inductive line impedance.

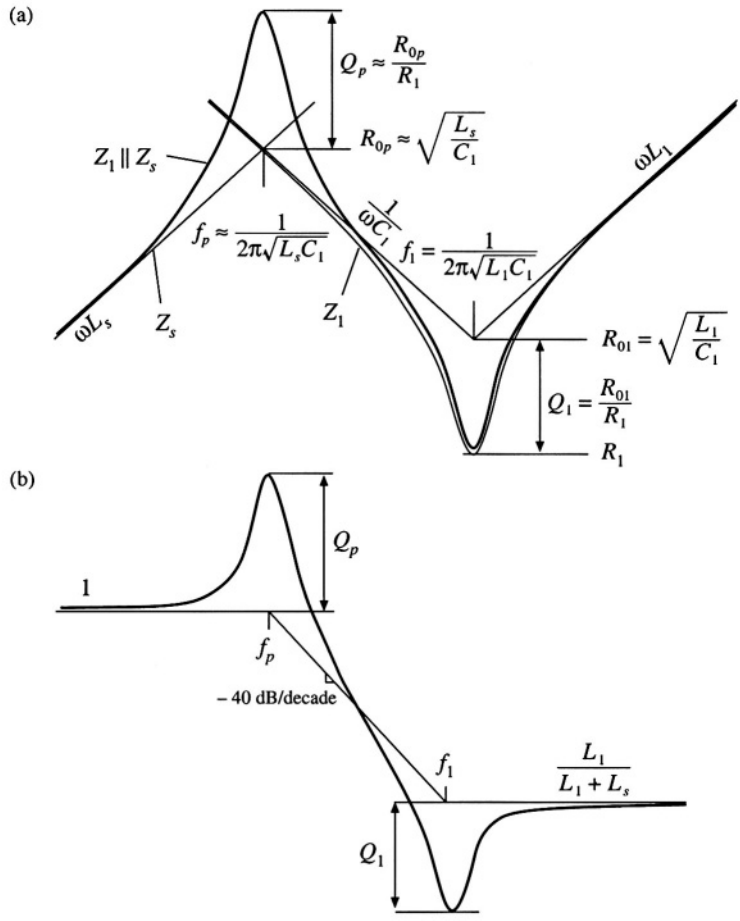

Fig. 17.21 Construction of approximate frequency response using the algebra-on-the-graph method: (a) impedance asymptotes, (b) transfer function asymptotes $\| H \|$.

the approximate asymptotes for the parallel combination $(Z_s \| Z_1)$. Recall that, to construct the approximate asymptotes for the parallel combination, we simply select the smaller of the Z_s and Z_1 asymptotes. The result is the shaded set of asymptotes shown in the figure: the parallel combination follows ωL_s at low frequency, and $\| Z_1 \|$ at high frequency. Note that, in addition to the intended series resonance at frequency f_1, a parallel resonance occurs at frequency f_p.

The filter transfer function $\| H(s) \|$ is now constructed using Eq. (17.14). As illustrated in Fig. 17.21(b), $\| H(s) \| = 1$ at low frequencies where both the numerator and the denominator of Eq. (17.14) are equal to ωL_s. The parallel resonance at frequency f_p leads to resonant poles and peaking in $\| H(s) \|$. The resonance at frequency f_1 leads to resonant zeroes and attenuation in $\| H(s) \|$. At high frequency, the gain is $L_1/(L_1 + L_s)$.

So if we want to attenuate fifth harmonic currents, we should choose the element values such that the series resonant frequency f_1 coincides with the fifth harmonic frequency. This frequency is sim-

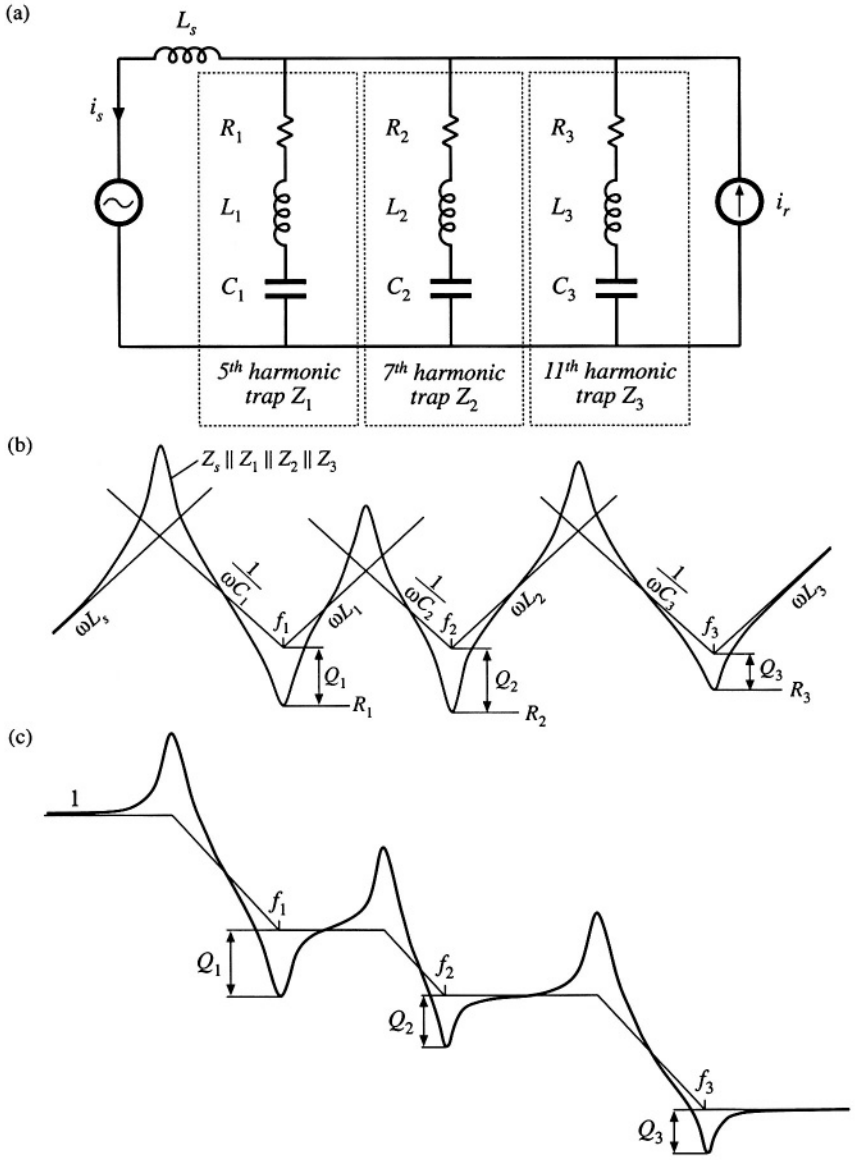

Fig. 17.22 Construction of approximate frequency response for a harmonic trap filter that attenuates the fifth, seventh, and eleventh harmonics: (a) impedance asymptotes, (b) transfer function asymptotes.

ply the resonant frequency of the shunt impedance Z_1, or

$$f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{17.15}$$

In addition, care must be exercised regarding the parallel resonance. Since no three-phase system is exactly balanced, small amounts of third harmonic currents always occur. These currents usually have negligible effect; however, the parallel resonance of the harmonic trap filter can increase their magnitudes significantly. Even worse, the Q-factor of the parallel resonance, Q_p, is greater than the series-resonance Q-factor Q_1.

The filter circuit of Fig. 17.20 is simple enough that an exact analysis can be performed easily. The exact transfer function is

$$H(s) = \frac{\left(1 + \frac{s}{\omega_1 Q_1} + \left(\frac{s}{\omega_1}\right)^2\right)}{\left(1 + \frac{s}{\omega_p Q_p} + \left(\frac{s}{\omega_p}\right)^2\right)} \tag{17.16}$$

where

$$f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi\sqrt{L_1 C_1}} \qquad f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\sqrt{(L_1 + L_s)C_1}}$$

$$Q_1 = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \qquad Q_p = \frac{1}{R_1}\sqrt{\frac{(L_1 + L_s)}{C_1}}$$

The resonant zeroes do indeed appear at the series resonant frequency, while the parallel resonance and its associated resonant poles appear at frequency f_p determined by the series combination of L_1 and L_p.

To attenuate several harmonics—for example, the fifth, seventh, and eleventh—series resonant networks can be tuned to provide resonant zeroes at each. A circuit is given in Fig. 17.22(a), with the impedance asymptotes of Fig. 17.22(b). The resulting approximate $\| H(s) \|$ is given in Fig. 17.22(c). It can be seen that, associated with each series resonance is a parallel resonance. Each parallel resonant frequency should be chosen such that it is not significantly excited by harmonics present in the network.

The filter transfer function can be given high-frequency single-pole rolloff by addition of a bypass resistor R_{bp}, as illustrated in Fig. 17.23(a). Typical impedance and transfer function asymptotes for this network are constructed in Fig. 17.24. The bypass resistor allows some additional attenuation of the higher-order harmonics, without need for series resonant traps tuned to each harmonic. The network of Fig. 17.23(a) is sometimes called a "high pass" network, because it allows high-frequency currents to flow through the shunt branch. But it causes the overall filter transfer function $H(s)$ to reject high frequencies. A simple harmonic trap filter that contains series resonances that can be tuned to the fifth and

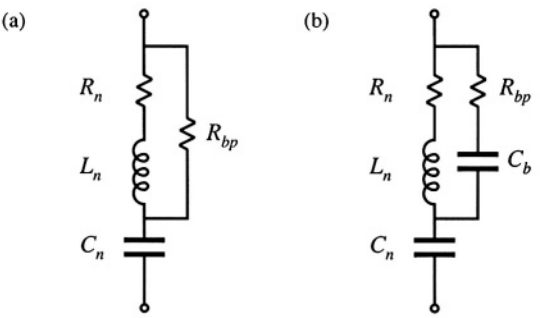

Fig. 17.23 Addition of bypass resistor R_{bp} to a series resonant network, to obtain a high-frequency rolloff characteristic: (a) basic circuit, (b) addition of blocking capacitor C_b to reduce power consumption at the fundamental frequency.

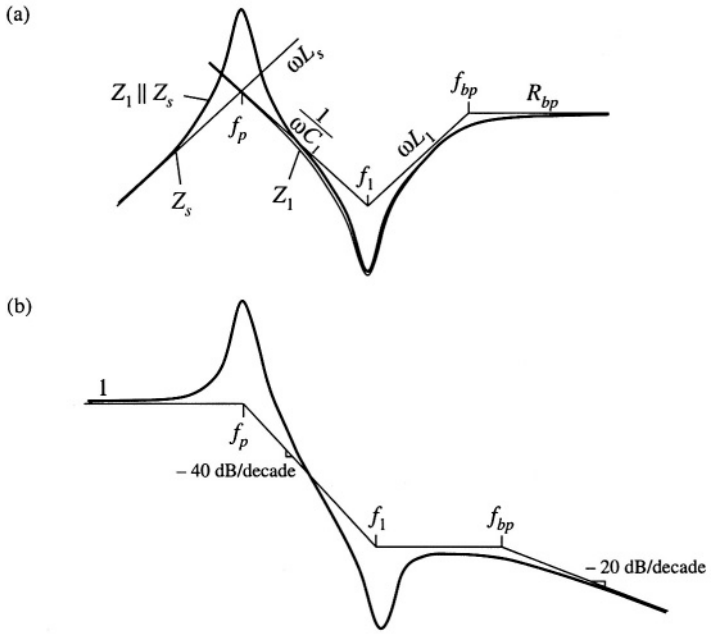

Fig. 17.24 Construction of approximate frequency response for a harmonic trap filter containing bypass resistor: (a) impedance asymptotes, (b) transfer function asymptotes.

seventh harmonics, with a single-pole rolloff to attenuate higher-order harmonics such as the eleventh and thirteenth, is illustrated in Fig. 17.25.

Power loss in the bypass resistor can be an issue: since R_{bp} is not part of the resonant network, significant fundamental (50 Hz or 60 Hz) currents can flow through R_{bp}. The power loss can be reduced by addition of blocking capacitor C_b as illustrated in Fig. 17.23(b). This capacitor is chosen to increase the impedance of the R_{bp}–C_b leg at the fundamental frequency, but have negligible effect at the higher-

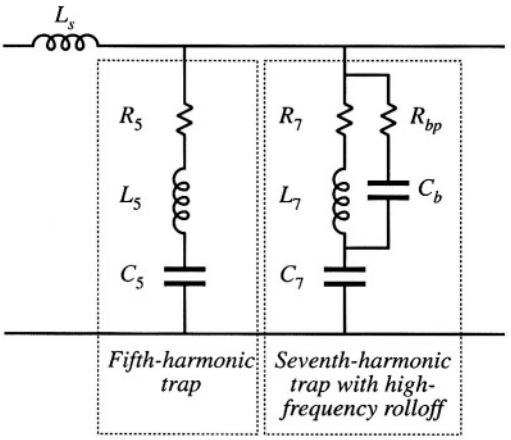

Fig. 17.25 A harmonic trap filter containing series resonances tuned to the fifth and seventh harmonics, and high-frequency rolloff characteristic.

order harmonic frequencies.

The harmonic trap filter network can also supply significant reactive power to the rectifier and power system. As given by Eq. (17.10), the rectifier fundamental current lags the voltage, and the rectifier consumes reactive power. As seen in Fig. 17.22(a), the impedances of the series resonant tank networks are dominated by their capacitor asymptotes at low frequency. Hence, at the fundamental frequency, the filter impedance reduces to an equivalent capacitor, equal to the parallel combination of the tank capacitors. The current through this capacitance leads the ac line voltage, and hence as mentioned in the previous chapter, the capacitor is a source of reactive power.

17.5 TRANSFORMER CONNECTIONS

A final conventional approach to reducing the input harmonics of three-phase rectifiers is the use of phase-shifting transformer circuits. With these schemes, the low-order harmonics, such as the fifth and seventh, can be eliminated. The remaining harmonics are smaller in magnitude, and also are easier to filter.

The rectifier circuit of Fig. 17.7 is known as a *six-pulse* rectifier because the diode output voltage waveform contains six pulses per ac line period. The output voltage ripple has a fundamental frequency that is six times the ac line frequency. As illustrated in Fig. 17.8, the ac line current waveforms contain three steps: at any given instant, $i_a(t)$ is equal to either i_L, 0, or $-i_L$. The spectrum of the current waveform contains fundamental and odd nontriplen harmonics (1, 5, 7, 11, 13,...), whose amplitudes vary as $1/n$.

It is possible to shift the phase of the ac line voltage using three-phase transformer circuits. For example, in the delta-wye transformer circuit of Fig. 17.26, the transformer primary windings are driven by the primary-side line-to-line voltages, while the transformer secondaries supply the secondary-side line-to-neutral voltages. In an ideal transformer, the secondary voltage is equal to the primary voltage multiplied by the turns ratio; hence, the phasor representing the secondary voltage is in phase with the

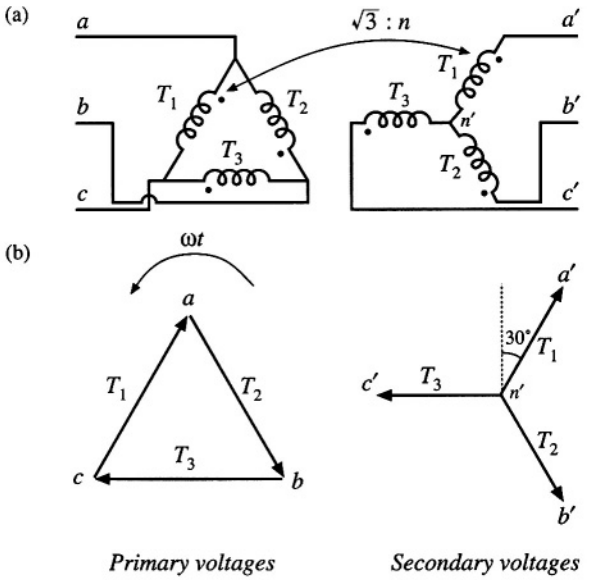

Fig. 17.26 Three-phase delta-wye transformer connection: (a) circuit, (b) voltage phasor diagram.

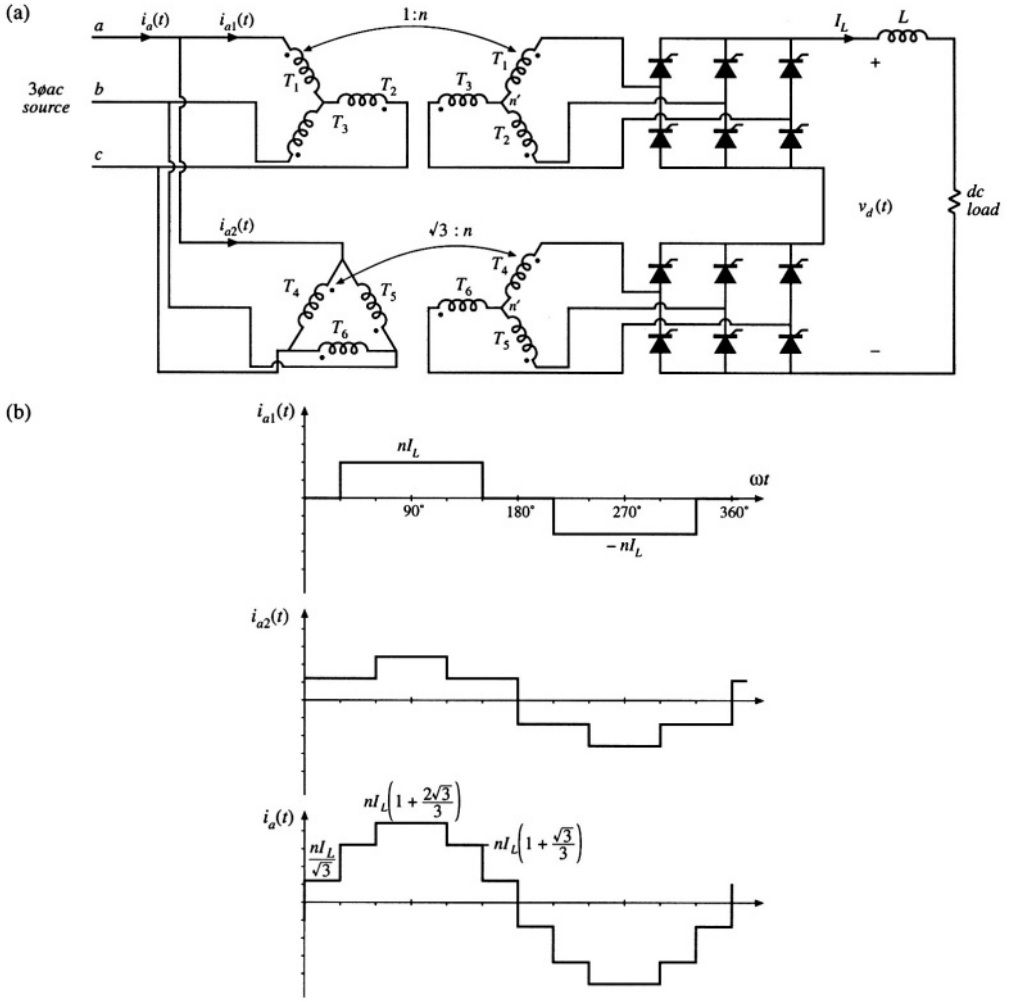

Fig. 17.27 Twelve-pulse rectifier: (a) circuit, (b) input phase *a* current waveforms.

primary voltage phasor, and is scaled in magnitude by the turns ratio. So in the delta-wye transformer connection, the secondary line-to-neutral voltages are in phase with the primary line-to-line voltages. In a balanced three-phase system, the line-to-line voltages are shifted in phase by 30° with respect to the line-to-neutral voltages, and are increased in magnitude by a factor of $\sqrt{3}$. Hence the secondary line-to-neutral voltages lag the primary line-to-neutral voltages by 30°. The wye-delta connection is also commonly used; this circuit causes the secondary voltages to lead the primary voltages by 30°. Many other more complicated transformer circuits are known, such as the zig-zag, forked-wye, and extended-delta connections, which can lead to phase shifts of any desired amount.

The 30° phase shift of the delta-wye transformer circuit is used to advantage in the twelve-pulse rectifier circuit of Fig. 17.27(a). This circuit consists of two bridge rectifier circuits driven by 3ø voltages

that differ in phase by 30°. The bridge rectifier outputs are connected in series to the dc filter inductor and load. The total rectifier output voltage $v_d(t)$ has a fundamental frequency that is twelve times the ac line frequency. The input phase *a* ac line current $i_a(t)$ is the sum of currents in three windings, and has the stepped waveshape illustrated in Fig. 17.27(b). It can be shown that this waveform contains Fourier components at the fundamental frequency and at the 11^{th}, 13^{th}, 23^{rd}, 25^{th},... harmonic frequencies, whose amplitudes vary as 1/*n*. Doing so is left as a homework problem. Thus, the twelve-pulse rectifier eliminates the 5^{th}, 7^{th}, 17^{th}, 19^{th},...harmonics.

An eighteen-pulse rectifier can be constructed using three six-pulse bridge rectifiers, with transformer circuits that shift the applied voltages by 0°, + 20°, and – 20°. A twenty-four pulse rectifier requires four six-pulse bridge rectifiers, fed by voltages shifted by 0°, + 15°, – 15°, and 30°. If *p* is the pulse number, then the rectifier produces line current harmonics of number $n = pk \pm 1$, where $k = 0, 1, 2, 3,...$. If the dc current ripple can be neglected, then the magnitudes of the remaining current harmonics vary as 1/*n*. The dc-side harmonics are of number *pk*.

So by use of polyphase transformer connections and rectifier circuits having high pulse number, quite good ac line current waveforms can be obtained. As the pulse number is increased, the current waveforms approaches a sinusoid, and contains a greater number of steps having smaller amplitude. The low-order harmonics can be eliminated, and the remaining high-frequency harmonics are easily filtered.

17.6 SUMMARY

1. With a large dc filter inductor, the single-phase full-wave rectifier produces a square-wave line current waveform, attaining a power factor of 90% and 48% THD. With smaller values of inductance, these figures are degraded. In the discontinuous conduction mode, THD greater than 100%, with power factors of 55% to 65% are typical. When the capacitance is large, the power factor, THD, displacement factor, and conversion ratio can be expressed as a function of only the dimensionless parameter K_L.

2. In the three-phase case, the bridge rectifier with large dc filter inductor produces a stepped waveform similar to the square wave, but missing the triplen harmonics. This waveform has 31% THD, and leads to a power factor of 95.5%. Reduced dc inductor values again lead to increased THD and reduced power factor, and as *L* tends to zero, the THD tends to infinity while the power factor tends to zero. In practice, the minimum effective series inductance is limited by the power system source inductance.

3. With a large dc inductor, phase control does not influence the distortion factor or THD, but does lead to a lagging fundamental current and decreased displacement factor. Phase-controlled rectifiers and inverters are consumers of reactive power.

4. If the load is capable of supplying power, then the phase-controlled rectifier can become an inverter. The delay angle a is greater than 90°, and the output voltage polarity is reversed with respect to rectifier operation. The maximum delay angle is limited by commutation failure to a value less than 180°.

5. Harmonic trap filters and multipulse-rectifier/polyphase transformer circuits find application in high-power applications where their large size and weight are less of a consideration than their low cost. In the harmonic trap filter, series resonant tank circuits are tuned to the offending harmonic frequencies, and shunt the harmonic currents away from the utility power network. Parallel resonances may cause unwanted peaks in the filter transfer function. Operation of these filters may be understood using the algebra-on-the-graph method, and computer simulations can be used to refine the accuracy of the analysis or design. Rectifiers of higher pulse number can also yield improved current waveforms, whose harmonics are of high frequency and small amplitude, and are easily filtered.

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PROBLEMS

17.1 The half-controlled single-phase rectifier circuit of Fig. 17.28 contains a large inductor L, whose current $i_L(t)$ contains negligible ripple. The thyristor delay angle is α.

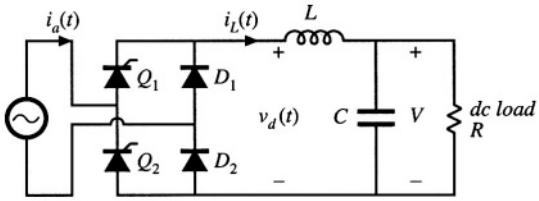

Fig. 17.28 Half-controlled rectifier circuit of Problem 17.1.

(a) Sketch the waveforms $v_d(t)$ and $i_a(t)$. Label the conduction intervals of each thyristor and diode.

(b) Derive an expression for the dc output voltage V, as a function of the rms line-line voltage and the delay angle.

(c) Derive an expression for the power factor.

(d) Over what range of α are your expressions of parts (b) and (c) valid?

17.2 The half-controlled rectifier circuit of Fig. 17.29 contains a large inductor L, whose current $i_L(t)$ contains negligible ripple. The thyristor delay angle is α.

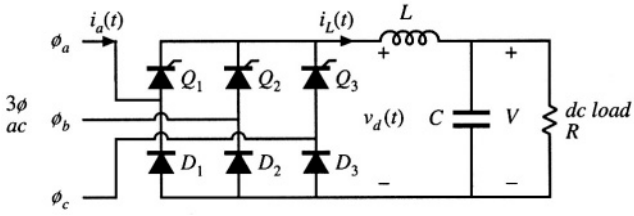

Fig. 17.29 Three-phase half-controlled rectifier circuit of Problem 17.2.

(a) Sketch the waveforms $v_d(t)$ and $i_a(t)$. Label the conduction intervals of each thyristor and diode.

(b) Derive an expression for the dc output voltage V, as a function of the rms line-line voltage and the delay angle.

(c) Derive an expression for the power factor.

(d) Over what range of α are your expressions of parts (b) and (c) valid?

17.3 A 3ø SCR bridge is connected directly to a resistive load, as illustrated in Fig. 17.30. This circuit operates in the continuous conduction mode for small delay angle α, and in the discontinuous conduction mode for sufficiently large α.

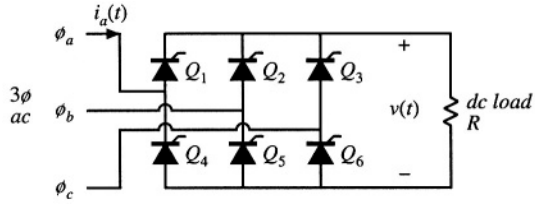

Fig. 17.30 Three-phase controlled rectifier circuit of Problem 17.3.

(a) Sketch the output voltage waveform $v(t)$. for CCM operation and for DCM operation. Clearly label the conduction intervals of each SCR.

(b) Under what conditions does the rectifier operate in CCM? in DCM?

(c) Derive an expression for the dc component of the output voltage in CCM.

(d) Repeat part (c), for DCM operation.

17.4 A rectifier is connected to the 60 Hz utility system. It is desired to design a harmonic trap filter that has negligible attenuation or amplification of 60 Hz currents, but which attenuates both the fifth- and seventh-harmonic currents by a factor of 10 (– 20 dB). The ac line inductance L_s is 500 μH.

(a) Select L_5, the inductance of the fifth harmonic trap, equal to 500 μH, and L_7, the inductance of the seventh harmonic trap, equal to 250 μH. Compute first-pass values for the resistor and capacitor values of the fifth and seventh harmonic trap circuits, neglecting the effects of parallel resonance.

(b) Plot the frequency response of your filter. It is suggested that you do this using SPICE or a similar computer program. Does your filter meet the attenuation specifications? Are there significant parallel resonances? What is the gain or attenuation at the third harmonic frequency?

(c) Modify your element values, to obtain the best design you can. You must choose L_s = 500 μH, but you may change all other element values. Plot the frequency response of your improved filter. "Best" means that the 20 dB attenuations are obtained at the fifth and seventh harmonic frequencies, that the gain at 60 Hz is essentially 0 dB, and that the Q-factors of parallel resonances are minimized.

17.5 A rectifier is connected to the 50 Hz utility system. It is desired to design a harmonic trap filter that has negligible attenuation or amplification of 50 Hz currents, but that attenuates the fifth-, seventh-, and eleventh-harmonic currents by a factor of 5 (– 14 dB). In addition, the filter must contain a single-pole response that attenuates the thirteenth and higher harmonics by a factor of $5n/13$, where n is the harmonic number. The ac line inductance L_s is 100 μH.

Design a harmonic trap filter that meets these specifications. Design the best filter you can, which meets the attenuation specifications, that has nearly unity (0 dB ± 1 dB) gain at 50 Hz, and that has minimum gains at the third and ninth harmonics. Plot the frequency response of your filter, and specify your circuit element values.

17.6 A single-phase rectifier operates from a 230 Vrms 50 Hz European single-phase source. The rectifier must supply a 1000 W dc load, and must meet the IEC-1000 class A or class D harmonic current limits. The circuit of Fig. 17.1 is to be used. The dc load voltage may have 100 Hz ripple whose peak-to-peak amplitude is no greater than 5% of the dc voltage component.

(a) Estimate the minimum value of inductance that will meet these requirements.

(b) Specify values of L and C that meet these requirements, and prove (by simulation) that your design is correct.

17.7 Figure 17.31 illustrates a twelve-pulse rectifier, containing six controlled (SCR) devices and six uncontrolled (diode) devices. The dc filter inductance L is large, such that its current ripple is negligible. The SCRs operate with delay angle α. The SCR bridge is driven by a wye-wye connected three-phase transformer circuit, while the diode bridge is driven by a wye-delta connected three-phase transformer circuit. Since both transformer circuits have wye-connected primaries, they can be combined to realize the circuit with a single wye-connected primary.

(a) Determine the rms magnitudes and phases of the line-to-line output voltages of the transformer secondaries $v_{a1'b1'}$ and $v_{a2'b2'}$, as a function of the applied line-line primary voltage v_{ab}.

(b) Sketch the waveforms of the voltages $v_{d1}(t)$ and $v_{d2}(t)$. Label the conduction intervals of each thyristor and diode.

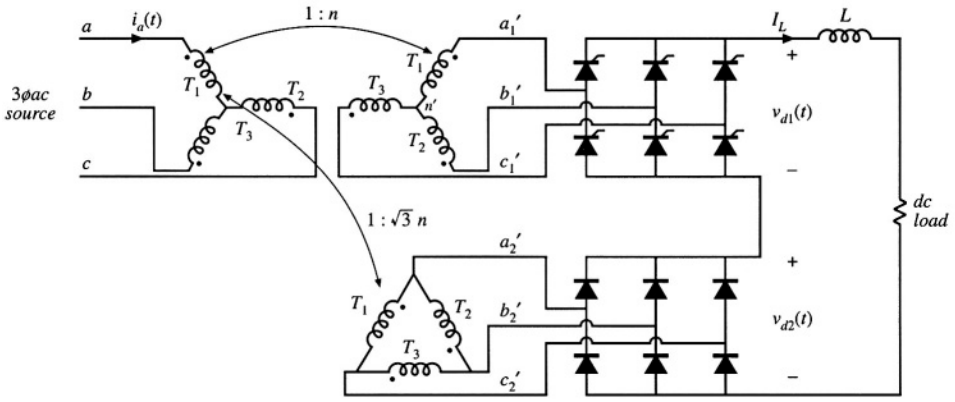

Fig. 17.31 Twelve-pulse rectifier circuit, with one controlled and one uncontrolled bridge, Problem 17.7.

(c) Derive an expression for the dc component of the output voltage, as a function of the rms line-line input voltage, the delay angle α, and the turns ratio n.

(d) Over what range of α is your expression of part (c) valid? What output voltages can be produced by this rectifier?

17.8 For the twelve-pulse rectifier circuit of Fig. 17.27(a), determine the Fourier coefficients, for the fundamental through the thirteenth harmonic, of the primary-side currents $i_{a1}(t)$ and $i_{a2}(t)$, as well as for the ac line current $i_a(t)$. Express your results in terms of the turns ratio n and the dc load current I_L. You may assume that the dc filter inductance L is large and that the transformers are ideal.

17.9 The single-phase controlled-bridge rectifier of Fig. 17.32 operates in the continuous conduction mode. It is desired to regulate the load voltage $v(t)$ in the presence of slow variations in the amplitude of the sinusoidal input voltage $v_g(t)$. Hence, a controller must be designed that varies the delay angle α such that $v(t)$ is kept constant, and it is of interest to derive a small-signal ac model for the dc side of the rectifier circuit.

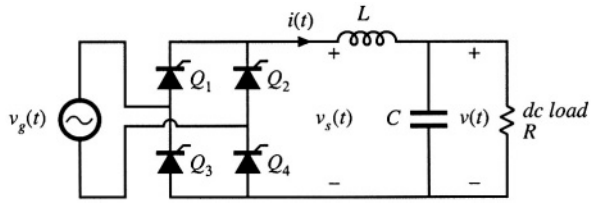

Fig. 17.32 Single-phase controlled rectifier, Problem 17.9.

(a) Sketch $v_s(t)$ and $v_g(t)$, and label the delay angle α.

(b) Use the circuit averaging method to determine the small-signal transfer functions

$$\frac{\hat{v}(s)}{\hat{\alpha}(s)}$$ control-to-output transfer function

and

$\frac{\hat{v}(s)}{\hat{v}_g(s)}$ line-to-output transfer function

as well as the steady-state relationship

$$V = f(V_g, A)$$

where

$$\alpha(t) = A + \hat{\alpha}(t)$$
$$v(t) = V + \hat{v}(t)$$
$$v_g(t) = \left(V_g + \hat{v}_g(t)\right) \sin(\omega t)$$

You may assume that the frequencies of the variations in α, v, and v_g are much slower that the ac line frequency ω, and that the inductor current ripple is small.