

DE ARTMENT OF COMPUTER SCIENCE

COURSE TITLE: COMPUTER ARCHITECTURE AND ORGANISATION

COURSE CODE: COSC 425 SESSION: 1st 2022/2023

LECTURERS: Agbaje /Somefun/Fatade

TIME ALLOWED: 2 Hours

INSTRUCTION: Answer all questions in Section A &B and any Two (2) in Section C

Section A(10marks)

- 1. The addressing mode used in an instruction of the form ADD X Y is
- a.Index b. immediate, c.indirect d. direct
- 2. A register capable of shifting is bits either left or right is called
- a. Shift register b. base register c. Data registers d. Address registers
- 3. Logic gates with a set of input and output are arrangement of:
 - a.Design circuit b.Logic circuit c.Register d.Combinational circuit
 - 4. 16 The operation executed in data and stored in the register is called:
 - a. byte operation b.Bit operation c.Micro operation d.Macro operation
 - 5. The average time required to reach a storage location in memory and obtain its content is called the?
 - a. Access time b. Seek time c. Transfer time dTurn Section B(2x5 marks) the idea that many unseriously are

- Define computer architecture. i.
- Define Moore Law ii.
- .What is a stored program computer? What is the function of the program counter (PC)? iii.

have related

- State Amdahl's Law and its purpose iv.

6. Von Neumann architecture is

a SIMD b SISD c.MISD d.MIMD

7. The instruction, Add R1, R2, R3 in RTN is

a.R3=[R1]+[R2][b.R3=R1+R2+R3 c. R3< [R1]+[R2] d R < [R1]+[R2] - [R]

- 8. What is meant by a dedicated computer?
- a. Which is used by a only one person b. Which is meant to application software only
- c. Which does one kind of software (d. Which is assigned to only one task
- 9. The most common addressing techniques used by CPU is:
- a.Immediate addressing techniques b.Direct addressing techniques c.Indirect addressing techniques d.All of the above
- 10/The combination between components in a microcomputer takes place via the address and:
- a.Data bus bI/O busc.Control lines d.Address

instruction are stored m the memored and program to execute if



- Q1. a. Explain Von Neumann's bottleneck
 - b. List 3 methods of mitigating the Von Neumann performance
 - c. The processes by which the Control Unit carries out its function is described as the Instruction Cycle, list out the steps involved in the cycle.
 - d. Memory Operations of two types. List and explain them.
- Q2 a. using the booths algorithm solve -5 x -5
 - b. Using straight-forward multiplication (Unsigned), implement the following using your chosen algorithm $0011_2 \times 0011_2 = X_2$
 - c.Discuss briefly parallelism mentioning explicitly it's a fundamental goal
 - d.List and explain 3 techniques aimed at exploiting and enhancing the capability for parallel processing.
- Q3. The processor executes each instruction in a series of small instruction execution steps which constitute a FETCH-DECODE-EXECUTE cycle or, more generally, an instruction steps execution of all computers. Using the following EXECUTION cycle. The cycle is central to the operation of all computers. Using the following diagram, explain each of the small instruction steps involved in the execution of an instruction by a processor, as highlighted in the diagram, in an operational order.

