Midsem

Monsoon -2020

Computer Architecture

ECE-511

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Q-1.) Non-pipelined cycle time: $4+5+10+10+7$

$= 36\text{ns}$

Pipelined cycle time $= 2 + \max(4, 5, 10, 10, 7)$

$= 2+10$

$= 12\text{ns}$

CPI for non pipelined $= 1$

CPI for pipelined ≈ 1 (assuming stalls are amortized)

Time / Instruction $=$ Cycles / Instruction $\times$

~~Time taken for one instruction~~

$\therefore$ Speed up $= 36/12 = 4\times$ for pipelined.

Realistically less than 4x due to stalls.

8-2.)

$$\frac{\text{Time}}{\text{Program}} = \underbrace{\frac{\text{Instr}^n}{\text{Program}}}_{x} \times \frac{\text{Cycles}}{\text{Instr}^n} \times \frac{\text{Time}}{\text{Cycle}}$$

$$CPI_A = 1.5$$

$$CPI_B = 2.5$$

$$\text{Time/Cycle}_A = 1/600 \times 10^6$$

$$\text{Time/Cycle}_B = 1/800 \times 10^6$$

$$\text{Time/Program}_A = \text{Time/Program}_B$$

$$\Rightarrow 50{,}000 \times \frac{3}{2} \times \frac{1}{600 \times 10^6} = x \times \frac{5}{2} \times \frac{1}{800 \times 10^6}$$

$$\Rightarrow x = \frac{50{,}000 \times 3 \times 8}{5} = 24000$$

Q-3.)

Addr size = 32 bits

Cache size = 16 kB $= 2^{14}$ bytes

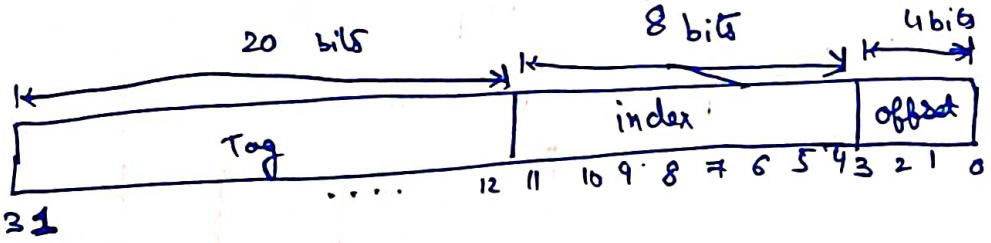
4 way set associative. $= 2^2$

Block size = 16 bytes $= 2^4$ bytes.

a.) No. of cache lines $= \frac{2^{14}}{2^4} = 2^{10}$

No. of sets $= \frac{2^{10}}{2^2} = 2^8$ sets $= 256$ sets

b.)



c.) 0x 10 FF CFF

- CFF → Used for offset
- FF → Used for index
- 10 → Used for tag.

0x 10FF CFF mapped to Set CF

Reason: the index bits determine set. these are bits 4 → 11 as shown above.

Instruction	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{16}	C_{17}	C_{18}	C_{19}	C_{20}	C_{21}	C_{22}	C_{23}
0x1000 ADDI R4,R0,4	F	D	X	M	W																	
0x1004 LD R5,0(R4)		F	D	X	M	W																
0x1008 ADD R5,R5,R4			F	D	D	X	M	W														
0x100C BEQ R4,R5,0x1000				F	F	D	X	M	W													
0x1001 LD R7,4(R0)						F	D	nop	nop	nop												
0x1004 ADD R5,R7,R5							F	nop	nop	nop	nop											
0x1008 ADDI R4,R0,4								F	D	X	M	W										
0x1004 LD R5,0(R4)									F	D	X	M	W									
0x1008 ADD R5,R5,R4										F	D	D	X	M	W							

Assuming data in memory at addr 0x0 is 0.

Assuming:

Memory to X bypass.

X to X bypass

Assuming value written at cycle i in W is visible in the same cycle @ D (on rising edge write, on falling edge read)

17 cycles required

8-1

Instructions	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{16}	C_{17}	C_{18}	C_{19}	C_{20}
ADD R14, R16, R17	F	D	X_A	M_A	W_A															
SUB R1, R2, R3	F	D	X_B	M_B	W_B															
SUB R2, R3, R5		F	D	X_A	M_A	W_A														
LD R11, 0(R2)		F	D	D	X_B	M_B	W_B													
ADDI R12, R13, 1			F	F	D	X_A	M_A	W_A												
LD R15, 4(R2)			F	F	D	X_B	M_B	W_B												
LD R15, 4(R15)					F	D	D	X_B	M_B	W_B										
SUB R2, R9, R11					F	D	X_A	M_A	W_A											
ADD R3, R11, R12						F	F	D	X_A	M_A	W_A									
ADD R4, R6, R7						F	F	D	X_B	M_B	W_B									

11 cycles needed.

Naming Convention:

Pipeline A: F D X_A M_A W_A

Pipeline B: F D X_B M_B W_B

Assuming Addr calculation in X

Assuming writes in W are visible in D in the same stage (write at rising edge, read at falling edge).

Assuming if one of the pipeline is stalled, then subsequent instructions is also stalled by 1 cycle. fetch of two