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CSE 3381 <Digital Logic Design N14 1172>

Post-Lab 02

1. Write Up

   I've learnt how to write a top code from the code base I have to compile and simulate the program. I've also learnt the logic of 2x4 decoder, and coding with the examples eased my transition for diagrams to pure Verilog. Also having part of the lab problems as pre-lab helped me better understand the outline and expectation of the lab session.

2. Source Code (gates4.v, gates4_top.v, eqdet2.v, eqdet2_top.v, decoder_2x4)

```
//-----------------------------------------------------------------------------
//
// Title           : \\decoder-2by4
// Design          : swled
// Author          : Seung Ki Lee
// Company         : SMU
//
//-----------------------------------------------------------------------------
//
// File            : c:\Users\lg\Desktop\DLD_License\DLD_Lab\Example1\swled\src\decoder-2by4.v
// Generated       : Mon Feb 13 17:16:19 2017
// From            : interface description file
// By              : Itf2Vhdl ver. 1.22
//-----------------------------------------------------------------------------
`timescale 1 ns / 1 ps

//{{ Section below this comment is automatically maintained
//      and may be overwritten
//{module {\\decoder-2by4}}
module \\decoder-2by4 ( x ,y ,en );
```

```
output [0:3] y ;
wire [0:3] y ;

input [0:1] x ;
wire [0:1] x ;
input en ;
wire en ;

//}} End of automatically maintained section

// -- Enter your statements here -- //

assign y[0] = ~x[0] & ~x[1] & en;
assign y[1] = x[0] & ~x[1] & en;
assign y[2] = ~x[0] & x[1] & en;
assign y[3] = x[0] & x[1] & en;

endmodule

//--------------------------------------------------------------------------------
//
// Title             : gates4
// Design            : swled
// Author            : Seung Ki Lee
// Company           : SMU
//
//--------------------------------------------------------------------------------
//
// File              : c:\Users\lg\Desktop\DLD_License\DLD_Lab\Example1\swled\src\gates4.v
// Generated         : Mon Feb 13 17:22:08 2017
```

```
// From            : interface description file
// By              : Itf2Vhdl ver. 1.22
//-----------------------------------------------------------------------------
`timescale 1 ns / 1 ps

//{{ Section below this comment is automatically maintained
//     and may be overwritten
//{module {gates4}}
module gates4 ( x ,and4_ ,or4_ ,xor4_ );

output and4_ ;
wire and4_ ;
output or4_ ;
wire or4_ ;
output xor4_ ;
wire xor4_ ;

input [3:0] x ;
wire [3:0] x ;

//}} End of automatically maintained section

// -- Enter your statements here -- //

assign and4_ = &x;
assign or4_ = |x;
assign xor4_ = ^x;

endmodule
```

```
//-------------------------------------------------------------------------
//
// Title             : gates4_top
// Design            : swled
// Author            : Seung Ki Lee
// Company           : SMU
//
//-------------------------------------------------------------------------
//
// File              : c:\Users\lg\Desktop\DLD_License\DLD_Lab\Example1\swled\src\gates4_top.v
// Generated         : Mon Feb 13 17:25:02 2017
// From              : interface description file
// By                : Itf2Vhdl ver. 1.22
//-------------------------------------------------------------------------
`timescale 1 ns / 1 ps

//{{ Section below this comment is automatically maintained
//      and may be overwritten
//{module {gates4_top}}
module gates4_top ( sw ,ld );

output [2:0] ld ;
wire [2:0] ld ;

input [3:0] sw ;
wire [3:0] sw ;

//}} End of automatically maintained section

// -- Enter your statements here -- //
```

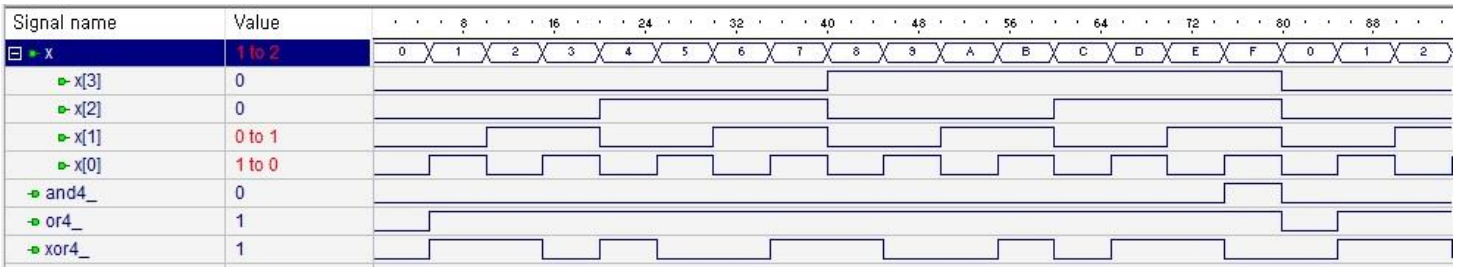
```
gates4 U1(
.and4_(ld[2]),
.or4_(ld[1]),
.x(sw),
.xor4_(ld[0])
);

Endmodule

//-------------------------------------------------------------------------
//
// Title             : eqdet2
// Design            : swled
// Author            : Seung Ki Lee
// Company           : SMU
//
//-------------------------------------------------------------------------
//
// File              : c:\Users\lg\Desktop\DLD_License\DLD_Lab\Example1\swled\src\eqdet2.v
// Generated         : Mon Feb 13 17:28:25 2017
// From              : interface description file
// By                : Itf2Vhdl ver. 1.22
//-------------------------------------------------------------------------
`timescale 1 ns / 1 ps

//{{ Section below this comment is automatically maintained
//      and may be overwritten
//{module {eqdet2}}
module eqdet2 ( a ,b ,eq );
```

```
output eq ;
wire eq;

input [1:0] a ;
wire [1:0] a ;
input [1:0] b ;
wire [1:0] b ;

wire eq1;
wire eq2;

//}} End of automatically maintained section

// -- Enter your statements here -- //

assign eq1 = ~(b[1] ^ a[1]);
assign eq2 = ~(b[0] ^ a[0]);
assign eq = eq2 & eq1;

endmodule

//---------------------------------------------------------------------------
//
// Title             : eqdet2_top
// Design            : swled
// Author            : Seung Ki Lee
// Company           : SMU
//
//---------------------------------------------------------------------------
```

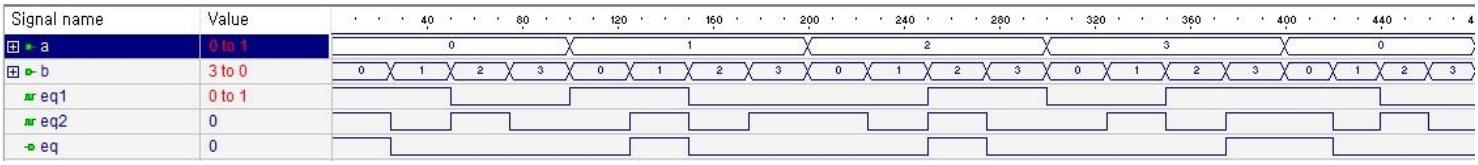
```
//
// File              : c:\Users\lg\Desktop\DLD_License\DLD_Lab\Example1\swled\src\eqdet2_top.v
// Generated         : Mon Feb 13 18:06:20 2017
// From              : interface description file
// By                : Itf2Vhdl ver. 1.22
//-----------------------------------------------------------------------------
`timescale 1 ns / 1 ps

//{{ Section below this comment is automatically maintained
//      and may be overwritten
//{module {eqdet2_top}}
module eqdet2_top ( sw , ld );

input wire [3:0] sw ;
output wire [0:0] ld ;




//}} End of automatically maintained section

// -- Enter your statements here -- //

eqdet2 U1(
.a(sw[1:0]),
.b(sw[3:2]),
.eq(ld[0])
);

endmodule
```

3. Simulation (gates4, eqdet2, decoder_2x4)

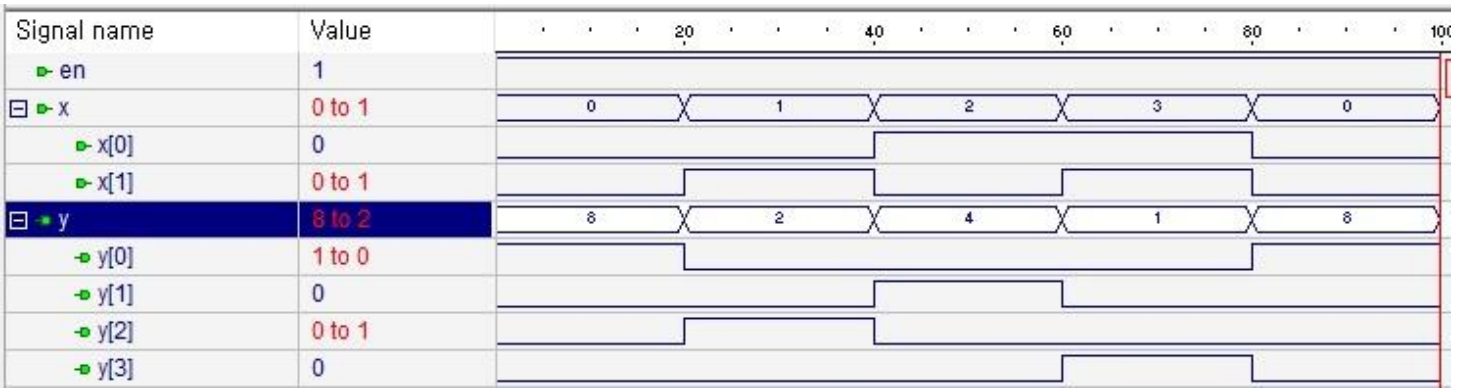
Gate4



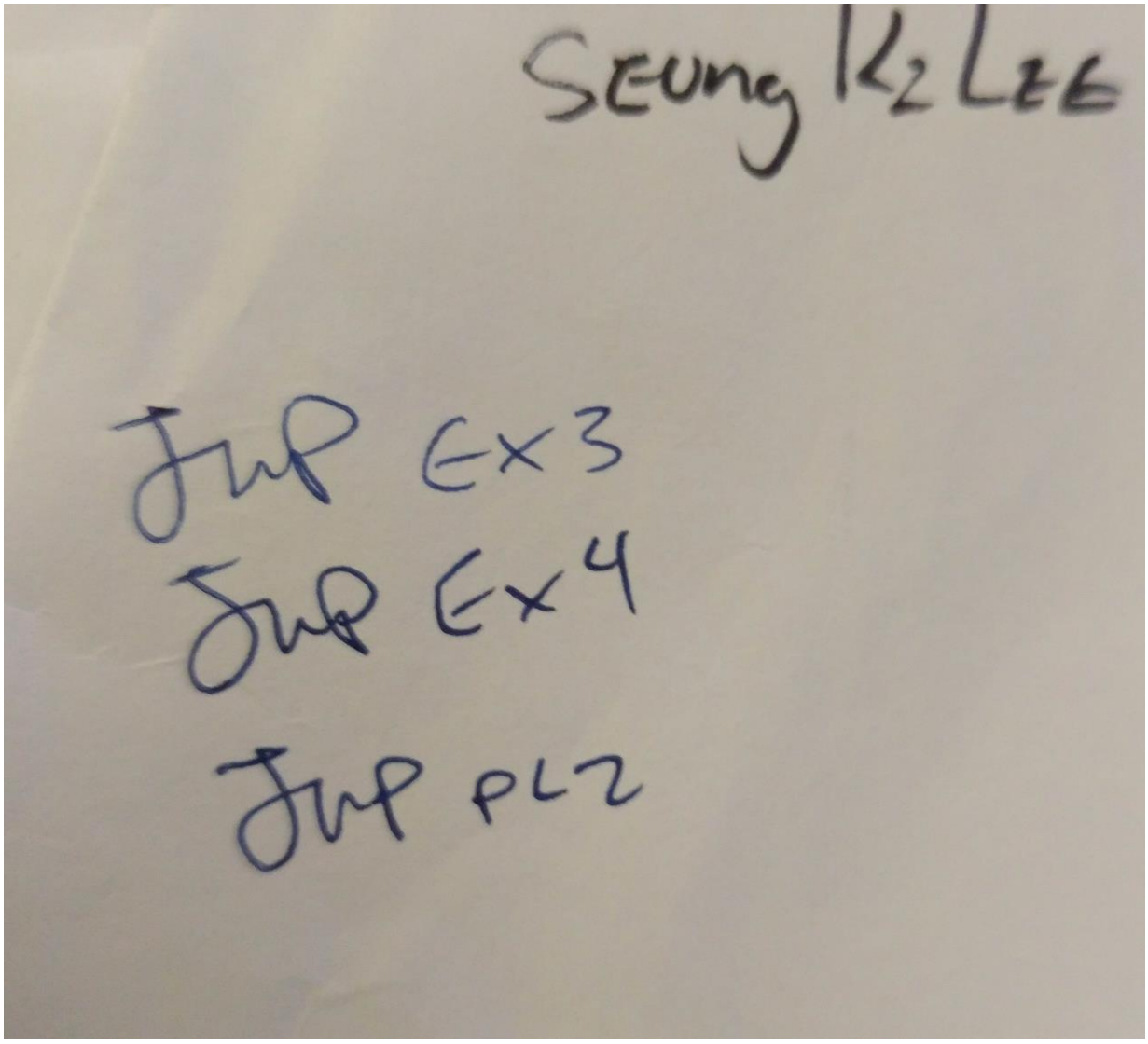
Eqdet2



Decoder2x4



4. Demo Signature (Example3, Example4, Prelab01)


Seung Ki Lee
Jmp Ex3
Jmp Ex4
Jmp plz