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CSE 3381 <Digital Logic Design N14 1172>

Post-Lab 07

1. Write Up & Prelab Code

   This week was the first week where code's framework was not available on the lab manual, so going over the prelab was a bit more challenging. But I was surprised at how much I've learnt since the beginning of the semester from being able to create code from the diagram.

   Prelab-Code: 4466

2. Source Code (clg.v, cla.v, cla_top.v)

clg.v

```
module clg(
      input wire [3:0] a,
      input wire [3:0] b,
      input cin,
      output wire [4:0] s
      );

   wire [3:0] p;
   wire [3:0] g;
   wire [4:0] c;

   assign p[3:0] = a[3:0] ^ b[3:0];
   assign g[3:0] = a[3:0] & b[3:0];

   assign c[0] = cin;

   assign c[1] = g[0] | (p[0] & c[0]);
```

```
   assign c[2] = g[1] | (p[1] & g[0]) | (p[1] & p[0] & c[0]);

   assign c[3] = g[2] | (p[2] & g[1]) | (p[2] & p[1] & g[0]) | (p[2]
& p[1] & p[0] & cin);

   assign c[4] = g[3] | (p[3] & g[2]) | (p[3] & p[2] & g[1]) | (p[3]
& p[2] & p[1] & g[0]) | (p[3] & p[2] & p[1] & p[0] & cin);

endmodule
```

cla.v

```
module cla(
      input [3:0] a,
      input [3:0] b,
      input cin,
      output [3:0]s,
      output cout
      );

   wire [3:0] p;
   wire [3:0] g;
   wire [4:0] c;

   assign p = a ^ b;
   assign g = a & b;

   assign c[0] = cin;

   assign c[1] = g[0] | (p[0] & c[0]);
```

```
   assign c[2] = g[1] | (p[1] & g[0]) | (p[1] & p[0] & c[0]);

   assign c[3] = g[2] | (p[2] & g[1]) | (p[2] & p[1] & g[0])
                      | (p[2] & p[1] & p[0] & cin);

   assign c[4] = g[3] | (p[3] & g[2]) | (p[3] & p[2] & g[1])
                    | (p[3] & p[2] & p[1] & g[0])
                    | (p[3] & p[2] & p[1] & p[0] & cin);
      assign cout = c[4];

   assign s = p ^ c;

endmodule
```

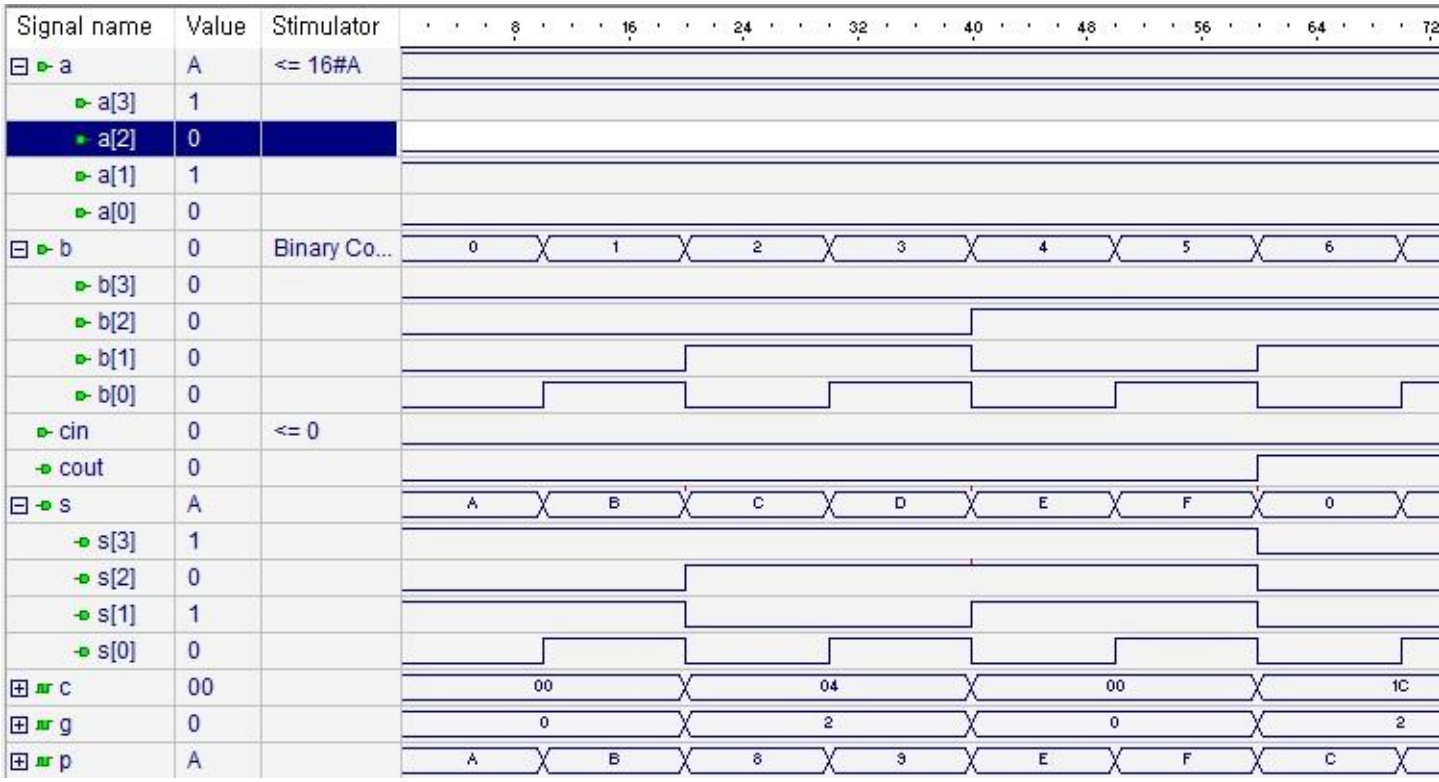
cla_top.v

```
module cla_top (
input wire [7:0] sw,
input wire [0:0] btn,
output wire [4:0] ld
      );

cla U1
(
.cin(btn[0]),
.a(sw[7:4]),
.b(sw[3:0]),
.cout(ld[4]),
.s(ld[3:0])
);

endmodule
```

3. Simulation (cla)



4. Demo Code

Demo-Code: 4723