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CSE 3381 <Digital Logic Design N14 1172>

Post-Lab 09

1. Write Up

   While concept of moore and mealy machine was introduced by Dr.Dworak earlier, seeing its implementation on the FPGA board and confirming the simulation clarified a lot of questions I had.

2. Source Code (moore.v, moore_top.v, mealy.v, mealy_top.v)

Moore.v

```
module moore (
      input wire clk,
      input wire rst,
      output wire [2:0] out
);
reg [2:0] state;
parameter S0=3'b000, S1=3'b001, S2=3'b010, S3=3'b011, S4=3'b100,
S5=3'b101, S6=3'b110, S7=3'b111;
always @(posedge clk or posedge rst)
      if(rst == 1)
            state <= S0;
      else
            case(state)
                  S0: state <= S4;
                  S4: state <= S7;
                  S7: state <= S3;
                  S3: state <= S5;
                  S5: state <= S0;
            endcase
      assign out = state;
endmodule
```

Moore_top.v

```
module moore_top (
      input wire mclk,
      input wire [0:0] btn,
      output wire [2:0] ld
);

moore U1(
      .clk(mclk),
      .rst(btn[0]),
      .out(ld[2:0])
);
endmodule
```

Mealy.v

```
module mealy (
      input wire clk,
      input wire rst,
      input wire cin,
      output wire out,
      output wire [3:0] state
);
reg [3:0] currState, nextState;
reg cout;
parameter A=4'b0001, B=4'b0010, C=4'b0100, D=4'b1000;
always @(posedge clk or posedge rst)
      if(rst == 1)
            currState <= A;
      else
            currState <= nextState;
always @(currState or cin)
```

```
if(cin == 1)
      case(currState)
            A:
            begin
            nextState <= A;
            cout <= 1;
            end
            B:
            begin
            nextState <= D;
            cout <= 0;
            end
            C:
            begin
            nextState <= B;
            cout <= 0;
            end
            D:
            begin
            nextState <= C;
            cout <= 1;
            end
      endcase
else
      case(currState)
            A:
            begin
            nextState <= B;
            cout <= 0;
            end
```

```
            B:
            begin
            nextState <= C;
            cout <= 1;
            end
            C:
            begin
            nextState <= A;
            cout <= 1;
            end
            D:
            begin
            nextState <= D;
            cout <= 0;
            end
      endcase

assign state = currState;

assign out = cout;

endmodule
```

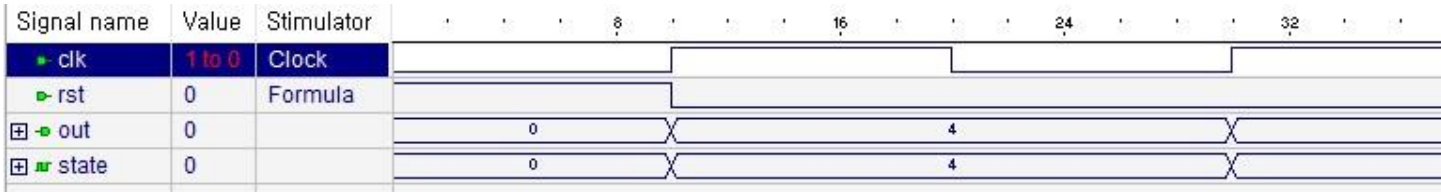
Mealy_top.v

```
module mealy_top (
      input wire mclk,
      input wire [0:0] sw,
      input wire [0:0] btn,
      output wire [4:0] ld
);
```

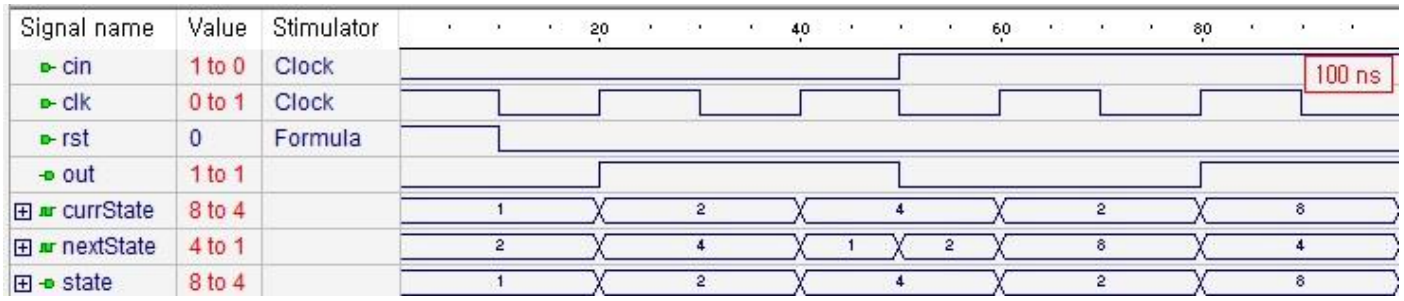
```
mealy U1 (
        .clk(mclk),
        .rst(btn[0]),
        .cin(sw[0]),
        .state(ld[3:0]),
        .out(ld[4])
);
endmodule
```

3. Simulation (moore, mealy)

Moore



Mealy



4. Demo Code

Demo-Code (moore):

Demo-Code (mealy):