Logical Circuit & Design Homework #02

Due date	May 11, 2020	Instructor	Yoo, Younghwan
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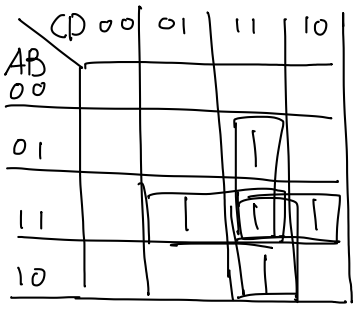
1. A majority function has an output value of 1 if there are more 1s than 0s on its inputs. The output is 0 otherwise. Design a four-input majority function.

A B C D	Out
0 0 0 0	0
0 0 0 1	0
0 0 1 0	0
0 0 1 1	0
0 1 0 0	0
0 1 0 1	0
0 1 1 0	0
0 1 1 1	1
1 0 0 0	0
1 0 0 1	0
1 0 1 0	0
1 0 1 1	1
1 1 0 1	1
1 1 1 0	1
1 1 1 1	1

1>05 ⇒ 1

아닌경우 ⇒ 0



⇒ $f = BCD + ABD + A\bar{B}C + ACD$

2. Design a circuit with a 3-bit input A, B, and C, in the form of Gray code, that produces a 3-bit output X, Y, and Z in binary form. For example, if the Gray code inputs are 001 and 011, then the circuit will produce 001 and 010, respectively.

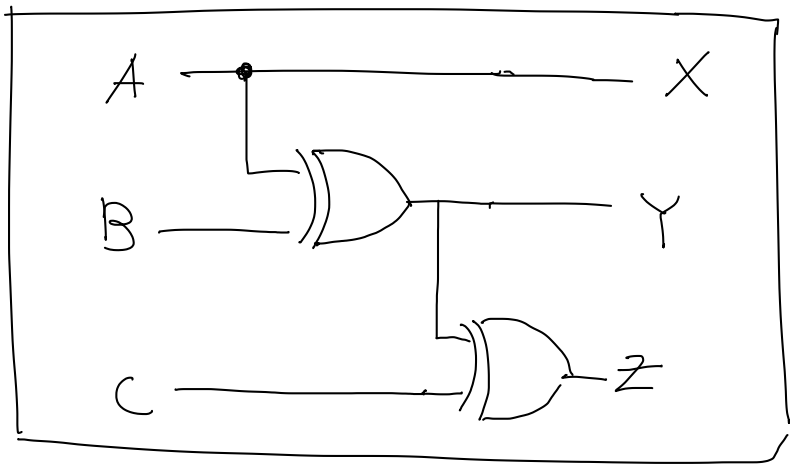
A B C	X Y Z
0 0 0	0 0 0
0 0 1	0 0 1
0 1 1	0 1 0
0 1 0	0 1 1
1 1 0	1 0 0
1 1 1	1 0 1
1 0 1	1 1 0
1 0 0	1 1 1

⇒

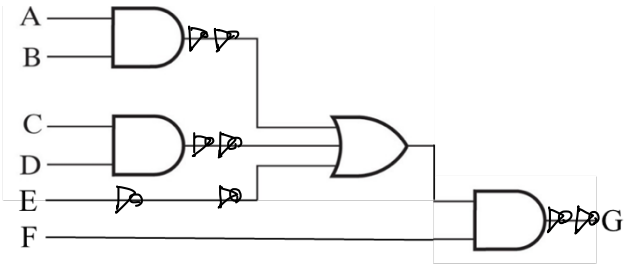
$X = A$

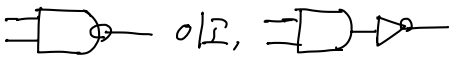
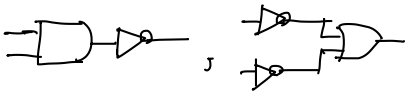
$Y = A \oplus B$

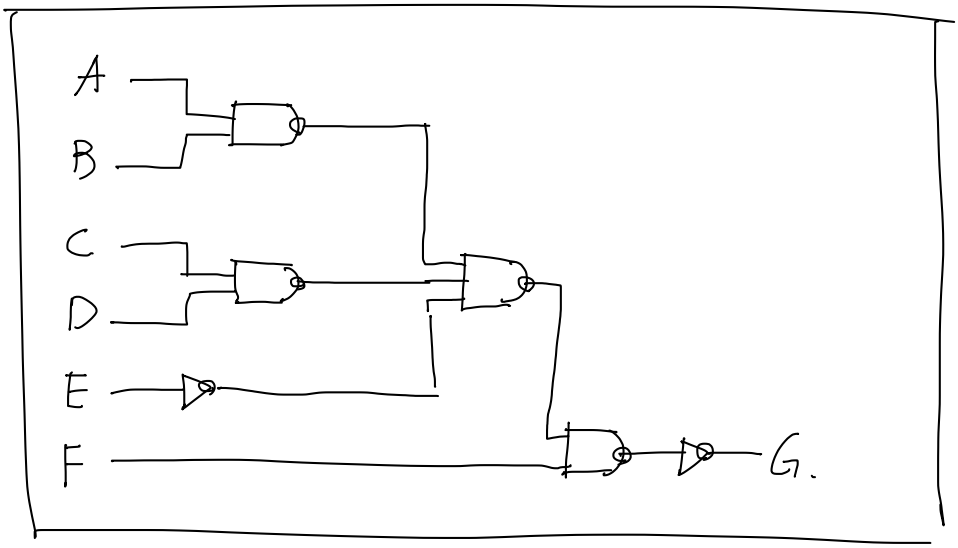
$Z = A \oplus B \oplus C$



3. Perform technology mapping to NAND gates for the circuit in the following figure. Use cell types selected from: Inverter (n=1), 2NAND, 3NAND, and 4NAND, as defined at the beginning of Section 3-2.



NAND 게이트는  이고,  로 표현가능하다.



4. A combinational circuit is defined by the following three Boolean functions:

$F_1 = \overline{X}Y\overline{Z} + \overline{X}\overline{Y}Z + X\overline{Y}\overline{Z}$

$F_2 = \overline{XY\overline{Z}} + YZ$

$F_3 = YZ + XY$

$F_4 = \overline{X}Y + XY\overline{Z}$

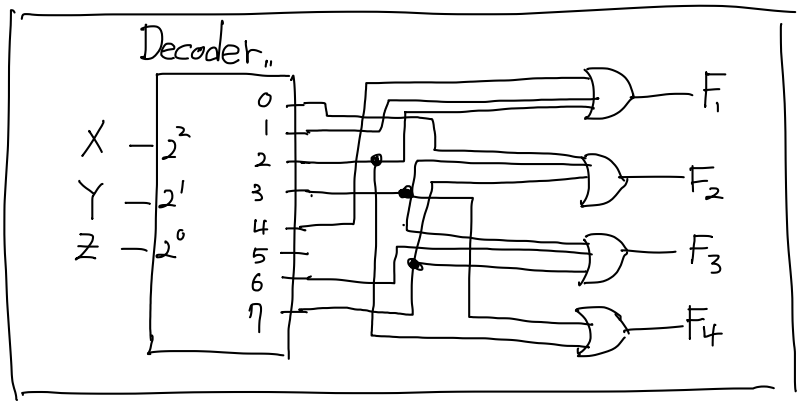
Design the circuit with a decoder and external OR gates.

$F_1 = \overline{X}Y\overline{Z} + \overline{X}\overline{Y}Z + X\overline{Y}\overline{Z} = \Sigma(1,2,4)$

$F_2 = \overline{XY\overline{Z}} + (X+\overline{X})YZ = \overline{X}\overline{Y}\overline{Z} + XYZ + \overline{X}YZ = \Sigma(0,3,7)$

$F_3 = (X+\overline{X})YZ + XY(Z+\overline{Z}) = XYZ + \overline{X}YZ + XY\overline{Z} + XY\overline{Z} = \Sigma(3,6,7)$

$F_4 = \overline{X}Y(Z+\overline{Z}) + XY\overline{Z} = \overline{X}YZ + \overline{X}Y\overline{Z} = \Sigma(2,3)$.



5. Perform the indicated subtractions with the following unsigned binary numbers by taking the 2s complement of the subtrahend:

(a) 11010 – 10001

(b) 11110 – 1110

(c) 101001 – 101

(a) $|11010 - 10001| \Rightarrow$ $10001 = 01111$ (2's complement).

$\Rightarrow$ $11010 + 01111 = \boxed{1}01001 \Rightarrow 01001$

(b) $11110 - 1110 \Rightarrow 11110 + 00010 = 00000$ (2).

(16 8 4 2) (8 4 2 1)

$\Rightarrow$ $11110 + 0010 = 100000$

(c) $|101001 - 101| = 101001 + 011 \Rightarrow 101001 + 011 = 101100$ ⇒ 자릿수 증가X

$\Rightarrow 0\,|\,0\,|\,00 \Rightarrow -010100_{(2)}$

6. Use contraction beginning with a 4-bit adder with carry out to design a 4-bit increment circuit with carry out that is incremented by 0011. The function to be implemented is $S = A + 0011$. Design the circuit with AND-OR-XOR gates.

Input				Output			
a_3	a_2	a_1	a_0	S_3	S_2	S_1	S_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

$S_3 \Rightarrow$

a_3a_2 \ a_1a_0	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	1	0	0	0
10	1	1	1	1

$= a_2a_3 + \bar{a}_0\bar{a}_1a_3 + a_0a_1\bar{a}_3 + a_1a_2\bar{a}_3$

$S_2 \Rightarrow$

a_3a_2 \ a_1a_0	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	1	0	0	0
10	0	1	1	1

$= \bar{a}_0\bar{a}_1a_2 + a_0\bar{a}_2 + \bar{a}_0a_1\bar{a}_2 = \bar{a}_0(a_1 \oplus a_2) + a_0\bar{a}_2$

$S_1 \Rightarrow$

a_3a_2 \ a_1a_0	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	1	0	1	0
10	1	0	1	0

$= \bar{a}_0\bar{a}_1 + a_0a_1 = \overline{(a_0 \oplus a_1)} = (a_0 \oplus a_1) \oplus 1$

$S_0 \Rightarrow$

a_3a_2 \ a_1a_0	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

$= \bar{a}_0\bar{a}_1 + \bar{a}_0a_1 = \bar{a}_0 = a_0 \oplus 1$