- **High-Performance Floating-Point Digital Signal Processor (DSP):**
  - **TMS320VC33-150**
    13-ns Instruction Cycle Time
    150 MFLOPS, 75 MIPS
  - **TMS320VC33-120**
    17-ns Instruction Cycle Time
    120 MFLOPS, 60 MIPS
- **34K × 32-Bit (1.1-Mbit) On-Chip Words of Dual Access SRAM Configured in 2 × 16K plus 2 × 1K Blocks to improve Internal Performance**
- **x5 PLL Clock Generator**
- **Very Low Power: < 200 mW @ 150 MFLOPS**
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **Four Internally Decoded Page Strobes to Simplify Interface to I/O and Memory Devices**
- **32-Bit Instruction Word, 24-Bit Addresses**
- **EDGEMODE Selectable External Interrupts**
- **Boot-Program Loader**
- **On-Chip Memory-Mapped Peripherals:**
  - **One Serial Port**
  - **Two 32-Bit Timers**
  - **Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation**
- **Fabricated Using the 0.18-Micron (l_{eff}-effective gate length) TImeline™ Technology by Texas Instruments (TI™)**
- **144-Pin Thin Quad Flat Pack (TQFP) (PGE Suffix)**
- **Eight Extended-Precision Registers**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two Low-Power Modes**
- **Two- and Three-Operand Instructions**
- **Parallel Arithmetic/Logic Unit (ALU) and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **Bus-Control Registers Configure Strobe-Control Wait-State Generation**
- **1.8-V (Core) and 3.3-V (I/O) Supply Voltages**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG)**

PRODUCT PREVIEW

description

The TMS320VC33 DSP is a 32-bit, floating-point processor manufactured in 0.18-micron four-level-metal CMOS (TImeline) technology. The TMS320VC33 is part of the TMS320C3x generation of DSPs from Texas Instruments.

The TMS320C3x's internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 150 million floating-point operations per second (MFLOPS). The TMS320C3x optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The TMS320C3x can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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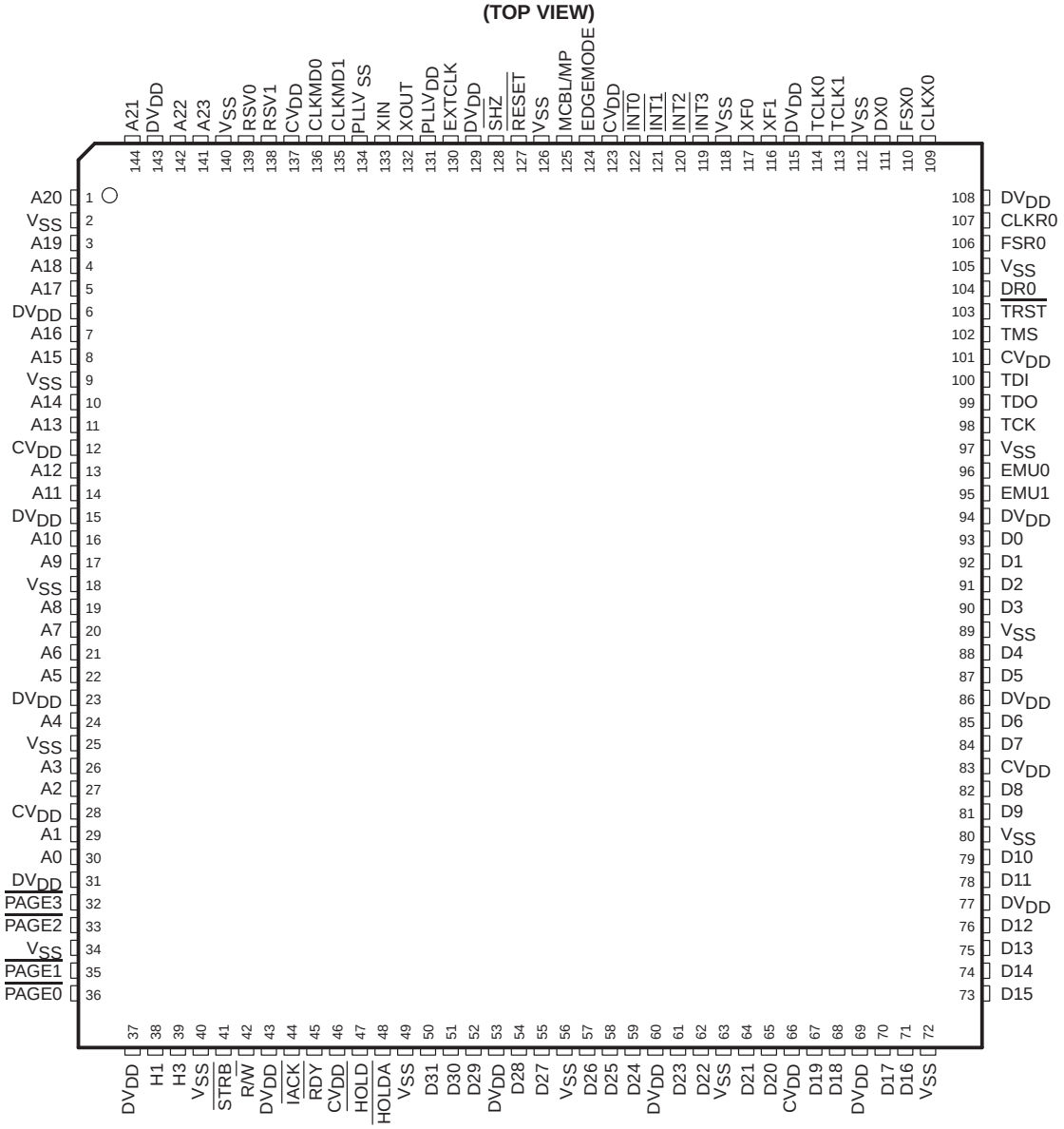
PRODUCT PREVIEW

description (continued)

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The TMS320C3x supports a wide variety of system applications from host processor to dedicated coprocessor. High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

TMS320VC33 pinout (top view)

TMS320VC33 PGE PACKAGE†‡
(TOP VIEW)



† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.
‡ $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

The TMS320VC33 device is packaged in 144-pin thin quad flatpacks (PGE Suffix).

TMS320VC33 Terminal Assignments (Alphabetical)

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER#
A0	30	D0	93		31	R/$\overline{W}$	42
A1	29	D1	92		37	$\overline{RDY}$	45
A2	27	D2	91		43	$\overline{RESET}$	127
A3	26	D3	90		53	RSV0	139
A4	24	D4	88		60	RSV1	138
A5	22	D5	87		69	$\overline{SHZ}$	128
A6	21	D6	85	DV_{DD}†	77	$\overline{STRB}$	41
A7	20	D7	84		86	TCK	98
A8	19	D8	82		94	TCLK0	114
A9	17	D9	81		108	TCLK1	113
A10	16	D10	79		115	TDI	100
A11	14	D11	78		129	TDO	99
A12	13	D12	76		143	TMS	102
A13	11	D13	75	DX0	111	$\overline{TRST}$	103
A14	10	D14	74	EDGEMODE	124		2
A15	8	D15	73	EMU0	96		9
A16	7	D16	71	EMU1	95		18
A17	5	D17	70	EXTCLK	130		25
A18	4	D18	68	FSR0	106		34
A19	3	D19	67	FSX0	110		40
A20	1	D20	65	H1	38		49
A21	144	D21	64	H3	39		56
A22	142	D22	62	$\overline{HOLD}$	47		63
A23	141	D23	61	$\overline{HOLDA}$	48	V_{SS}	72
CLKMD0	136	D24	59	$\overline{IACK}$	44		80
CLKMD1	135	D25	58	$\overline{INT0}$	122		89
CLKR0	107	D26	57	$\overline{INT1}$	121		97
CLKX0	109	D27	55	$\overline{INT2}$	120		105
	12	D28	54	$\overline{INT3}$	119		112
	28	D29	52	MCBL/MP	125		118
	46	D30	51	$\overline{PAGE0}$	36		126
	66	D31	50	$\overline{PAGE1}$	35		140
CV_{DD}	83	DR0	104	$\overline{PAGE2}$	33	XIN	133
	101		6	$\overline{PAGE3}$	32	XOUT	132
	123	DV_{DD}	15	$PLLV_{DD}$‡	131	XF0	117
	137		23	$PLLV_{SS}$‡	134	XF1	116

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

‡ $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS} respectively.

PRODUCT PREVIEW

PRODUCT PREVIEW

TMS320VC33 Terminal Assignments† (Numerical)

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	A20	37	DV_{DD}	73	D15	109	CLKX0
2	V_{SS}	38	H1	74	D14	110	FSX0
3	A19	39	H3	75	D13	111	DX0
4	A18	40	V_{SS}	76	D12	112	V_{SS}
5	A17	41	$\overline{STRB}$	77	DV_{DD}	113	TCLK1
6	DV_{DD}	42	R/$\overline{W}$	78	D11	114	TCLK0
7	A16	43	DV_{DD}	79	D10	115	DV_{DD}
8	A15	44	$\overline{IACK}$	80	V_{SS}	116	XF1
9	V_{SS}	45	$\overline{RDY}$	81	D9	117	XF0
10	A14	46	CV_{DD}	82	D8	118	V_{SS}
11	A13	47	$\overline{HOLD}$	83	CV_{DD}	119	$\overline{INT3}$
12	CV_{DD}	48	$\overline{HOLDA}$	84	D7	120	$\overline{INT2}$
13	A12	49	V_{SS}	85	D6	121	$\overline{INT1}$
14	A11	50	D31	86	DV_{DD}	122	$\overline{INT0}$
15	DV_{DD}	51	D30	87	D5	123	CV_{DD}
16	A10	52	D29	88	D4	124	EDGEMODE
17	A9	53	DV_{DD}	89	V_{SS}	125	MCBL/MP
18	V_{SS}	54	D28	90	D3	126	V_{SS}
19	A8	55	D27	91	D2	127	$\overline{RESET}$
20	A7	56	V_{SS}	92	D1	128	$\overline{SHZ}$
21	A6	57	D26	93	D0	129	DV_{DD}
22	A5	58	D25	94	DV_{DD}	130	EXTCLK
23	DV_{DD}	59	D24	95	EMU1	131	$PLLV_{DD}$‡
24	A4	60	DV_{DD}	96	EMU0	132	XOUT
25	V_{SS}	61	D23	97	V_{SS}	133	XIN
26	A3	62	D22	98	TCK	134	$PLLV_{SS}$‡
27	A2	63	V_{SS}	99	TDO	135	CLKMD1
28	CV_{DD}	64	D21	100	TDI	136	CLKMD0
29	A1	65	D20	101	CV_{DD}	137	CV_{DD}
30	A0	66	CV_{DD}	102	TMS	138	RSV1
31	DV_{DD}	67	D19	103	$\overline{TRST}$	139	RSV0
32	$\overline{PAGE3}$	68	D18	104	DR0	140	V_{SS}
33	$\overline{PAGE2}$	69	DV_{DD}	105	V_{SS}	141	A23
34	V_{SS}	70	D17	106	FSR0	142	A22
35	$\overline{PAGE1}$	71	D16	107	CLKR0	143	DV_{DD}
36	$\overline{PAGE0}$	72	V_{SS}	108	DV_{DD}	144	A21

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

‡ $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS} respectively.

TMS320VC33 Terminal Functions

TERMINAL NAME	QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡		
PRIMARY-BUS INTERFACE						
D31–D0	32	I/O/Z	32-bit data port	S	H	R
A23–A0	24	O/Z	24-bit address port	S	H	R
R/$\overline{W}$	1	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{STRB}$	1	O/Z	Strobe. For all external-accesses	S	H	
$\overline{PAGE0}$ – $\overline{PAGE3}$	1	O/Z	Page strobes. Four decoded page strobes for external access	S	H	
$\overline{RDY}$	1	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.			
$\overline{HOLD}$	1	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.			
$\overline{HOLDA}$	1	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set.	S		
CONTROL SIGNALS						
$\overline{RESET}$	1	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.			
EDGEMODE	1	I	Edge mode. Enables interrupt edge mode detection.			
$\overline{INT3}$–$\overline{INT0}$	4	I	External interrupts			
$\overline{IACK}$	1	O/Z	Internal acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate when a section of code is being executed.	S		
MCBL/$\overline{MP}$	1	I	Microcomputer Bootloader/microprocessor mode-select			
$\overline{SHZ}$	1	I	Shutdown high impedance. When active, $\overline{SHZ}$ places all pins in the high-impedance state. $\overline{SHZ}$ can be used for board-level testing or to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S		R
SERIAL PORT 0 SIGNALS						
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S		R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S		R
DR0	1	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S		R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S		R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S		R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S		R

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
§ Recommended decoupling. Four 0.1 μF for V_{DDL} and eight 0.1 μF for V_{DDP}.

PRODUCT PREVIEW

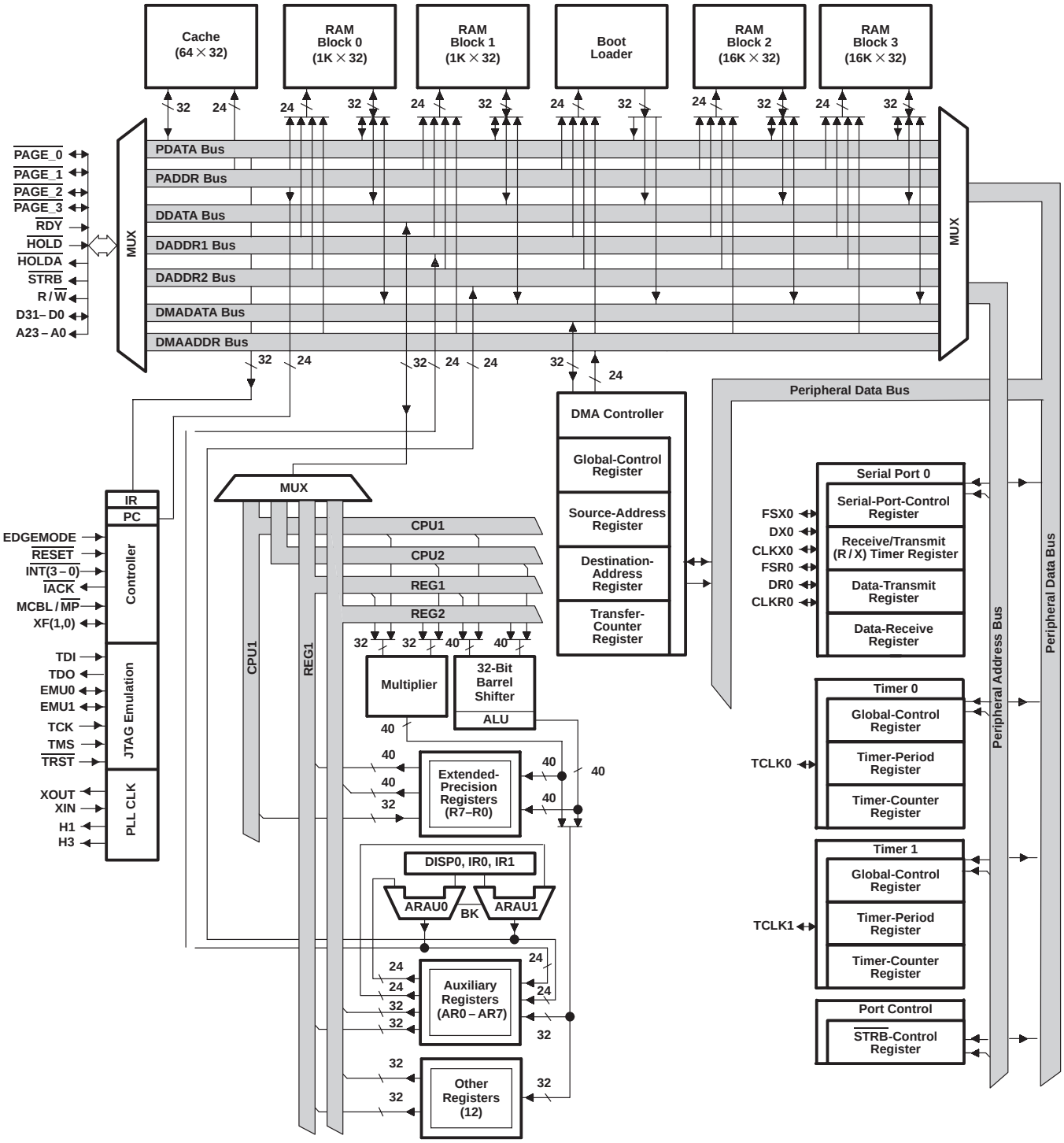
TMS320VC33 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡	
TIMER SIGNALS					
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK0 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS					
H1	1	O/Z	External H1 clock	S	
H3	1	O/Z	External H3 clock	S	
CV_{DD}	10	I	$+V_{DD}$. Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane.§		
DV_{DD}	10	I	$+V_{DD}$. Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane.§		
V_{SS}	24	I	Ground. All grounds must be connected to a common ground plane.		
$PLLV_{DD}$	1	I	Internally isolated PLL supply. Connect to CV_{DD} (1.8 V)		
$PLLV_{SS}$	1	I	Internally isolated PLL ground. Connect to V_{SS}		
EXTCLK	1	I	External clock. Logic level compatible clock input. If an oscillator is used, tie this pin to ground.		
XOUT	1	O	Clock out. Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.		
XIN	1	I	Clock in. Internal-oscillator input from a crystal. If EXTCLK is used, tie this pin to ground.		
RSV0 – RSV1	2	I	Reserved. Use individual pullups to DV_{DD}.		
JTAG EMULATION					
EMU1–EMU0	2	I	Emulation pins 0 and 1		
TDI	1	I	Test data input		
TDO	1	O	Test data output		
TCK	1	I	Test clock		
TMS	1	I	Test mode select		
$\overline{TRST}$	1	I	Test reset		

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
§ Recommended decoupling. Four 0.1 μF for V_{DDL} and eight 0.1 μF for V_{DDP}.

PRODUCT PREVIEW

functional block diagram



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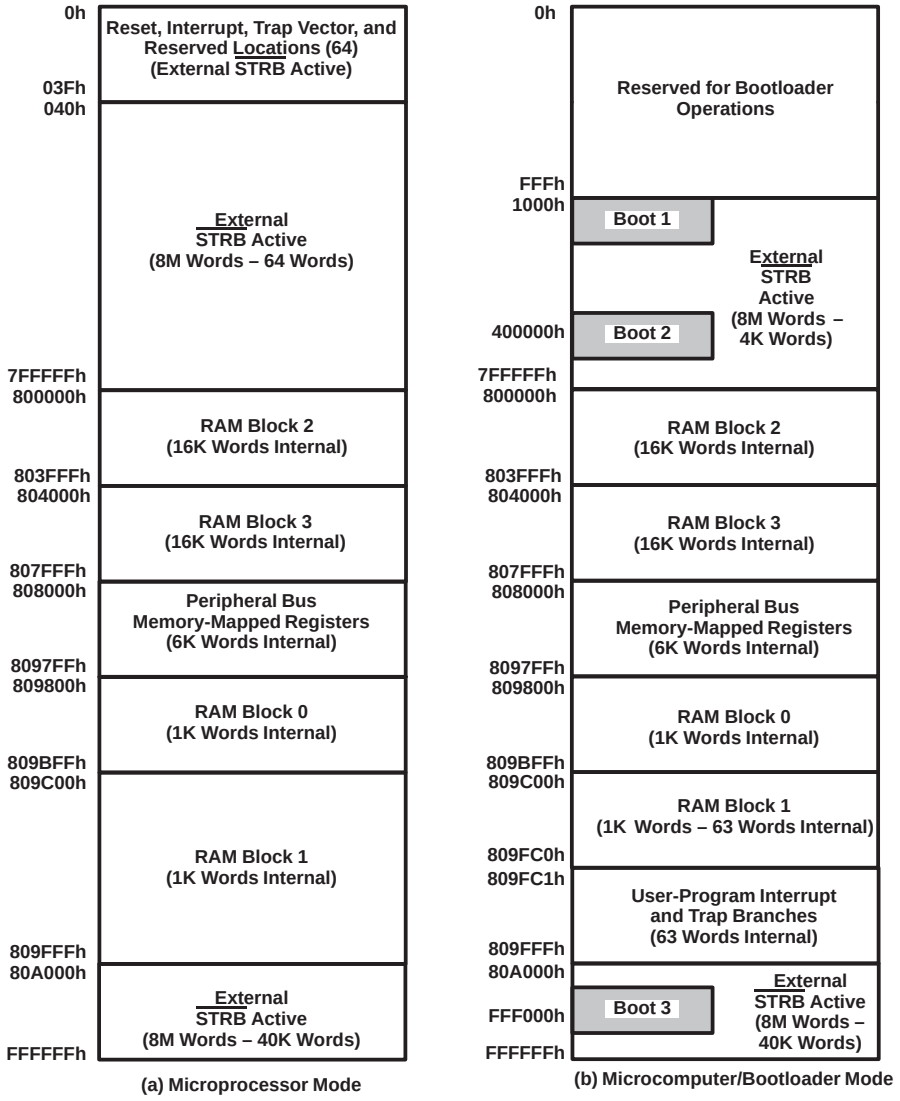
memory map



NOTE A: $\overline{\text{STRB}}$ is active over all external memory ranges. $\overline{\text{PAGE\_0}}$ to $\overline{\text{PAGE\_3}}$ are configured as external bus strobes. These are simple decoded strobes that have no configuration registers and are active only during external bus activity over the following ranges:

Name	Active range
$\overline{\text{PAGE\_0}}$	0000000h – 03FFFFFh
$\overline{\text{PAGE\_1}}$	0400000h – 07FFFFFh
$\overline{\text{PAGE\_2}}$	0800000h – 0BFFFFFh
$\overline{\text{PAGE\_3}}$	0C00000h – 0FFFFFFh
$\overline{\text{STRB}}$	0000000h – 0FFFFFFh

Figure 1. TMS320C33 Memory Maps

memory map (continued)

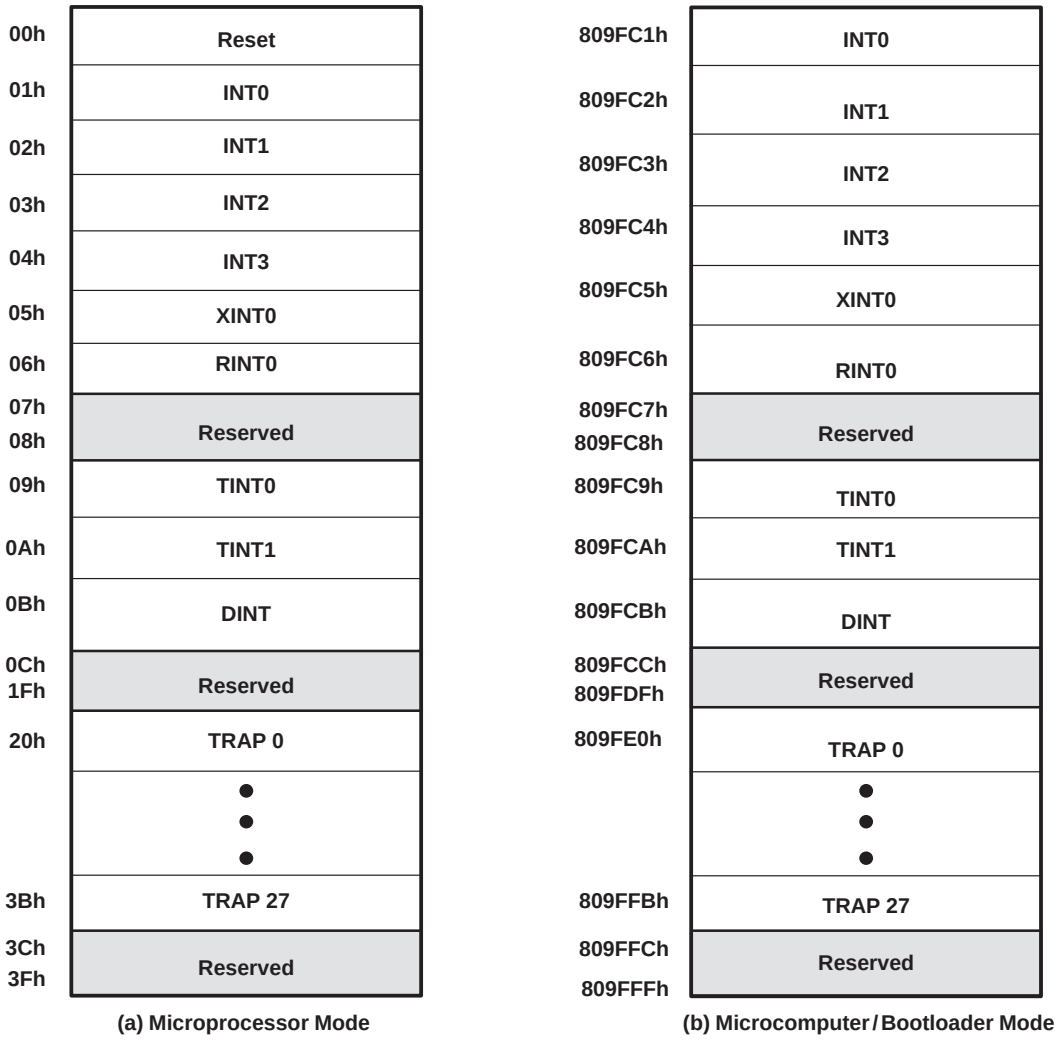


Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

PRODUCT PREVIEW

memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period Register
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Global Control
808042h	FSX/DX/CLKX Serial Port Control
808043h	FSR/DR/CLKR Serial Port Control
808044h	Serial R/X Timer Control
808045h	Serial R/X Timer Counter
808046h	Serial R/X Timer Period Register
808048h	Data-Transmit
80804Ch	Data-Receive
808064h	Primary-Bus Control

NOTE A: Shading denotes reserved address locations.

Figure 3. Peripheral Bus Memory-Mapped Registers

PRODUCT PREVIEW

clock generator

The clock generator provides clocks to the ’VC33 device, and consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided by using a crystal resonator with the internal oscillator, or from an external clock source. The PLL circuit generates the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU.The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

PLL and clock oscillator control

The clock mode control pins are decoded into four operational modes as shown in Figure 4. These modes control clock divide ratios, oscillator, and PLL power (see Table 1).

When an external clock input or crystal is connected, the opposite unused input is simply grounded. An XOR gate then passes one of the two signal sources to the PLL stage. This allows the direct injection of a clock reference into EXTCLK, or 1–20 MHz crystals and ceramic resonators with the oscillator circuit. The two clock sources include:

- A crystal oscillator circuit, where a crystal or ceramic resonator is connected across the XOUT and XIN pins and EXTCLK is grounded.
- An external clock input, where an external clock source is directly connected to the EXTCLK pin, and XOUT is left unconnected and XIN is grounded.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. The PLL is a simple x5 reference multiplier with bypass and power control.

The clock divider, under CPU control, reduces the clock reference by 1 (MAXSPEED), 1/16 (LOWPOWER), or clock stop (IDLE2). Wakeup from the IDLE2 state is accomplished by a RESET or interrupt pin logic low state.

A divide-by-two TMS320C31 equivalent mode of operation is also provided. In this case, the clock output reference is further divided by two with clock synchronization being determined by the timing of RESET falling relative to the present H1/H3 state.

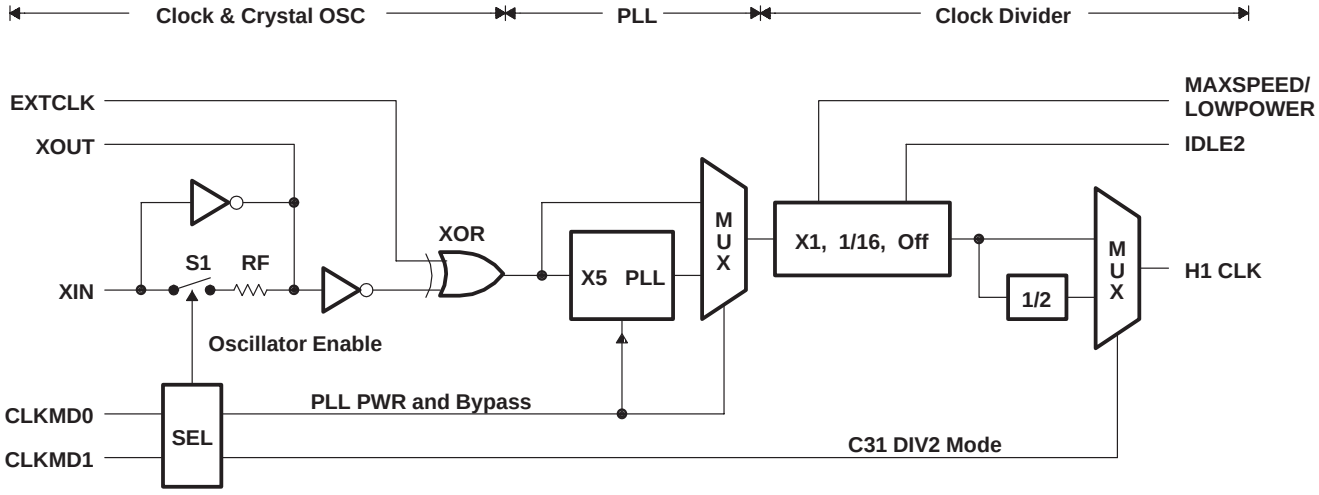


Figure 4. Clock Generation

Table 1. Clock Mode Select Pins

CLKMD0	CLKMD1	FEEDBACK	PLLPWR	RATIO	NOTES
0	0	Off	Off	1	Fully static, very low power
0	1	On	Off	1/2	Oscillator enabled
1	0	On	Off	1	Oscillator enabled
1	1	On	On	5	10 mA @ 1.8 V PLL power. Oscillator enabled

PRODUCT PREVIEW

PRODUCT PREVIEW

PLL and clock oscillator control (continued)

Typical crystals in the 8 – 30 MHz range have a series resistance of 25 Ω which increases below 8 MHz. To maintain proper filtering and phase relationships, R_d and Z_{out} of the oscillator circuit should be 10x – 40x that of the crystal. A series compensation resistor (Rd), shown in Figure 5, is recommended when using lower frequency crystals. The XOUT output, the square wave inverse of XIN, is then filtered by the XOUT output impedance, C1 load capacitor, and R_d (if present). The crystal and C2 input load capacitor then refilters this signal resulting in a XIN signal that is 30 – 80% of the oscillator supply voltage.

NOTE: Some ceramic resonators are available in a low-cost, three-terminal package that includes C1 and C2 internally. Typically ceramic resonators do not provide the frequency accuracy of crystals.

NOTE: Better PLL stability can be achieved using the optional power supply isolation circuit shown in Figure 5. A similar filter can be used to isolate the $PLLV_{SS}$, as shown in Figure 6. $PLLV_{DD}$ can also be directly connected to CV_{DD}.

Table 2. Typical Crystal Circuit Loading

FREQUENCY (MHz)	Rd (Ω)	C1 (pF)	C2 (pF)	CL† (pF)	RL† (Ω)
2	4.7K	18	18	12	200
5	2.2K	18	18	12	60
10	470	15	15	12	30
15	0	15	12	12	25
20	0	9	9	10	25

† CL and RL are typical internal series load capacitance and resistance of the crystal.

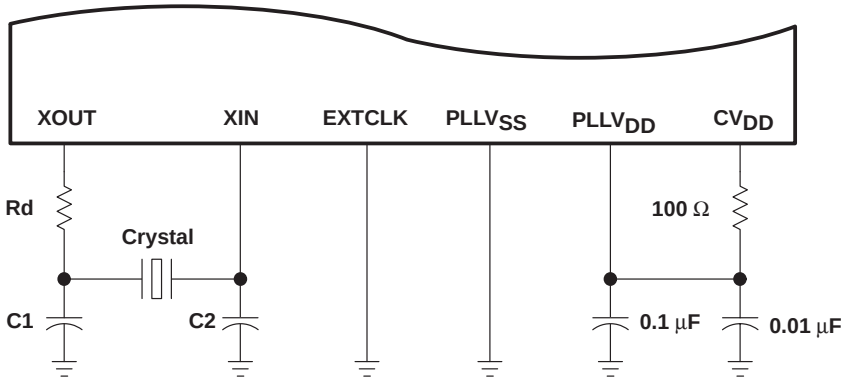


Figure 5. Self-Oscillation Mode

PLL isolation

The internal PLL supplies can be directly connected to CV_{DD} and V_{SS} (0 Ω case) or fully isolated as shown in Figure 6. The RC network prevents the PLL supplies from turning high frequency noise in the CV_{DD} and V_{SS} supplies into jitter.

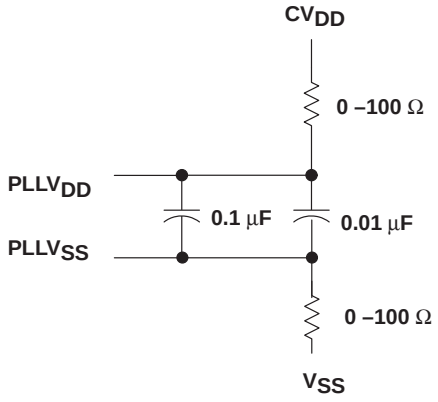


Figure 6. PLL Isolation Circuit Diagram

EDGEMODE

When EDGEMODE = 1 a sampled digital delay line is decoded to generate a pulse on the falling edge of the interrupt pin. To guarantee interrupt recognition, input signal logic high and logic low states must be held longer than the synchronizer delay of one CPU clock cycle. Holding these inputs to no less than two cycles in both the logic low and logic high states is sufficient.

When EDGEMODE = 0, a logic low interrupt pin will continually set the corresponding interrupt flag. The CPU or DMA can clear this flag within two cycles of it being set. This is the maximum interrupt width that can be applied if only one interrupt is to be recognized. The CPU can manually clear IF bits within an ISR, effectively lengthening the maximum ISR width.

After reset, EDGEMODE is temporarily disabled allowing logic low INT pins to be detected for bootload operation.

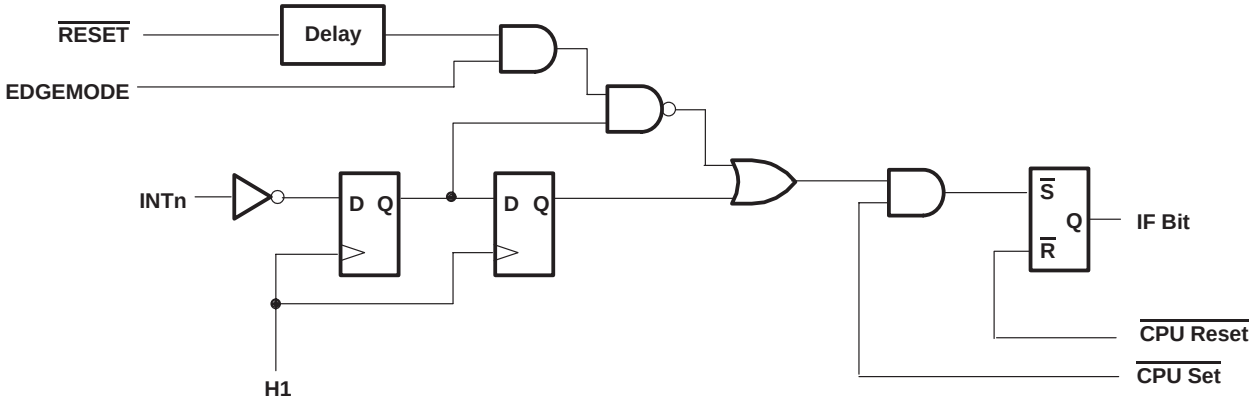


Figure 7. EDGEMODE and Interrupt Flag CIrcuit

PRODUCT PREVIEW

reset operation

When $\overline{\text{RESET}}$ is applied, the CPU attempts to safely exit any pending read or write operations that may be in progress. This can take as much as 10 CPU cycles, after which, the address, data, and control pins will be in a high-impedance state.

When both $\overline{\text{RESET}}$ and $\overline{\text{SHZ}}$ are applied, the device will immediately enter the reset state with the pins held in high impedance mode. $\overline{\text{SHZ}}$ should then be disabled at least 10 CPU cycles before $\overline{\text{RESET}}$ is set high. $\overline{\text{SHZ}}$ can be used during power-up sequencing to prevent undefined address, data, and control pins, avoiding system conflicts.

PAGE0 – PAGE3 select lines

To facilitate simpler and higher speed connection to external devices, the TMS320VC33 includes four predecoded select pins that have the same timings as $\overline{\text{STRB}}$. These pins are decoded from A22, A23, and $\overline{\text{STRB}}$ and are active only during external accesses over the ranges shown in Table 3. All external bus accesses are controlled by a single bus control register.

Table 3. PAGE0 – PAGE3 Ranges

	START	END
PAGE0	0x000000	0x3FFFFF
PAGE1	0x400000	0x7FFFFF
PAGE2	0x800000	0xBFFFFF
PAGE3	0xC00000	0xFFFFFF

PRODUCT PREVIEW

boot loader operation

When MCBL/MP = 0, an internal ROM is decoded into the address range of 0x000000–0x001000. Therefore, when reset occurs, execution begins within the internal ROM program and vector space. No external activity will be evident until one of the boot options is enabled. These options are enabled by pulling an external interrupt pin low, which the boot load software then detects, causing a particular routine to be executed (see Table 4).

Table 4. INT0 – INT3 Sources

ACTIVE INTERRUPT	ADDRESS/SOURCE WHERE BOOT DATA IS READ FROM	DATA FORMAT
INT0	0x001000	8, 16, or 32-bit width
INT1	0x400000	8, 16, or 32-bit width
INT2	0xFFF000	8, 16, or 32-bit width
INT3	Serial Port	32-bit, external clock, and frame synch

When MCBL/MP = 0, the reset and interrupt vectors are hard coded within the internal ROM. Since this is a read-only device, these vectors cannot be modified. To enable user defined interrupt routines, the internal vectors contain fixed values that point to an internal section of SRAM beginning at 0x809FC1. Code execution begins at these locations so it is important to place branch instructions (to the interrupt routine) at these locations and not vectors.

The bootloader program requires a small stack space for calls and returns. Two SRAM locations a 0x809800 and 0x809801 are used for this stack. You should not try to bootload data into these locations as it will corrupt the boot loader program run time stack. After the bootload operation is complete, your program can reclaim these locations. The simplest solution is to begin your programs uninitialized data section at this location.

For additional detail on boot loader operation including the boot loader source code, see the *TMS320C3x Users Guide* (literature number SPRU031).

PRODUCT PREVIEW

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, DV_{DD} (see Note 1) . . . . . –0.3 V to 4 V
Supply voltage range, CV_{DD} (see Note 1) . . . . . –0.3 V to 2 V
Input voltage range, V_I . . . . . –0.3 V to 4.5 V
Output voltage range, V_O . . . . . –0.3 V to 4.5 V
Continuous power dissipation (worst case) (see Note 2) . . . . . 500 mW (for TMS320VC33-150)
Operating case temperature range, T_C PQL (commercial) . . . . . 0°C to 85°C
PQA (industrial) . . . . . – 40°C to 125°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. Actual operating power is much lower. This value was obtained under specially produced worst-case test conditions for the TMS320VC33, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external data and address buses at the maximum possible rate with a capacitive load of 30 pF. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 3 and Note 4)

		MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage for the core CPU	1.71	1.8	1.89	V
DV_{DD}	Supply voltage for the I/O pins	3	3.3	3.6	V
V_{SS}	Supply ground		0		V
V_{IH}	High-level input voltage	0.7 * DV_{DD}		DV_{DD} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3‡		0.3 * DV_{DD}	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current			4	mA
T_C	Operating case temperature (commercial)	0		85	°C
	Operating case temperature (industrial)				
C_L	Capacitive load per output pin			30	pF

NOTES: 3. All voltage values are with respect to V_{SS}. EXTCLK can be driven by a CMOS clock.
4. All inputs and I/O pins configured as inputs, except $\overline{SHZ}$ and D0–D31, use Schmidt hysteresis inputs. Hysteresis is approximately 10% of DV_{DD} and is centered at 0.5 * DV_{DD}.

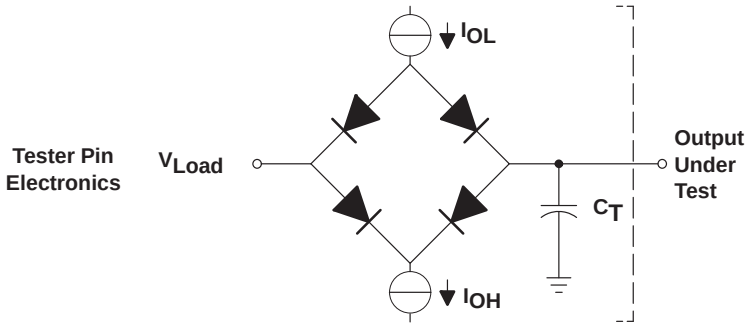
PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 3)†

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = MIN, I_{OH} = MAX			2.4			V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OH} = MAX					0.4	V
I_Z	High-impedance current	V_{DD} = MAX			– 5		+ 5	µA
I_I	Input current	V_I = V_{SS} to V_{DD}			– 5		+ 5	µA
I_{IPU}	Input current (with internal pullup)	Inputs with internal pullups§			– 600		10	µA
I_{IPD}	Input current (with internal pulldown)	Inputs with internal pulldowns			600		– 10	µA
I_{BKU}	Input current (with bus keeper) pullup¶	Bus keeper opposes until conditions match			– 600		10	µA
I_{BKD}	Input current (with bus keeper) pulldown¶				600		– 10	µA
I_{DDD}	Supply current, pins#‖	T_A = 25°C, DV_{DD} = MAX	f_x = 60 MHz	'VC33-120		20	120	mA
			f_x = 75 MHz	'VC33-150		25	150	
I_{DDC}	Supply current, core CPU#‖	T_A = 25°C, CV_{DD} = MAX	f_x = 60 MHz	'VC33-120		40	50	mA
			f_x = 75 MHz	'VC33-150		45	60	
I_{DD}	IDLE2, Supply current, I_{DDD} plus I_{DDC}	PLL enabled, oscillator enabled				10		mA
		PLL disabled, oscillator enabled				500		µA
		PLL disabled, oscillator disabled, FCLK = 0				50		
C_i	Input capacitance	All inputs except XIN					10	pF
		XIN					10	
C_o	Output capacitance						10	pF

† All input and output voltage levels are TTL compatible.
‡ For 'VC33, all typical values are at DV_{DD} = 3.3, CV_{DD} = 1.8 V, T_A (air temperature) = 25°C.
§ Pins with internal pullup devices: TDI, TCK, and TMS. Pin with internal pulldown device: $\overline{TRST}$.
¶ Pins D0–D31 include internal bus keepers to maintain valid logic levels when the bus is not driven.
# Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).
‖ f_x is the PLL output clock frequency.
NOTE 3: All voltage values are with respect to V_{SS}. EXTCLK can be driven by a CMOS clock.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 4 mA (all outputs)
I_{OH} = 4 mA (all outputs)
V_{LOAD} = $DV_{DD}/2$
C_T = 30-pF typical load-circuit capacitance

Figure 8. TMS320VC33 Test Load Circuit

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23–A0	H	H1 and H3
ASYNCH	Asynchronous reset signals	HOLD	$\overline{\text{HOLD}}$
C	CLKX0	HOLDA	$\overline{\text{HOLDA}}$
CI	CLKIN	IACK	$\overline{\text{IACK}}$
CLKR	CLKR0	INT	$\overline{\text{INT3}}$–$\overline{\text{INT0}}$
CONTROL	Control signals	PAGE	$\overline{\text{PAGE0}}$–$\overline{\text{PAGE3}}$
D	D31–D0	RDY	$\overline{\text{RDY}}$
DR	DR	RW	R/$\overline{\text{W}}$
DX	DX	RESET	$\overline{\text{RESET}}$
FS	FSX/R	S	$\overline{\text{STRB}}$
FSX	FSX0	SCK	CLKX/R
FSR	FSR0	SHZ	$\overline{\text{SHZ}}$
GPI	General-purpose input	TCLK	TCLK0, TCLK1, or TCLKx
GPIO	General-purpose input/output; peripheral pin	XF	XF0, XF1, or XFx
GPO	General-purpose output	XFIO	XFx switching from input to output

PRODUCT PREVIEW

timing

Timing specifications apply to the TMS320VC33.

EXTCLK, H1, and H3 timing

The following table defines the timing parameters for the EXTCLK, H1, and H3 interface signals. The numbers shown in Figure 9 and Figure 10 correspond with those in the number (NO.) column of the table below.

timing parameters for EXTCLK, H1, and H3 in 'C31 divide-by-2 mode† (see Figure 9 and Figure 10)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		1		1	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low $t_{c(CI)}$ = min (time below V_{IL})	4		4		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high $t_{c(CI)}$ = min (time above V_{IH})	4		4		ns
4	$t_{r(CI)}$	Rise time, CLKIN		1		1	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	10		10		ns
6	$t_{f(H)}$	Fall time, H1 and H3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1 and H3 low	$t_{c(CL)} - 2$	$t_{c(CL)} + 2$	$t_{c(CL)} - 2$	$t_{c(CL)} + 2$	ns
8	$t_{w(HH)}$	Pulse duration, H1 and H3 high	$t_{c(CL)} - 2$	$t_{c(CL)} + 2$	$t_{c(CL)} - 2$	$t_{c(CL)} + 2$	ns
9	$t_{r(H)}$	Rise time, H1 and H3		3		3	ns
10	$t_{d(HL-HH)}$	Delay time. from H1 low to H3 high or from H3 low to H1 high	–1.5	1.5	–1.5	1.5	ns
11	$t_{c(H)}$	Cycle time, H1 and H3	$2 * t_{c(CL)}$			$2 * t_{c(CL)}$	ns

† Similar loading characteristics must be used on all pins.

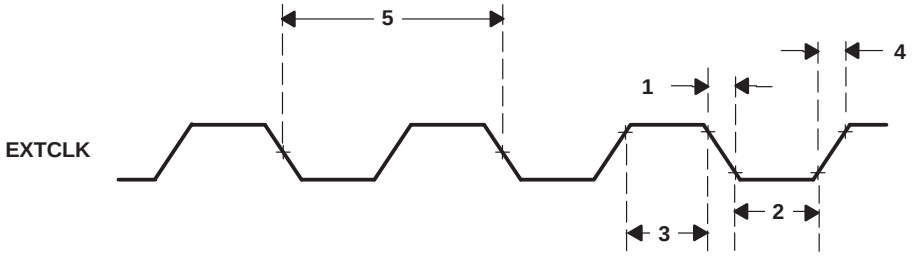


Figure 9. Timing for EXTCLK

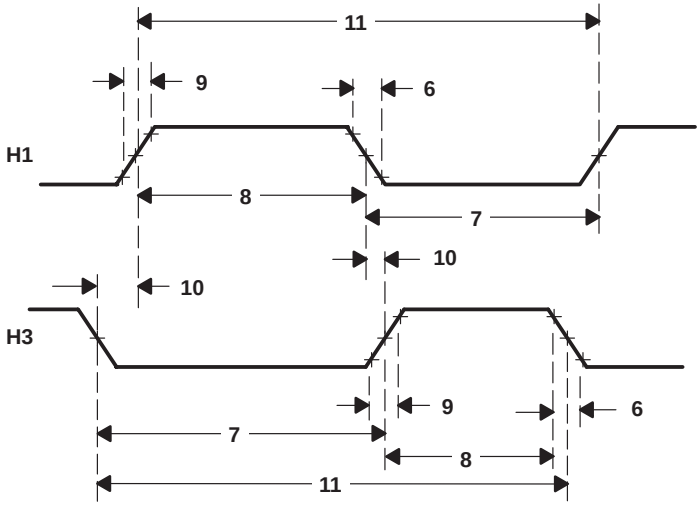


Figure 10. Timing for H1 and H3

PRODUCT PREVIEW

PRODUCT PREVIEW

clock circuit timing

The following table defines the timing parameters for the clock circuit signals.

timing and circuit parameters for on-chip crystal oscillator† (see Figure 11)

		MIN	TYP	MAX	UNIT
V_O	Oscillator internal supply voltage		CV_{DD}		V
F_O	Fundamental mode frequency range	5		20	MHz
V_{bias}	DC bias point (input threshold)	40	50	60	$\%V_O$
R_{fbk}	Feedback resistance	100	300	500	KΩ
R_{out}	Small signal AC output impedance	250	500	1000	Ω
V_{xoutac}	AC output voltage with test crystal‡		80		$\%V_O$
V_{xinac}	AC input voltage with test crystal‡		50		$\%V_O$
V_{xoutl}	$V_{xin} = V_{xinh}$, I_{xout} = 0, F_O=0 (logic input)	V_{SS} – 0.1		V_{SS} + 0.3	V
V_{xouth}	$V_{xin} = V_{xinl}$, I_{xout} = 0, F_O=0 (logic input)	CV_{DD} – 0.3		CV_{DD} + 0.1	V
V_{inl}	When used for logic level input, oscillator enabled	–0.3		0.2 * V_O	V
V_{inh}	When used for logic level input, oscillator enabled	0.8 * V_O		DV_{DD} + 0.3	V
V_{xinh}	When used for logic level input, oscillator disabled	0.7 * DV_{DD}		DV_{DD} + 0.3	V
C_{xout}	XOUT internal load capacitance	2	3	5	pF
C_{xin}	XIN internal load capacitance	2	3	5	pF
$t_{d(XIN-H1)}$	Delay time, XIN to H1 x1 and x0.5 modes		9	12	ns
I_{inl}	Input current, feedback enabled, V_{il} = 0			50	µA
I_{inh}	Input current, feedback enabled, $V_{il} = V_{ih}$			–50	µA

† This circuit is intended for fundamental mode operation.
‡ Signal amplitude is dependent on the crystal and load used.

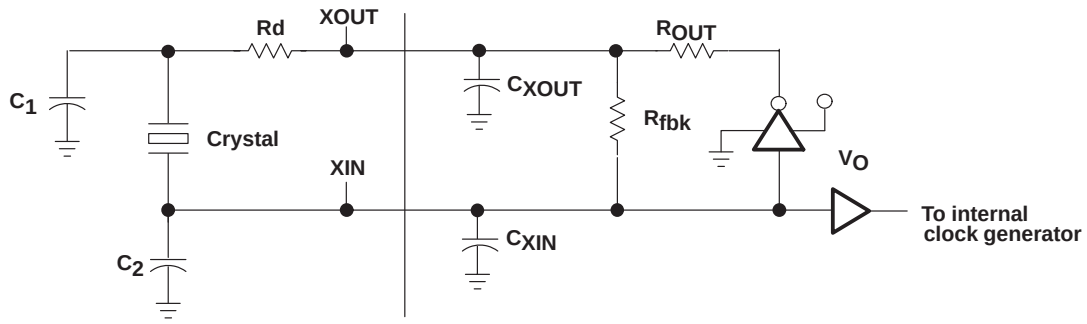


Figure 11. On-Chip Oscillator Circuit

clock circuit timing (continued)

The following table defines the timing parameters for EXTCLK.

timing and circuit parameters for EXTCLK, all modes (see Figure 12 and Figure 13)

NO.				MIN	TYP	MAX	UNIT
5a	F_{ext}	Frequency range, $1/t_{c(H)}$, 'VC33-120	x5 mode	5		12	MHz
			x1 mode	0		60	
			x0.5 mode	0		100	
		Frequency range, $1/t_{c(H)}$, 'VC33-150	x5 mode	5		15	
			x1 mode	0		75	
			x1 mode	0		100	
	V_{mid}	Mid level, used to measure duty cycle			0.5*DV_{DD}		V
4	T_r	Rise time	$F=F_{max}$, x0.5 and x1 mode			1	ns
			$F<F_{max}$			4	
1	T_r	Fall time	$F=F_{max}$, x0.5 and x1 mode			1	ns
			$F<F_{max}$			4	
2	T_{lo}	V_{il} pulse time	x5 mode	21			ns
			x1 mode	5.5			
			x0.5 mode	4.0			
3	T_{hi}	V_{ih} pulse time	x5 mode	21			ns
			x1 mode	5.5			
			x0.5 mode	4.0			
5b	EXTCLKDC	Input duty cycle	x5 PLL mode	40		60	%
			x1 and x0.5 mode, F=max	45		55	
			x1 and x0.5 mode, F=0 Hz	0		100	
10b	$td_{(EXTCLK-H1)}$	Delay time, EXTCLK to H1	x1 mode		7	10	ns
			x0.5 mode		9	12	

phase-locked loop characteristics using EXTCLK or on-chip crystal oscillator†

		MIN	TYP	MAX	UNIT
F_{pllin}	Frequency range, PLL input	5		15	MHz
F_{pllout}	Frequency range, PLL output	25		75	MHz
I_{pll}	PLL current, CV_{DD} supply			10	mA
P_{pll}	PLL power, CV_{DD} supply			20	mW
PLL_{dc}	PLL output duty cycle at H1	45		55	%
PLLJ	PLL output jitter, F_{pllout} = 25 MHz			100	pS

† Duty cycle is defined as $100*t_1/(t_1+t_2)$%

PRODUCT PREVIEW

clock circuit timing (continued)

To ensure clean internal clock references, the minimal low and high pulse duration must be maintained. At high frequencies this may require a fast rise and fall time as well as a tightly controlled duty cycle. At lower frequencies these requirements are less restrictive when in x1 and x0.5 modes. The PLL, however, must have an input duty cycle of between 40% and 60% for proper operation.

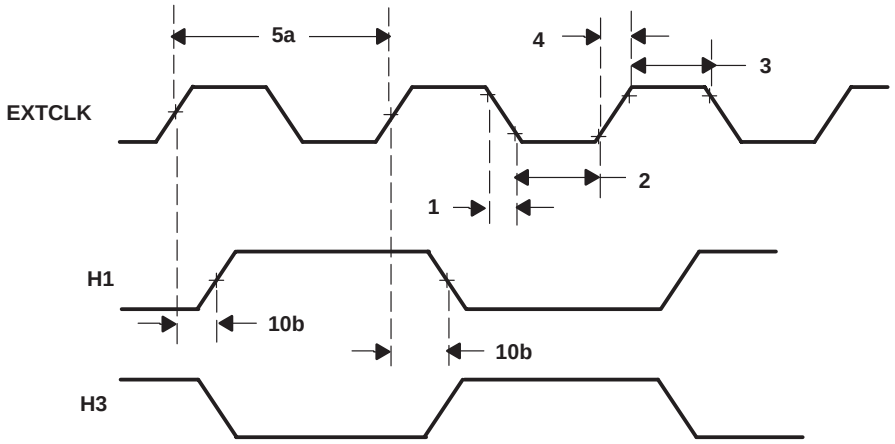


Figure 12. Divide-By-Two Mode

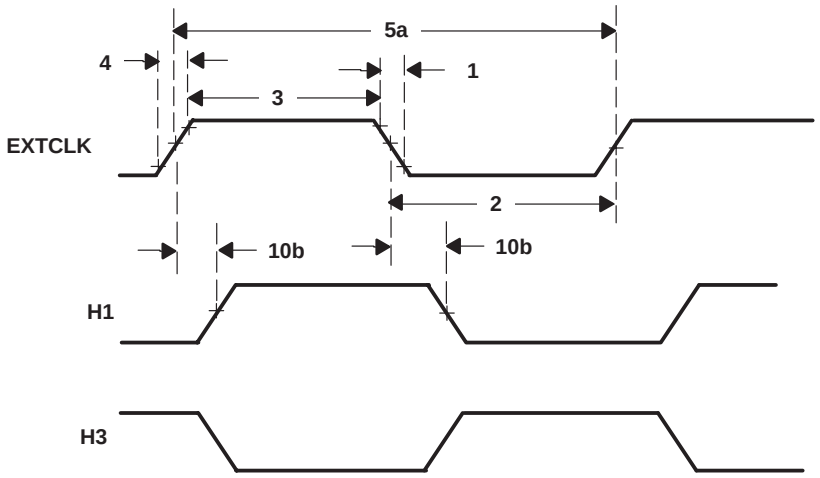


Figure 13. Divide-By-One Mode

PRODUCT PREVIEW

memory read/write timing

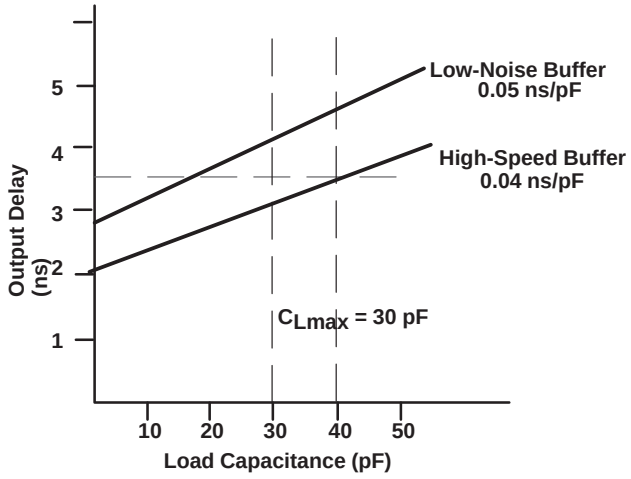
The following table defines memory read/write timing parameters for $\overline{\text{STRB}}$. The numbers shown in Figure 15 and Figure 16 correspond with those in the NO. column of the table below.

timing parameters for memory ($\overline{\text{STRB}}$ = 0) read/write† (see Figure 14, Figure 15, and Figure 16)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
12	$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{\text{STRB}}$ low	0	4	0	3	ns
13	$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{\text{STRB}}$ high	0	4	0	3	ns
14	$t_{d(H1H-RWL)R}$	Delay time, H1 high to R/$\overline{\text{W}}$ low (read)	0	4	0	3	ns
15	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0	4	0	3	ns
16	$t_{su(D-H1L)R}$	Setup time, D before H1 low (read)	6		5		ns
17	$t_{h(H1L-D)R}$	Hold time, D after H1 low (read)	1		1		ns
18	$t_{su(RDY-H1H)}$	Setup time, $\overline{\text{RDY}}$ before H1 high	5		4		ns
19	$t_{h(H1H-RDY)}$	Hold time, $\overline{\text{RDY}}$ after H1 high	0		0		ns
20	$t_{d(H1H-RWH)W}$	Delay time, H1 high to R/$\overline{\text{W}}$ high (write)		4		3	ns
21	$t_{v(H1L-D)W}$	Valid time, D after H1 low (write)		7		6	ns
22	$t_{h(H1H-D)W}$	Hold time, D after H1 high (write)	0	7	0	6	ns
23	$t_{d(H1H-A)W}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		4		3	ns
24	$t_{d(A-RDY)}$	Delay time, $\overline{\text{RDY}}$ from A valid		P–6‡		P–5‡	ns
24A	T_{aa}	Address valid to data valid (read), 0 wait state, C_L = 30 pF		9		6	ns
24B	T_{aa}	Address valid to data valid (read), 1 wait state		24.6		19.3	ns

† These timings assume a similar loading of 30 pF on all pins.
‡ P = $t_{c(CL)}$

Output load characteristics for high-speed and low-speed (low-noise) output buffers are shown in Figure 14. High-speed buffers are used on A0 – A23, $\overline{\text{PAGE0}}$ – $\overline{\text{PAGE3}}$, H1, H3, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$. All other outputs use the low-speed, (low-noise) output buffer.

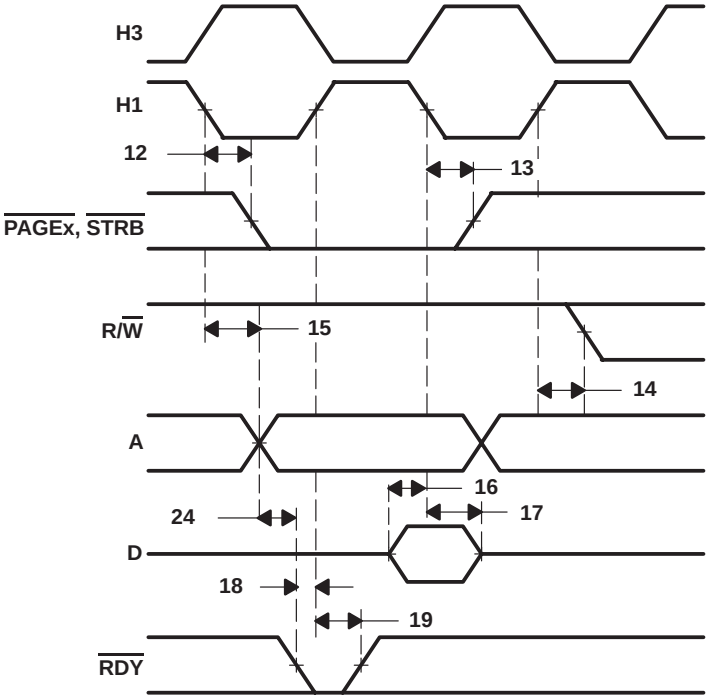


LOAD	HIGH SPEED	LOW NOISE
0 pF	2.0	2.8
15 pF	2.6	3.4
30 pF	3.2	4.4
50 pF	4.0	5.25

Figure 14. Output Load Characteristics, Buffer Only

PRODUCT PREVIEW

memory read/write timing (continued)



NOTE A: STRB remains low during back-to-back read operations.

Figure 15. Timing for Memory (STRB = 0 and PAGEx = 0) Read

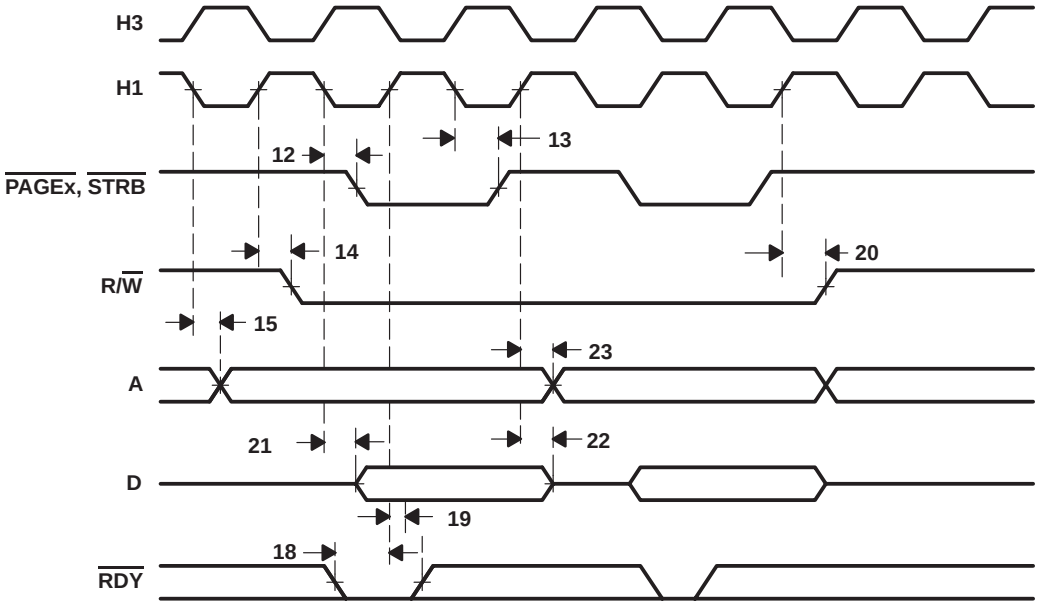


Figure 16. Timing for Memory (STRB = 0 and PAGEx = 0) Write

PRODUCT PREVIEW

XF0 and XF1 timing when executing LDFI or LDII

The following tables define the timing parameters for XF0 and XF1 during execution of LDFI or LDII. The numbers shown in Figure 17 correspond with those in the NO. column of the tables below.

timing parameters for XF0 and XF1 when executing LDFI or LDII for TMS320VC33 (see Figure 17)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
25	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		5		4	ns
26	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	6		5		ns
27	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		ns

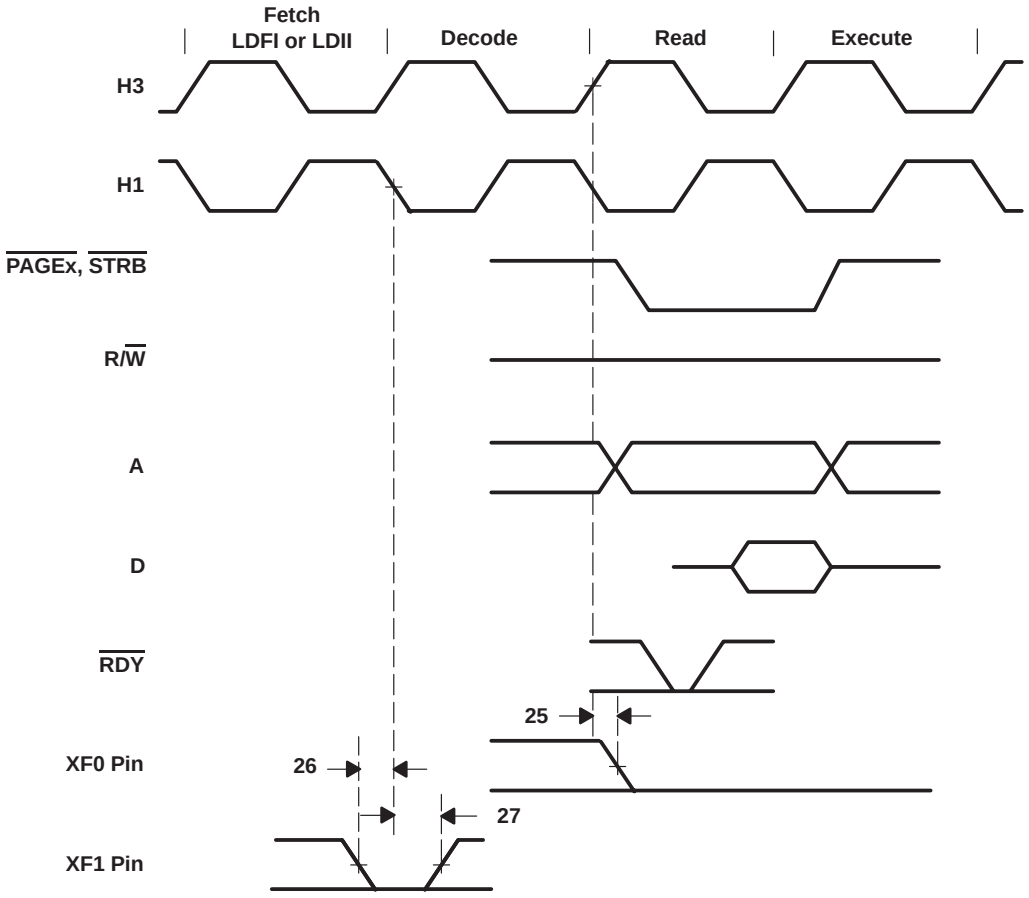


Figure 17. Timing for XF0 and XF1 When Executing LDFI or LDII

PRODUCT PREVIEW

XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII. The number shown in Figure 18 corresponds with the number in the NO. column of the table below.

timing parameters for XF0 when executing STFI or STII (see Figure 18)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
28	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high†		5		4	ns

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

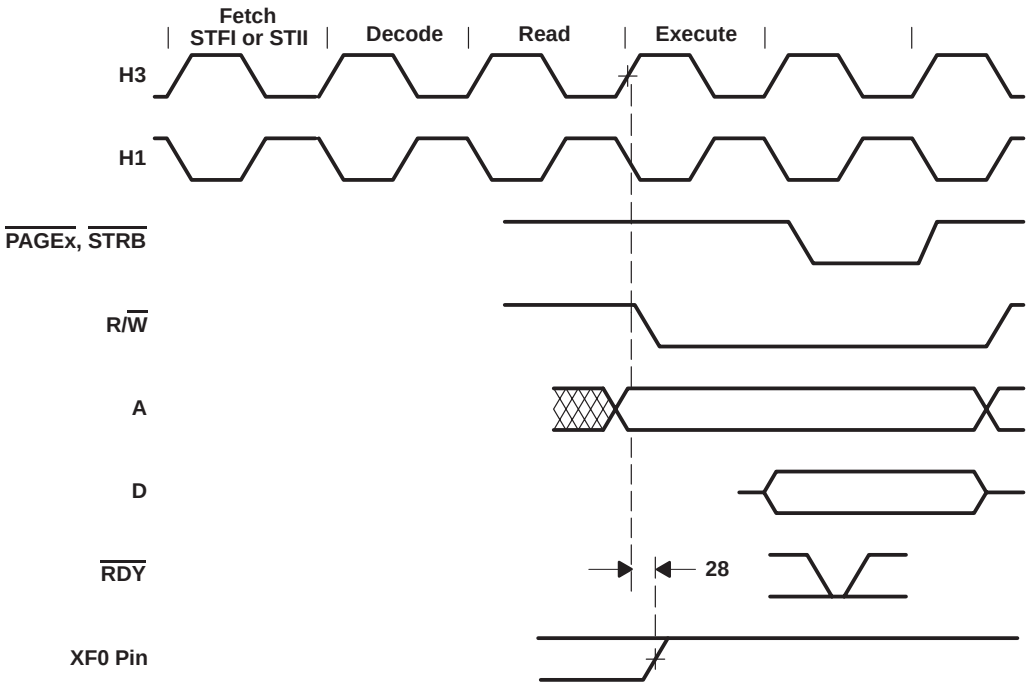


Figure 18. Timing for XF0 When Executing an STFI or STII

PRODUCT PREVIEW

XF0 and XF1 timing when executing SIGI

The following tables define the timing parameters for the XF0 and XF1 pins during execution of SIGI. The numbers shown in Figure 19 correspond with those in the NO. column of the tables below.

timing parameters for XF0 and XF1 when executing SIGI (see Figure 19)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
29	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		5		4	ns
30	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		5		4	ns
31	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	6		5		ns
32	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		ns

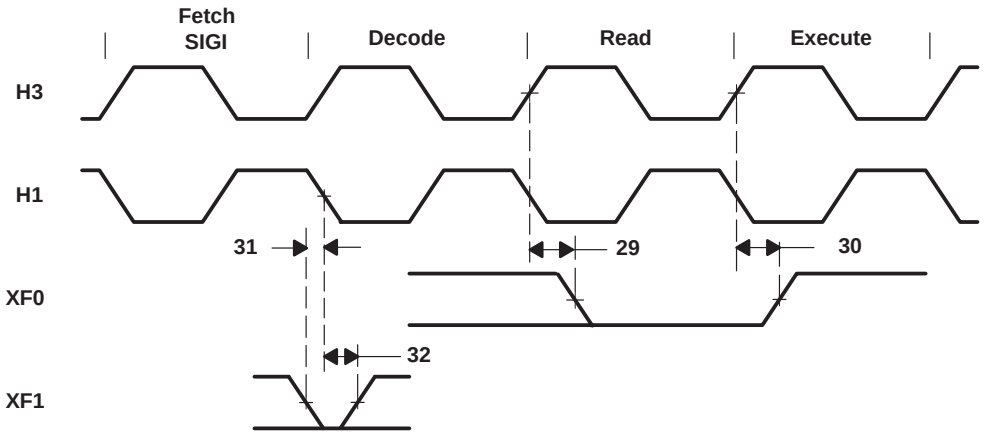


Figure 19. Timing for XF0 and XF1 When Executing SIGI

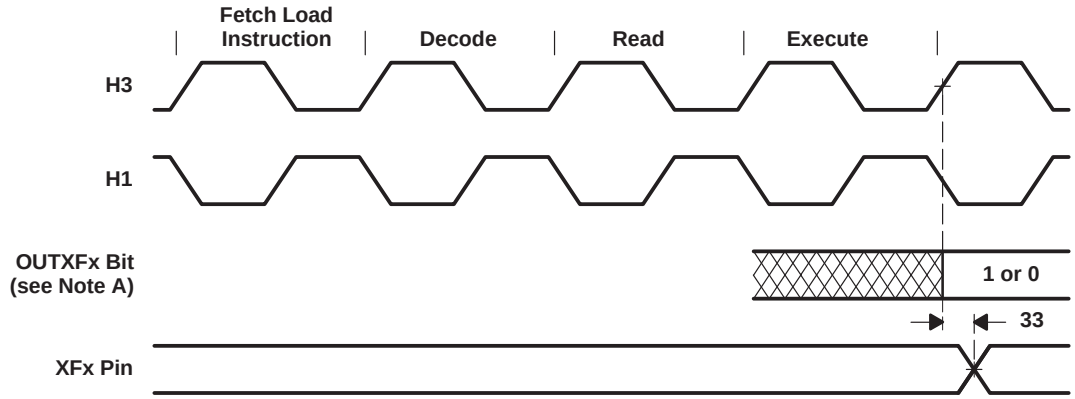
PRODUCT PREVIEW

loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output. The number shown in Figure 20 corresponds with the number in the NO. column of the table below.

timing parameters for loading the XF register when configured as an output pin (see Figure 20)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
33	$t_{v(H3H-XF)}$	Valid time, H3 high to XFx		5		4	ns



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 20. Timing for Loading XF Register When Configured as an Output Pin

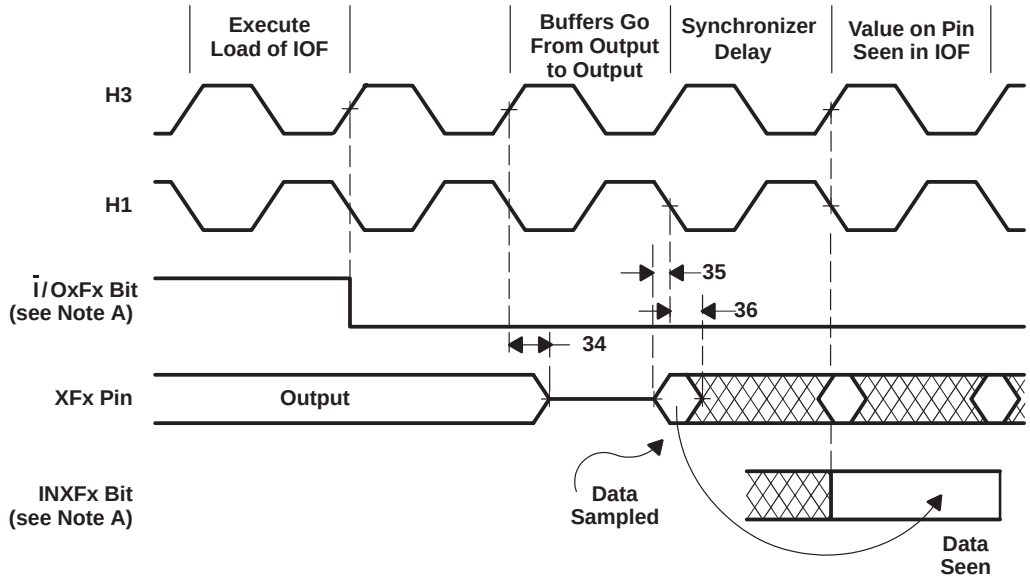
PRODUCT PREVIEW

changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin. The numbers shown in Figure 21 correspond with those in the NO. column of the table below.

timing parameters of XFx changing from output to input mode (see Figure 21)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
34	$t_{h(H3H-XF)}$	Hold time, XFx after H3 high		6		5	ns
35	$t_{su(XF-H1L)}$	Setup time, XFx before H1 low	5		4		ns
36	$t_{h(H1L-XF)}$	Hold time, XFx after H1 low	0		0		ns



NOTE A: I/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

Figure 21. Timing for Change of XFx From Output to Input Mode

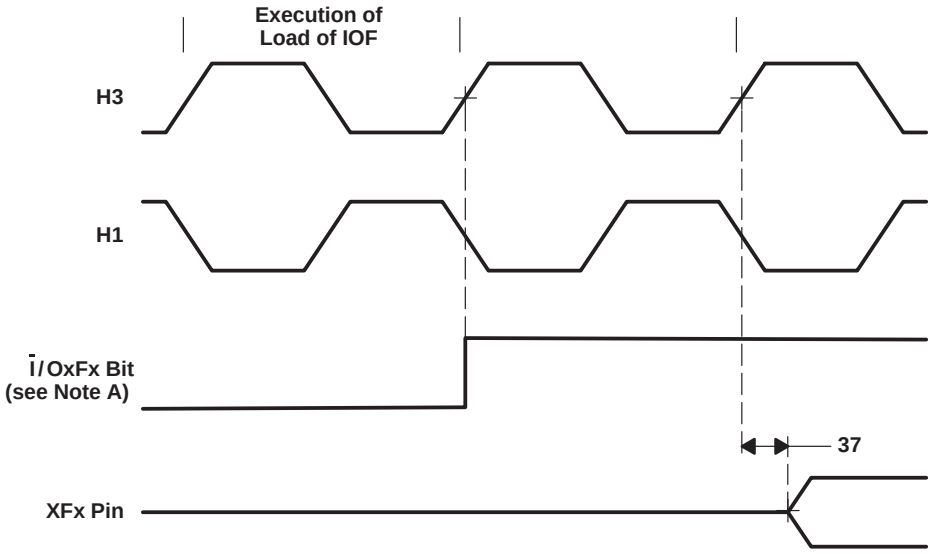
PRODUCT PREVIEW

changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin. The number shown in Figure 22 corresponds with the number in the NO. column of the table below.

timing parameters of XFx changing from input to output mode (see Figure 22)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
37	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XFx switching from input to output		6		5	ns



NOTE A: Ī/OxFx represents either bit 1 or bit 5 of the IOF register.

Figure 22. Timing for Change of XFx From Input to Output Mode

reset timing

$\overline{\text{RESET}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 23 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

The following table defines the timing parameters for the $\overline{\text{RESET}}$ signal. The numbers shown in Figure 23 correspond with those in the NO. column of the following table.

Resetting the device initializes the bus control register to seven software wait states and therefore results in slow external accesses until these registers are initialized.

$\overline{\text{HOLD}}$ is a synchronous input that can be asserted during reset. It can take nine CPU cycles before $\overline{\text{HOLDA}}$ is granted.

PRODUCT PREVIEW

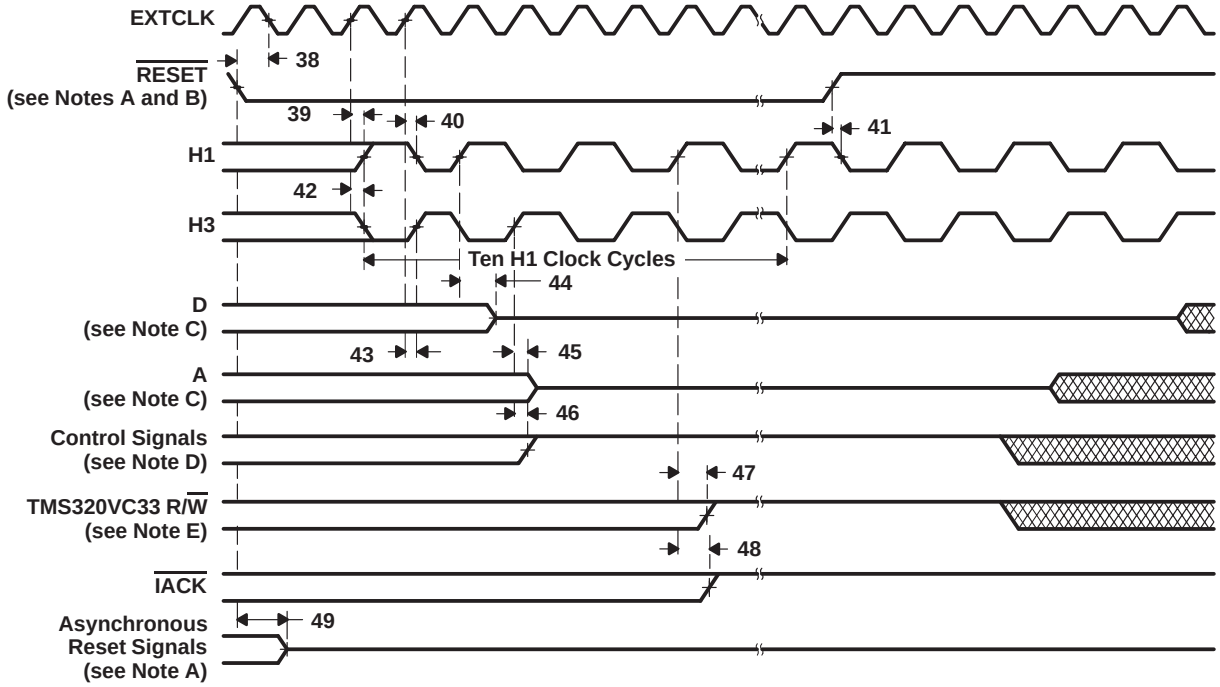
timing parameters for $\overline{\text{RESET}}$ for the TMS320VC33 (see Figure 23)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
38	$t_{su(RESET-CIL)}$	Setup time, $\overline{\text{RESET}}$ before EXTCLK low	8	P†	7		ns
39	$t_{d(CLKINH-H1H)}$	Delay time, EXTCLK high to H1 high	2	8	2	7	ns
40	$t_{d(CLKINH-H1L)}$	Delay time, EXTCLK high to H1 low	2	8	2	7	ns
41	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	6		5		ns
42	$t_{d(CLKINH-H3L)}$	Delay time, EXTCLK high to H3 low	2	8	2	7	ns
43	$t_{d(CLKINH-H3H)}$	Delay time, EXTCLK high to H3 high	2	8	2	7	ns
44	$t_{dis(H1H-DZ)}$	Disable time, H1 high to D (high impedance)		7		6	ns
45	$t_{dis(H3H-AZ)}$	Disable time, H3 high to A (high impedance)		7		6	ns
46	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		7		6	ns
47	$t_{d(H1H-RWH)}$	Delay time, H1 high to R/$\overline{\text{W}}$ high		7		6	ns
48	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		7		6	ns
49	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals disabled (high impedance)		8		7	ns

† $P = t_{c(CL)}$

PRODUCT PREVIEW

timing parameters for $\overline{\text{RESET}}$ for the TMS320VC33 (continued)



NOTES: A. Clock circuit is configured in ’C31 compatible divide-by-2 mode. If configured for x1 mode, EXTCLK directly drives H1.
B. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
C. $\overline{\text{RESET}}$ is a synchronous input that can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
D. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
E. Control signals include $\overline{\text{STRB}}$ and $\overline{\text{PAGE\_x}}$.
F. The R/$\overline{\text{W}}$ outputs are placed in a high-impedance state during reset and can require a resistive pullup, nominally 18–22 kΩ, if not, undesirable spurious writes can occur when these outputs are driven.

Figure 23. Timing for $\overline{\text{RESET}}$

PRODUCT PREVIEW

interrupt response timing

The following table defines the timing parameters for the $\overline{\text{INT}}$ signals. The numbers shown in Figure 24 correspond with those in the NO. column of the table below.

timing parameters for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ response (see Figure 24)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
50	$t_{su(INT-H1L)}$	Setup time, $\overline{\text{INT3}}$– $\overline{\text{INT0}}$ before H1 low	6		5		ns
51	$t_{w(INT)}$	Pulse duration, interrupt to ensure only one interrupt	P†	2P†	P†	2P†	ns

† $P = t_{c(CL)}$

The interrupt ($\overline{\text{INT}}$) pins are synchronized inputs that can be asserted at any time during a clock cycle. The TMS320C3x interrupts are selectable as level- or edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of the internal H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt when level mode is selected, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

When EDGEMODE=1, the falling edge of the INT0–INT3 pins are detected using synchronous logic (see Figure 7). The pulse low and high time should be two CPU clocks or greater.

The TMS320C3x can set the interrupt flag from the same source as quickly as two H1 clock cycles after it has been cleared.

If the specified timings are met, the exact sequence shown in Figure 24 occurs; otherwise, an additional delay of one clock cycle is possible.

PRODUCT PREVIEW

interrupt response timing (continued)

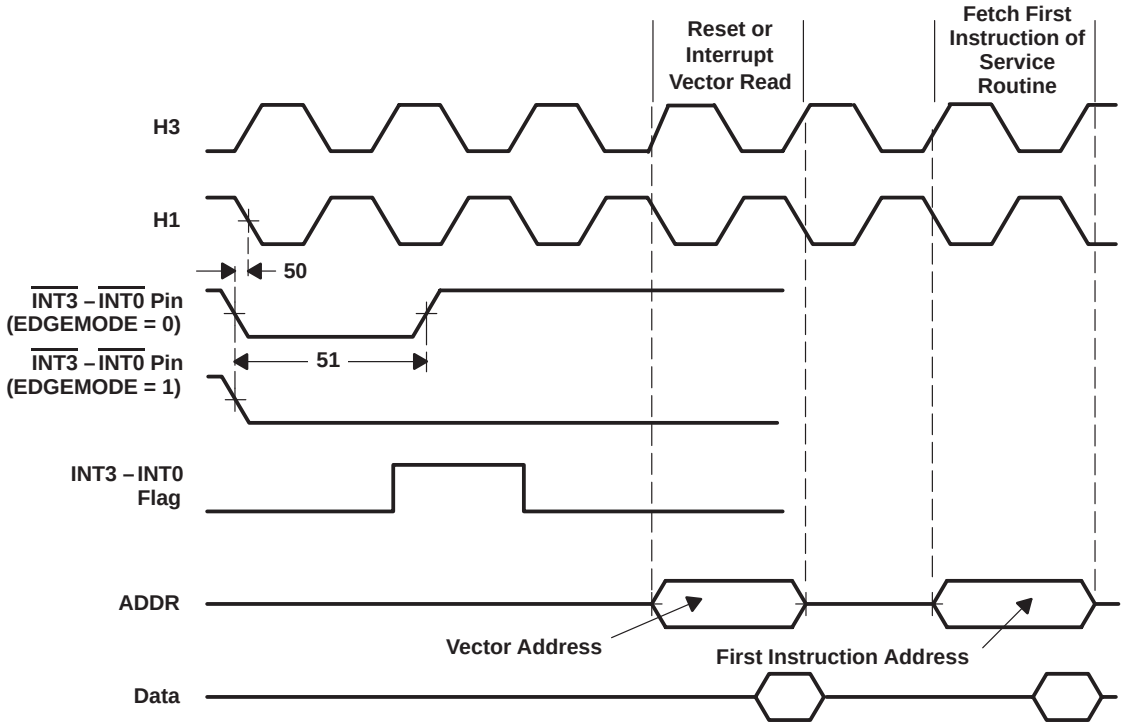


Figure 24. Timing for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ Response

PRODUCT PREVIEW

interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (HI rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (HI rising) of the read phase of the IACK instruction.

The following table defines the timing parameters for the $\overline{\text{IACK}}$ signal. The numbers shown in Figure 25 correspond with those in the NO. column of the table below.

NOTE: The IACK instruction can be executed at anytime to signal an event. It is most often used within an interrupt routine to signal which interrupt has occurred.

timing parameters for $\overline{\text{IACK}}$ (see Figure 25)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
52	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low		5		4	ns
53	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		5		4	ns

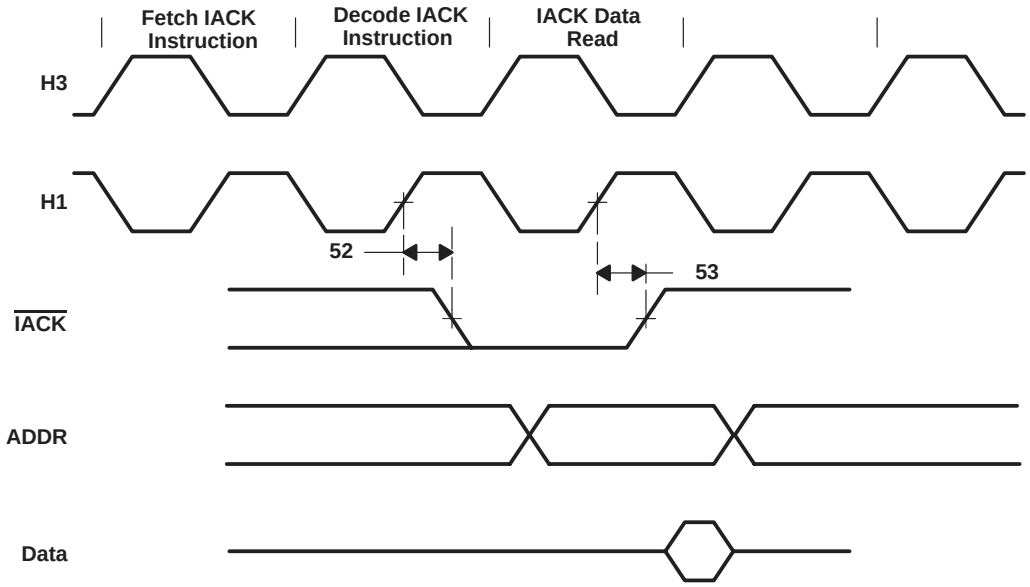


Figure 25. Timing for $\overline{\text{IACK}}$

PRODUCT PREVIEW

serial-port timing parameters for TMS320VC33-120 (see Figure 26 and Figure 27)

NO.				’VC33-120		UNIT
				MIN	MAX	
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			5	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)} * 2.6$		ns
			CLKX/R int	$t_{c(H)} * 2$	$t_{c(H)} * 2^{32}$	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)} + 4$		ns
			CLKX/R int	$[t_{c(SCK)}/2] – 4$	$[t_{c(SCK)}/2] + 4$	
57	$t_{r(SCK)}$	Rise time, CLKX/R			3	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			3	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		9	ns
			CLKX int		7	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	4		ns
			CLKR int	8		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	3		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		9	ns
			CLKX int		7	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	3		ns
			CLKR int	3		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	3		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	$–[t_{c(H)} – 6]$	$[t_{c(SCK)}/2] – 6$	ns
			CLKX int	$–[t_{c(H)} – 10]$	$t_{c(SCK)}/2$	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		8	ns
			CLKX int		5	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			8	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			5	ns

PRODUCT PREVIEW

serial-port timing parameters for TMS320VC33-150 (see Figure 26 and Figure 27)

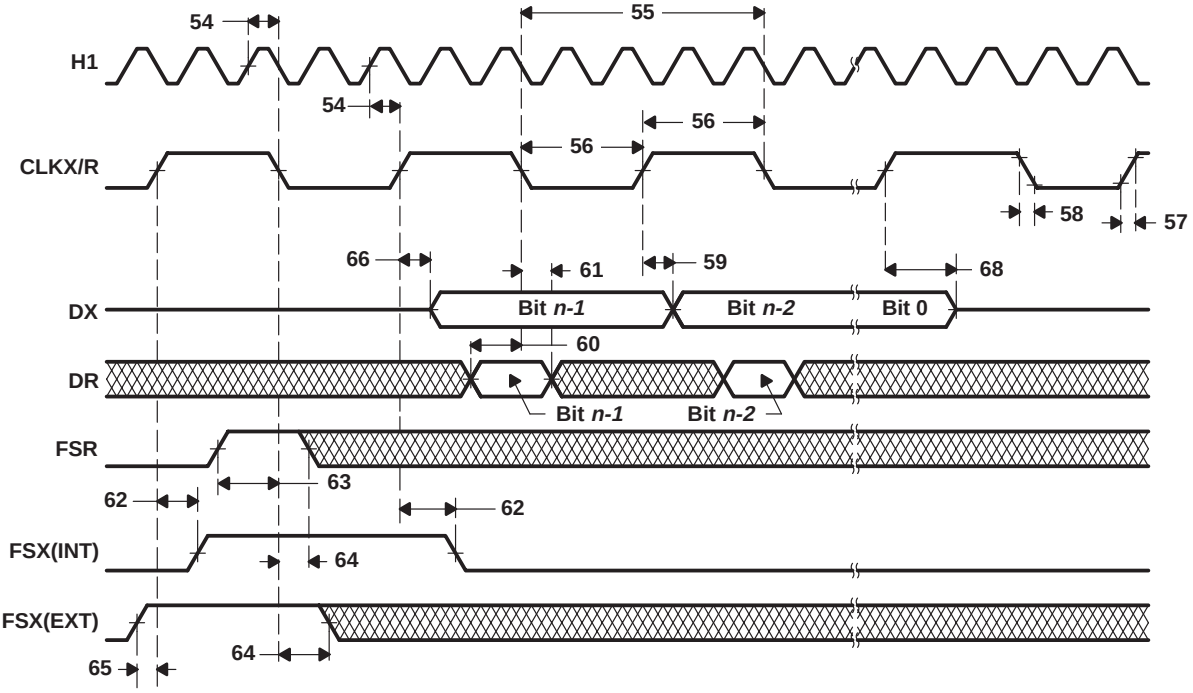
NO.				'VC33-150		UNIT
				MIN	MAX	
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			4	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)} * 2.6$		ns
			CLKX/R int	$t_{c(H)} * 2$	$t_{c(H)} * 2^{32}$	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)} + 3$		ns
			CLKX/R int	$[t_{c(SCK)}/2] - 3$	$[t_{c(SCK)}/2] + 3$	
57	$t_{r(SCK)}$	Rise time, CLKX/R			3	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			3	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		8	ns
			CLKX int		6	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	3		ns
			CLKR int	9		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	3		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		8	ns
			CLKX int		6	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	3		ns
			CLKR int	3		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	3		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	$-[t_{c(H)} - 5]$	$[t_{c(SCK)}/2] - 5$	ns
			CLKX int	$-[t_{c(H)} - 8]$	$t_{c(SCK)}/2$	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		8	ns
			CLKX int		5	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			8	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			5	ns

PRODUCT PREVIEW

data-rate timing modes

Unless otherwise indicated, the data-rate timings shown in Figure 26 and Figure 27 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation refer to subsection 8.2.12 of the *TMS320C3x User's Guide* (literature number SPRU031).

The serial-port timing parameters for seven 'C3x devices are defined in the preceding "serial-port timing parameters" tables. The numbers shown in Figure 26 and Figure 27 correspond with those in the NO. column of each table.

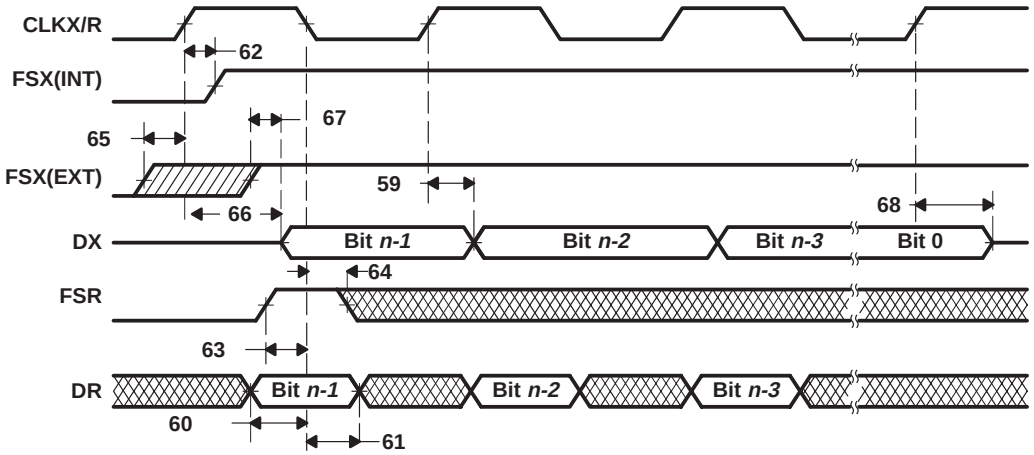


NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 26. Timing for Fixed Data-Rate Mode

PRODUCT PREVIEW

data-rate timing modes (continued)



NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 27. Timing for Variable Data-Rate Mode

PRODUCT PREVIEW

$\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is a synchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The table, "timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$", defines the timing parameters for the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. The numbers shown in Figure 28 correspond with those in the NO. column of the table.

The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

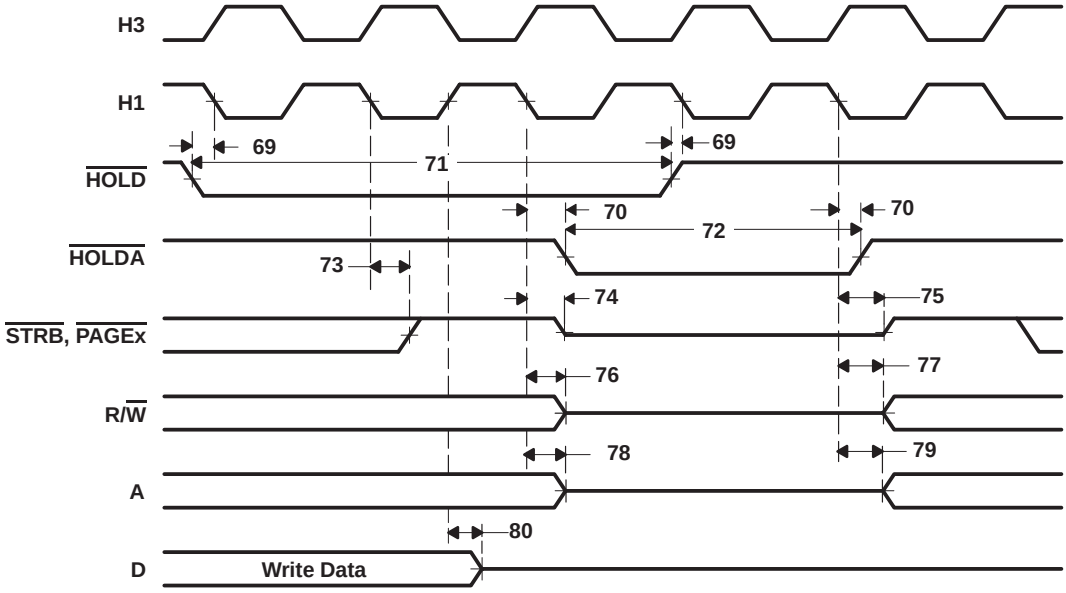
Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue (internally) until a second external write is encountered.

timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ (see Figure 28)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
69	$t_{su(HOLD-H1L)}$	Setup time, $\overline{\text{HOLD}}$ before H1 low	4		3		ns
70	$t_{v(H1L-HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low	5		4		ns
71	$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low	$2t_{c(H)}$		$2t_{c(H)}$		ns
72	$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low	$t_{c(H)} - 4$		$t_{c(H)} - 4$		ns
73	$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$		4		3	ns
74	$t_{dis(H1L-S)}$	Disable time, H1 low to $\overline{\text{STRB}}$ to the high-impedance state		5		4	ns
75	$t_{en(H1L-S)}$	Enable time, H1 low to $\overline{\text{STRB}}$ enabled (active)		5		4	ns
76	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/$\overline{\text{W}}$ to the high-impedance state		5		4	ns
77	$t_{en(H1L-RW)}$	Enable time, H1 low to R/$\overline{\text{W}}$ enabled (active)		5		4	ns
78	$t_{dis(H1L-A)}$	Disable time, H1 low to address to the high-impedance state		5		4	ns
79	$t_{en(H1L-A)}$	Enable time, H1 low to address enabled (valid)		6		5	ns
80	$t_{dis(H1H-D)}$	Disable time, H1 high to data to the high-impedance state		5		4	ns

PRODUCT PREVIEW

$\overline{\text{HOLD}}$ timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 28. Timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$

PRODUCT PREVIEW

general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

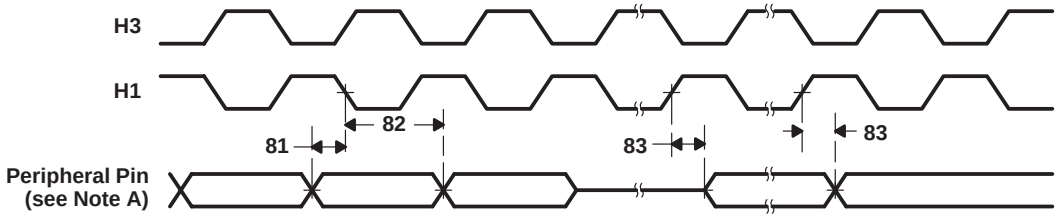
peripheral pin I/O timing

The table, timing parameters for peripheral pin general-purpose I/O, defines peripheral pin general-purpose I/O timing parameters. The numbers shown in Figure 29 correspond with those in the NO. column of the table below.

timing parameters for peripheral pin general-purpose I/O (see Note 5 and Figure 29)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
81	$t_{su(GPIO-H1L)}$	Setup time, general-purpose input before H1 low	5		4		ns
82	$t_{h(H1L-GPIO)}$	Hold time, general-purpose input after H1 low	0		0		ns
83	$t_{d(H1H-GPIO)}$	Delay time, general-purpose output after H1 high		5		4	ns

NOTE 5: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 29. Timing for Peripheral Pin General-Purpose I/O

PRODUCT PREVIEW

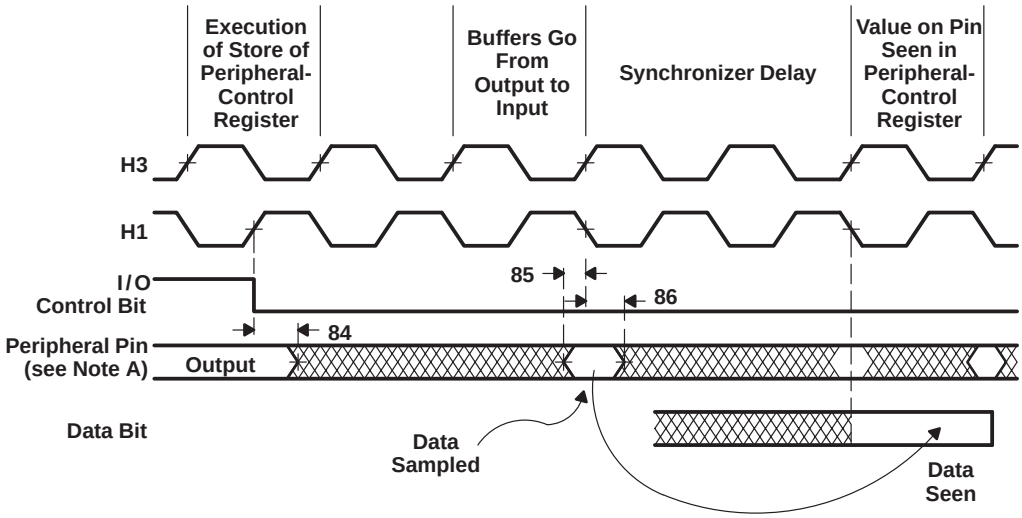
changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa. The numbers shown in Figure 30 and Figure 31 correspond to those shown in the NO. column of the tables below.

timing parameters for peripheral pin changing from general-purpose output to input mode (see Note 5 and Figure 30)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
84	$t_{h(H1H)}$	Hold time, peripheral pin after H1 high		5		4	ns
85	$t_{su(GPIO-H1L)}$	Setup time, peripheral pin before H1 low	5		4		ns
86	$t_{h(H1L-GPIO)}$	Hold time, peripheral pin after H1 low	0		0		ns

NOTE 5: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

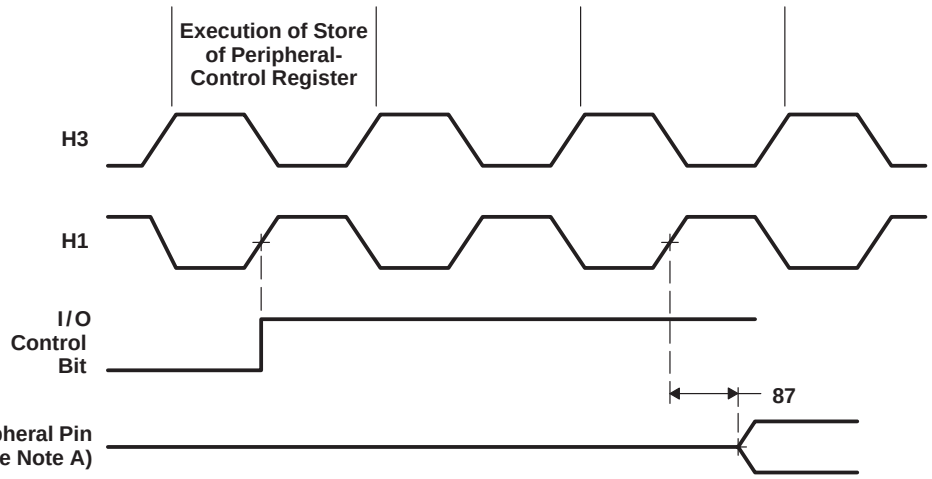
Figure 30. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

PRODUCT PREVIEW

timing parameters for peripheral pin changing from general-purpose input to output mode (see Note 5 and Figure 31)

NO.		’VC33-120		’VC33-150		UNIT
		MIN	MAX	MIN	MAX	
87	$t_{d(H1H-GPIO)}$ Delay time, H1 high to peripheral pin switching from input to output		5		4	ns

NOTE 5: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 31. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

PRODUCT PREVIEW

timer pin timing

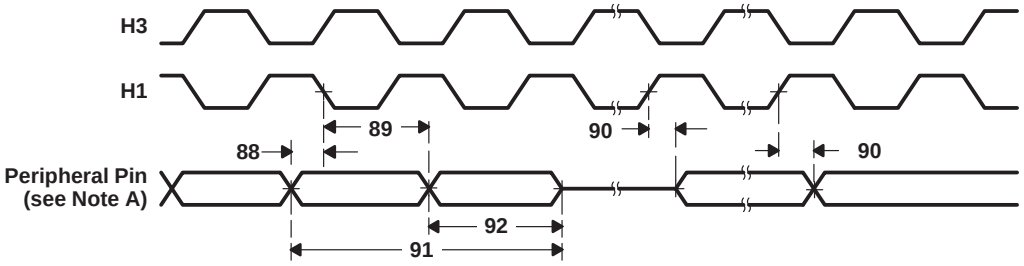
Valid logic-level periods and polarity are specified by the contents of the internal control registers.

The following tables define the timing parameters for the timer pin. The numbers shown in Figure 32 correspond with those in the NO. column of the tables below.

timing parameters for timer pin for TMS320VC33 (see Figure 32)†

NO.	DESCRIPTION‡		’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
88	$t_{su(TCLK-H1L)}$	Setup time, TCLK external before H1 low	5		4		ns
89	$t_{h(H1L-TCLK)}$	Hold time, TCLK external after H1 low	0		0		ns
90	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK internal valid		5		4	ns
91	$t_{c(TCLK)}$	TCLK ext	$t_{c(H)} * 2.6$		$t_{c(H)} * 2.6$		ns
		TCLK int	$t_{c(H)} * 2$	$t_{c(H)} * 2^{32}$	$t_{c(H)} * 2$	$t_{c(H)} * 2^{32}$	
92	$t_{w(TCLK)}$	TCLK ext	$t_{c(H)} + 6$		$t_{c(H)} + 5$		ns
		TCLK int	$[t_{c(TCLK)}/2] - 4$	$[t_{c(TCLK)}/2] + 4$	$[t_{c(TCLK)}/2] - 4$	$[t_{c(TCLK)}/2] + 4$	

† Timing parameters 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 32. Timing for Timer Pin

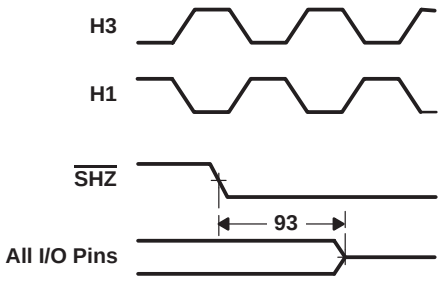
$\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin. The number shown in Figure 33 corresponds with that in the NO. column of the table below.

PRODUCT PREVIEW

timing parameters for $\overline{\text{SHZ}}$ (see Figure 33)

NO.			MIN	MAX	UNIT
93	$t_{dis(SHZ)}$	Disable time, $\overline{\text{SHZ}}$ low to all O, I/O pins disabled (high impedance)	0	20	ns



NOTE A: Enabling $\overline{\text{SHZ}}$ destroys TMS320C3x register and memory contents. Assert $\overline{\text{SHZ}}$ = 1 and reset the TMS320C3x to restore it to a known condition.

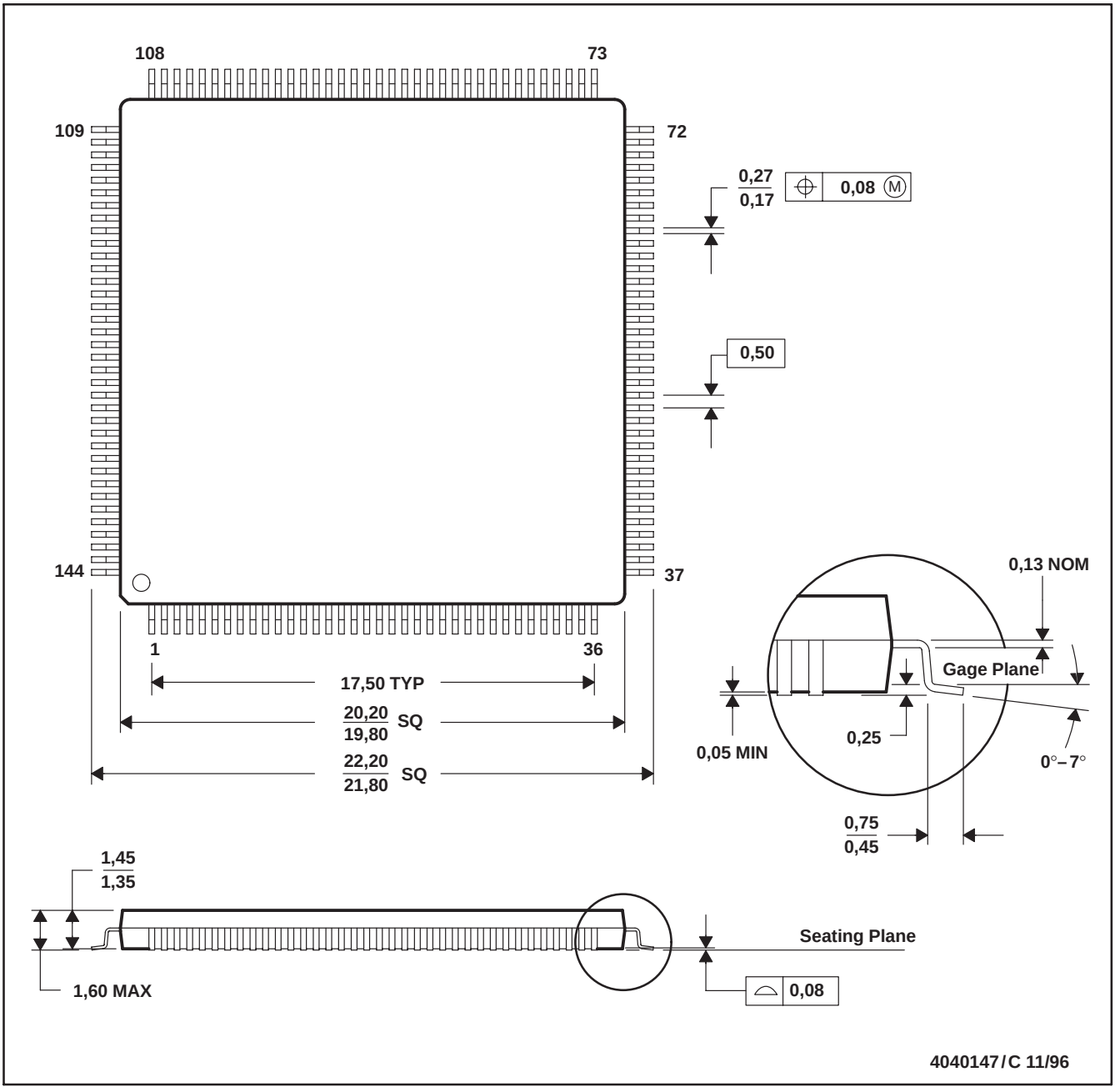
Figure 33. Timing for $\overline{\text{SHZ}}$

PRODUCT PREVIEW

MECHANICAL DATA

TMS320VC33 144-Pin Plastic Thin Quad Flatpack (TQFP)

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	56
$R_{\Theta JC}$	5

PRODUCT PREVIEW

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