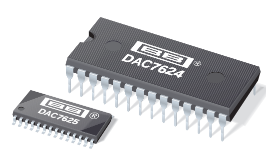
BURR - BROWN®



DAC7624
DAC7625

12-Bit Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 20mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10µs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- RESET TO MID-SCALE (DAC7624) OR ZERO-SCALE (DAC7625)
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS

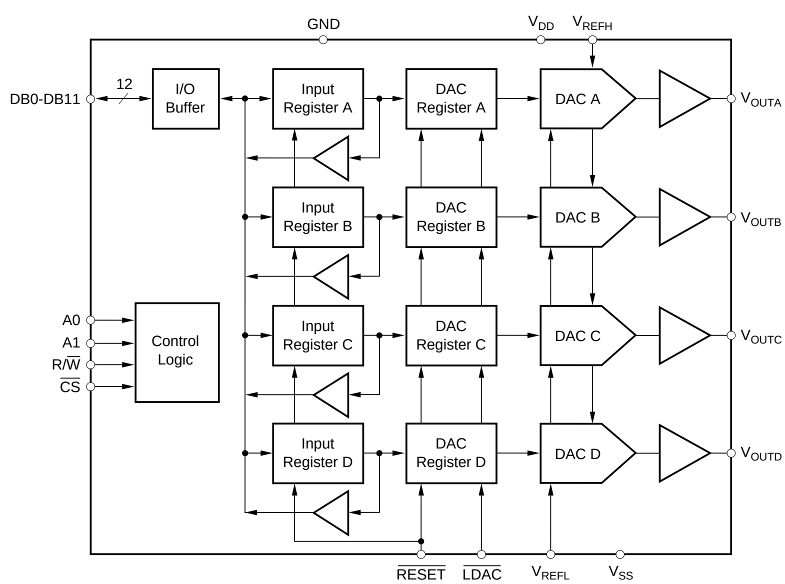
APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS
- DAC-PER-PIN PROGRAMMERS

DESCRIPTION

The DAC7624 and DAC7625 are 12-bit quad voltage output digital-to-analog converters with guaranteed 12-bit monotonic performance over the specified temperature range. They accept 12-bit parallel input data, have double-buffered DAC input logic (allowing simultaneous update of all DACs), and provide a readback mode of the internal input registers. An asynchronous reset clears all registers to a mid-scale code of 800_H (DAC7624) or to a zero-scale of 000_H (DAC7625). The DAC7624 and DAC7625 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7624 and DAC7625 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7624 and DAC7625 are available in a 28-pin plastic double-wide or a 28-lead SOIC package, and offer guaranteed specifications over the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATION

At T_A = –40°C to +85°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, unless otherwise noted.

		DAC7624P, U DAC7625P, U			DAC7624PB, UB DAC7625PB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ACCURACY								
Linearity Error(1)	V_{SS} = 0V or –5V			±2			±1	LSB(2)
Linearity Matching(3)	V_{SS} = 0V or –5V			±2			±1	LSB
Differential Linearity Error	V_{SS} = 0V or –5V			±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 000_H			±4			*	LSB
Zero-Scale Drift			2	5		*	*	ppm/°C
Zero-Scale Matching(3)				±2			±1	LSB
Full-Scale Error	Code = FFF_H			±4			*	LS
Full-Scale Matching(3)				±2			±1	LSB
Zero-Scale Error	Code = $00A_H$, V_{SS} = 0V			±8			*	LSB
Zero-Scale Drift	V_{SS} = 0V		5	10		*	*	ppm/°C
Zero-Scale Matching(3)	V_{SS} = 0V			±4			±2	LSB
Full-Scale Error	Code = FFF_H, V_{SS} = 0V			±8			*	LSB
Full-Scale Matching(3)	V_{SS} = 0V			±4			±2	LSB
Power Supply Rejection			30			*		ppm/V
ANALOG OUTPUT								
Voltage Output(4)	V_{REFL} = 0V, V_{SS} = 0V	0		V_{REFH}	*		*	V
	V_{SS} = –5V	V_{REFL}		V_{REFH}	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Load Capacitance	No Oscillation		100			*		pF
Short-Circuit Current			+5, –120			*		mA
Short-Circuit Duration			Momentary			*		
REFERENCE INPUT								
V_{REFH} Input Range	V_{SS} = 0V or –5V	V_{REFL} +1.25		+2.5	*		*	V
V_{REFL} Input Range	V_{SS} = 0V	0		V_{REFH} –1.25	*		*	V
V_{REFL} Input Range	V_{SS} = –5V	–2.5		V_{REFH} –1.25	*		*	V
DYNAMIC PERFORMANCE								
Settling Time(5)	To ±0.012%		5	10		*	*	µs
Channel-to-Channel Crosstalk	Full-Scale Step On any other DAC		0.25			*		LSB
Output Noise Voltage	0Hz to 1MHz		40			*		nV/√Hz
DIGITAL INPUT/OUTPUT								
Logic Family		TTL-Compatible CMOS				*		
Logic Levels								
V_{IH}	I_{IH} ≤ ±10µA	2.4		V_{DD} +0.3	*		*	V
V_{IL}	I_{IL} ≤ ±10µA	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –0.8mA	3.6		V_{DD}	*		*	V
V_{OL}	I_{OL} = 1.6mA	0.0		0.4	*		*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{DD}		4.75		5.25	*		*	V
V_{SS}	If V_{SS} ≠ 0V	–5.25		–4.75	*		*	V
I_{DD}			1.5	1.9		*	*	mA
I_{SS}		–2.1	–1.6		*	*		mA
Power Dissipation	V_{SS} = –5V		15	20		*	*	mW
	V_{SS} = 0V		7.5	10		*	*	mW
TEMPERATURE RANGE								
Specified Performance	DAC7624P, U, PB, UB DAC7625P, U, PB, UB	–40		+85	*		*	°C

NOTES: (1) If V_{SS} = 0V, specification applies at code $00A_H$ and above. (2) LSB means Least Significant Bit, when V_{REFH} equals +2.5V and V_{REFL} equals –2.5V, then one LSB equals 1.22mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage, does not take into account zero or full-scale error. (5) If V_{SS} = –5V, full-scale 5V step. If V_{SS} = 0V, full-scale positive 2.5V step and negative step from code FFF_H to $00A_H$.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to V_{SS}	–0.3V to 11V
V_{DD} to GND	–0.3V to 5.5V
V_{REFL} to V_{SS}	–0.3V to (V_{DD} – V_{SS})
V_{DD} to V_{REFH}	–0.3V to (V_{DD} – V_{SS})
V_{REFH} to V_{REFL}	–0.3V to (V_{DD} – V_{SS})
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

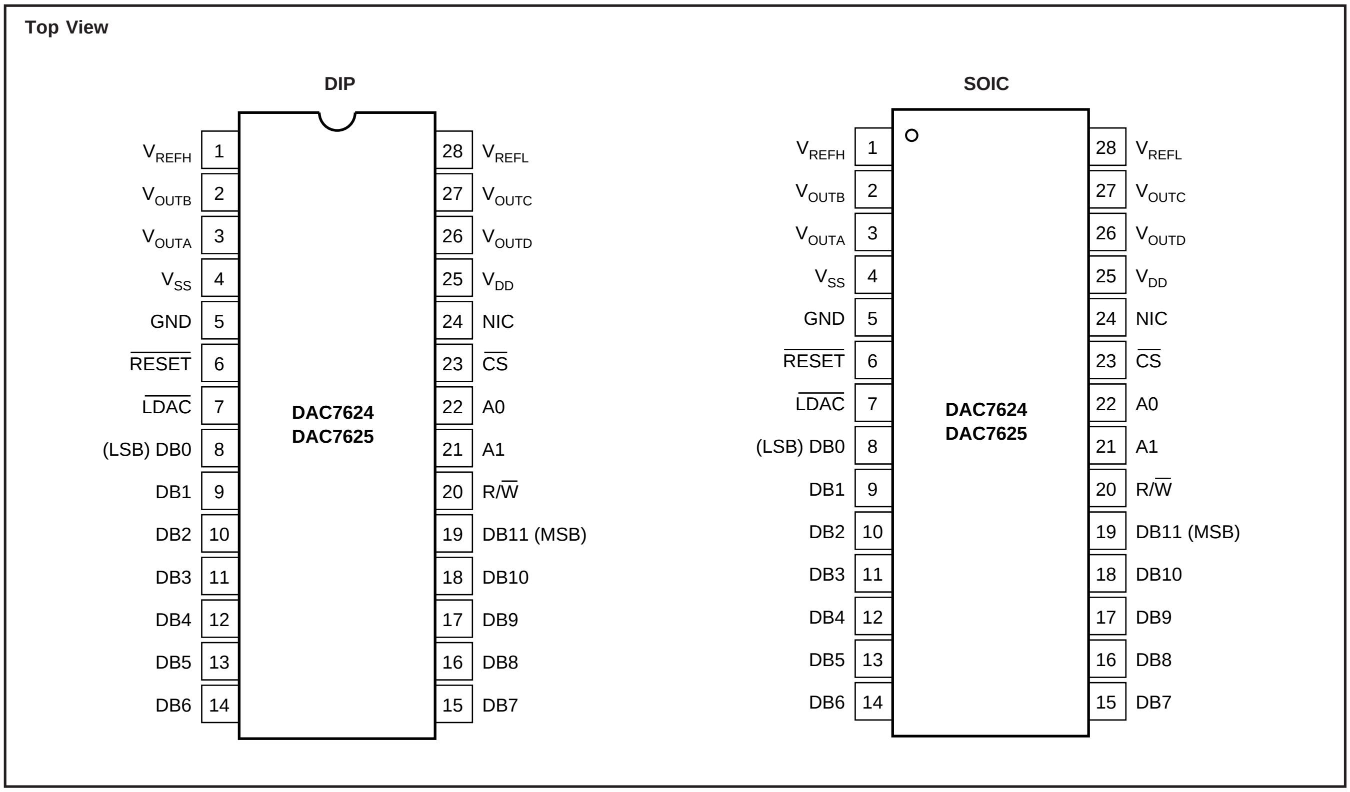
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7624P	±2	±1	–40°C to +85°C	28-Pin Plastic DIP	215
DAC7624U	±2	±1	–40°C to +85°C	28-Lead SOIC	217
DAC7624PB	±1	±1	–40°C to +85°C	28-Pin Plastic DIP	215
DAC7624UB	±1	±1	–40°C to +85°C	28-Lead SOIC	217
DAC7625P	±2	±1	–40°C to +85°C	28-Pin Plastic DIP	215
DAC7625U	±2	±1	–40°C to +85°C	28-Lead SOIC	217
DAC7625PB	±1	±1	–40°C to +85°C	28-Pin Plastic DIP	215
DAC7625UB	±1	±1	–40°C to +85°C	28-Lead SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATIONS



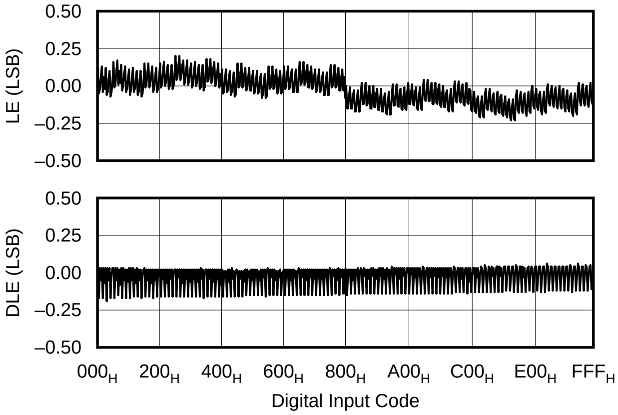
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
2	V_{OUTB}	DAC B Voltage Output.
3	V_{OUTA}	DAC A Voltage Output.
4	V_{SS}	Negative Analog Supply Voltage, 0V or –5V.
5	GND	Ground.
6	$\overline{RESET}$	Asynchronous Reset Input. Sets DAC and input registers to either mid-scale (800_H, DAC7624) or zero-scale (000_H, DAC7625) when LOW.
7	$\overline{LDAC}$	Load DAC Input. All DAC Registers are transparent when LOW.
8	DB0	Data Bit 0. Least significant bit of 12-bit word.
9	DB1	Data Bit 1
10	DB2	Data Bit 2
11	DB3	Data Bit 3
12	DB4	Data Bit 4
13	DB5	Data Bit 5
14	DB6	Data Bit 6
15	DB7	Data Bit 7
16	DB8	Data Bit 8
17	DB9	Data Bit 9
18	DB10	Data Bit 10
19	DB11	Data Bit 11. Most significant bit of 12-bit word.
20	R/$\overline{W}$	Read/Write Control Input (read = HIGH, write = LOW).
21	A1	Register/DAC Select (C or D = HIGH, A or B = LOW).
22	A0	Register/DAC Select (B or D = HIGH, A or C = LOW).
23	$\overline{CS}$	Chip Select Input.
24	NIC	Not Internally Connected. Pin has no internal connection to the device.
25	V_{DD}	Positive Analog Supply Voltage, +5V nominal.
26	V_{OUTD}	DAC D Voltage Output.
27	V_{OUTC}	DAC C Voltage Output.
28	V_{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.

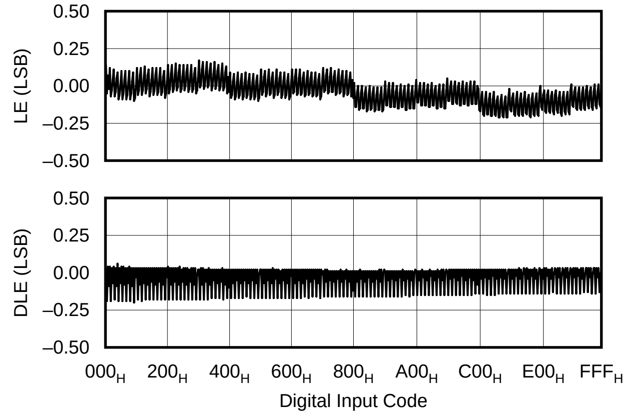
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

At T_A = +25°C, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

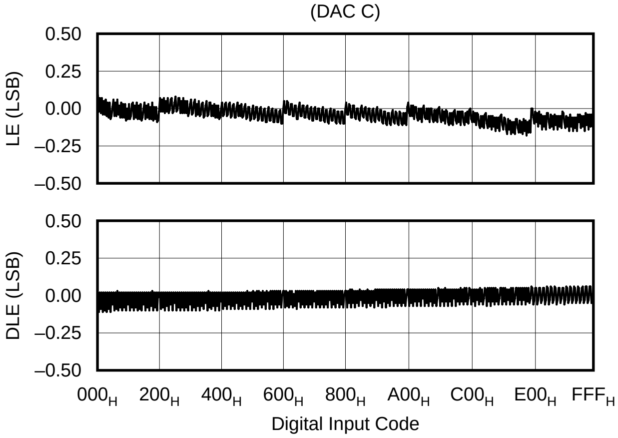
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A)



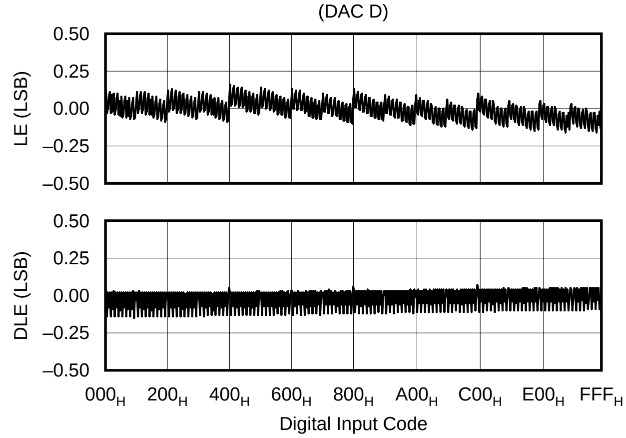
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B)



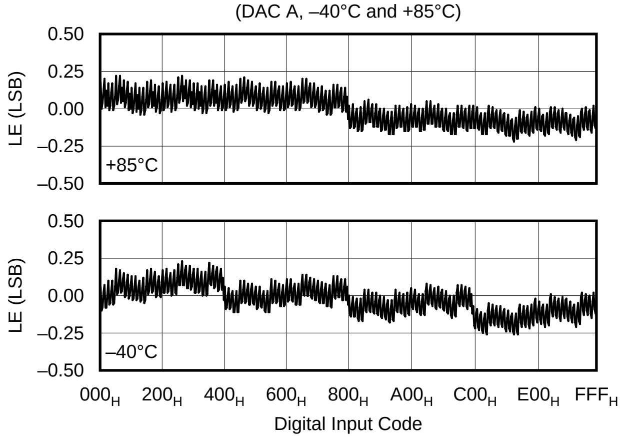
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C)



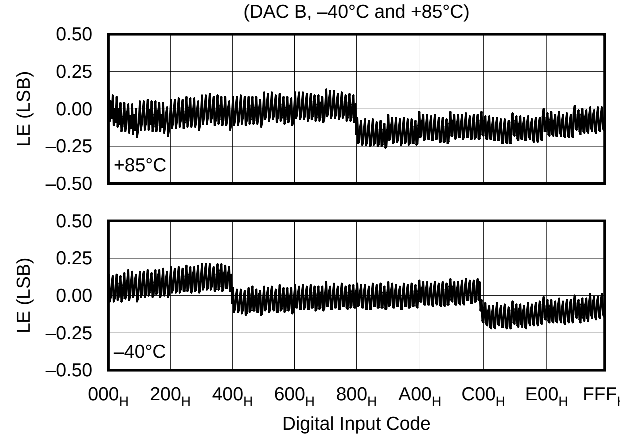
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D)



LINEARITY ERROR vs CODE
(DAC A, –40°C and +85°C)

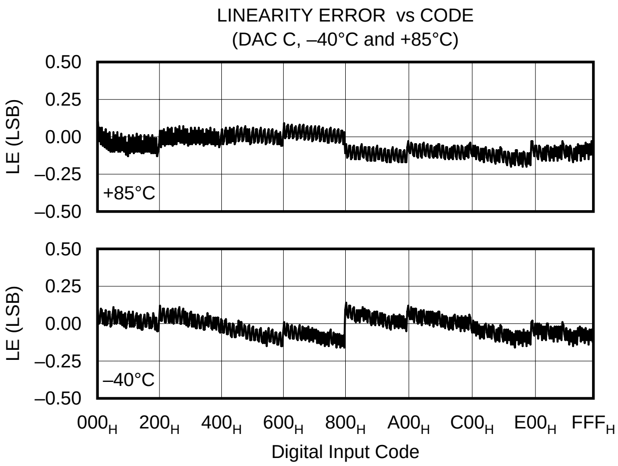


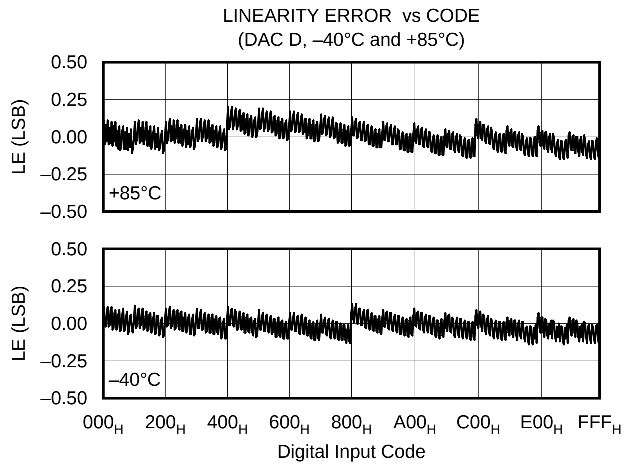
LINEARITY ERROR vs CODE
(DAC B, –40°C and +85°C)

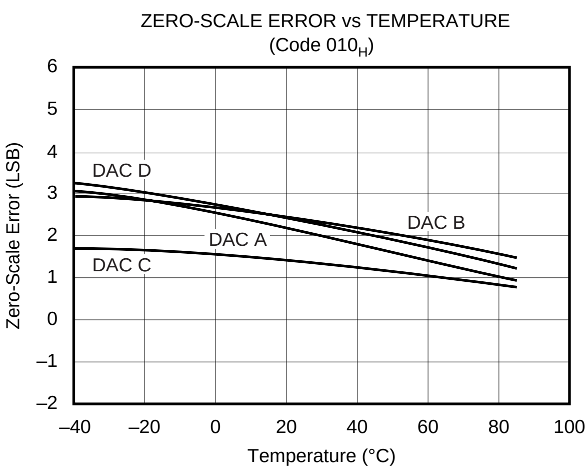


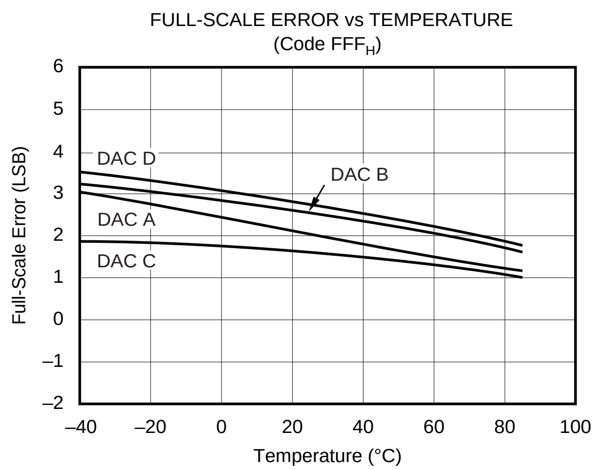
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (CONT)

At T_A = +25°C, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.





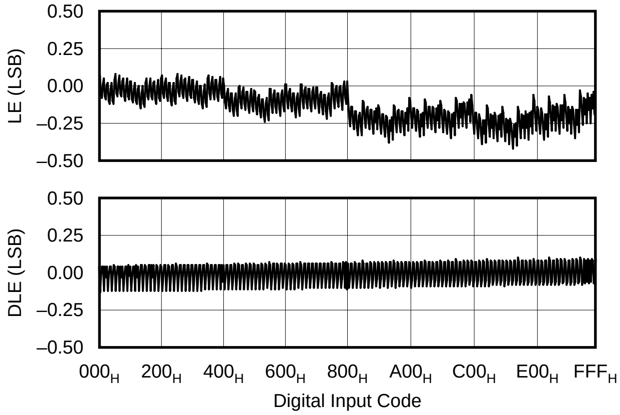




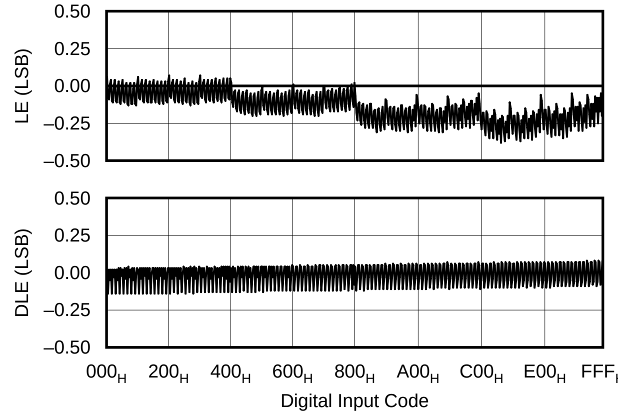
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V

At T_A = +25°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

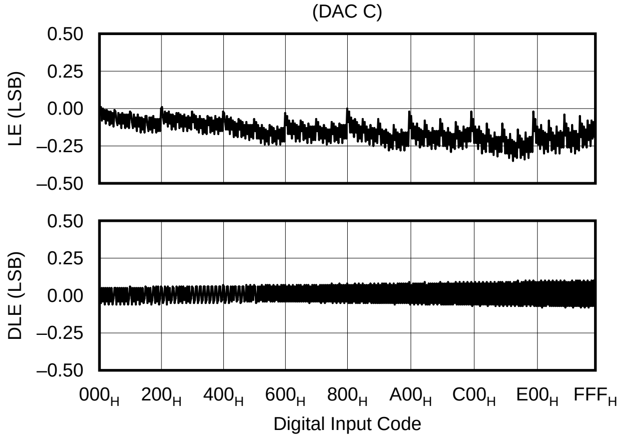
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A)



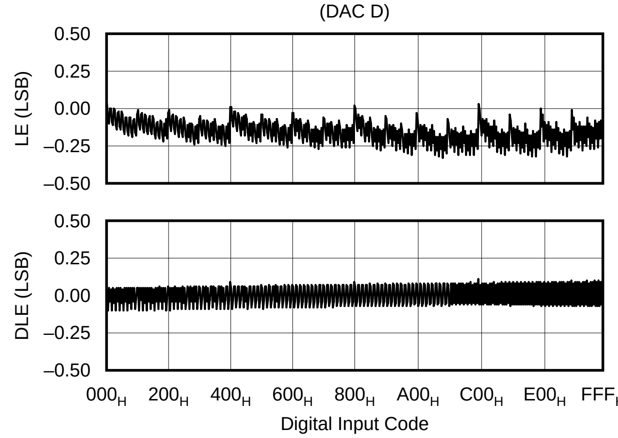
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B)



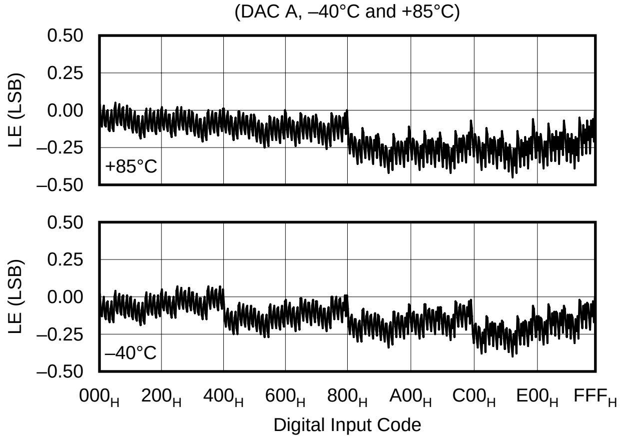
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C)



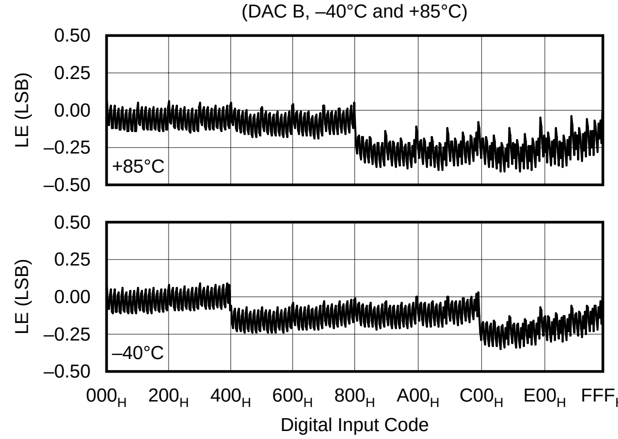
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D)



LINEARITY ERROR vs CODE
(DAC A, –40°C and +85°C)

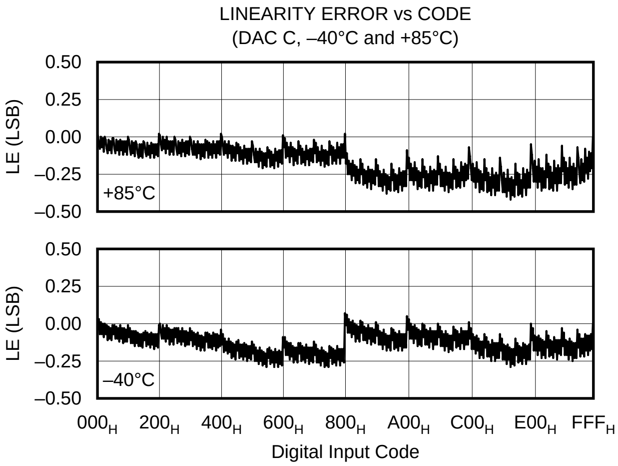


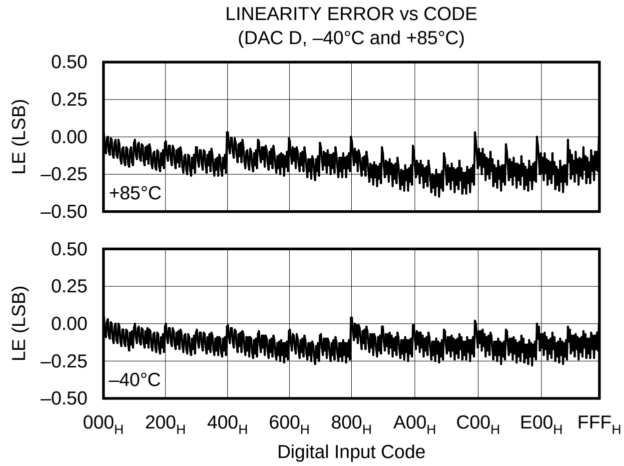
LINEARITY ERROR vs CODE
(DAC B, –40°C and +85°C)

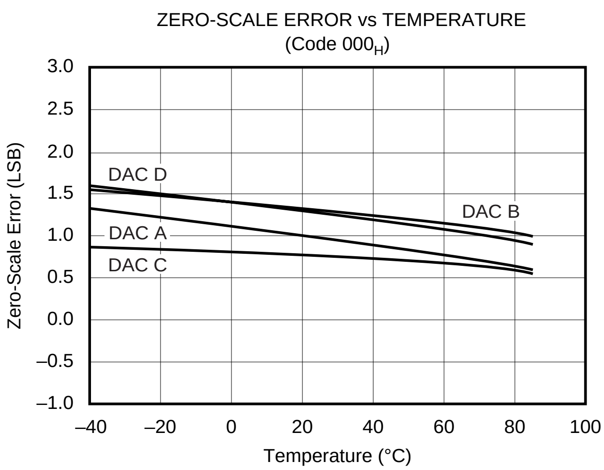


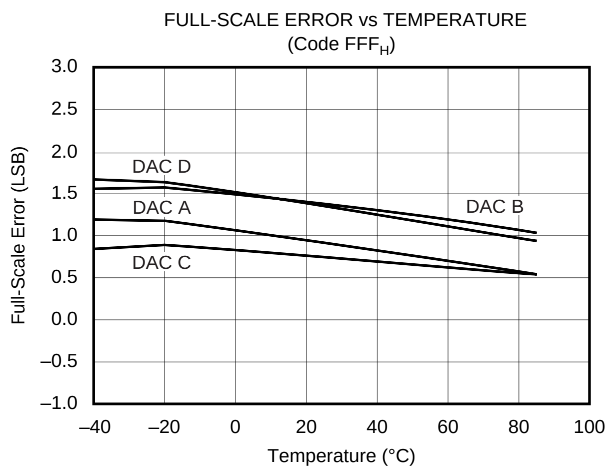
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (CONT)

At T_A = +25°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.



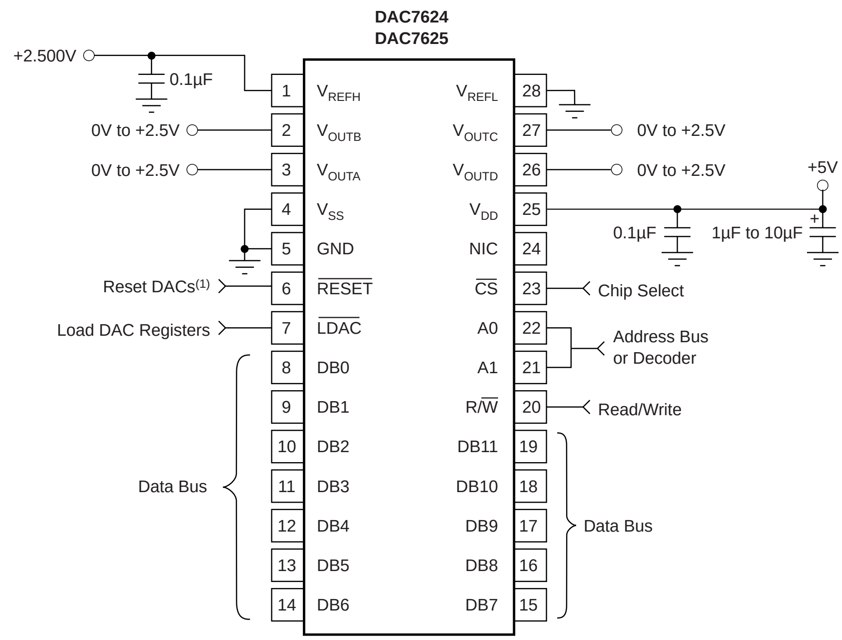






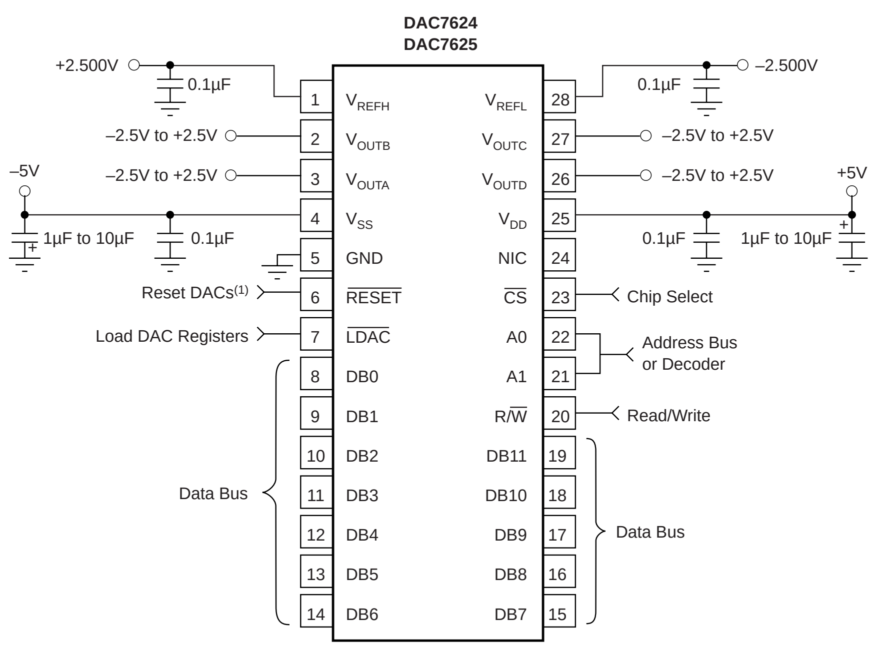
THEORY OF OPERATION

The DAC7624 and DAC7625 are quad, voltage output, 12-bit digital-to-analog converters (DACs). The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op-amp, but all share the reference voltage inputs. The minimum voltage output (“zero-scale”) and maximum voltage output (“full-scale”) are set by the external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 12-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from a single +5V supply or a dual ±5V supply. Each device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale (DAC7624, code 800_H) or to zero-scale (DAC7625, code 000_H). See Figures 1 and 2 for the basic operation of the DAC7624/25.



NOTE: (1) Reset LOW sets all DACs to code 800_H on the DAC7624 and to code 000_H on the DAC7625.

FIGURE 1. Basic Single-Supply Operation of the DAC7624/25.



NOTE: (1) Reset LOW sets all DACs to code 800_H on the DAC7624 and to code 000_H on the DAC7625.

FIGURE 2. Basic Dual-Supply Operation of the DAC7624/25.

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation), the output can swing to ground. Note that the settling time of the output op-amp will be longer with voltages very near ground. Also, care must be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) if the output amplifier has a negative offset.

The behavior of the output amplifier can be critical in some applications. Under short circuit conditions (DAC output shorted to ground), the output amplifier can sink a great deal more current than it can source. See the specification table for more details concerning short circuit current.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH}, can be any voltage between V_{SS}+2.25V and V_{DD}–2.25V provided that V_{REFH} is at least 1.25V greater than V_{REFL}. The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op-amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter, if V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REFH} input depends on the DAC output voltages and can vary from a few microamps to approximately 0.5 milliamp. The V_{REFH} source will not be required to sink current, only source it. Bypassing the reference voltage or voltages with at least a 0.1uF capacitor placed as close to the DAC7624/25 package is strongly recommended.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7624/25. Note that each internal register is level triggered and not edge triggered. When the appropriate signal is LOW, the register becomes transparent. When this signal is returned HIGH, the digital word currently in the register is latched. The first set of registers (the Input Registers) are triggered via the A0, A1, $R/\overline{W}$, and $\overline{CS}$ inputs. Only one of these registers is transparent at any given time. The second set of registers (the DAC Registers) are all transparent when $\overline{LDAC}$ input is pulled LOW.

Each DAC can be updated independently by writing to the appropriate Input Register and then updating the DAC Register. Alternatively, the entire DAC Register set can be configured as always transparent by keeping $\overline{LDAC}$ LOW—the DAC update will occur when the Input Register is written.

The double buffered architecture is mainly designed so that each DAC Input Register can be written at any time and then all DAC voltages updated simultaneously by pulling $\overline{LDAC}$ LOW. It also allows a DAC Input Register to be written to at any point and the DAC voltage to be synchronously changed via a trigger signal connected to $\overline{LDAC}$.

A1	A0	$R/\overline{W}$	$\overline{CS}$	$\overline{RESET}$	$\overline{LDAC}$	SELECTED INPUT REGISTER	STATE OF SELECTED INPUT REGISTER	STATE OF ALL DAC REGISTERS
L(1)	L	L	L	H(2)	L	A	Transparent	Transparent
L	H	L	L	H	L	B	Transparent	Transparent
H	L	L	L	H	L	C	Transparent	Transparent
H	H	L	L	H	L	D	Transparent	Transparent
L	L	L	L	H	H	A	Transparent	Latched
L	H	L	L	H	H	B	Transparent	Latched
H	L	L	L	H	H	C	Transparent	Latched
H	H	L	L	H	H	D	Transparent	Latched
L	L	H	L	H	H	A	Readback	Latched
L	H	H	L	H	H	B	Readback	Latched
H	L	H	L	H	H	C	Readback	Latched
H	H	H	L	H	H	D	Readback	Latched
X(3)	X	X	H	H	L	NONE	(All Latched)	Transparent
X	X	X	H	H	H	NONE	(All Latched)	Latched
X	X	X	X	L	X	ALL	Reset(4)	Reset(4)

NOTES: (1) L = Logic LOW. (2) H= Logic HIGH. (3) X = Don't Care. (4) DAC7624 resets to 800_H, DAC7625 resets to 000_H. When $\overline{RESET}$ rises, all registers that are in their latched state retain the reset value.

TABLE I. DAC7624 and DAC7625 Control Logic Truth Table.

DIGITAL TIMING

Figure 3 and Table II provide detailed timing for the digital interface of the DAC7624 and DAC7625.

DIGITAL INPUT CODING

The DAC7624 and DAC7625 input data is in straight binary format. The output voltage is given by the following equation:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \bullet N}{4096}$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

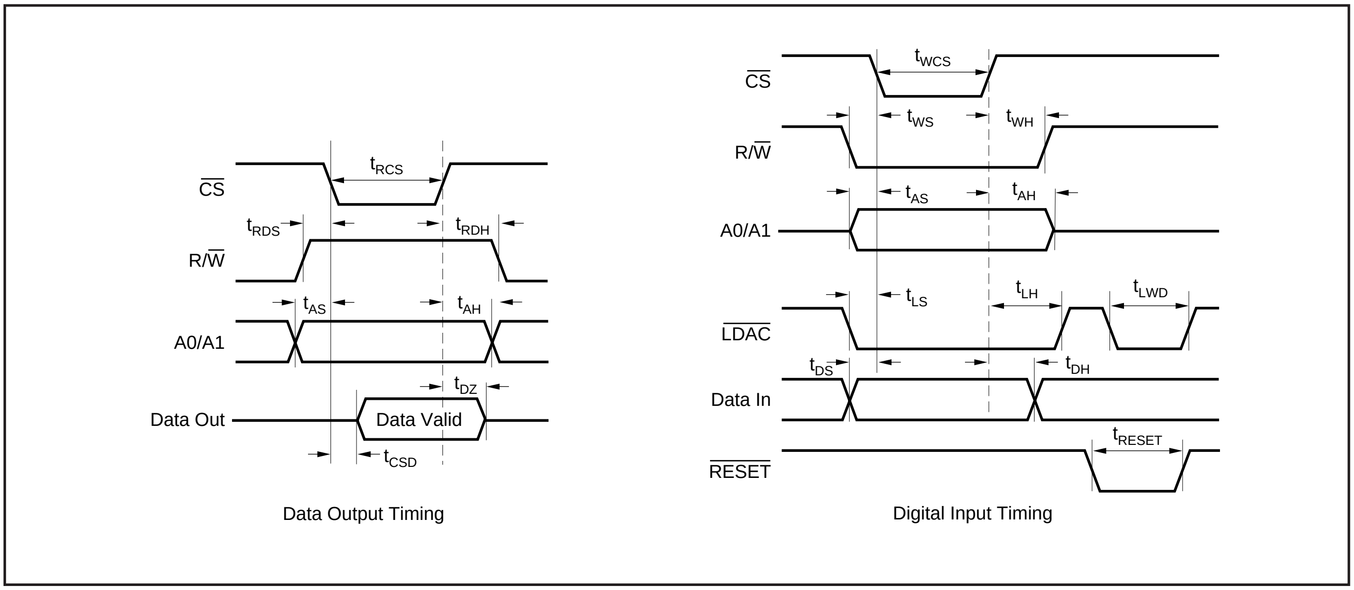


FIGURE 3. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	200			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	0			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance		100		ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	160	ns
t_{WCS}	$\overline{CS}$ LOW for Write	50			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	0			ns
t_{AS}	Address Valid to $\overline{CS}$ LOW	0			ns
t_{AH}	Address Valid after $\overline{CS}$ HIGH	0			ns
t_{LS}	$\overline{LDAC}$ LOW to $\overline{CS}$ LOW	70			ns
t_{LH}	$\overline{LDAC}$ LOW after $\overline{CS}$ HIGH	50			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	0			ns
t_{LWD}	$\overline{LDAC}$ LOW	50			ns
t_{RESET}	$\overline{RESET}$ LOW	50			ns

TABLE II. Timing Specifications (T_A = –40°C to +85°C).

IMPORTANT NOTICE