KISTA 1um CMOS SOI
Mixed Signal Flow

Version 0.0.1

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Contents

List of Code Listings

1 Introduction

This manual shows how to use the analog-mixed signal flow to create and simulate digital and analog circuits designed using the KISTA 1um CMOS SOI PDK. This version has been tested with the following tools:

```
IC618 (Virtuoso Schematic and layout editor)
PVS161 (DRC & LVS physical verification)
XCELIUM1803 (Mixed signal simulator)
SPECTRE181 (Analog simulator)
```

There are three examples that are shown in this manual: creation and simulation of a digital cell/block, creatino an simulation of an analog circuit, and simulation of a mixed-signal block containing both analog and digital circuits.

2 Digital Cell

Digital cells need at least the following views:

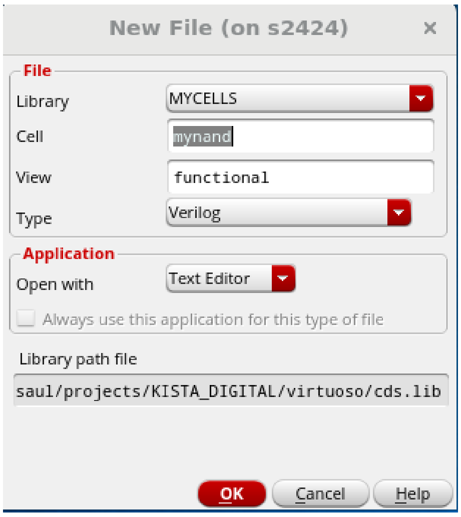
```
symbol (schematic symbol)
functional (verilog representation)
schematic (transistor level implementation at schematic level)
layout (physical implementation)
abstract (abstracted physical implementation)
analog_extracted (parasitic extraction)
```

The recommended procedure to create a digital cell is to first to import the verilog representation as a functional view, automatically create a symbol, create a schematic view, create layout view, create an analog extracted view, and finally generate the abstract view.

2.1 Functional View

Start virtuoso and go to Tools -> Library manager. Go to File -> New -> Library and create a new library MYCELLS. Attach it to the technology KISTA_SOI_STDLIB_TECH.

Now go to File -> New -> Cell. In the "Cell" field write mynand, and in "View" write functional. The "Type" should have automatically changed to Verilog (Fig. 1). Press "OK" and a text editor will open with a place holder for the code of the Verilog module. Change the Verilog code as shown in Fig. 2. When you save the file, you will be asked if you want to create a symbol. Click



File

Library: MYCELLS

Cell: mynand

View: functional

Type: Verilog

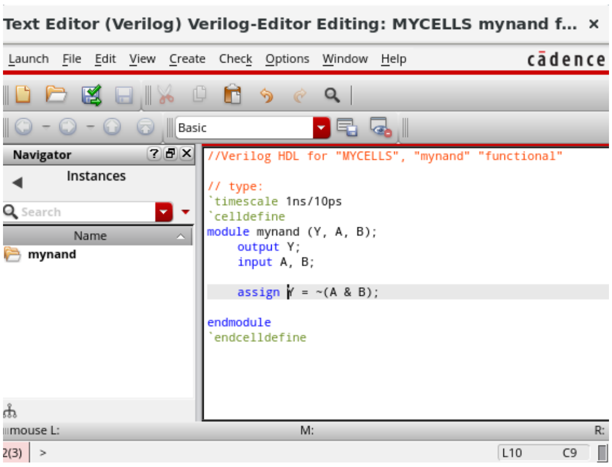
Application

Open with: Text Editor

□ Always use this application for this type of file

Library path file: saul/projects/KISTA_DIGITAL/virtuoso/cds.lib

Figure 1: Cell creation



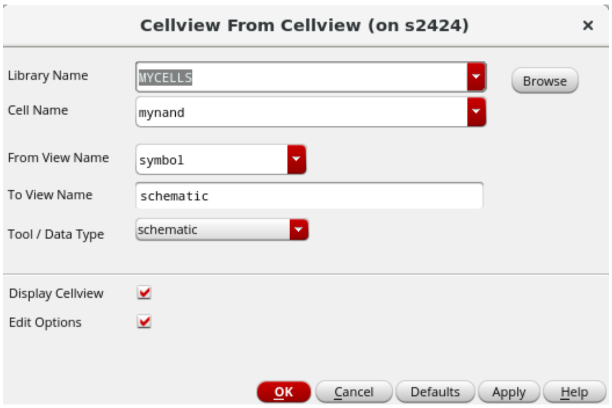
Text Editor (Verilog) Verilog-Editor Editing: MYCELLS mynand f...
Launch File Edit View Create Check Options Window Help
cādence
Basic
Navigator
Instances
Search
Name
mynand
mouse L:
M:
R:
2(3)
>
L10
C9

```
//Verilog HDL for "MYCELLS", "mynand" "functional"

// type:
`timescale 1ns/10ps
`celldefine
module mynand (Y, A, B);
    output Y;
    input A, B;

    assign Y = ~(A & B);

endmodule
`endcelldefine
```

Figure 2: Functional view

Yes/Accept and the symbol view will be created. You can edit the symbol if you want so that it resembles a nand gate.

Note: Although it is possible to create the symbol manually as a separate step, it is much better that you do it precisely as shown above. Manually creation of the symbol may result in inconsistent port order with the Verilog code which needs to be troubleshooted later at CDL level.



Cellview From Cellview (on s2424)

Library Name: MYCELLS

Cell Name: mynand

From View Name: symbol

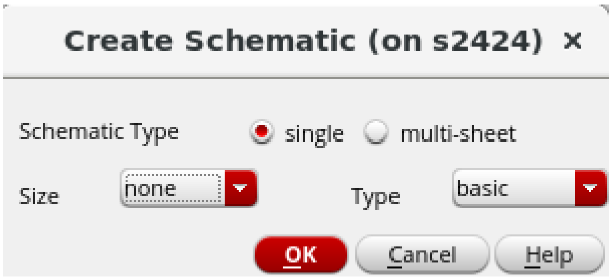
To View Name: schematic

Tool / Data Type: schematic

Display Cellview ☑

Edit Options ☑

Figure 3: Schematic cell creation



Create Schematic (on s2424)

Schematic Type ● single ○ multi-sheet

Size: none

Type: basic

Figure 4: Create Schematic form

2.2 Schematic View

Now open the symbol view and go to Create -> Cell View -> From Cell View. The popup window for creating a new view will appear. It is already configured to create a schematic so you just have to click "OK" (Fig. 3). Then, the "Create Schematic" popup window will appear. Here change the size to "none" and click "OK".

You can create the schematic of the nand gate using nmos3 and pmos3 transistors (Fig. 5). You will also need to create pins for global nets VDD! and VSS!. Click on Create -> Pin. Write VDD! or VSS! in "Names". In the "Signal type" drop-down menu select "power" or "ground". Check "Attach to Pin" and "Derive from pin name". Finally remove the ! in the "Property Name". The form should look like Fig. 6

2.3 Test Bench Creation

In the Library managed go to File -> New -> Cell View and create cell called mynand_tb (Fig. 7).

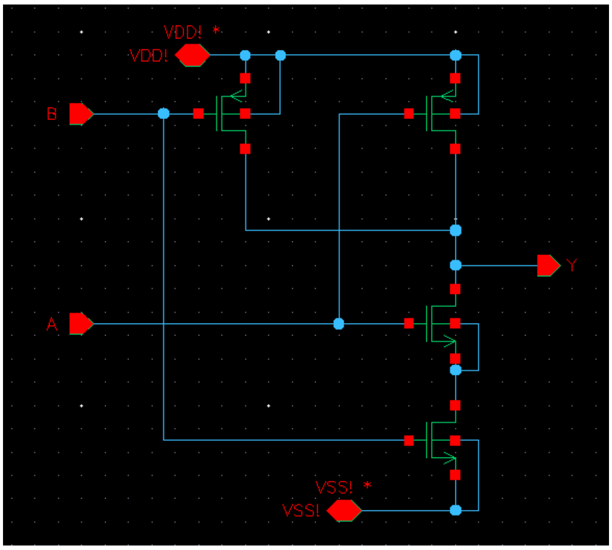


Figure 5: Final Schematic

Now add the mynand cell, vpulse sources, a load capacitor, and two DC sources as shown in Fig. 8. Set V0 to 10ns period and 5 ns pulse width, and V1 to 20ns period and 10 ns pulse width. Place labels on all the wires. Note that global nets end with !.

2.4 Config view creation

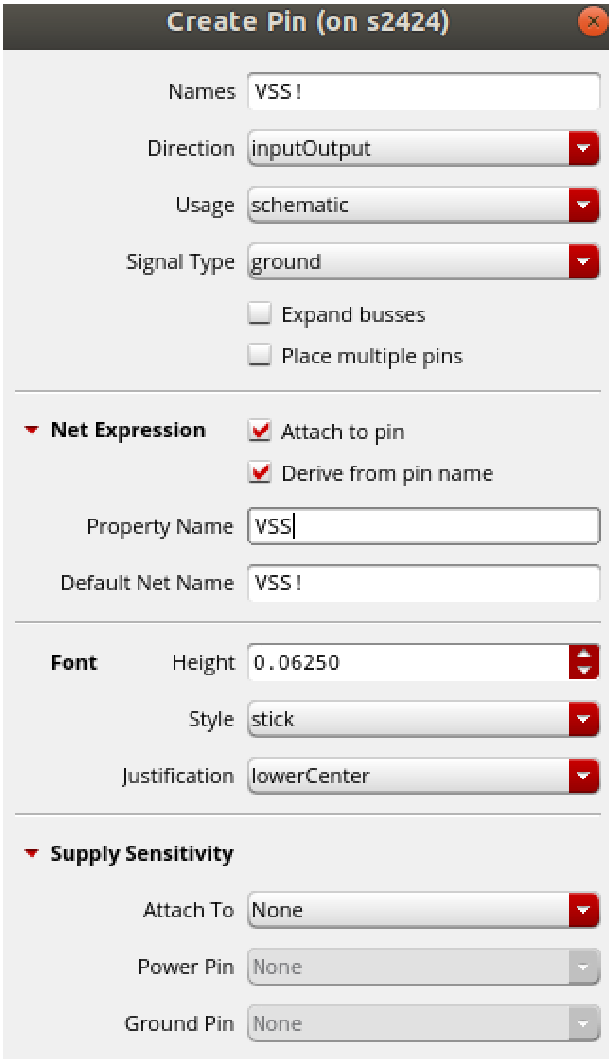
To use the AMS simulator, the first thing that is needed is to create a config view for the test bench. Go to the Library manager and select the "mynand_tb" cell. Then go to File -> New -> Cell View and change "Type" to "config" (Fig. 9). Press OK.

A new configuration window will appear. In the "View" drop-down menu select "schematic". Then go to the bottom and click "Use Template". Then Select "AMS". Press OK (Fig. 10). This will configure the Global Bindings. Press Ok again and you will see the config view window with all the cells and views used in the test bench (Fig. 11).

Press Save and close the config view.

2.5 AMS simulation

In the Library Manager open the config view (double-click). A pop-up window will appear. Make sure that both the config view and the schematic will open for editing (Fig. 12).



Create Pin (on s2424)

Names: VSS!

Direction: inputOutput

Usage: schematic

Signal Type: ground

□ Expand busses

□ Place multiple pins

Net Expression

☑ Attach to pin

☑ Derive from pin name

Property Name: VSS

Default Net Name: VSS!

Font

Height: 0.06250

Style: stick

Justification: lowerCenter

Supply Sensitivity

Attach To: None

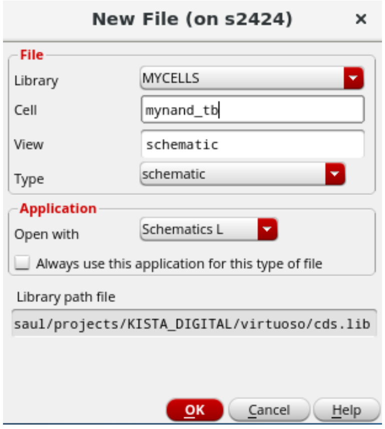
Power Pin: None

Ground Pin: None

Figure 6: Global pin creation

Now in the test bench's schematic got to Launch -> ADE XL, and click on "Create a New View" and OK. A new window will open. Make sure that the "Cell" field is "mynand_tb" and that the "View" field is "adexl". Press OK. Now the schematic window change its name to Virtuoso Analog Design Environment XL Editing and it will have two tabs: one for the schematic and the other for the adexl. You will use the adexl to setup and run simulations.

Go to the "Data View" box on the left side and double click on "Tests". Then double click on "click to add test". A popup window will appear. Make sure that "mynand_tb" is selected and click OK (Fig. 13). Now it pops ups the ADE XL Test Editor window that you can use to configure the simulations. Note that this ADE XL window is only used to configure simulations and you



New File (on s2424)

File

Library: MYCELLS

Cell: mynand_tb

View: schematic

Type: schematic

Application

Open with: Schematics L

□ Always use this application for this type of file

Library path file

saul/projects/KISTA_DIGITAL/virtuoso/cds.lib

Figure 7: Test bench creation

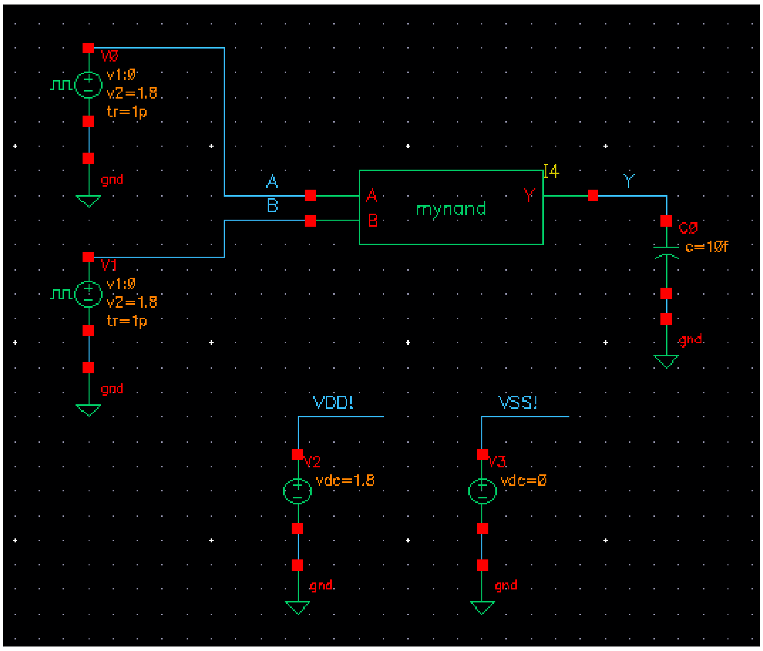
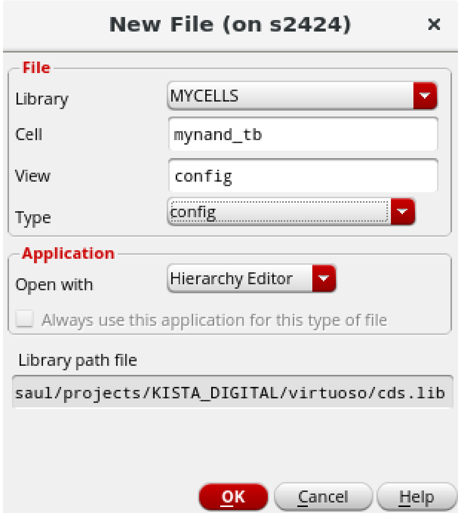


Figure 8: Test bench schematic

should not run simulations from this window!

In the ADE Go to Setup -> Simulator and select "ams" (Fig. 14). Then go to Setup -> Model Libraries and add the device simulation libraries (Fig. 15). Then finally go to Setup-> Connect Rules / IE Setup and select the OSS "Connect Rule/Connect Module Based Setup" (Fig. 16).

Now go to Analyses -> Choose and setup a transient analysis with Stop Time of 200 ns, and moderate precision (Fig. 17). Then go to Outputs -> To Be Plotted -> Select on Design and select the nets A,B, and Y (Fig. 18). Now,



New File (on s2424)

File

Library: MYCELLS

Cell: mynand_tb

View: config

Type: config

Application

Open with: Hierarchy Editor

☐ Always use this application for this type of file

Library path file

saul/projects/KISTA_DIGITAL/virtuoso/cds.lib

Figure 9: Creation of config view

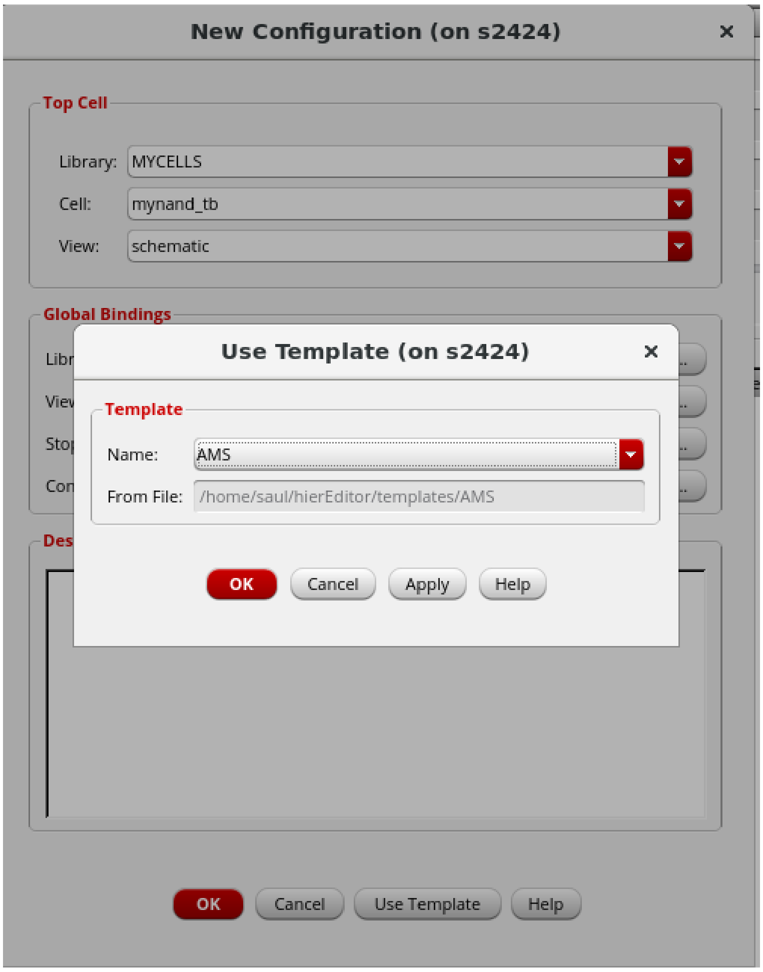
you can close the ADE XL Test editor.

Now go to the hierarchy editor and make sure that the "View Found" for the mynand cell is "functional". Press the "Recompute the hierarchy" button in the toolbar (the icon is a page with an arrow pointing up). The window should look as Fig. 19.

Then go to the Virtuoso Analog Design Environment XL and click the green button "run". The simulation will start and when it is done, the Results tab will open. Click the "Plot All" button (waveform icon beside "Replace"). The Virtuoso Visualization & Analysis window will open. Here you can analyse the waveforms. Press the toolbar button "Split all Strips" at the right top corner. Then Press "v" to create a vertical cursor (Fig 21).

You can check the netlist used for simulation by right-clicking on the test. A pop-up menu will appear. Go down and select Netlist -> Display. You will see a verilog netlist in which the module mynand is instantiated.

Now, go to the config view and right-click the "View to Use" for the cell mynand and select schematic. The button "Recompute the hierarchy" now show an exclamation mark which means that the configuration has changed and the hierarchy must be recomputed (Fig. 22). Click on the "Recompute the hierarchy" button and run the simulation again. Change "Replace" to "Append" so that you can see both functional and schematic simulations in the same plot. Once the simulation finishes, click the "Plot All" button. Again, split the waveforms and move those with same name to the same plot. Here you can check if your circuit implementation matches the functional implementation (Fig. 23).



New Configuration (on s2424)

Top Cell

Library: MYCELLS

Cell: mynand_tb

View: schematic

Global Bindings

Use Template (on s2424)

Template

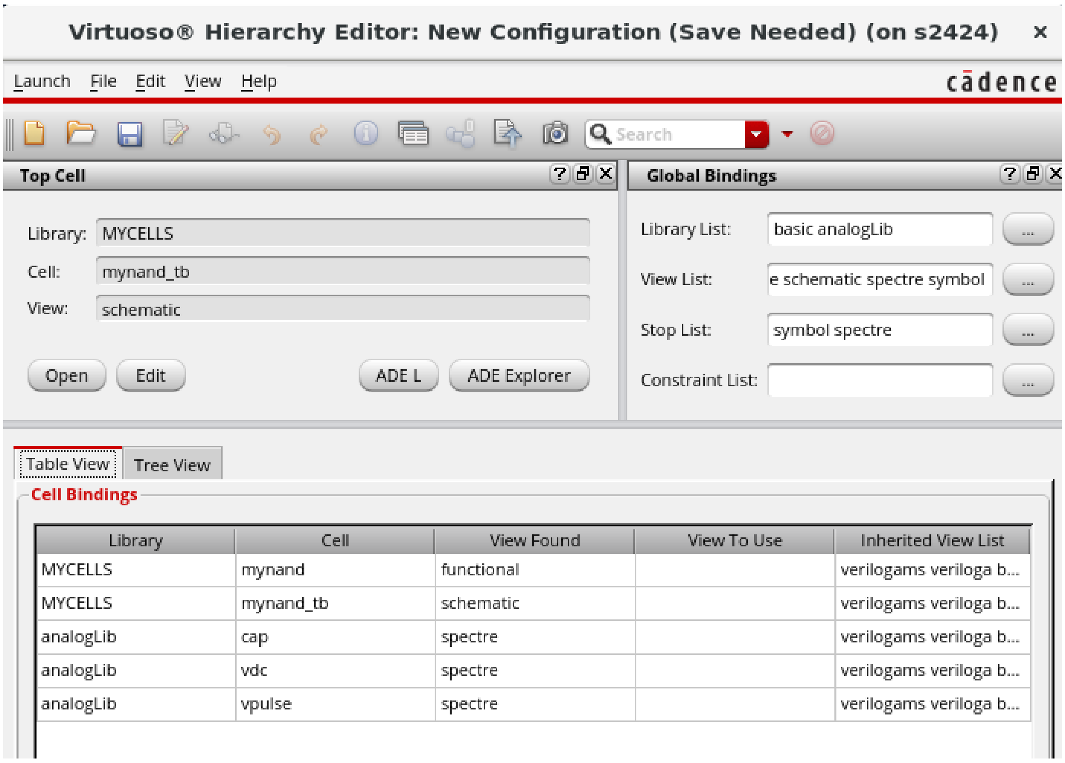
Name: AMS

From File: /home/saul/hierEditor/templates/AMS

Figure 10: Config View - template Selection

2.6 Digital Cell Layout

In the Virtuoso schematic window click on Launch->Layout XL, and then Connectivity -> Generate -> All from Source. Go to the I/O Pins and select "Metal1 pin", press Apply, and then press OK (Fig. 24). Then click on Create-> P&R Objects -> P&R Boundary and create the boundary rectangle with cell dimensions compatible with SiteDefs in the std lib technology file. In this case, the height for the core is 36 um and the width is 12 um. Activate the routing "Grids" and place the pins in the centers of the intersections (these are the best positions for innovus to do P & R). Connect all the devices using metal1 drawing. Once you are done, select "metal1 label" and use the automatically addition of labels feature (Fig. 25). Make sure you place labels inside pins, over drawing metal1 layer (you may need to add metal1 drawing rectangles). The final layout looks like in fig. 26.


Virtuoso® Hierarchy Editor: New Configuration (Save Needed) (on s2424)
Launch File Edit View Help
cadence
Search
Top Cell
Global Bindings
Open
Edit
ADE L
ADE Explorer
Table View
Tree View

Library: MYCELLS

Cell: mynand_tb

View: schematic

Library List: basic analogLib

View List: e schematic spectre symbol

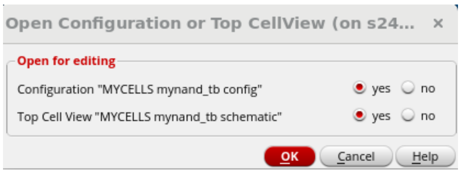
Stop List: symbol spectre

Constraint List:

Cell Bindings

Library	Cell	View Found	View To Use	Inherited View List
MYCELLS	mynand	functional		verilogams veriloga b...
MYCELLS	mynand_tb	schematic		verilogams veriloga b...
analogLib	cap	spectre		verilogams veriloga b...
analogLib	vdc	spectre		verilogams veriloga b...
analogLib	vpulse	spectre		verilogams veriloga b...

Figure 11: Config view

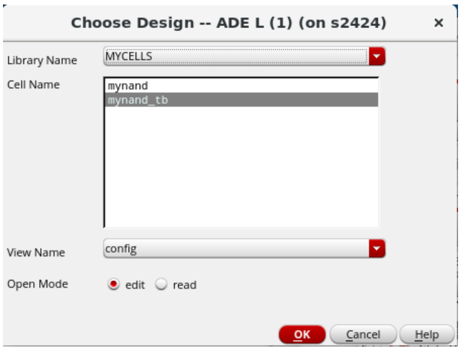


Open for editing

Configuration "MYCELLS mynand_tb config" ● yes ○ no

Top Cell View "MYCELLS mynand_tb schematic" ● yes ○ no

Figure 12: Config view - open for edit



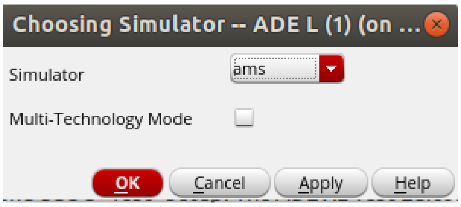
Library Name: MYCELLS

Cell Name: mynand, mynand_tb

View Name: config

Open Mode: ● edit ○ read

Figure 13: Config view - open for edit

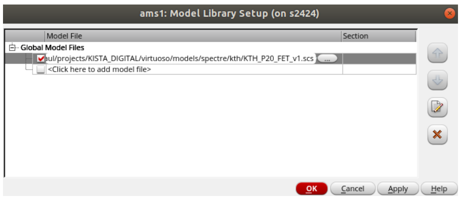


Choosing Simulator -- ADE L (1) (on ...

Simulator: ams

Multi-Technology Mode □

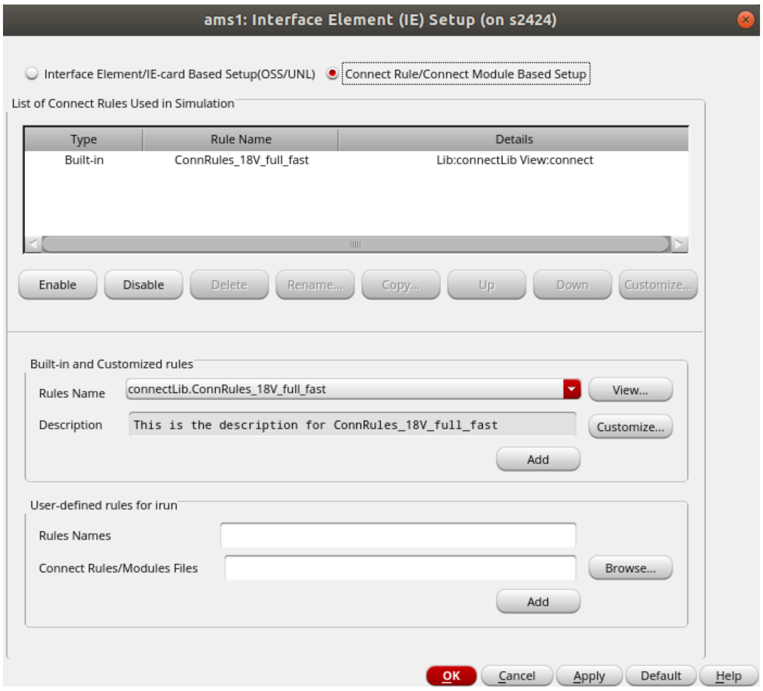
Figure 14: Choosing ams simulator



ams1: Model Library Setup (on s2424)

	Model File	Section
Global Model Files		
☑	aul/projects/KISTA_DIGITAL/virtuoso/models/spectre/kth/KTH_P20_FET_v1.scs	
□	<Click here to add model file>	

Figure 15: select analog simulation models



ams1: Interface Element (IE) Setup (on s2424)

○ Interface Element/IE-card Based Setup(OSS/UNL) ● Connect Rule/Connect Module Based Setup

List of Connect Rules Used in Simulation

Type	Rule Name	Details
Built-in	ConnRules_18V_full_fast	Lib:connectLib View:connect

Built-in and Customized rules

Rules Name: connectLib.ConnRules_18V_full_fast

Description: This is the description for ConnRules_18V_full_fast

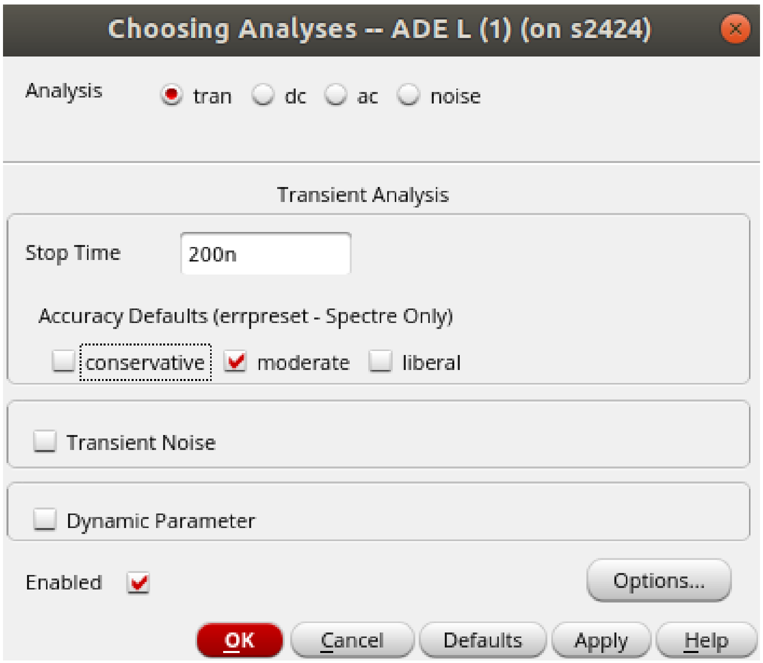
User-defined rules for irun

Rules Names:

Connect Rules/Modules Files:

Figure 16: select Connect rules

Now you are going to check for DRC violations. Go to PVS -> Run DRC. Make sure you provide a separate directory for the drc runs (Fig. 27). Otherwise your work directory will be cluttered with drc intermediate files! Select the kista_pvs Technology, default Rule Set (Fig. 28). Then go to the Input tab, Layer Map List and select "kista_1u.layermap" under the pvs directory



Choosing Analyses -- ADE L (1) (on s2424)

Analysis ● tran ○ dc ○ ac ○ noise

Transient Analysis

Stop Time 200n

Accuracy Defaults (errpreset - Spectre Only)

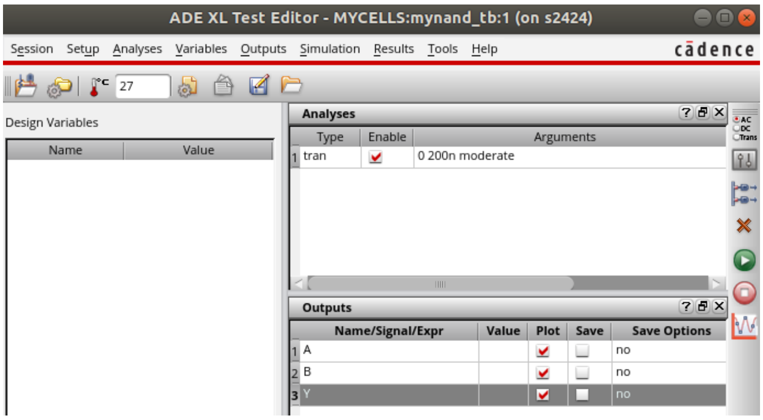
□ conservative ☑ moderate □ liberal

□ Transient Noise

□ Dynamic Parameter

Enabled ☑

Figure 17: Transient setup



ADE XL Test Editor - MYCELLS:mynand_tb:1 (on s2424)

Design Variables

Name	Value

Analyses

	Type	Enable	Arguments
1	tran	☑	0 200n moderate

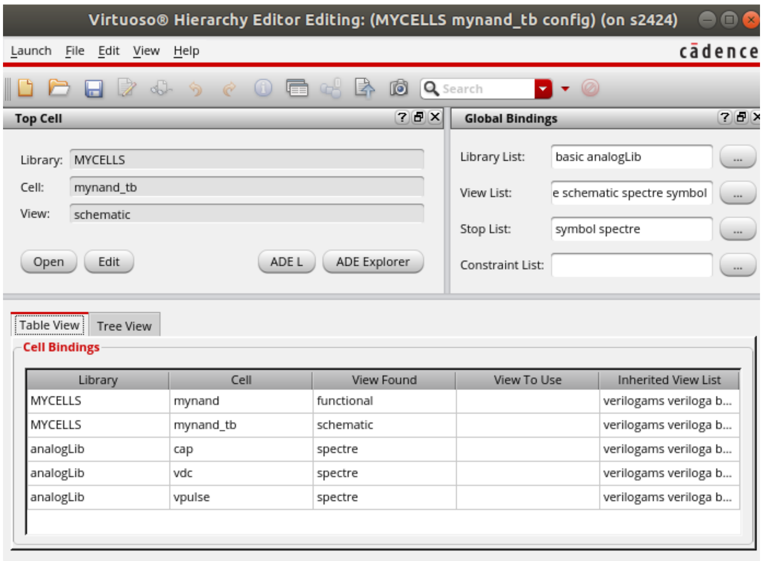
Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	□	no
2	B		☑	□	no
3	Y		☑	□	no

Figure 18: Simulation setup i ADE XL

(Fig. 29). Press "Submit" and correct any violations that the layout may have before checking LVS.

Go to PVS -> Run LVS. Make sure you provide a separate directory for the lvs runs (Fig. 30). Otherwise your work directory will be cluttered with drc intermediate files! Select the kista_pvs Technology, default Rule Set (Fig. 31). Then go to the Input tab, Layer Map List and select "kista_1u.layermap" under the pvs directory (Fig. 32). Then go to the Output tab and check the "Create Quantus QRC Input Data" (Fig. 33). Press Submit and check for mismatches.



Virtuoso® Hierarchy Editor Editing: (MYCELLS mynand_tb config) (on s2424)

Library: MYCELLS

Cell: mynand_tb

View: schematic

Library List: basic analogLib

View List: e schematic spectre symbol

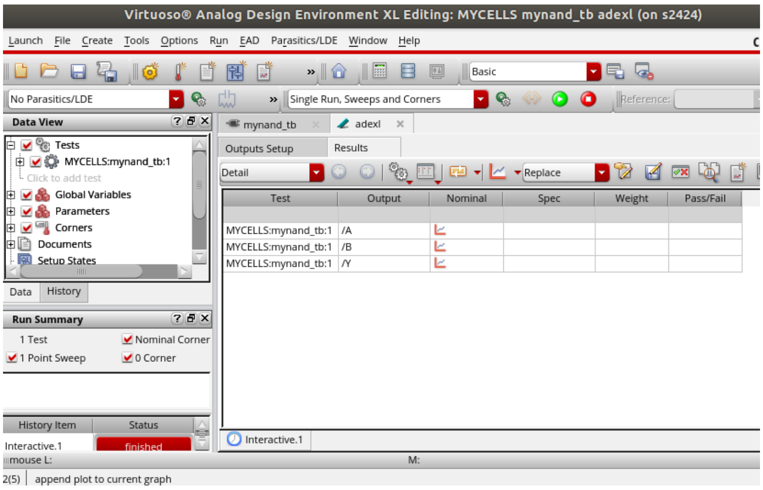
Stop List: symbol spectre

Constraint List:

Cell Bindings

Library	Cell	View Found	View To Use	Inherited View List
MYCELLS	mynand	functional		verilogams veriloga b...
MYCELLS	mynand_tb	schematic		verilogams veriloga b...
analogLib	cap	spectre		verilogams veriloga b...
analogLib	vdc	spectre		verilogams veriloga b...
analogLib	vpulse	spectre		verilogams veriloga b...

Figure 19: Config view - functional view



Virtuoso® Analog Design Environment XL Editing: MYCELLS mynand_tb adexl (on s2424)

Test	Output	Nominal	Spec	Weight	Pass/Fail
MYCELLS:mynand_tb:1	/A	📈			
MYCELLS:mynand_tb:1	/B	📈			
MYCELLS:mynand_tb:1	/Y	📈			

History Item	Status
Interactive.1	finished

Figure 20: ADEXL results

2.7 Parasitic Extraction and Parasitic Simulation

This step can be done only after PVS LVS has finished without problems and if it was configured to generate Quantus data. In the virtuoso layout go to Quantus -> Run PVS Quantus. A pop-up window will appear with all fields already filled (Fig. 34). Press OK and the Quantus Parasitic Extraction Run Form will appear. If not already pre-selected, choose the Technology "kista_pvs" and in RuleSet "rcx_typical". In Output select "Spice". The Setup tab should look like Fig. 35. Then go to the Extraction tab and select "RC" in

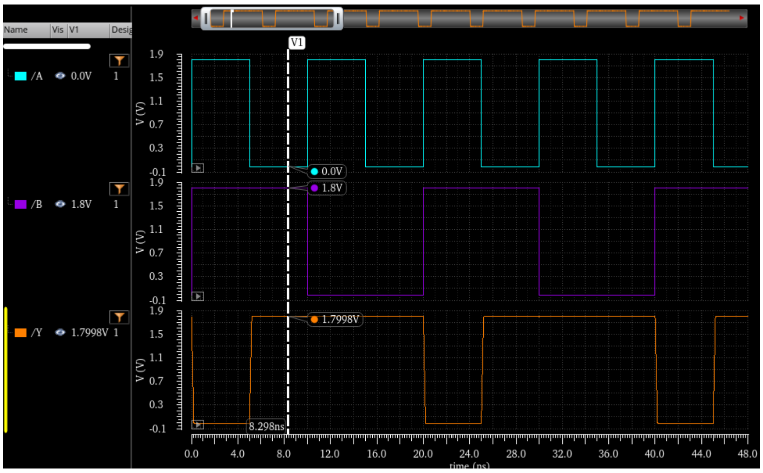
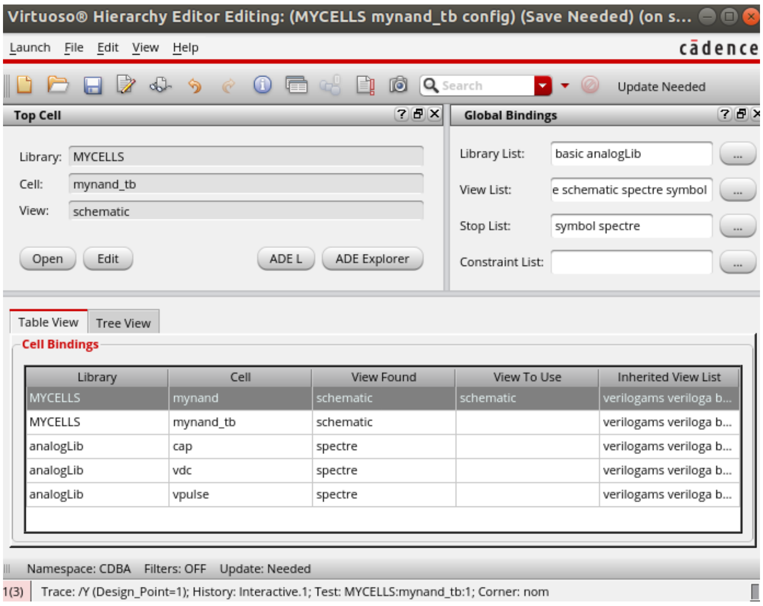


Figure 21: Functional simulation waveforms


Virtuoso® Hierarchy Editor Editing: (MYCELLS mynand_tb config) (Save Needed) (on s...

Library: MYCELLS
Cell: mynand_tb
View: schematic

Library List: basic analogLib
View List: e schematic spectre symbol
Stop List: symbol spectre
Constraint List:

Cell Bindings

Library	Cell	View Found	View To Use	Inherited View List
MYCELLS	mynand	schematic	schematic	verilogams veriloga b...
MYCELLS	mynand_tb	schematic		verilogams veriloga b...
analogLib	cap	spectre		verilogams veriloga b...
analogLib	vdc	spectre		verilogams veriloga b...
analogLib	vpulse	spectre		verilogams veriloga b...

Namespace: CDBA Filters: OFF Update: Needed

1(3) Trace: /Y (Design_Point=1); History: Interactive.1; Test: MYCELLS:mynand_tb:1; Corner: nom

Figure 22: Changing View to use

"Extraction Type". Change the "Cap Coupling Mode" to "Coulped" and give the reference node net name, which in this case is "VSS!" (Fig. 36). Now go to the Filtering tab and make sure that the "Exclude Floating Nets" is NOT checked. This is because the substrate is defined as a floating net in SOI devices. Finally go to the Netlisting tab and make sure that the "Input Hierarchy Delimiter" in the Netlisting tab is different from "/". This is not accepted in verilog and will cause at netlisting problem when using ams. Use instead "_" as shown in Fig. 37. Press Apply/OK and check the log. The spice file should have been

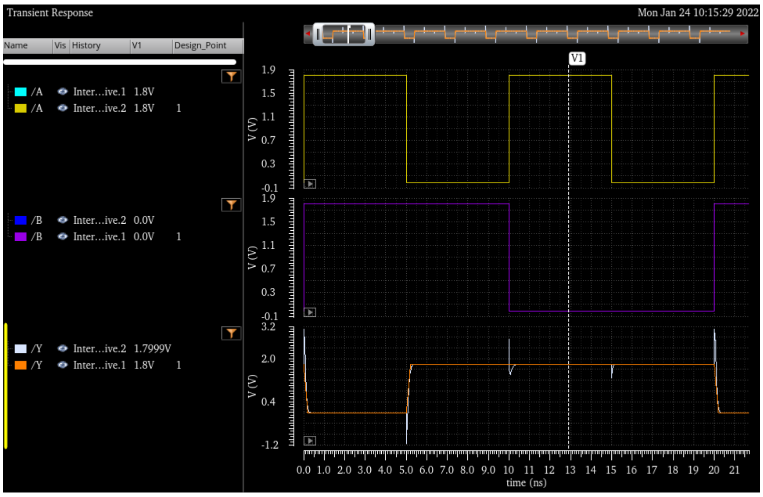
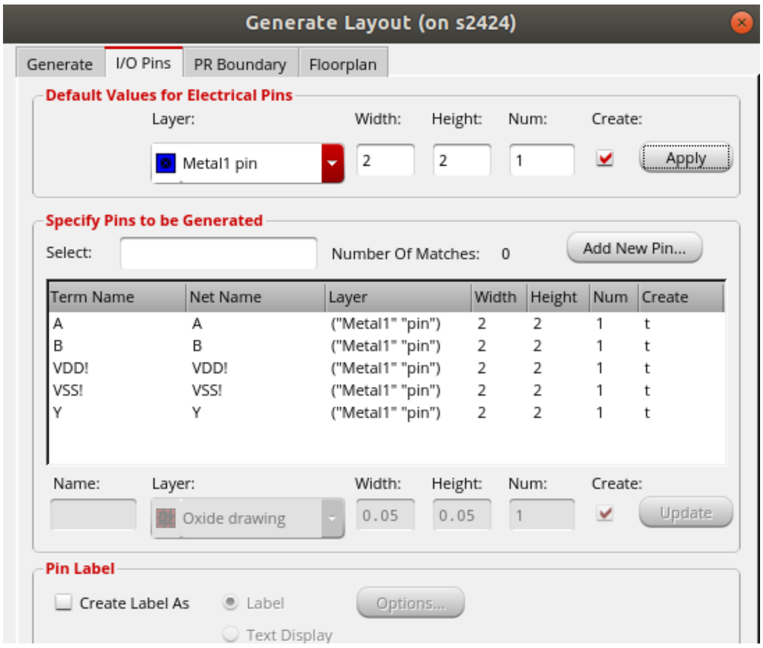


Figure 23: Schematic and Functional simulation waveforms



Generate Layout (on s2424)

Generate | I/O Pins | PR Boundary | Floorplan

Default Values for Electrical Pins

Layer:	Width:	Height:	Num:	Create:
Metal1 pin	2	2	1	☑

Apply

Specify Pins to be Generated

Select: Number Of Matches: 0

Add New Pin...

Term Name	Net Name	Layer	Width	Height	Num	Create
A	A	("Metal1" "pin")	2	2	1	t
B	B	("Metal1" "pin")	2	2	1	t
VDD!	VDD!	("Metal1" "pin")	2	2	1	t
VSS!	VSS!	("Metal1" "pin")	2	2	1	t
Y	Y	("Metal1" "pin")	2	2	1	t

Name:	Layer:	Width:	Height:	Num:	Create:
	Oxide drawing	0.05	0.05	1	☑

Update

Pin Label

□ Create Label As ● Label ○ Text Display

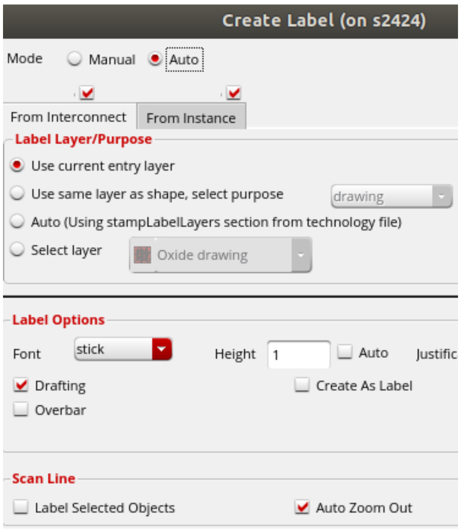
Options...

Figure 24: Generate Layout window

generated in the work directory.

Now open the spice file with gedit and check that the spice file contains the devices and parasitics:

The subcircuit definition in the spice file generated by Quantus includes global nets VDD! and VSS! as regular nets. This needs to be changed manually. The solution is simple. Go to the header of the extracted spice file and



Create Label (on s2424)

Mode ○ Manual ● Auto

☑ ☑

From Interconnect | From Instance

Label Layer/Purpose

● Use current entry layer

○ Use same layer as shape, select purpose drawing

○ Auto (Using stampLabelLayers section from technology file)

○ Select layer Oxide drawing

Label Options

Font stick Height 1 □ Auto Justific

☑ Drafting □ Create As Label

□ Overbar

Scan Line

□ Label Selected Objects ☑ Auto Zoom Out

Figure 25: Create label window

remove the global nets from the subcircuit definition and add them as global nets:

Before:

```
*
.SUBCKT mynand VSS! VDD! B Y A
*
```

After:

```
*
.global VSS! VDD!
.SUBCKT mynand B Y A
*
```

In addition, it is needed to manually connect the substrate to a known potential. The substrate is extracted as a floating node and it is named with an integer number. It is the only node that is named like that and it is easy to spot because many parasitic capacitors are connected to it. In this example, the substrate is node number 3 (Fig. 39). This node can be connected to ground by using for instance a small resistor that mimics the substrate resistance. Add the following line at the end of the list of parasitic resistors:

```
Rs1 3 VSS! 50
```

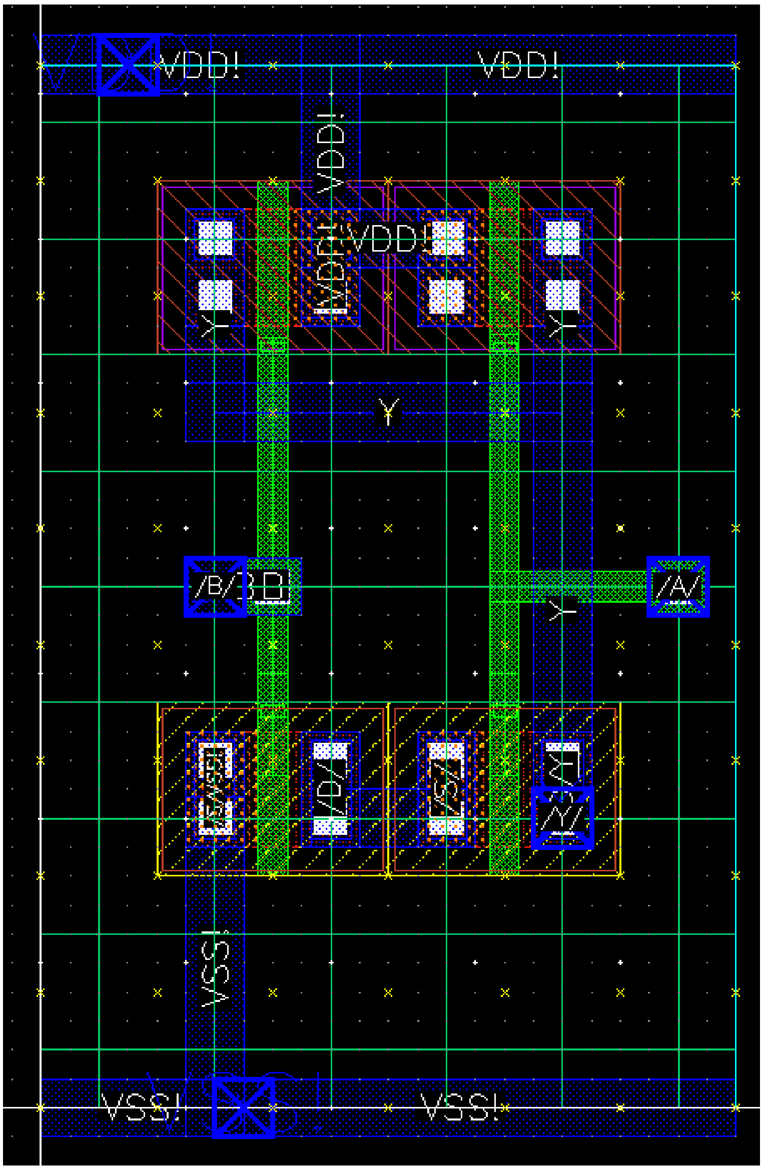
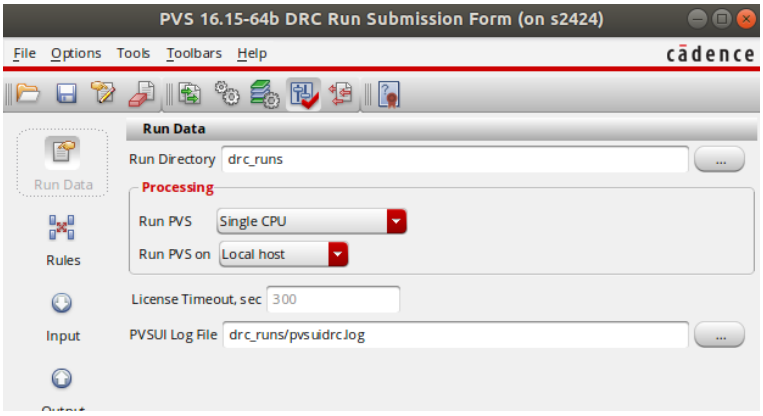


Figure 26: Final layout

Now you import this spice file and create a schematic cell. In the CIW go to File -> Import -> Spice. In the "Input" tab provide the netlist file, change the "Netlist Language" to SPICE, add "analogLib" and "KISTA_1UM" to the "Reference Library List", and check "Device Mapping File" as shown in Fig. 40.

Go to the "Output" tab and update the "Output Library" with the library containing the cell mynand. In "Output View Name" write "analog_extracted" (Fig. **??**).

Finally, go to the "Device Map" cell, click in the "File" button and load the


PVS 16.15-64b DRC Run Submission Form (on s2424)
File Options Tools Toolbars Help
cādence
Run Data
Rules
Input
Output
Run Data
Processing

Run Directory drc_runs

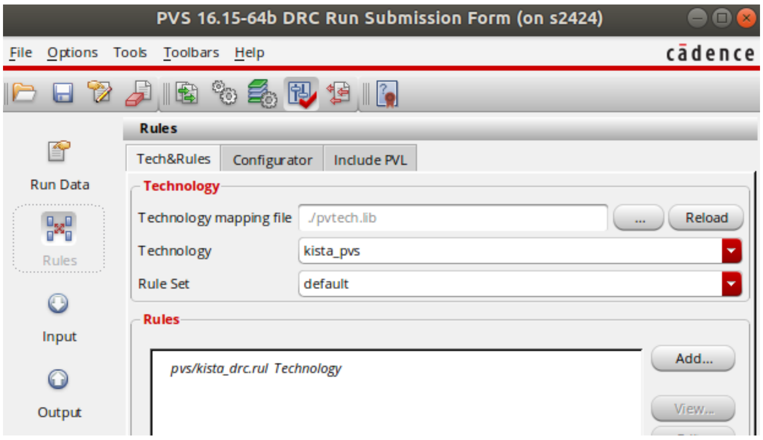
Run PVS Single CPU

Run PVS on Local host

License Timeout, sec 300

PVSUI Log File drc_runs/pvsuidrc.log

Figure 27: PVS DRC - Run Data



Technology mapping file ./pvtech.lib

Technology kista_pvs

Rule Set default

pvs/kista_drc.rul Technology

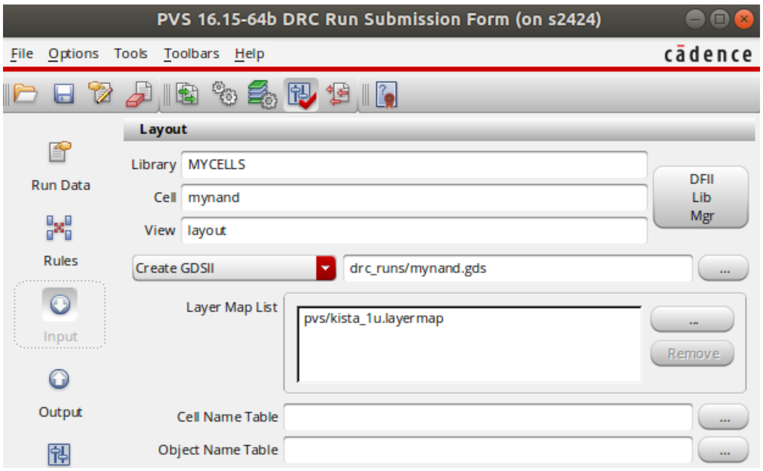
Figure 28: PVS DRC - Rules

"map_spice.txt" file located under the qrc directory. Press OK and check the log.

At this point, a new schematic view called analog_extracted is available. Open it and check that the substrate node (node 3 in this case) is correctly connected to VSS! through resistor Rs1 (Fig. 43).

2.8 Simulation of Parasitic extraction

You need to use exactly the same config and adexl views that you already used in 2.5. Open the config view (including the scheamtic) for mynand_tb and launch ADE-XL from the schematic window. Now go to the config view and right-click on mynand and select the "analog_extracted" view. Click on the "Recompute the hierarchy" button, and run the simulation. Click on "Plot All" and you will see the waveforms after parasitic extraction. Change "Re-


PVS 16.15-64b DRC Run Submission Form (on s2424)
File Options Tools Toolbars Help
cādence
Run Data
Rules
Input
Output
DFII Lib Mgr
...
Remove

Layout

Library MYCELLS

Cell mynand

View layout

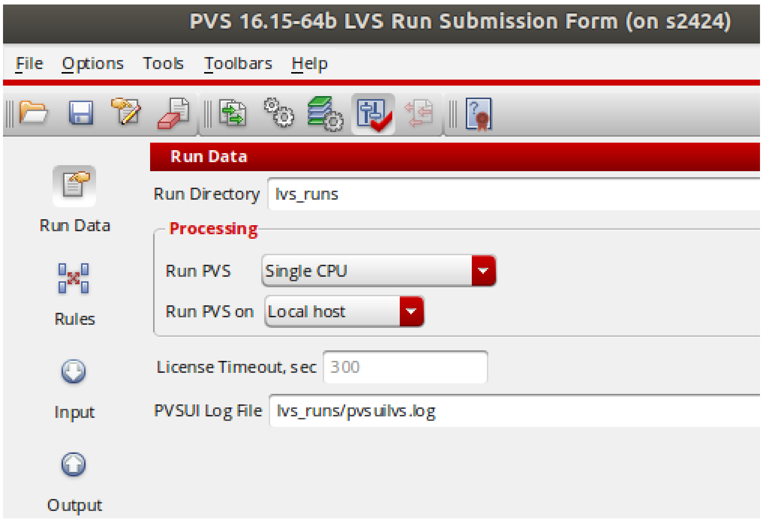
Create GDSII drc_runs/mynand.gds

Layer Map List pvs/kista_1u.layermap

Cell Name Table

Object Name Table

Figure 29: PVS DRC - Input


PVS 16.15-64b LVS Run Submission Form (on s2424)
File Options Tools Toolbars Help
Run Data
Rules
Input
Output

Run Data

Run Directory lvs_runs

Processing

Run PVS Single CPU

Run PVS on Local host

License Timeout, sec 300

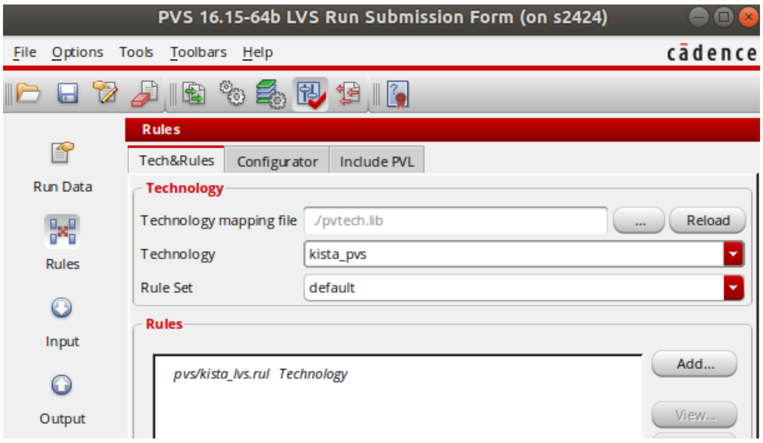
PVSUI Log File lvs_runs/pvsuilvs.log

Figure 30: PVS LVS - Run Data

place" for "Append" in the ADE XL and run simulations for "functional" and "schematic" views. Now you can see the waveforms for functional (RTL), schematic (transistor level), and parasitic extracted views (Fig. 45).

3 Analog Block

4 Mixed Signal Circuit



Technology

Technology mapping file ./pvtech.lib

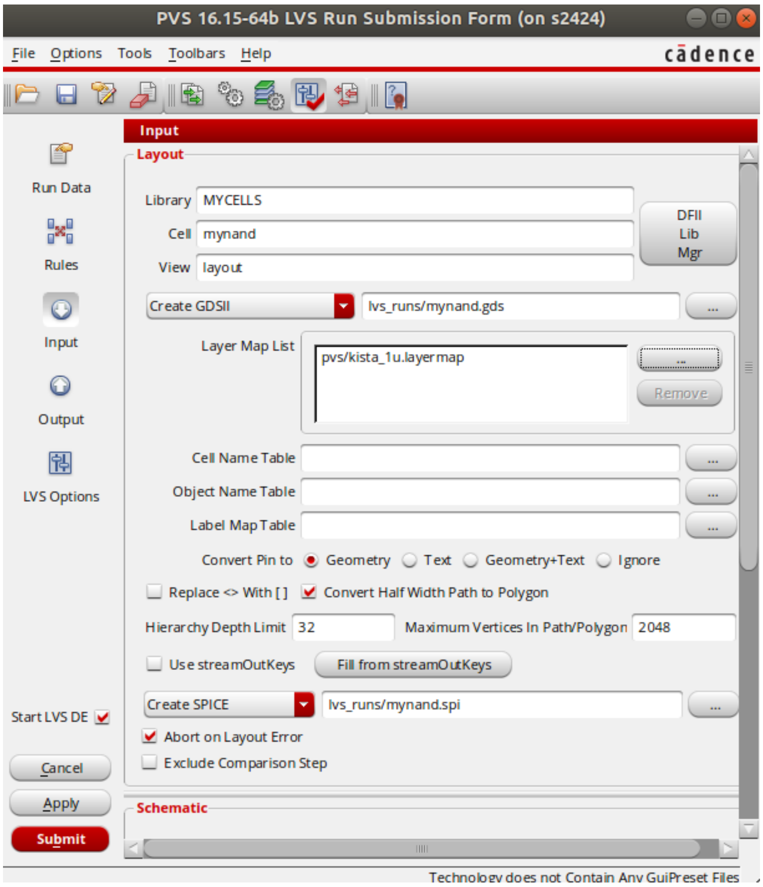
Technology kista_pvs

Rule Set default

Rules

pvs/kista_lvs.rul Technology

Figure 31: PVS DRC - Rules



Layout

Library MYCELLS

Cell mynand

View layout

Create GDSII lvs_runs/mynand.gds

Layer Map List pvs/kista_1u.layermap

Cell Name Table

Object Name Table

Label Map Table

Convert Pin to ● Geometry ○ Text ○ Geometry+Text ○ Ignore

□ Replace <> With [ ] ☑ Convert Half Width Path to Polygon

Hierarchy Depth Limit 32 Maximum Vertices In Path/Polygon 2048

□ Use streamOutKeys

Create SPICE lvs_runs/mynand.spi

☑ Abort on Layout Error

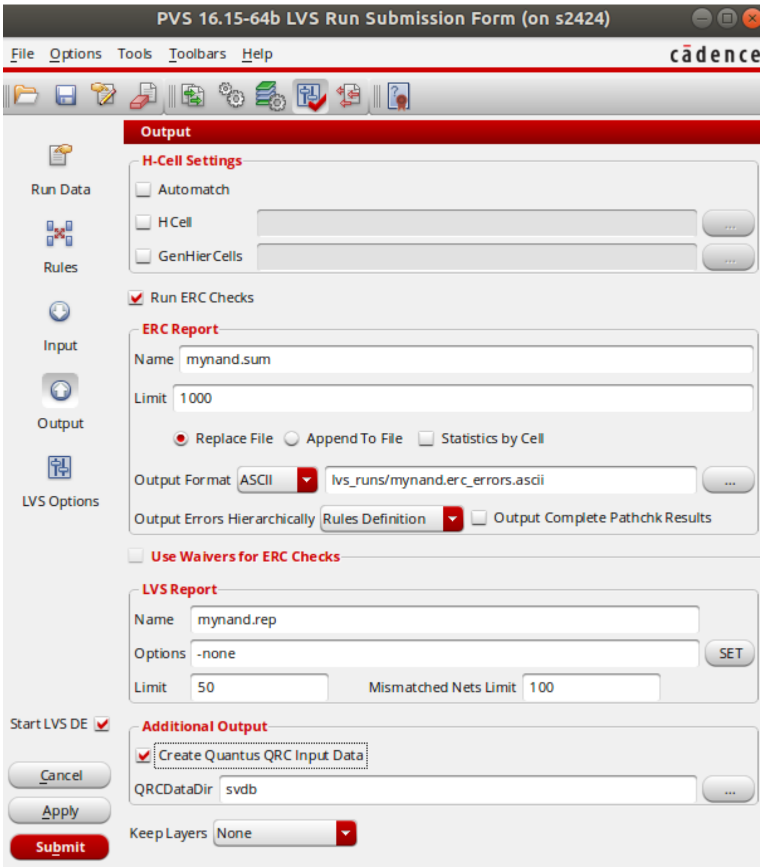
□ Exclude Comparison Step

Start LVS DE ☑

Schematic

Technology does not Contain Any GuiPreset Files

Figure 32: PVS DRC - Input


PVS 16.15-64b LVS Run Submission Form (on s2424)
File Options Tools Toolbars Help
cādence
Run Data
Rules
Input
Output
LVS Options
Cancel
Apply
Submit

Output

H-Cell Settings

□ Automatch

□ HCell

□ GenHierCells

☑ Run ERC Checks

ERC Report

Name mynand.sum

Limit 1000

● Replace File ○ Append To File □ Statistics by Cell

Output Format ASCII lvs_runs/mynand.erc_errors.ascii

Output Errors Hierarchically Rules Definition □ Output Complete Pathchk Results

□ Use Waivers for ERC Checks

LVS Report

Name mynand.rep

Options -none SET

Limit 50 Mismatched Nets Limit 100

Start LVS DE ☑

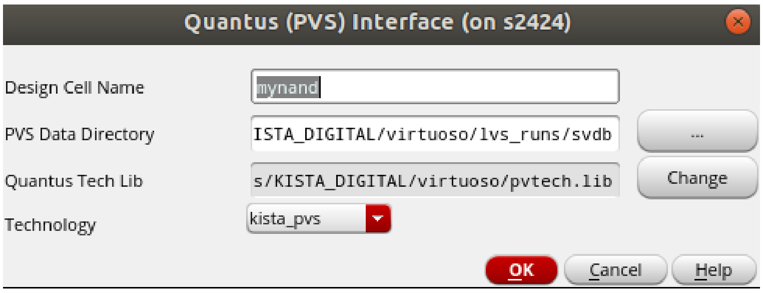
Additional Output

☑ Create Quantus QRC Input Data

QRCDataDir svdb

Keep Layers None

Figure 33: PVS DRC - Output



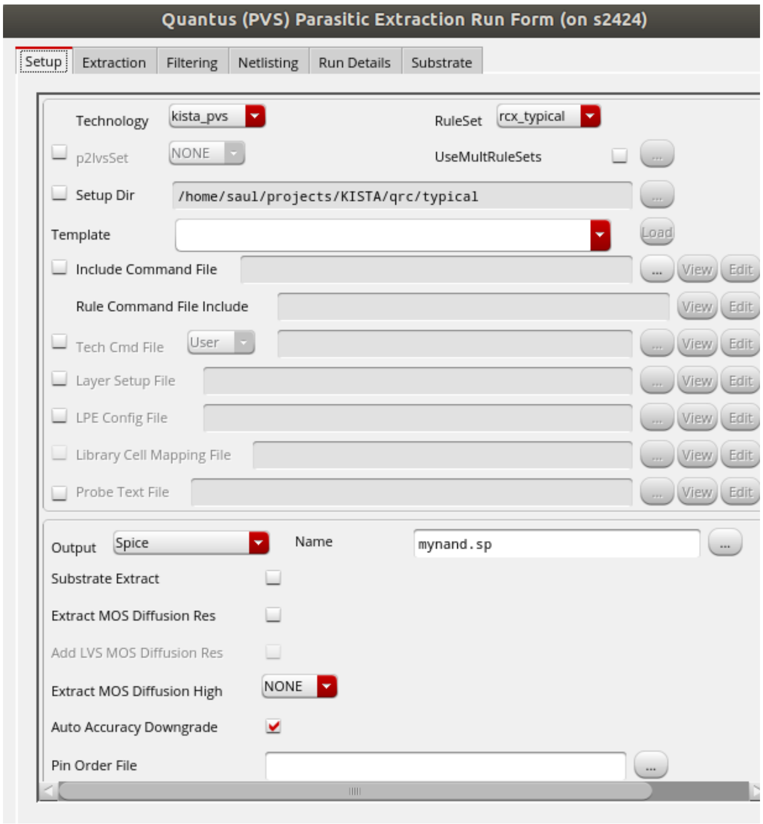
Design Cell Name mynand

PVS Data Directory ISTA_DIGITAL/virtuoso/lvs_runs/svdb ...

Quantus Tech Lib s/KISTA_DIGITAL/virtuoso/pvtech.lib Change

Technology kista_pvs

Figure 34: Quantus Config



Technology kista_pvs

RuleSet rcx_typical

□ p2lvsSet NONE

UseMultRuleSets □

□ Setup Dir /home/saul/projects/KISTA/qrc/typical

Template

□ Include Command File

Rule Command File Include

□ Tech Cmd File User

□ Layer Setup File

□ LPE Config File

□ Library Cell Mapping File

□ Probe Text File

Output Spice

Name mynand.sp

Substrate Extract □

Extract MOS Diffusion Res □

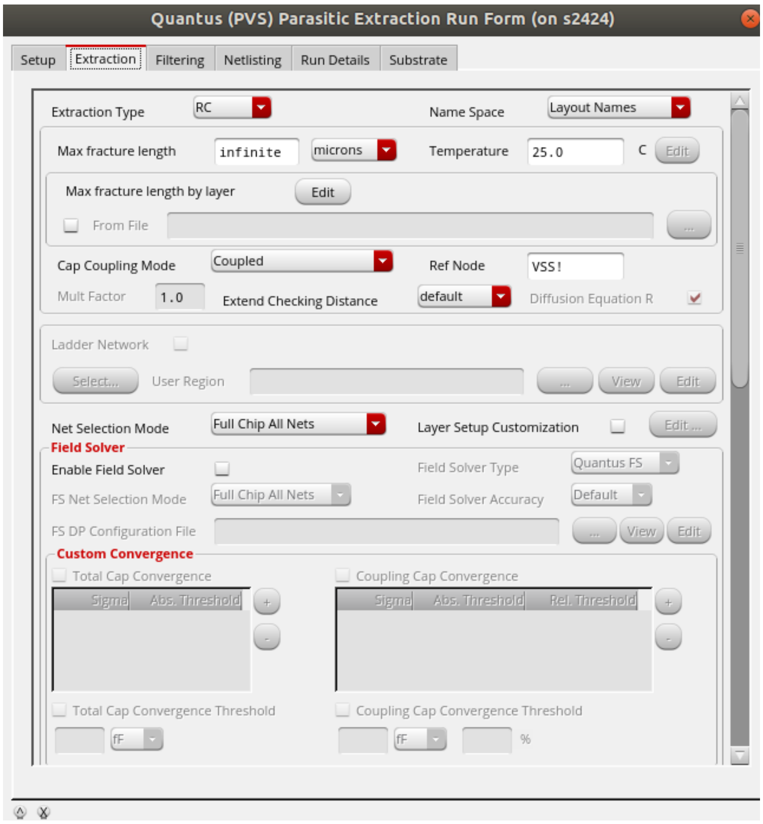
Add LVS MOS Diffusion Res □

Extract MOS Diffusion High NONE

Auto Accuracy Downgrade ☑

Pin Order File

Figure 35: Quantus Setup Tab



Quantus (PVS) Parasitic Extraction Run Form (on s2424)

Extraction Type: RC

Name Space: Layout Names

Max fracture length: infinite microns

Temperature: 25.0 C

Max fracture length by layer

□ From File

Cap Coupling Mode: Coupled

Ref Node: VSS!

Mult Factor: 1.0

Extend Checking Distance: default

Diffusion Equation R ☑

Ladder Network □

User Region

Net Selection Mode: Full Chip All Nets

Layer Setup Customization □

Field Solver

Enable Field Solver □

Field Solver Type: Quantus FS

FS Net Selection Mode: Full Chip All Nets

Field Solver Accuracy: Default

FS DP Configuration File

Custom Convergence

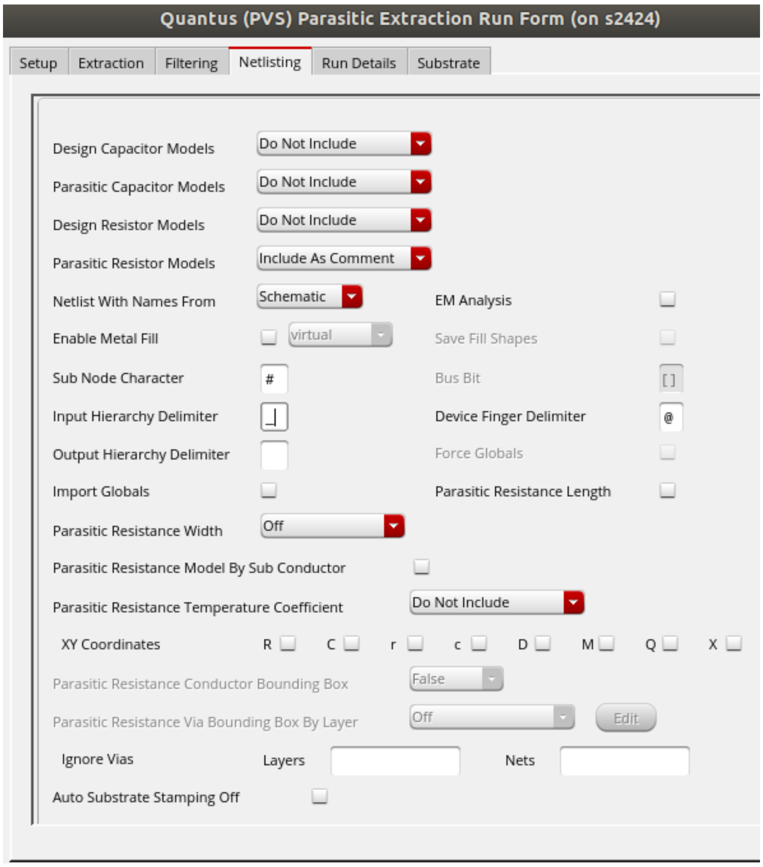
□ Total Cap Convergence

□ Coupling Cap Convergence

□ Total Cap Convergence Threshold

□ Coupling Cap Convergence Threshold

Figure 36: Quantus Extraction Tab



Design Capacitor Models: Do Not Include

Parasitic Capacitor Models: Do Not Include

Design Resistor Models: Do Not Include

Parasitic Resistor Models: Include As Comment

Netlist With Names From: Schematic

EM Analysis □

Enable Metal Fill □ virtual

Save Fill Shapes □

Sub Node Character: #

Bus Bit: []

Input Hierarchy Delimiter: _

Device Finger Delimiter: @

Output Hierarchy Delimiter:

Force Globals □

Import Globals □

Parasitic Resistance Length □

Parasitic Resistance Width: Off

Parasitic Resistance Model By Sub Conductor □

Parasitic Resistance Temperature Coefficient: Do Not Include

XY Coordinates R □ C □ r □ c □ D □ M □ Q □ X □

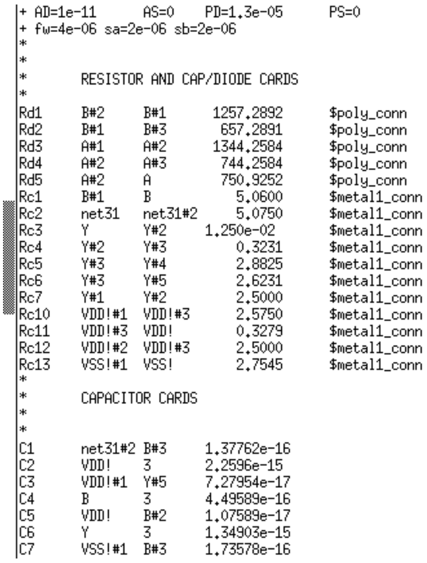
Parasitic Resistance Conductor Bounding Box: False

Parasitic Resistance Via Bounding Box By Layer: Off

Ignore Vias Layers: Nets:

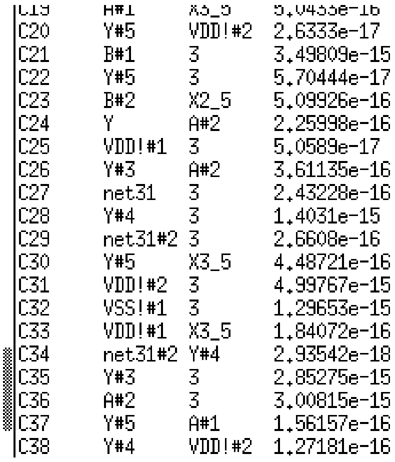
Auto Substrate Stamping Off □

Figure 37: Quantus Netlisting Tab



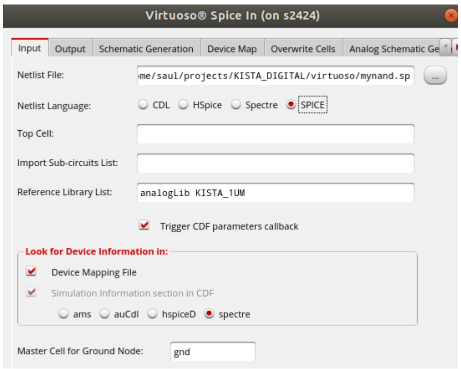
```
+ AD=1e-11      AS=0    PD=1.3e-05      PS=0
+ fw=4e-06 sa=2e-06 sb=2e-06
*
*
*       RESISTOR AND CAP/DIODE CARDS
*
Rd1     B#2     B#1      1257.2892      $poly_conn
Rd2     B#1     B#3       657.2891      $poly_conn
Rd3     A#1     A#2      1344.2584      $poly_conn
Rd4     A#2     A#3       744.2584      $poly_conn
Rd5     A#2     A         750.9252      $poly_conn
Rc1     B#1     B            5.0600     $metal1_conn
Rc2     net31   net31#2      5.0750     $metal1_conn
Rc3     Y       Y#2     1.250e-02       $metal1_conn
Rc4     Y#2     Y#3          0.3231     $metal1_conn
Rc5     Y#3     Y#4          2.8825     $metal1_conn
Rc6     Y#3     Y#5          2.6231     $metal1_conn
Rc7     Y#1     Y#2          2.5000     $metal1_conn
Rc10    VDD!#1  VDD!#3       2.5750     $metal1_conn
Rc11    VDD!#3  VDD!         0.3279     $metal1_conn
Rc12    VDD!#2  VDD!#3       2.5000     $metal1_conn
Rc13    VSS!#1  VSS!         2.7545     $metal1_conn
*
*       CAPACITOR CARDS
*
*
C1      net31#2 B#3     1.37762e-16
C2      VDD!    3       2.2596e-15
C3      VDD!#1  Y#5     7.27954e-17
C4      B       3       4.49589e-16
C5      VDD!    B#2     1.07589e-17
C6      Y       3       1.34903e-15
C7      VSS!#1  B#3     1.73578e-16
```

Figure 38: Spice Netlist with parasitics



```
C19     A#1     X3_5    5,04553e-16
C20     Y#5     VDD!#2  2,6333e-17
C21     B#1     3       3,49809e-15
C22     Y#5     3       5,70444e-17
C23     B#2     X2_5    5,09926e-16
C24     Y       A#2     2,25998e-16
C25     VDD!#1  3       5,0589e-17
C26     Y#3     A#2     3,61135e-16
C27     net31   3       2,43228e-16
C28     Y#4     3       1,4031e-15
C29     net31#2 3       2,6608e-16
C30     Y#5     X3_5    4,48721e-16
C31     VDD!#2  3       4,99767e-15
C32     VSS!#1  3       1,29653e-15
C33     VDD!#1  X3_5    1,84072e-16
C34     net31#2 Y#4     2,93542e-18
C35     Y#3     3       2,85275e-15
C36     A#2     3       3,00815e-15
C37     Y#5     A#1     1,56157e-16
C38     Y#4     VDD!#2  1,27181e-16
```

Figure 39: Floating substrate net identification



Netlist File: me/saul/projects/KISTA_DIGITAL/virtuoso/mynand.sp

Netlist Language: ○ CDL ○ HSpice ○ Spectre ● SPICE

Top Cell:

Import Sub-circuits List:

Reference Library List: analogLib KISTA_1UM

☑ Trigger CDF parameters callback

Look for Device Information in:

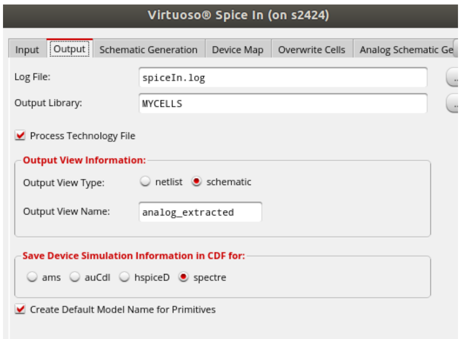
☑ Device Mapping File

☑ Simulation Information section in CDF

○ ams ○ auCdl ○ hspiceD ● spectre

Master Cell for Ground Node: gnd

Figure 40: Virtuoso Spice In - Input



Log File: spiceIn.log

Output Library: MYCELLS

☑ Process Technology File

Output View Information:

Output View Type: ○ netlist ● schematic

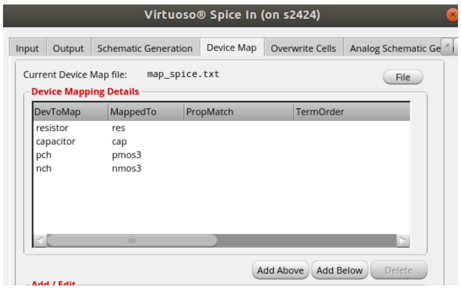
Output View Name: analog_extracted

Save Device Simulation Information in CDF for:

○ ams ○ auCdl ○ hspiceD ● spectre

☑ Create Default Model Name for Primitives

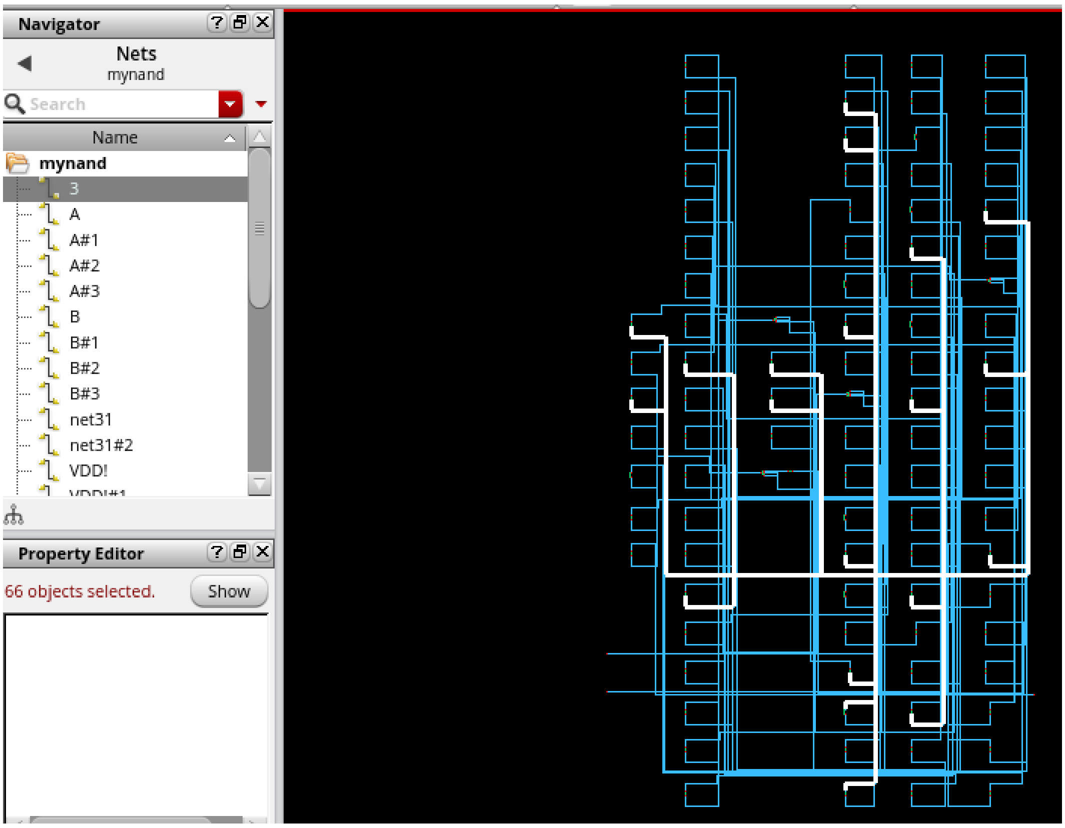
Figure 41: Virtuoso Spice In - Output



Current Device Map file: map_spice.txt

DevToMap	MappedTo	PropMatch	TermOrder
resistor	res		
capacitor	cap		
pch	pmos3		
nch	nmos3		

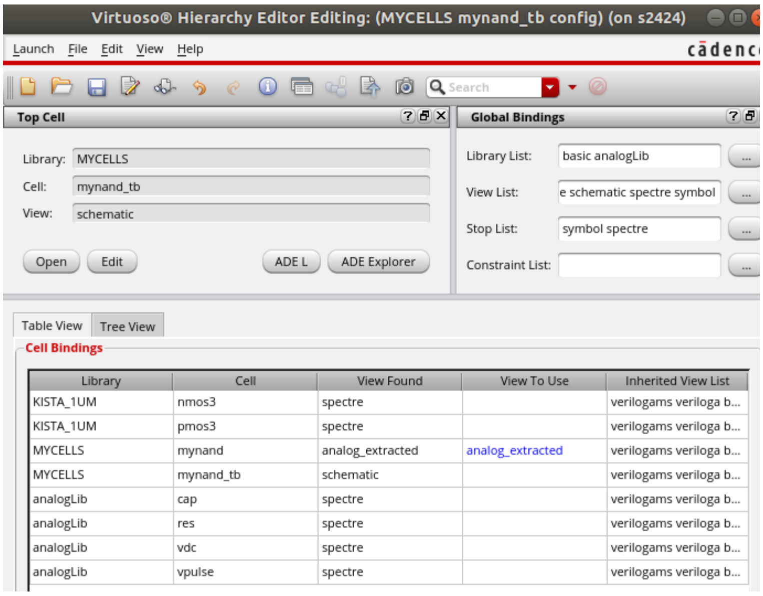
Figure 42: Virtuoso Spice In - Device Map



mynand
3
A
A#1
A#2
A#3
B
B#1
B#2
B#3
net31
net31#2
VDD!
VDD!#1

66 objects selected.

Figure 43: Schematic Extracted View



Virtuoso® Hierarchy Editor Editing: (MYCELLS mynand_tb config) (on s2424)

Top Cell

Library: MYCELLS

Cell: mynand_tb

View: schematic

Global Bindings

Library List: basic analogLib

View List: e schematic spectre symbol

Stop List: symbol spectre

Constraint List:

Cell Bindings

Library	Cell	View Found	View To Use	Inherited View List
KISTA_1UM	nmos3	spectre		verilogams veriloga b...
KISTA_1UM	pmos3	spectre		verilogams veriloga b...
MYCELLS	mynand	analog_extracted	analog_extracted	verilogams veriloga b...
MYCELLS	mynand_tb	schematic		verilogams veriloga b...
analogLib	cap	spectre		verilogams veriloga b...
analogLib	res	spectre		verilogams veriloga b...
analogLib	vdc	spectre		verilogams veriloga b...
analogLib	vpulse	spectre		verilogams veriloga b...

Figure 44: Config view - parasitic extraction

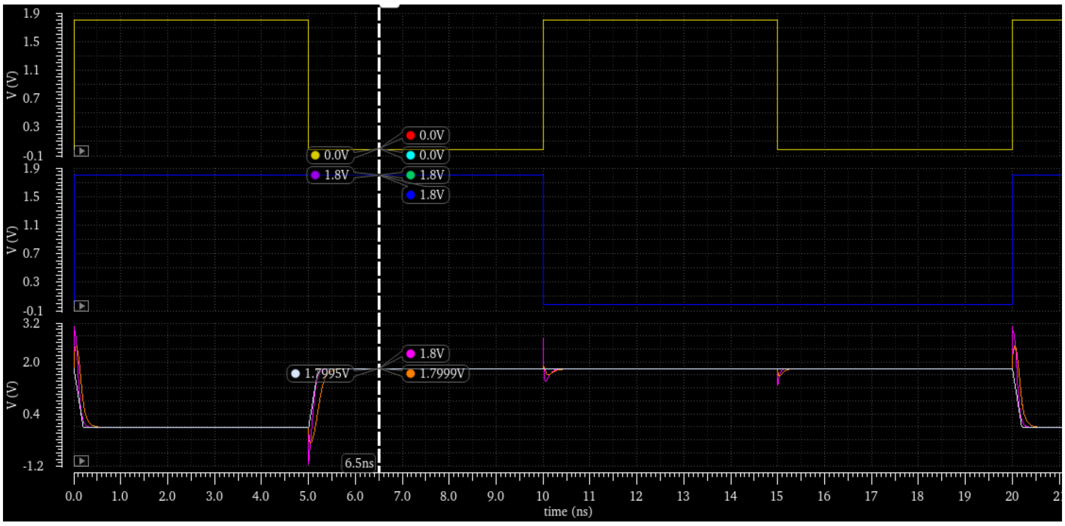


Figure 45: Config view - parasitic extraction

]