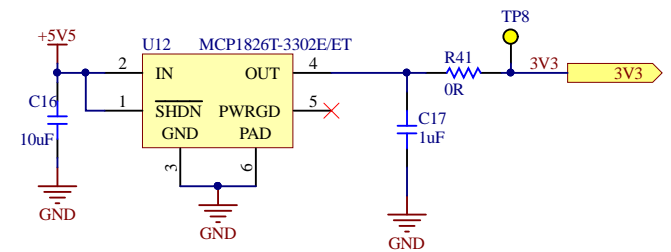
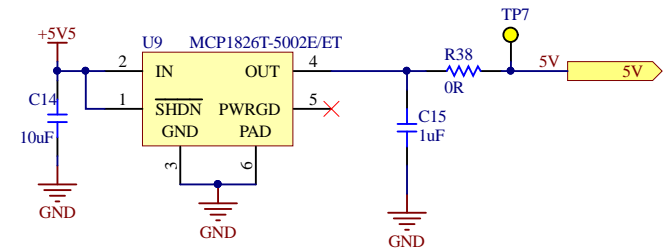
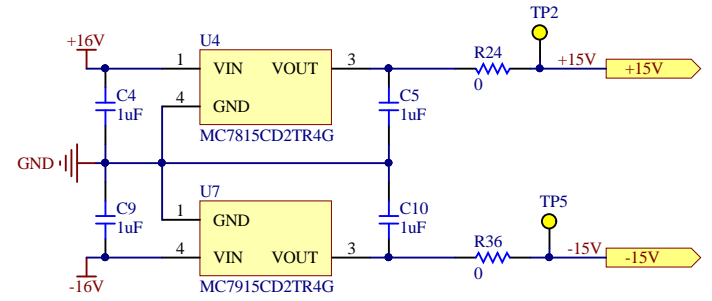


LDOs



Title: **Isolated Power**

File: PowerIsolation.SchDoc

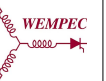
Sheet: 2 of 5

Revision: C

Time: 2:06:54 PM

Date: 4/13/2020

Engineer: Ashad Farhan



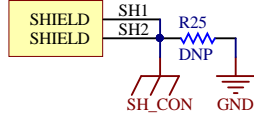
CON1A

ICD15S13E6GX00LF

1	1	5V_IN
2	2	SPI1_IN_P
3	3	SPI1_IN_N
4	4	SPI2_IN_P
5	5	SPI2_IN_N
6	6	
7	7	SPI1_IP
8	8	SPI1_IM
9	9	SPI2_IP
10	10	SPI2_IM
11	11	GND_IN
12	12	SPI1_OUT_P
13	13	SPI1_OUT_N
14	14	SPI2_OUT_P
15	15	SPI2_OUT_N

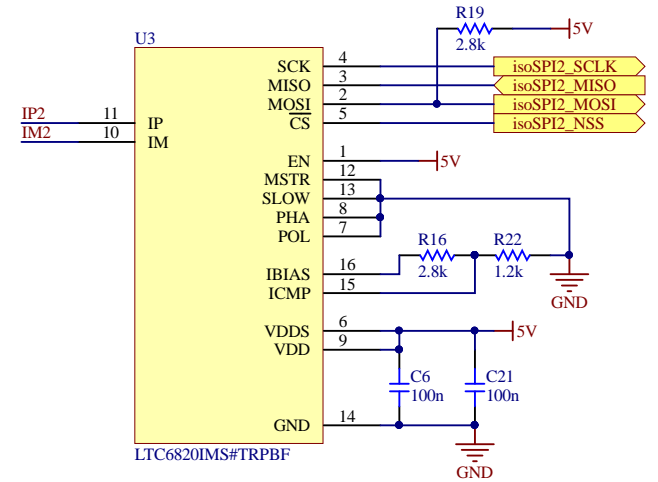
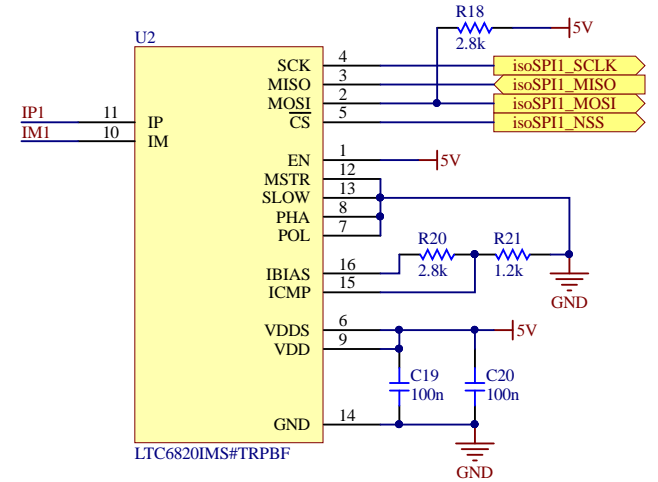
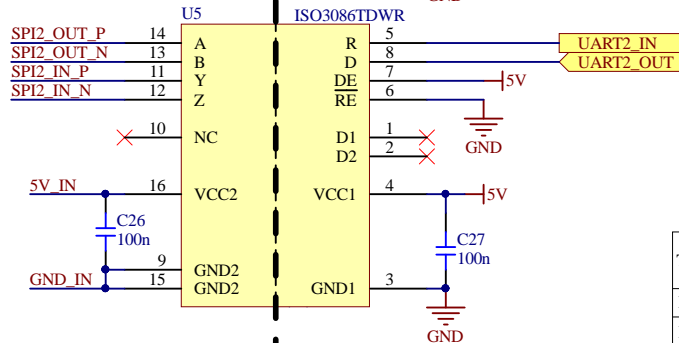
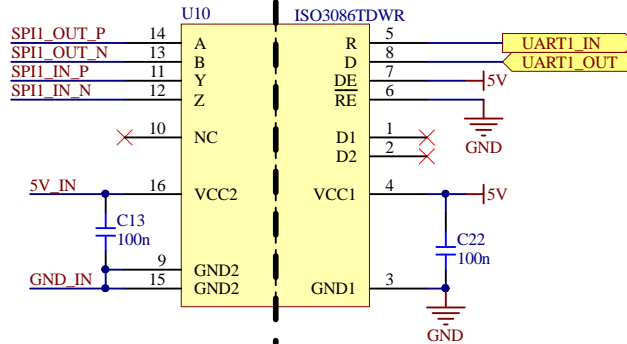
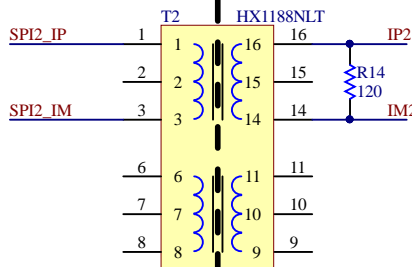
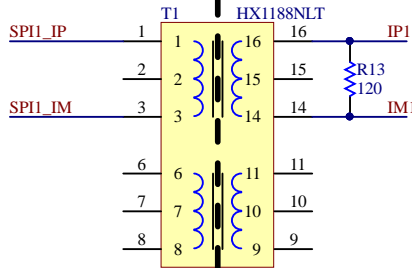
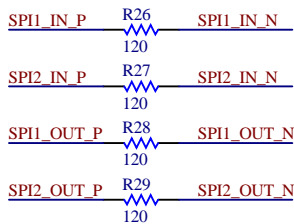
CON1B

ICD15S13E6GX00LF



NOTE: HD15 CON labels match AMDC, so IN / OUT are flipped for this board.

IN is our output
OUT is our input



Title: **Connector + Isolation**

File: ConnectorIsolation.SchDoc

Sheet: 3 of 5

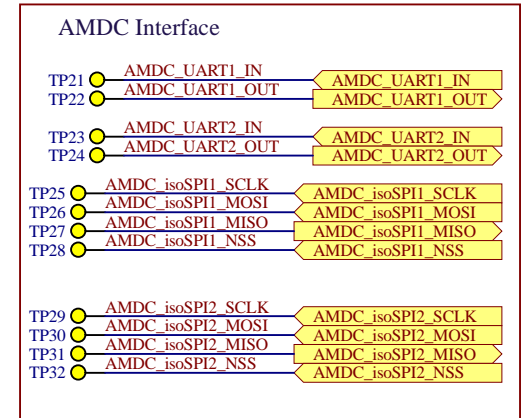
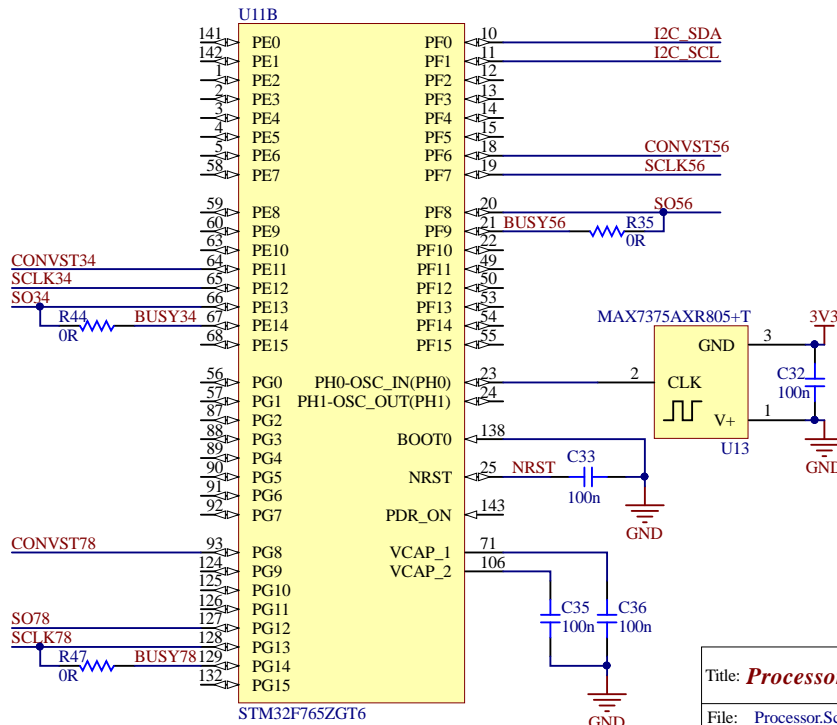
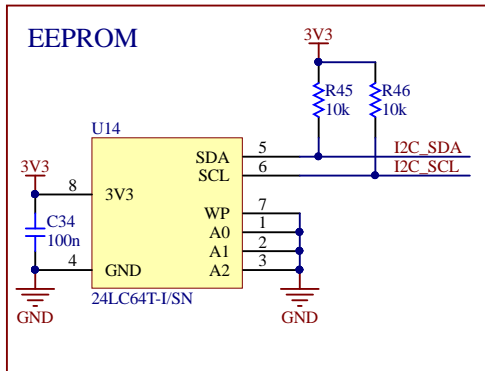
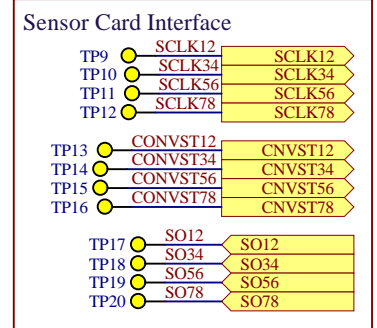
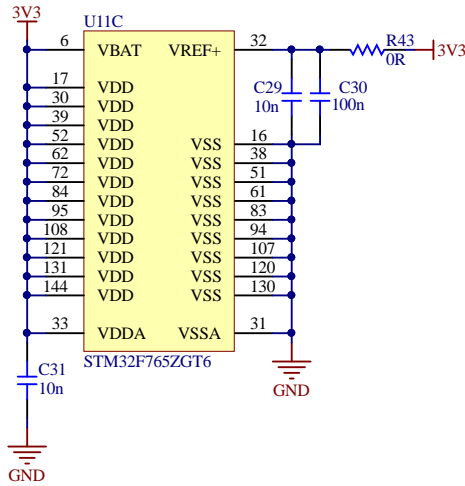
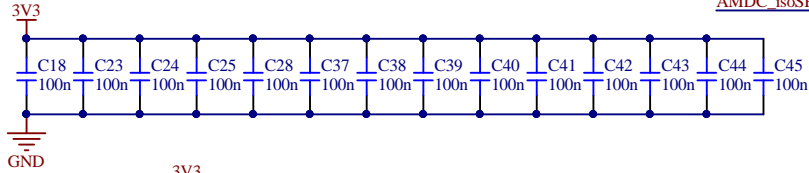
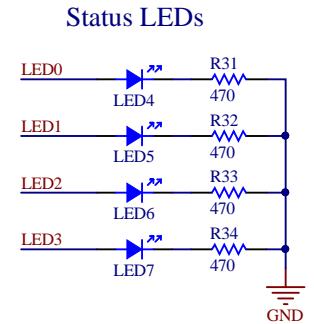
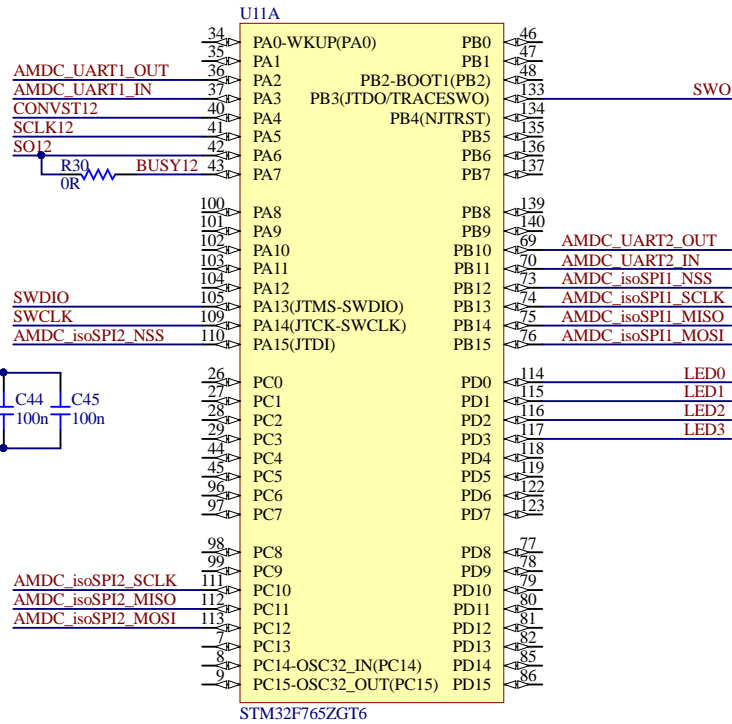
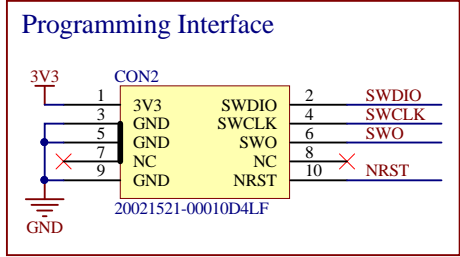
Revision: C

Time: 2:06:55 PM

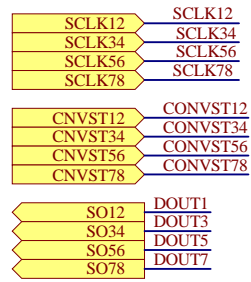
Date: 4/13/2020

Engineer: Nathan Petersen

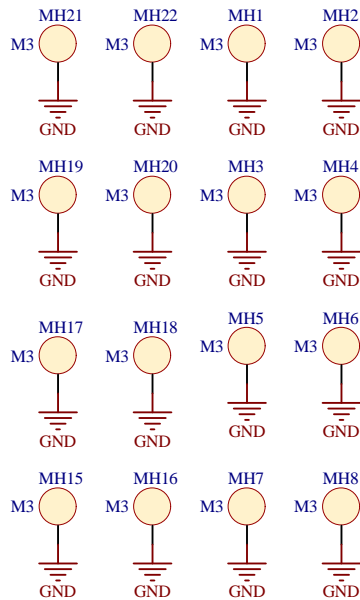




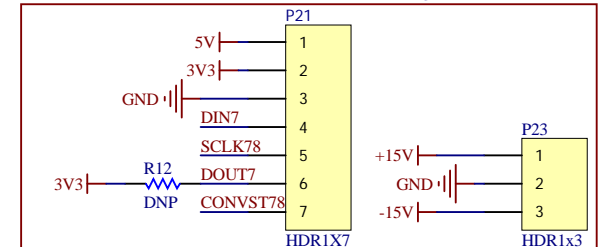
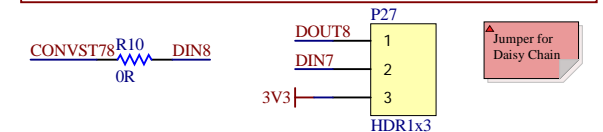
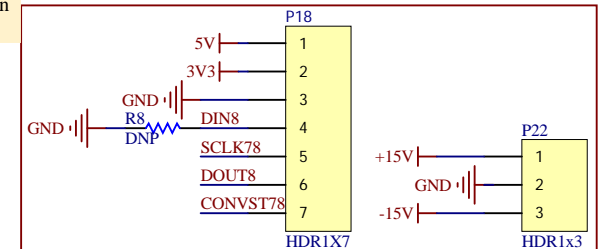
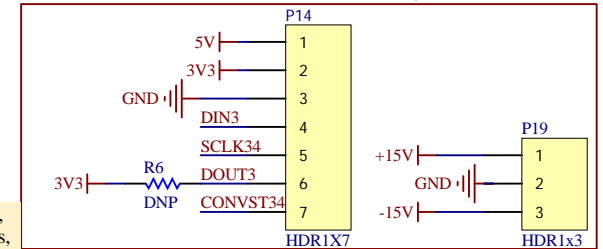
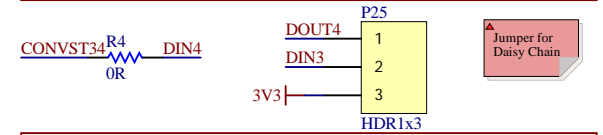
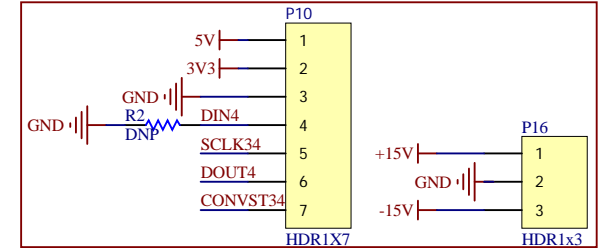
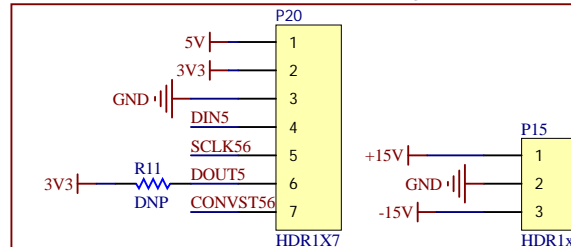
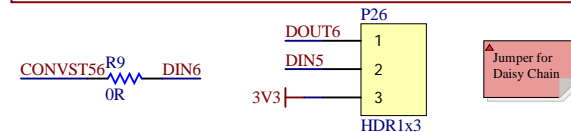
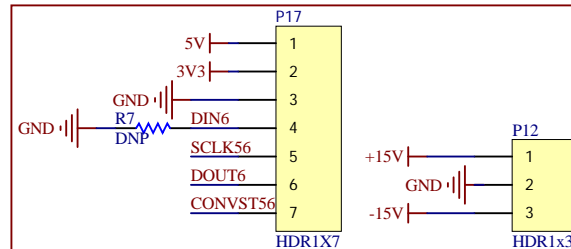
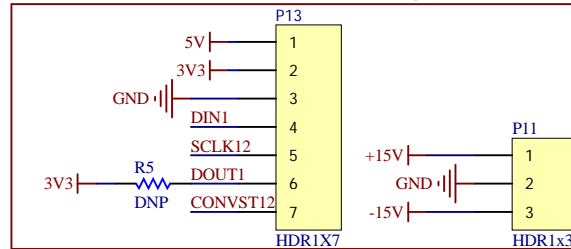
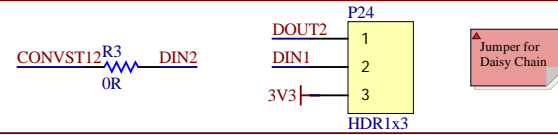
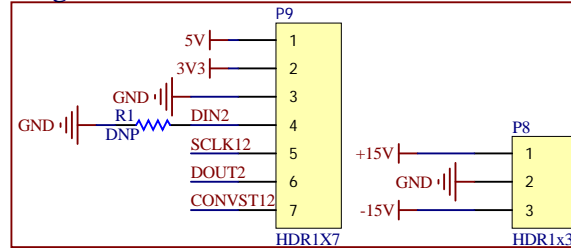
Processor Interface



Daughterboard Mounting



Daughterboard Connections



Eight daughterboards, divided into four pairs, each pair has two boards connected in daisy chain connection

Title: **Daughterboard Connections**

File: SensorCard_headers.SchDoc

Sheet: 5 of 5

Revision: C

Date: 4/13/2020

Time: 2:06:55 PM

Severson Group
WEMPEC
UW-Madison

Engineer: Ashad Farhan

