Differential Amplifier Design and Validation

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1. Introduction

Objective:

- Design and validate a differential amplifier, focusing on AC performance, stability, and layout implementation.

Approach:

- Utilized Synopsys Custom Compiler for schematic design, simulation, and layout implementation.

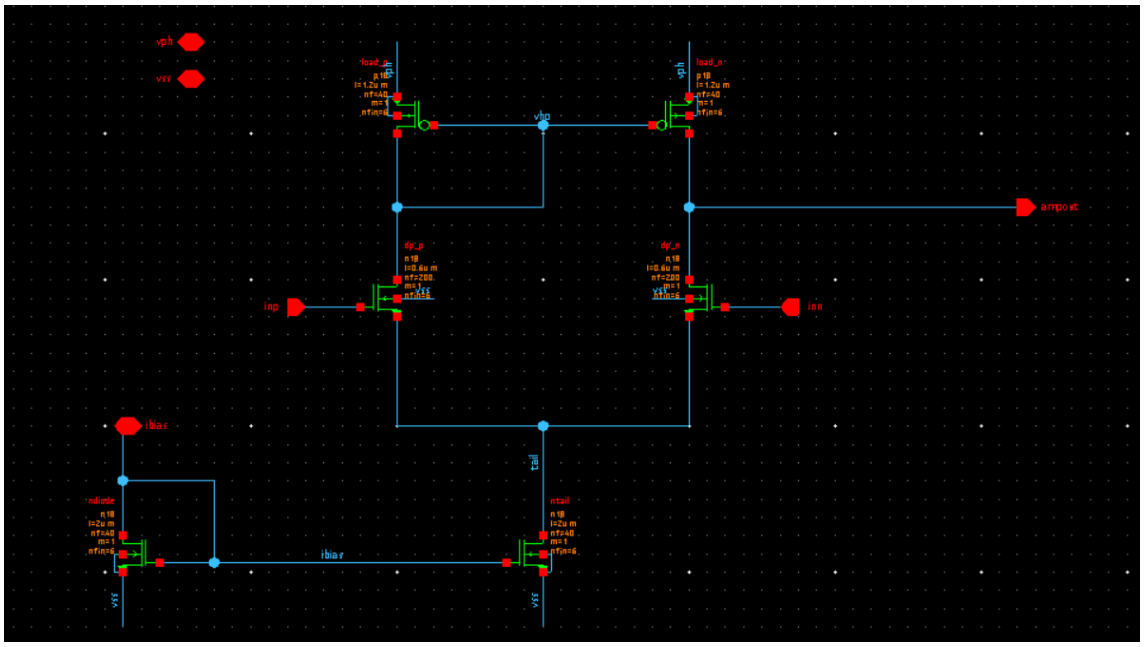

Figure 1 - Circuit of the Differential Amplifier.

2. Methodology

Design Process:

- Followed Synopsys' analog design flow, encompassing schematic creation, AC analysis, and layout verification.

Simulation Setup:

- Conducted simulations for DC gain, bandwidth, stability (LSTB), and PSRR using a 1.8V power supply at typical transistor models and 25°C.

Key Steps:

1. **Dimensioning**: Replaced the current source with a resistor to achieve I_{BIAS} = 100µA.
2. **Validation**: Simulated under various corners (temperature and voltage variations).
3. **Implementation**: Finalized with layout and design rule checks (DRC).

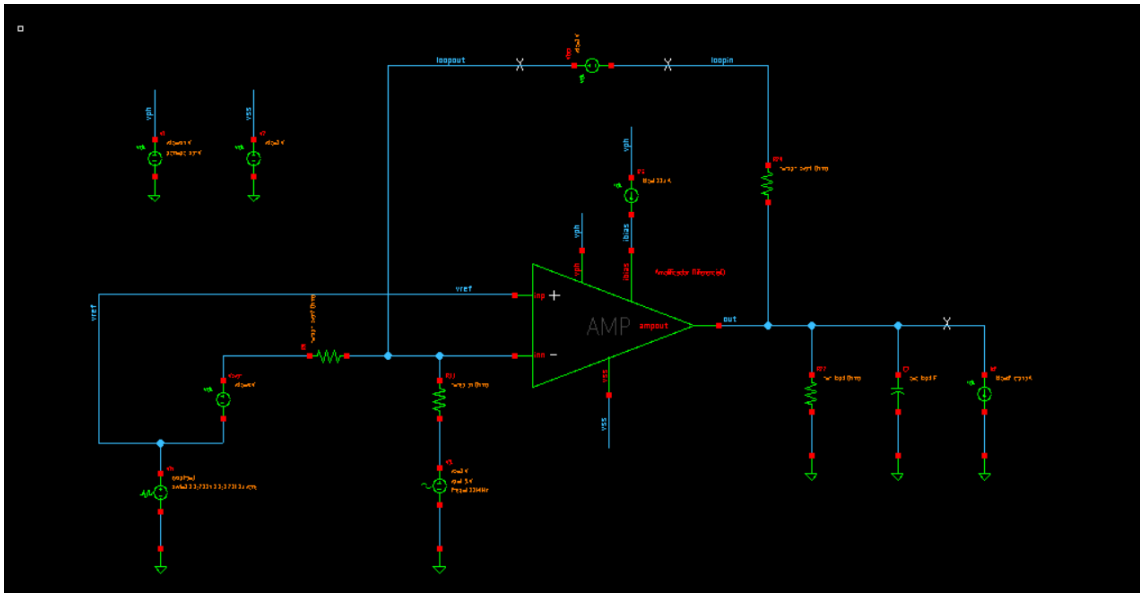

Figure 2 - Testbench Circuit.

3. Results

3.1 AC Analysis

- **DC Gain**: Achieved 51.3 dB.
- **Bandwidth (GBW)**: 171MHz.
- **Phase Margin**: 74.88°, indicating stability.

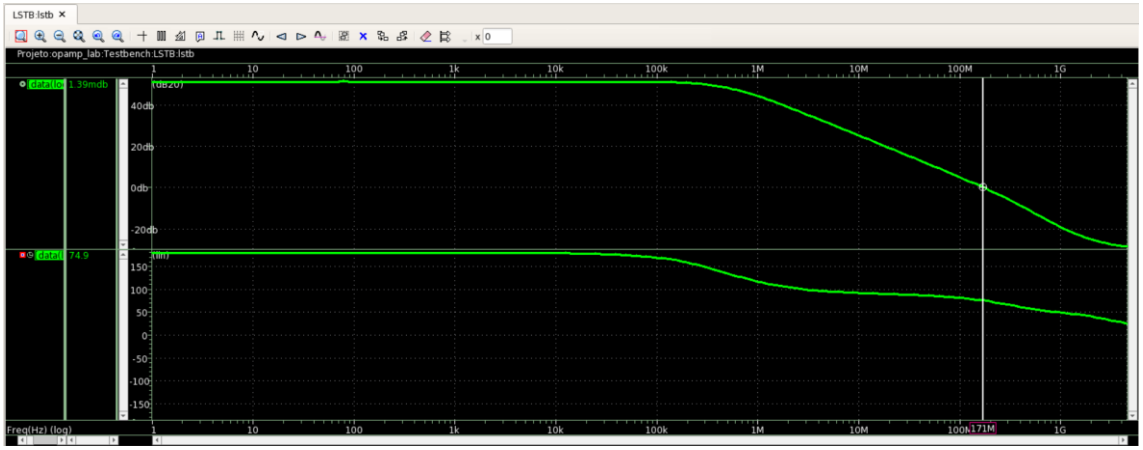

Figure 3 - Bode Diagram.

Tabela 1 - Phase Margin Values.

Phase Margin	Phase Margin Frequency
74.8753	170.840 MHz

3.2 PSRR Analysis

- Demonstrated effective suppression of power supply noise, especially at ~400MHz.

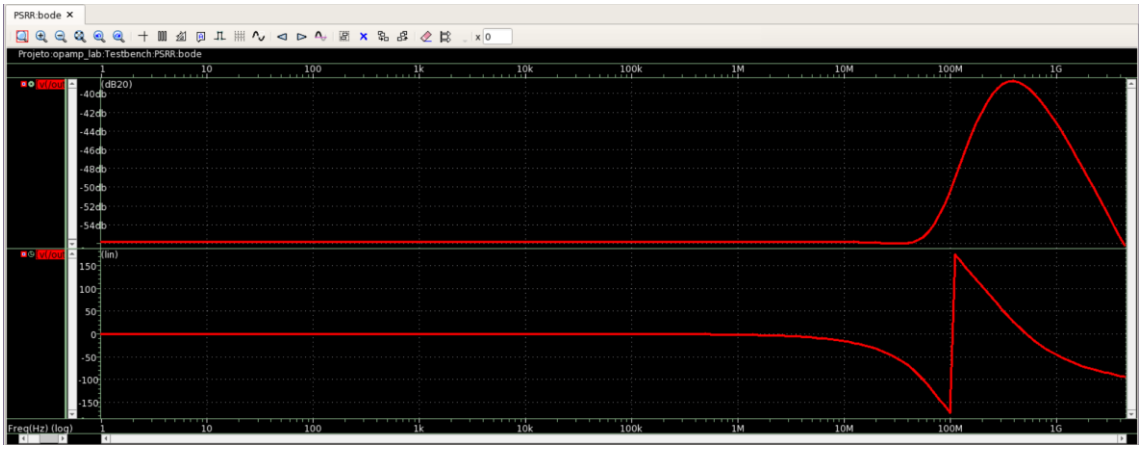

Figure 4 - PSRR Analysis.

3.3 Validation and Corners

- Evaluated across temperature variations (−40°C to 125°C) and process variations (FF, FS, SF, SS).
- Maintained consistent DC gain and bandwidth across scenarios.

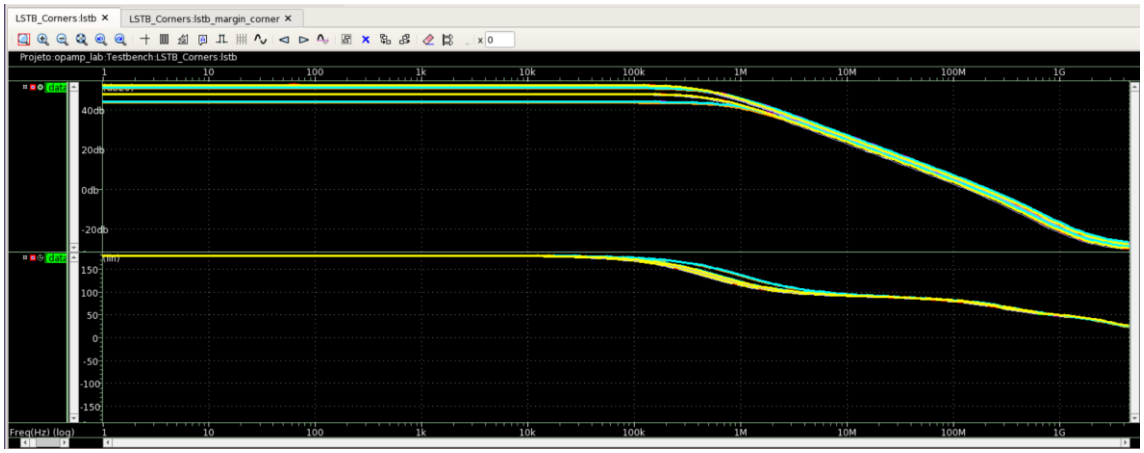

Figure 5 - Validation Results Under Multiple Corners.

3.4 Slew Rate and Overshoot

- **Slew Rate**: Achieved 94.8 V/µs, ensuring rapid response to input variations.
- **Overshoot**: Minimal at 3.79 mV, indicating stable performance.

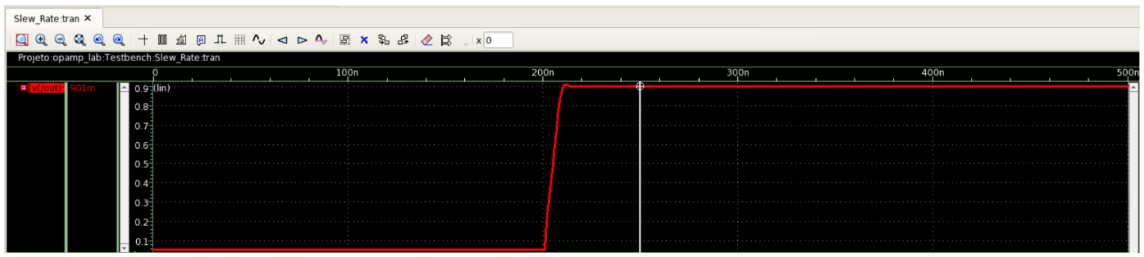

Figure 6 - Overshoot Measurement.

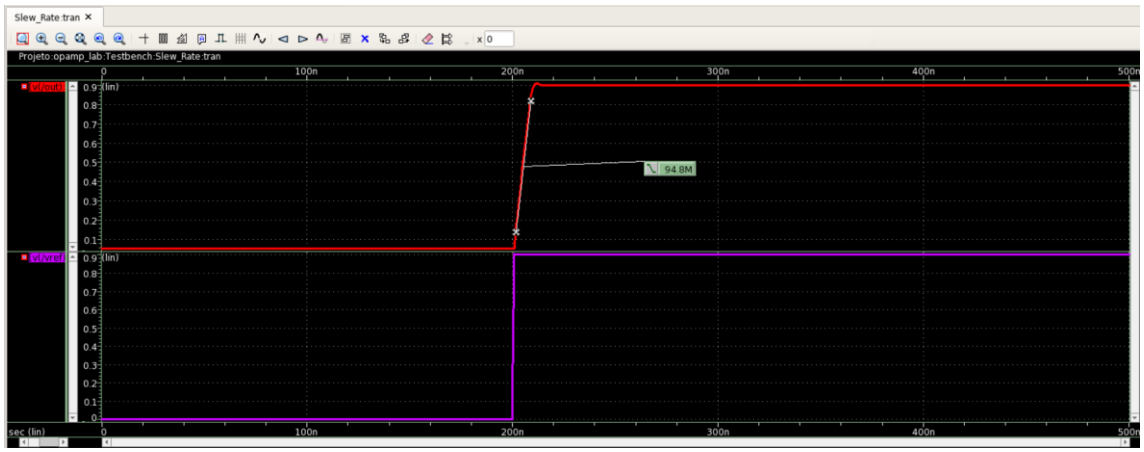

Figure 7 - Slew Rate Analysis.

3.5 Layout

- Achieved compact design with an area of 750.50 μm^2.
- Passed DRC with no violations.

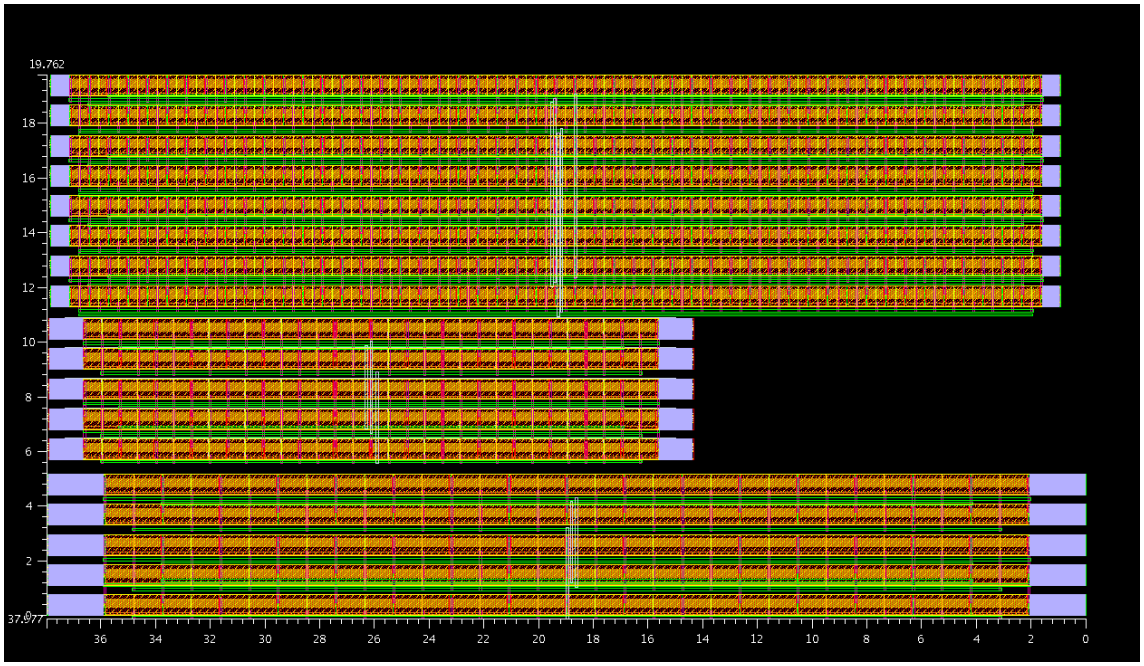

Figure 8 - Layout Representation.

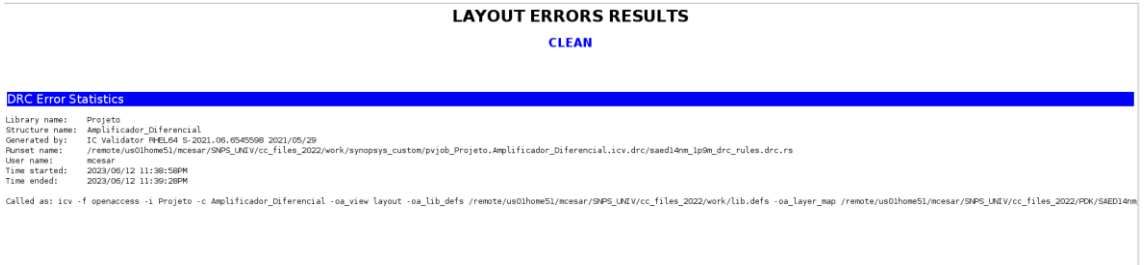

Figure 9 - DRC Verification.

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4. Conclusion

Summary:

- Successfully designed and validated a differential amplifier.
- Met target specifications for gain, stability, and noise rejection.