Step-Down DC-DC Converter Design and Simulation

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1. Introduction

Objective:

- Design and simulate a switched-capacitor DC-DC converter to generate three regulated output voltages:
  - $V_{out1} = \frac{VDD}{2}$
  - $V_{out2} = \frac{3VDD}{4}$
  - $V_{out3} = \frac{VDD}{4}$

Motivation:

- Evaluate efficiency, stability, and performance of step-down DC-DC converters under ideal and non-ideal conditions.

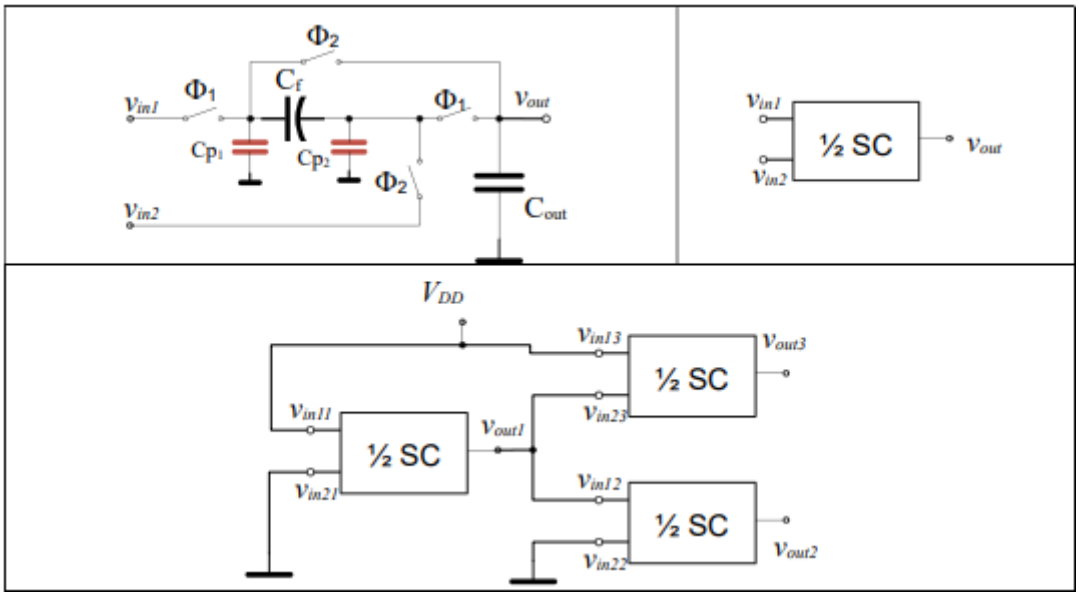

Figure 1 - Schematic of the SC DC-DC Converter.

2. Methodology

Circuit Analysis:

- Derived expressions for:
    - Output voltage V_{out} without and with parasitic capacitances.
    - Efficiency η\etaη as a function of input and output parameters.

Key Equations:

1. Output Voltage: $V_{out} = \frac{2C_{fly}F_{clk}R_{out}(V_{in1}+V_{in2})}{4C_{fly}F_{clk}R_{out}+1}$
2. Efficiency (Ideal): $\eta = \frac{V_{out}(2V_{in1}+2V_{in2}-4V_{out})}{(V_{in1}+V_{in2})(V_{in1}-2V_{out})}$

Simulation Setup:

- Simulated the circuits with:
    - $C_{fly} = 10nF$, $C_{out} = 500nF$, $R_{out} = 16\Omega$, $F_{clk} = 12MHz$.

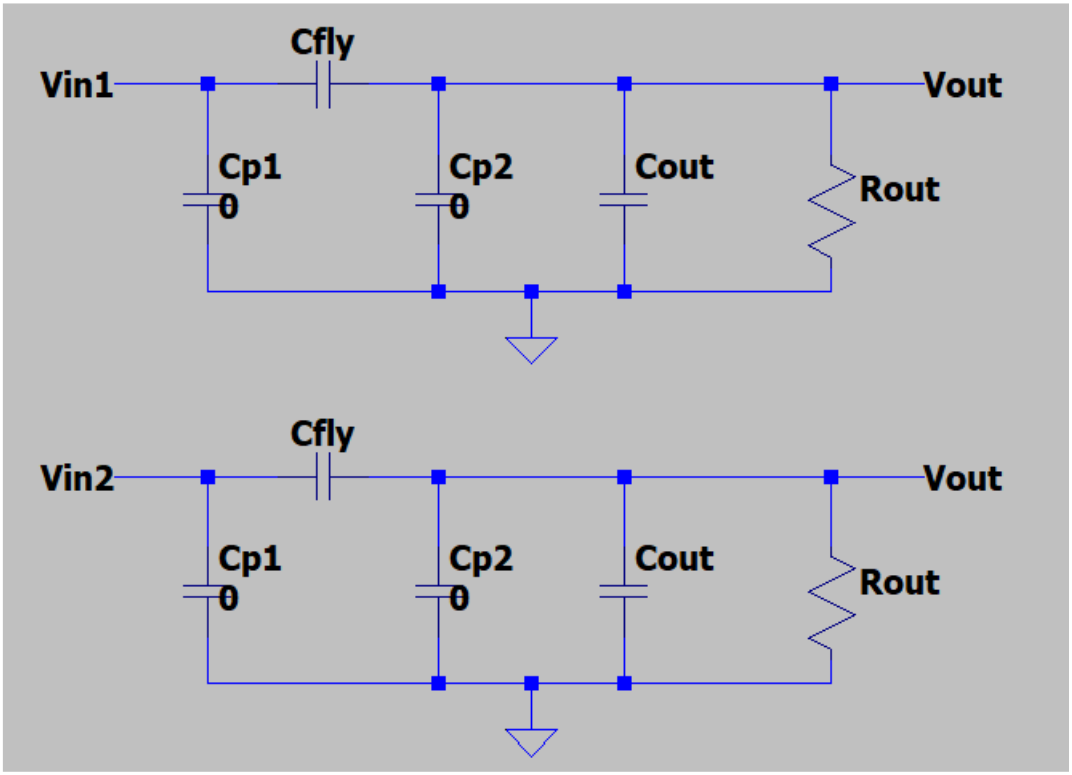

Figure 2 - Equivalent Schematic of Phase 1 (Top) and Phase 2 (Bottom) of the DC-DC converter.

3. Results

3.1 Ideal Simulations

- **Half-Bridge Converter (1/2):**
    - Output Voltage: $V_{out} \approx 493.5\ mV$;
    - Efficiency: $\eta = 85.22\%$.

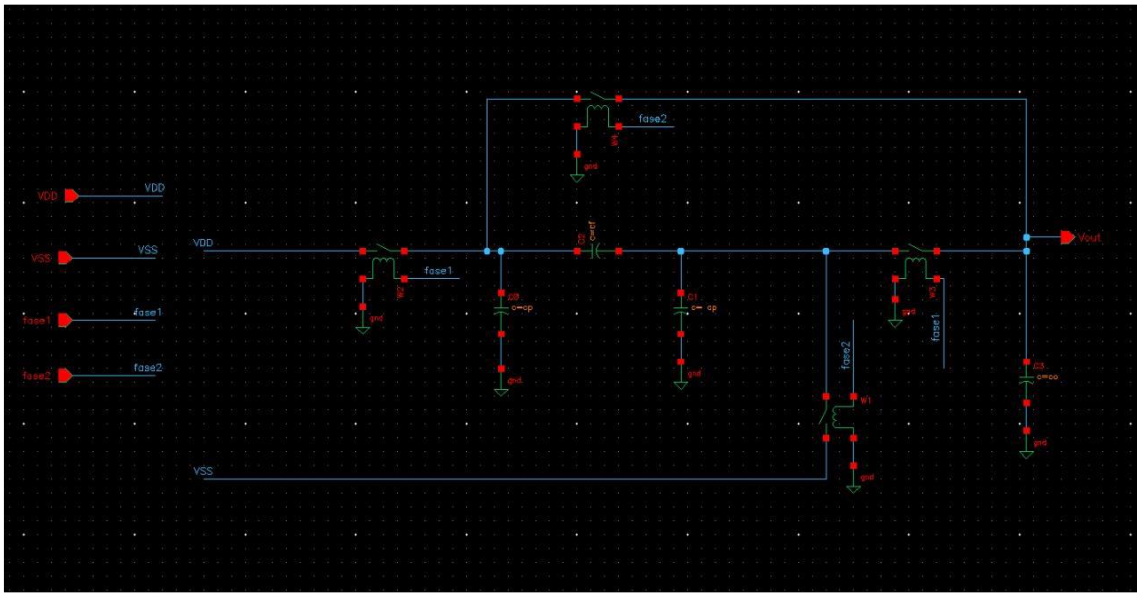

Figure 3 - Cadence Circuit of the 1/2 Converter.

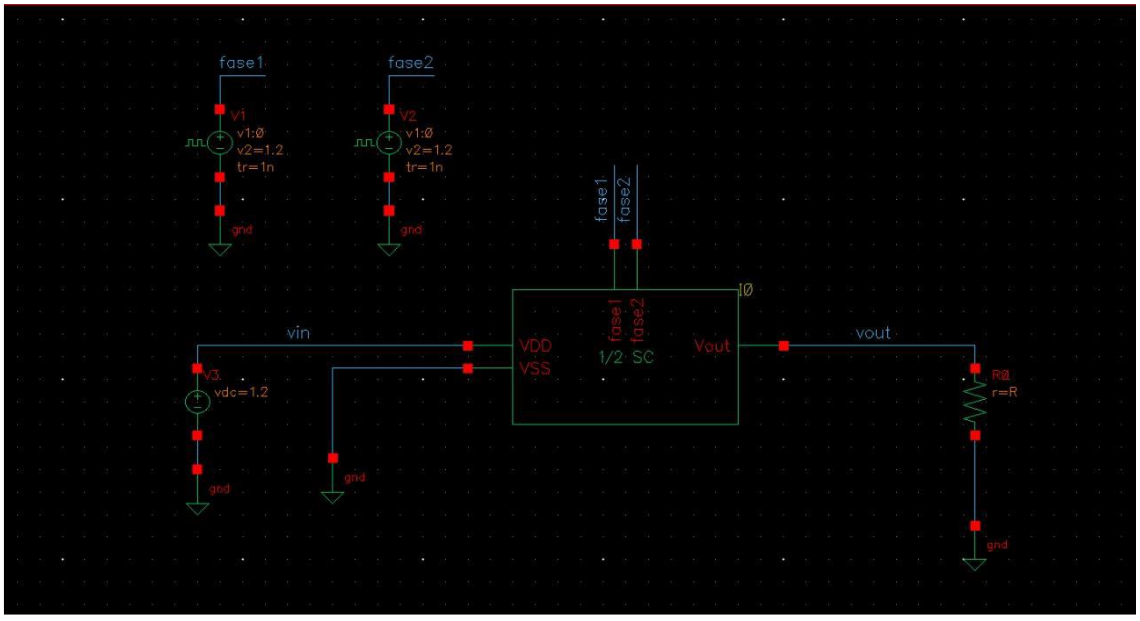

Figure 4 - Cadence Testebench Circuit of the 1/2 Converter.

- Output voltage remains stable across different loads.

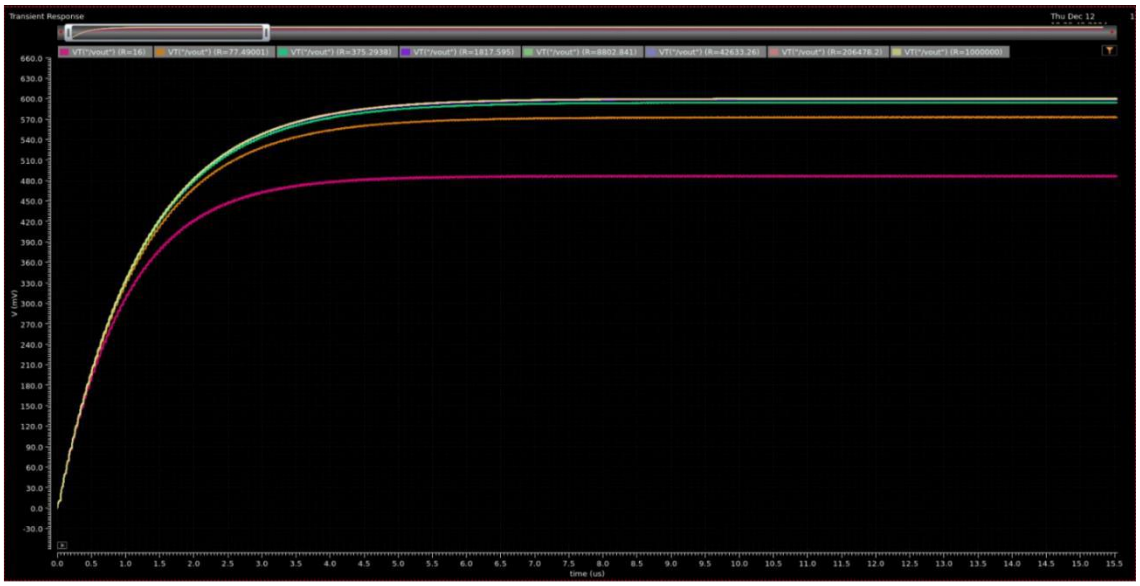

Figure 5 - Output Voltage Plot for Different Resistance Values for the 1/2 Converter.

3.2 Non-Ideal Simulations

- Analyzed the impact of parasitic capacitances:
    - Efficiency dropped to 60% when parasitic capacitances reached 10% of C_{fly}.
    - Significant power dissipation observed under non-ideal conditions.

Parameters: cp=6.51p			
1	lab_cia_1_2_SC_t...	Pin	-18.27m
1	lab_cia_1_2_SC_t...	Pout	14.75m
1	lab_cia_1_2_SC_t...	/V3/MINUS	
1	lab_cia_1_2_SC_t...	/R0/MINUS	
1	lab_cia_1_2_SC_t...	Rendimento	80.72
1	lab_cia_1_2_SC_t...	Vout	485.8m
Parameters: cp=65.1p			
2	lab_cia_1_2_SC_t...	Pin	-18.78m
2	lab_cia_1_2_SC_t...	Pout	14.76m
2	lab_cia_1_2_SC_t...	/V3/MINUS	
2	lab_cia_1_2_SC_t...	/R0/MINUS	
2	lab_cia_1_2_SC_t...	Rendimento	78.59
2	lab_cia_1_2_SC_t...	Vout	485.9m
Parameters: cp=651p			
3	lab_cia_1_2_SC_t...	Pin	-23.77m
3	lab_cia_1_2_SC_t...	Pout	14.8m
3	lab_cia_1_2_SC_t...	/V3/MINUS	
3	lab_cia_1_2_SC_t...	/R0/MINUS	
3	lab_cia_1_2_SC_t...	Rendimento	62.25
3	lab_cia_1_2_SC_t...	Vout	486.6m

Figure 6 - Simulation Results for Different Parasitic Capacitances.

3.3 Multi-Stage Converter (3/2):

- Generated three stable output voltages:
- $V_{out1} \approx 600\ mV$
- $V_{out2} \approx 300\ mV$
- $V_{out3} \approx 900\ mV$
- Efficiency slightly lower than the 1/2 converter due to increased circuit complexity.

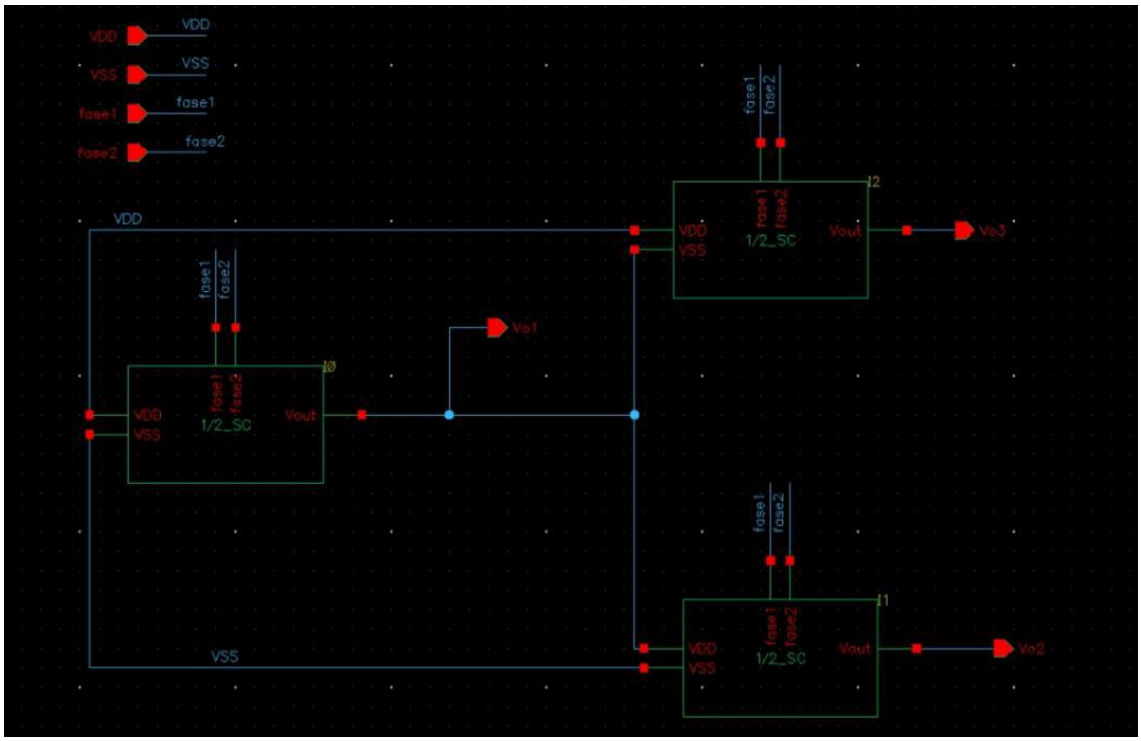

Figure 7 - Cadence Circuit of the 3/2 Converter.

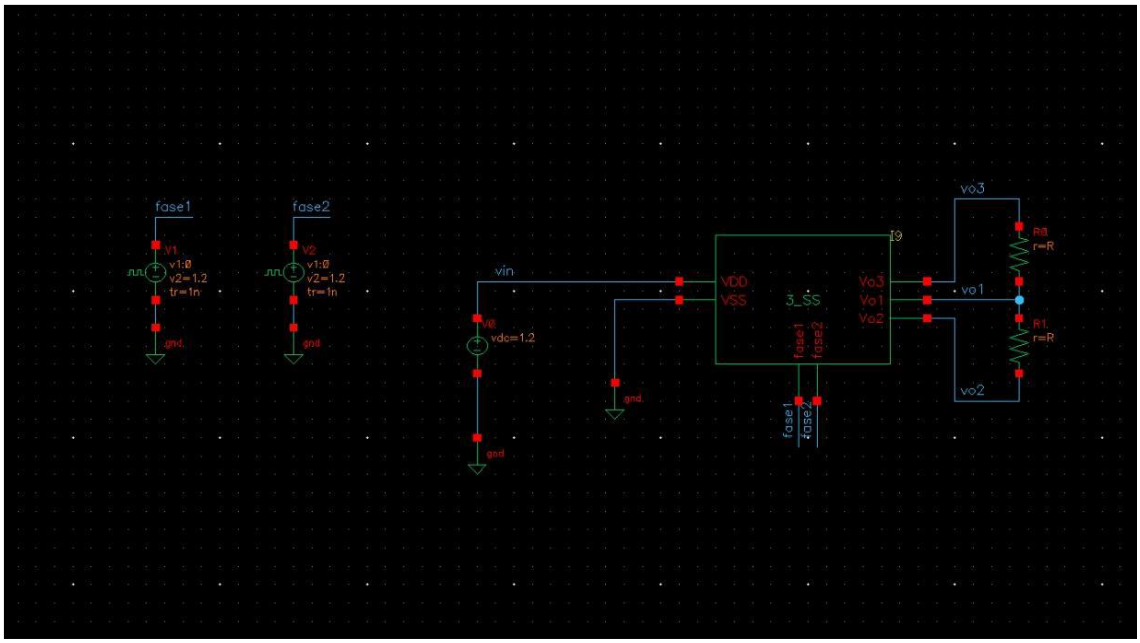

Figure 8 - Cadence Testebench Circuit of the 3/2 Converter.

Figure 9 - Output Voltage Stability Plot for 3/2 converter.

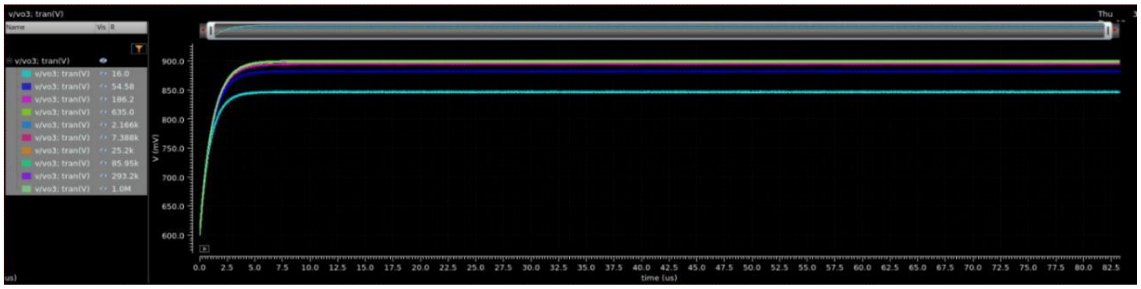

Figure 10 -Voltage Behavior of V_{out3} for Varying Load Resistances.

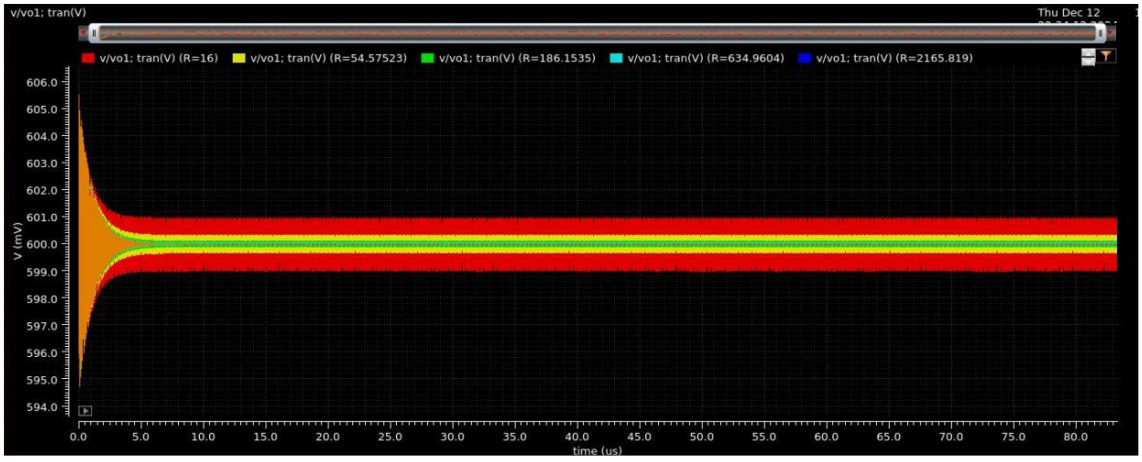

Figure 11 - Voltage Behavior of V_{out1} for Varying Load Resistances.

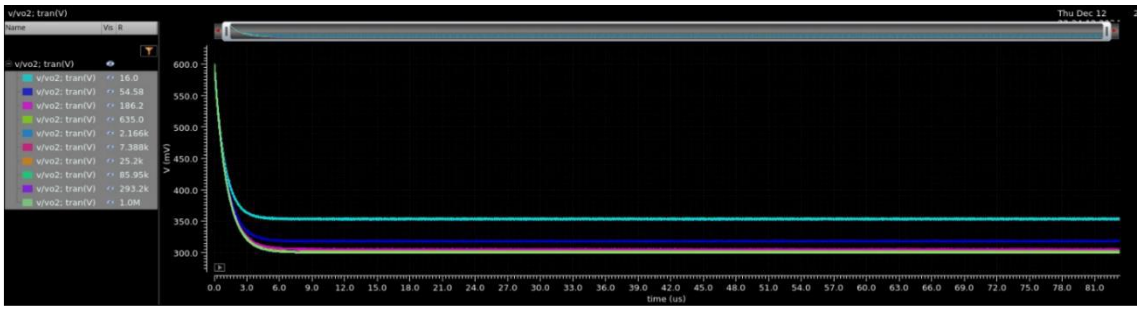

Figure 12 - Voltage Behavior of V_{out2} for Varying Load Resistances.

4. Discussion

- **Ideal Conditions**:
  - High efficiency (>85%) achieved under low load currents and ideal parameters.
  - Demonstrated stable output regulation across a range of load resistances.
- **Non-Ideal Conditions**:
  - Efficiency heavily impacted by parasitic capacitances (>40% drop at 10% C_{fly}).
  - Highlights the importance of minimizing parasitic effects in practical implementations.

Parameters: cp=6.51p			
1	lab_cia_SC_3_ou...	Pin	-9.334m
1	lab_cia_SC_3_ou...	v/vo1; tran(V)	
1	lab_cia_SC_3_ou...	v/vo2; tran(V)	
1	lab_cia_SC_3_ou...	v/vo3; tran(V)	
1	lab_cia_SC_3_ou...	vo1	600m
1	lab_cia_SC_3_ou...	vo2	353.8m
1	lab_cia_SC_3_ou...	vo3	846.2m
1	lab_cia_SC_3_ou...	Rendimento	81.18
1	lab_cia_SC_3_ou...	po1	3.789m
1	lab_cia_SC_3_ou...	po2	3.788m
1	lab_cia_SC_3_ou...	/vin	
Parameters: cp=65.1p			
2	lab_cia_SC_3_ou...	Pin	-10.05m
2	lab_cia_SC_3_ou...	v/vo1; tran(V)	
2	lab_cia_SC_3_ou...	v/vo2; tran(V)	
2	lab_cia_SC_3_ou...	v/vo3; tran(V)	
2	lab_cia_SC_3_ou...	vo1	600m
2	lab_cia_SC_3_ou...	vo2	353.6m
2	lab_cia_SC_3_ou...	vo3	846.4m
2	lab_cia_SC_3_ou...	Rendimento	75.51
2	lab_cia_SC_3_ou...	po1	3.796m
2	lab_cia_SC_3_ou...	po2	3.795m
2	lab_cia_SC_3_ou...	/vin	
Parameters: cp=651p			
3	lab_cia_SC_3_ou...	Pin	-17.71m
3	lab_cia_SC_3_ou...	v/vo1; tran(V)	
3	lab_cia_SC_3_ou...	v/vo2; tran(V)	
3	lab_cia_SC_3_ou...	v/vo3; tran(V)	
3	lab_cia_SC_3_ou...	vo1	600m
3	lab_cia_SC_3_ou...	vo2	351.9m
3	lab_cia_SC_3_ou...	vo3	848.1m
3	lab_cia_SC_3_ou...	Rendimento	43.46
3	lab_cia_SC_3_ou...	po1	3.848m
3	lab_cia_SC_3_ou...	po2	3.848m
3	lab_cia_SC_3_ou...	/vin	

Figure 13 - Power Dissipation and Efficiency Impact Under Parasitic Capacitance.

5. Conclusion

Summary:

- Successfully designed and simulated a step-down DC-DC converter with high efficiency under ideal conditions.
- Identified significant performance degradation due to parasitic capacitances, emphasizing the need for careful circuit optimization.

Takeaways:

- Reinforces the importance of balancing design trade-offs in switched-capacitor DC-DC converters for practical applications.
- Highlights the scalability of the multi-stage conFiguretion to achieve higher output voltages.