Class AB CMOS Amplifier Design

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1. Introduction

Objective:

- Design and analyze a Class AB CMOS audio amplifier capable of:
    - Driving a 16Ω load with a 1.2V power supply.
    - Achieving >54dB gain at 20kHz.
    - Maintaining a phase margin >55° for stability.
    - Limiting input noise to <100μVrms between 20Hz and 40kHz.

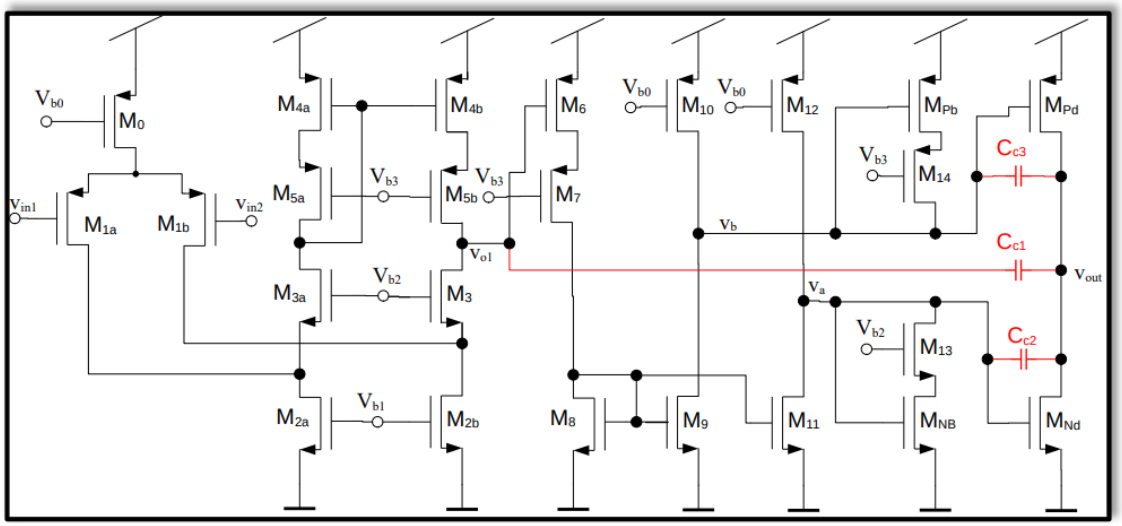

Figure 1 - Class AB Amplifier Circuit.

Approach:

- A combination of circuit modeling, transistor sizing, and simulation was used to meet design specifications while minimizing power consumption and area.

2. Circuit Design and Analysis

- **Circuit Simplification**:
    - Nested Miller Compensation was applied to simplify the AC model and facilitate pole-zero analysis.

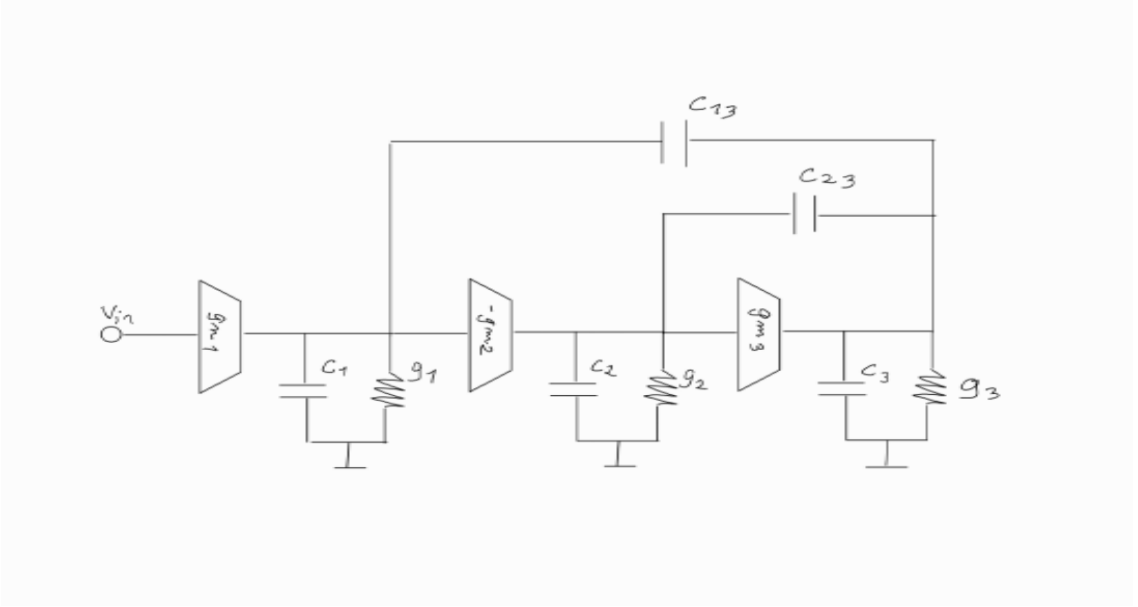

Figure 2 - Simplified Circuit with Nested Miller Compensation.

- **Key Design Parameters:**
    - DC Gain: ~59 dB (theoretical), ~28 dB (simulated).
    - Dominant Pole (P1): 10 kHz (simulated), 20 kHz (theoretical).
    - Phase Margin: Approximately 55°, ensuring stability.
    - Noise Performance: Input noise compliant in medium frequencies, with significant flicker noise observed at low frequencies.

3. Methodology

Transistor Sizing:

- Transistors were dimensioned to balance gain, bandwidth, and noise performance:
    - Example M_1 and M_0 (L_n = 120 nm, gm/Id = 29.3).
- Sizing decisions informed by plots of pole and gain behavior.

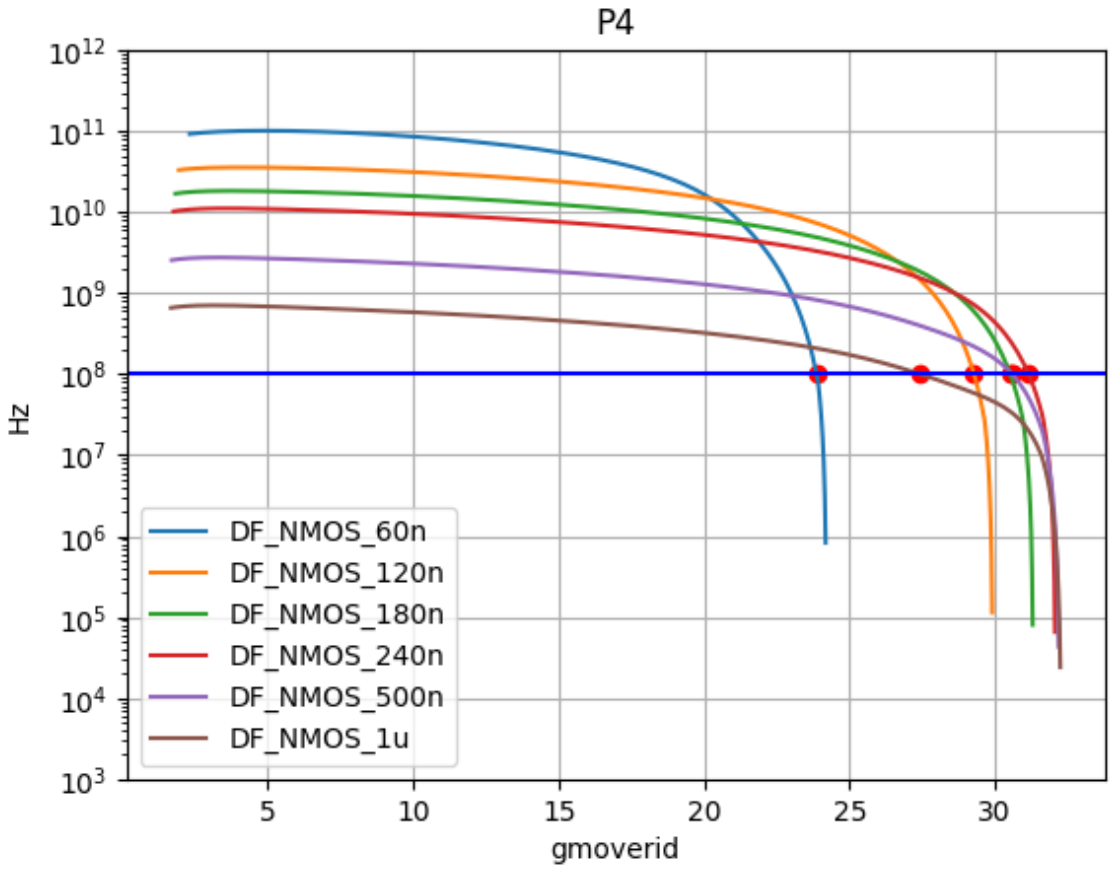

Figure 3 - Pole Frequency Behaviour Plot.

Symbolic Analysis:

- Used Python's SymPy library to derive and validate transfer functions.
- Key equations for poles and zeros simplified for dominant contributions.

4. Simulations and Results

Key Simulation Results:

1. **DC Operating Point:**
    - Verified correct transistor operation, VDSAT values below expected thresholds, indicating potential redesign for optimized operation.

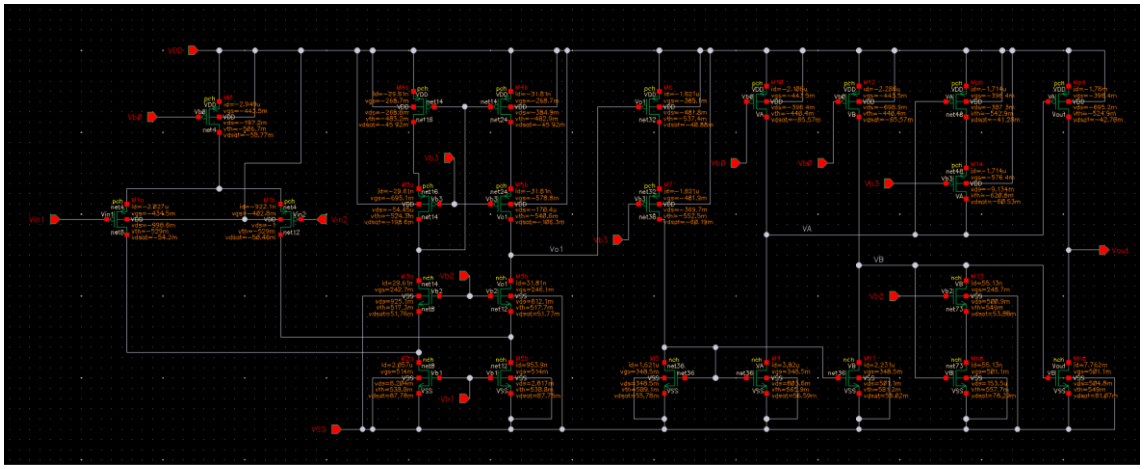

Figure 4 - Operating Point Simulation of the Class AB Amplifier.

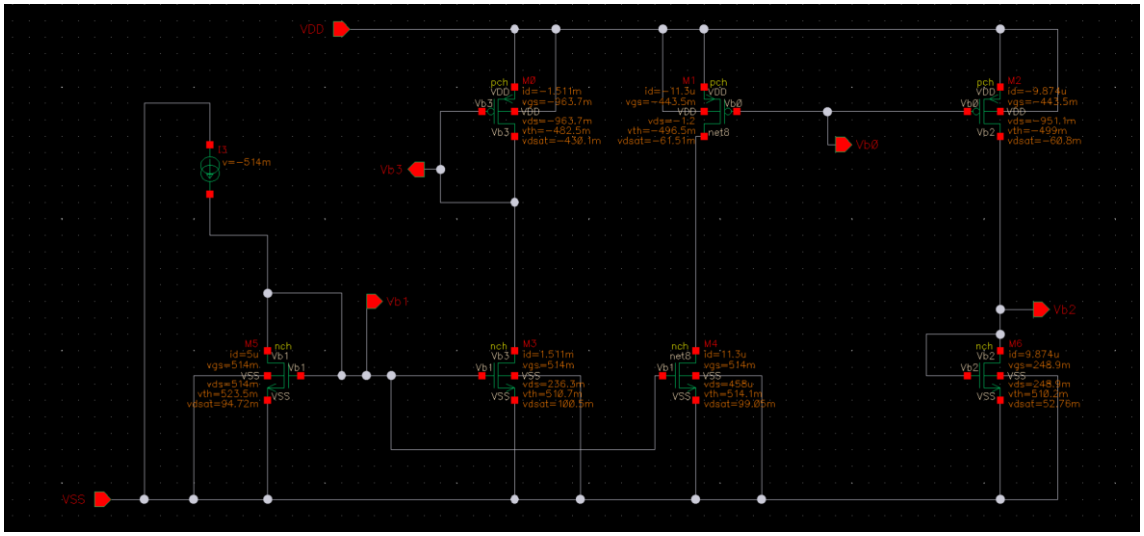

Figure 5 - Operating Point Simulation of the BIAS Circuit.

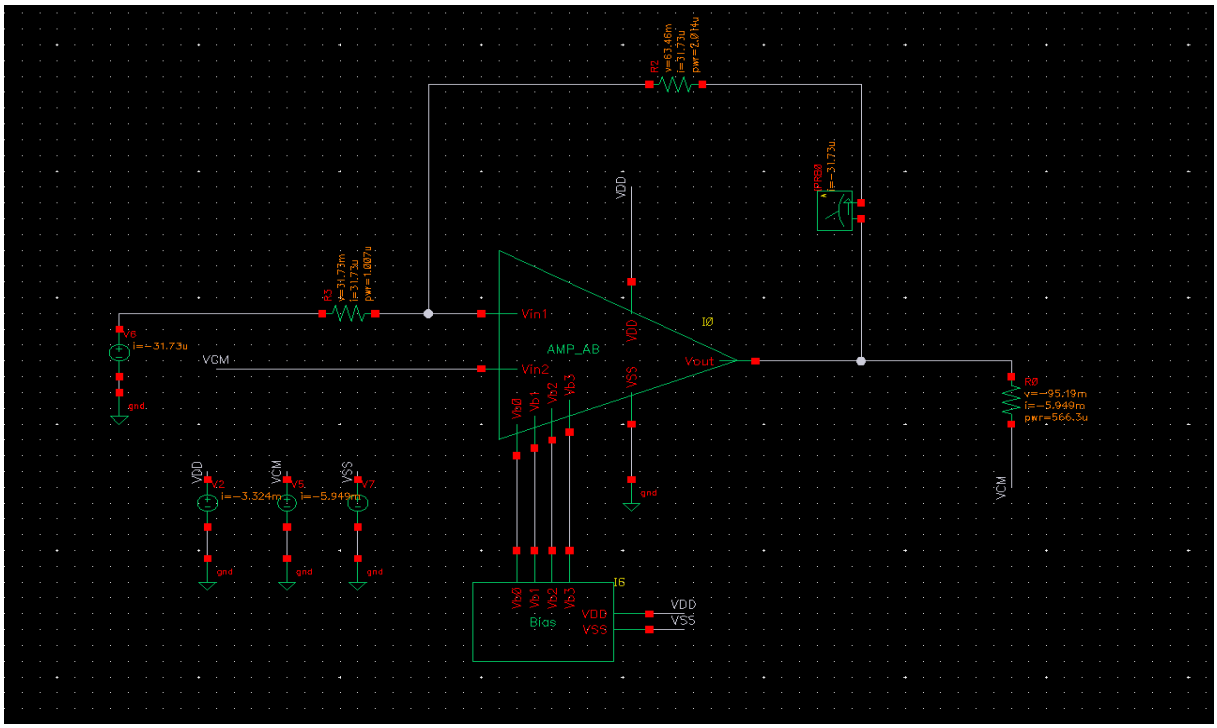

Figure 6 - Operating Point Simulation of the Testbench Circuit.

2. **Gain and Phase Stability**:

   - **Simulated Gain**: ~28 dB.
   - **Phase Margin**: Approximately 10°, very distant value from the required specification.

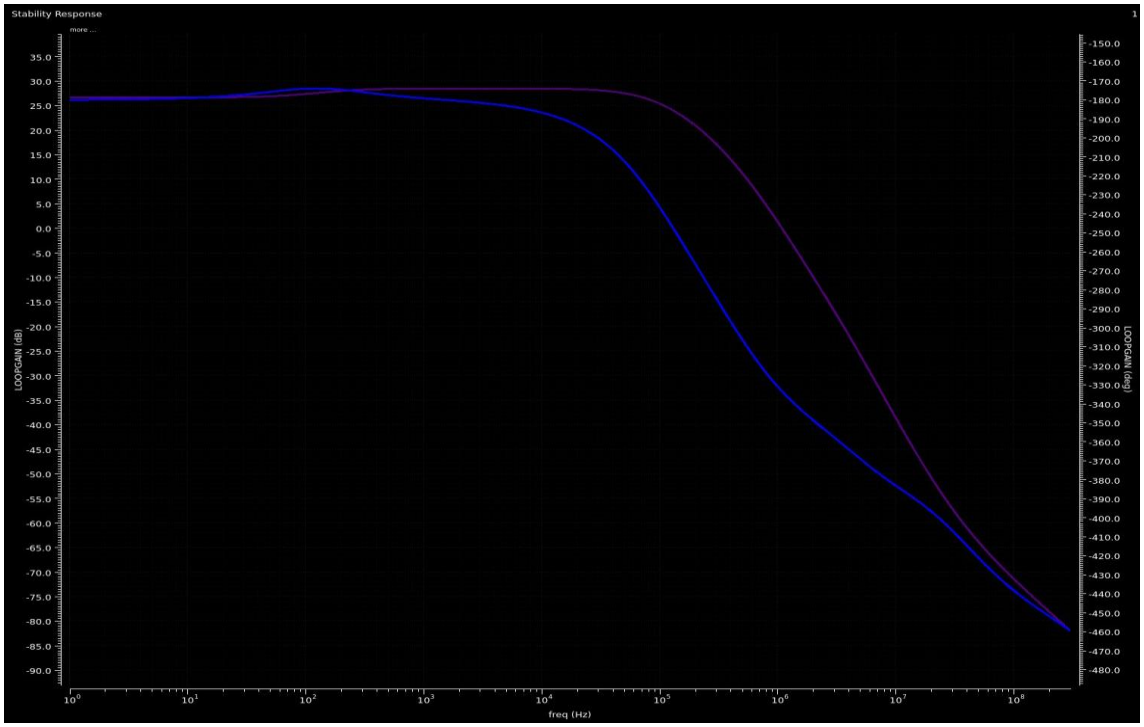

Figure 7 - Closed Loop Simulation Plot.

3. **Noise Analysis**:

    - Input noise within acceptable limits in medium frequencies.
    - Flicker noise prominent at low frequencies; suggested mitigation via additional filtering.

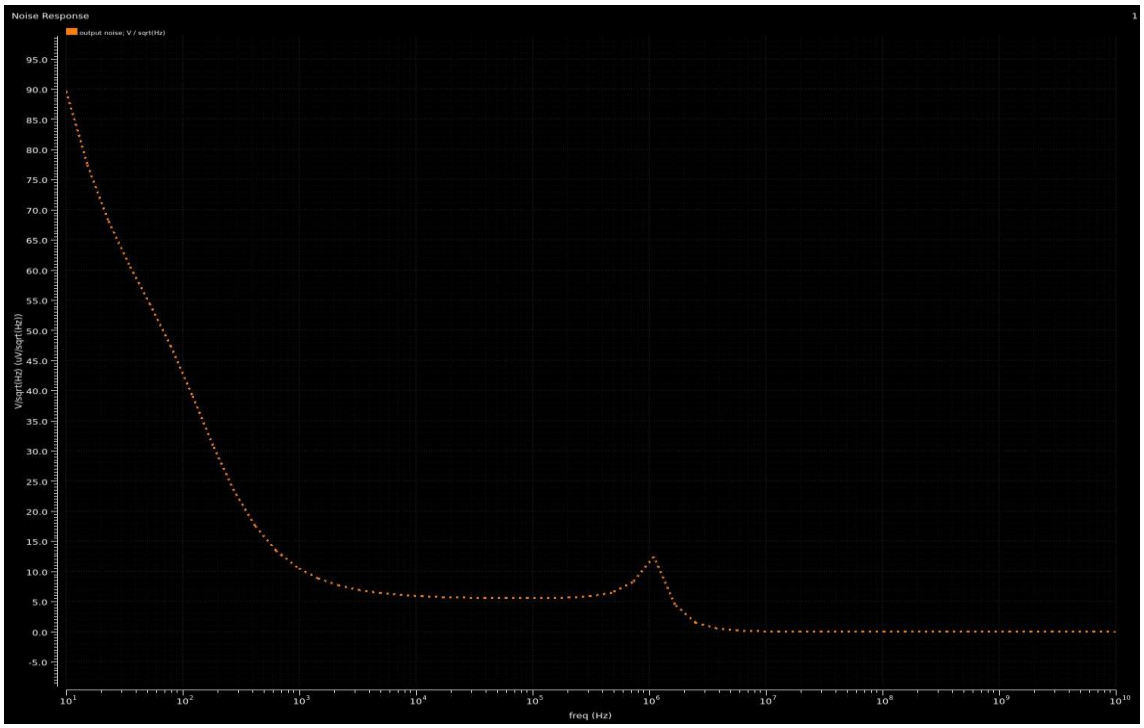

Figure 8 – Input Referred Noise Simulation Plot.

4. **Power Supply Rejection Ratio (PSRR)**:

    - Strong performance at low frequencies; drop-off at higher frequencies.

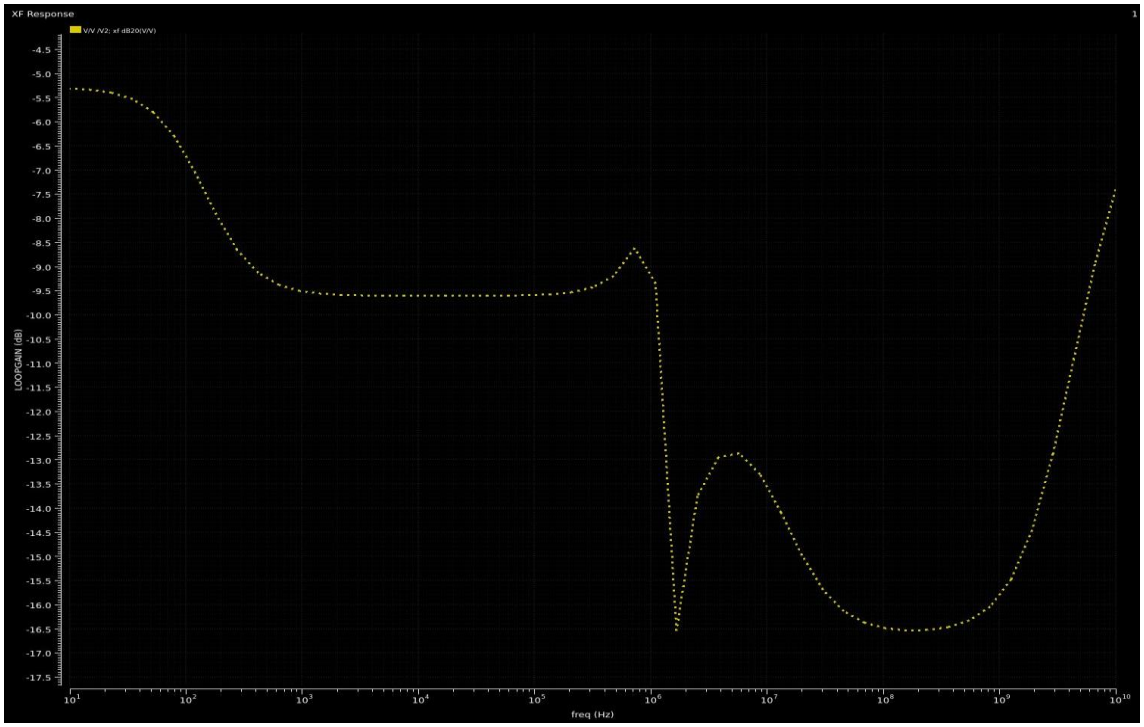

Figure 9 - PSSR Simulation Plot.

5. **Time-Domain Analysis**:

    - Stable output with minimal distortion under a 400mV input signal.

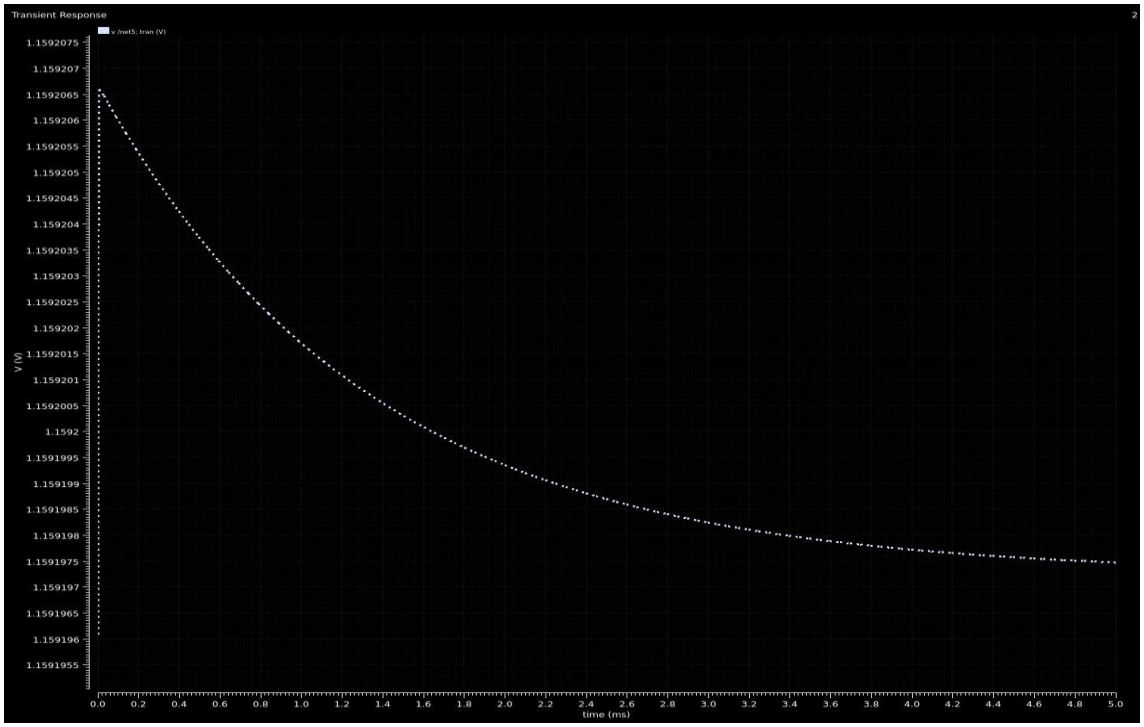

Figure 10 - Time Domain Operation Plot of the Closed Loop Circuit.

5. Conclusion

Strengths:

- Stable, low-distortion output for a 400 mV input signal.
- Noise compliance in medium frequencies.

Areas for Improvement:

- **Gain**: ~28 dB(below the required >54 dB).
- **Phase Margin**: ~10° (below the required >55°), indicating instability. Compensation design must be revised.
- **Flicker Noise**: Significant at low frequencies, requiring mitigation strategies.
- **PSRR**: Performance drops at high frequencies and needs optimization.
- **Transistor Sizing**: Biasing conditions and V_{DSAT} should be re-evaluated for improved operation.