Low Noise Amplifier Design and Analysis

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1. Introduction

Objective:

- The project aimed to design and analyze Low Noise Amplifiers (LNAs) optimized for high-frequency telecommunications applications. Two distinct technologies were explored:
    - BJT-based LNAs for focused performance on narrowband systems.
    - CMOS-based LNAs for scalable designs in advanced semiconductor technologies.

Motivation:

- LNAs are critical in RF systems to amplify weak antenna signals while minimizing noise contributions. Effective impedance matching and stability are essential for optimal performance.

Approach:

- BJT LNA designs were analyzed and simulated using LTSpice.
- CMOS LNAs were evaluated across three technology nodes: 350nm, 130nm, and 45nm. Simulations for the 130nm technology were conducted using Cadence Spectre and the 350nm and 45nm technology through LTSpice, focusing on gain, noise figure (NF), and impedance matching.

2. Methodology

Simulation Details for CMOS 130nm:

- Simulated with Cadence Spectre, focusing on two scaling conFiguretions:
    - L_{min} with n=1.
    - L_{min} with n=2.25.
- Design adjustments included iterative optimization of:
    - Transistor dimensions (W/L).
    - Bias voltages and impedance networks.

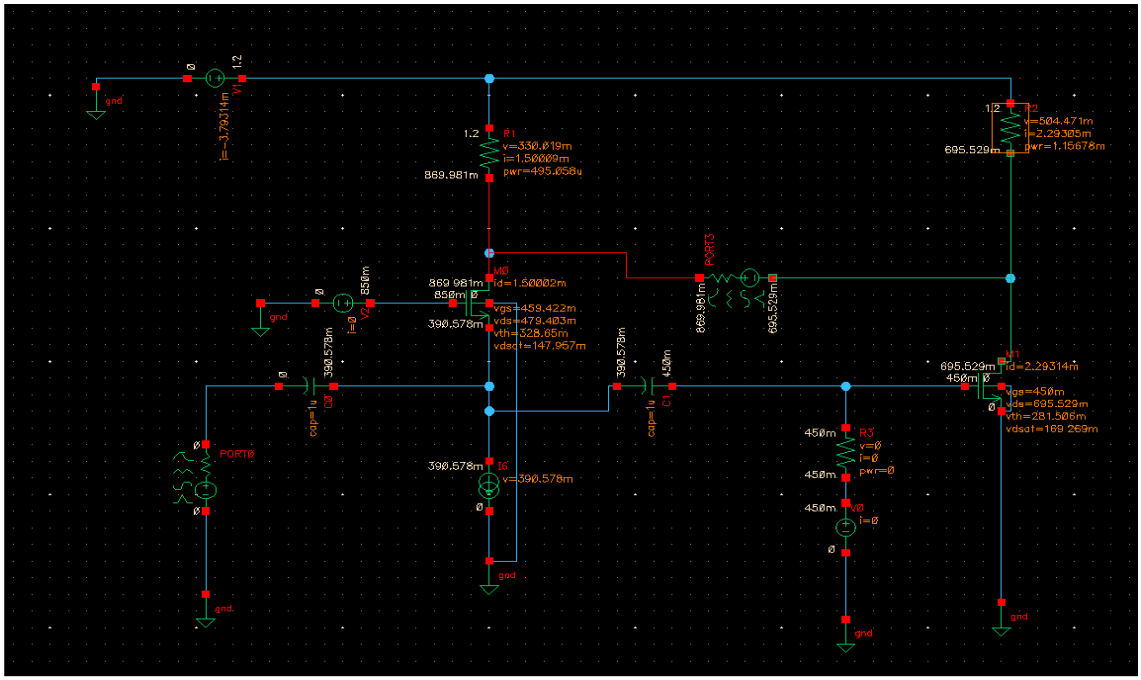

Figure 1 - Cadence LNA Circuit for 130nm Technology.

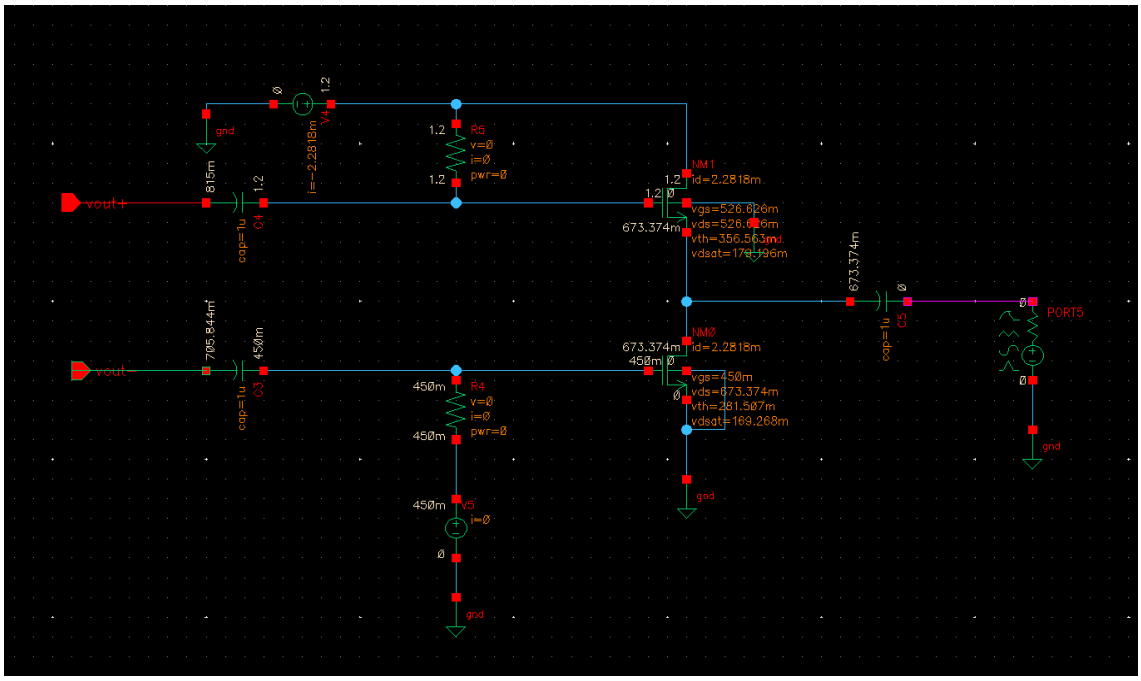

Figure 2 - Cadence Circuit for Buffer.

- **Performance metrics:**
  - Noise figure (NF).
  - Gain (S_{21}).
  - Impedance matching (Z_{in}, Z_{out}).

3. Results

Performance Metrics (130nm CMOS):

Key Observations:

- Increasing the scaling factor (n=2.25) reduced the noise figure but decreased the gain and bandwidth.
- Simulations in Cadence validated the feasibility of achieving stable operation and effective impedance matching.

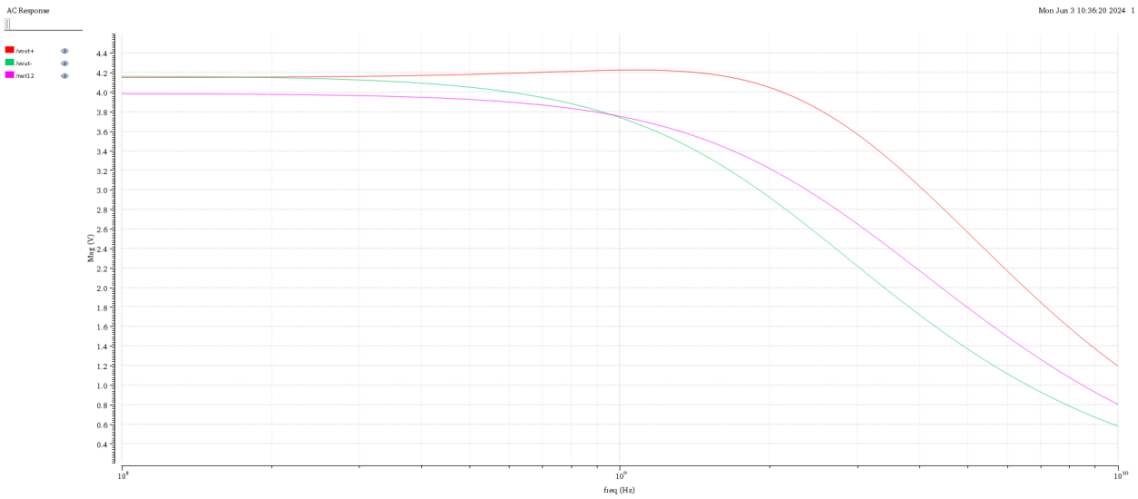

Figure 3 - Simulated Gain.

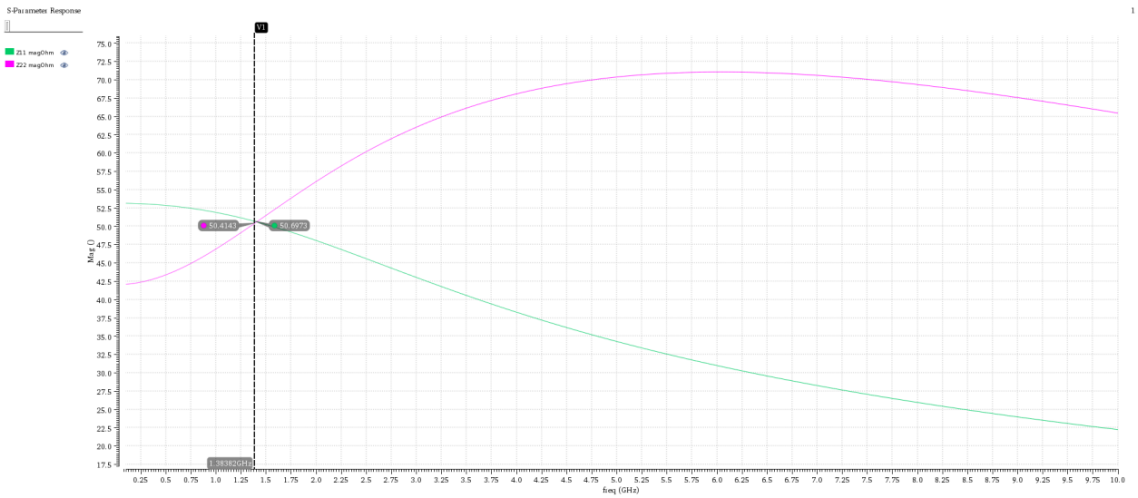

Figure 4 - Simulated Impedance Matching.

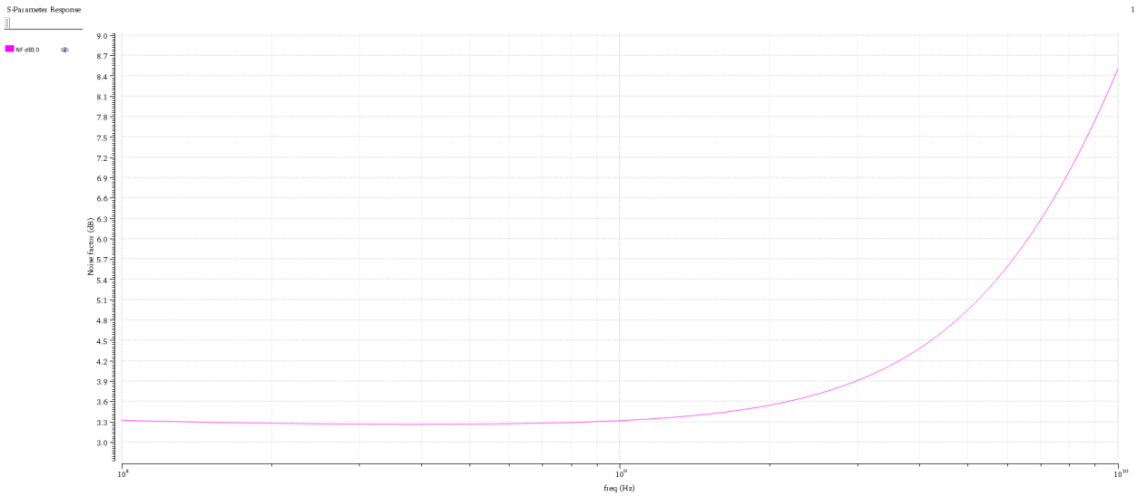

Figure 5 - Simulated Noise Figure.

4. Discussion

The following table summarizes the results across the evaluated technologies:

Technology (nm)	Gain (S_{21}) (dB)	Noise Figure (dB)	Bandwidth (GHz)	Comments
350	11.4	3.8	0.8	Limited RF capabilities
130 (n=1)	11.82	3.1	2.5	Best trade-off overall
130 (n=2.25)	12.04	2.3	2	Optimized for noise reduction
45	7.66	6.2	10	Challenging to implement

Insights:

- The **130nm node** provided the best balance of gain and noise figure, making it ideal for high-frequency applications.
- Parasitic effects and noise contributions from buffer stages required careful design adjustments, particularly in the 130nm and 45nm nodes.
- While the 45nm node offered potential for higher bandwidth, its implementation complexity limited its applicability.

5. Conclusion

This project explored the design and simulation of LNAs using both BJT and CMOS technologies for RF applications. CMOS designs across multiple technology nodes were analyzed, revealing the trade-offs between performance metrics like gain, NF, and bandwidth.

Key Takeaways:

- The 130nm CMOS node was identified as the optimal choice for balanced performance, providing high gain and low NF with manageable design complexity.
- Scaling factors (nnn) significantly impacted noise performance but required compromises in gain and bandwidth.
- Effective simulation tools like Cadence Spectre were critical for validating designs and analyzing trade-offs.