Folded-Cascode Amplifier Design and Optimization

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1. Introduction

Objective:

- Design and simulate a folded-cascode OTA in 130nm CMOS technology, optimizing key performance metrics like DC gain, GBW, and area.

Motivation:

- Folded-cascode OTAs are essential in high-speed, low-power applications such as switched-capacitor circuits.

Specifications:

- **DC Gain**: >66dB;
- **GBW**: >100MHz;
- **Second Pole Frequency**: >200MHz;
- **Third Pole Frequency**: >1GHz;
- **Power Dissipation**: <0.15mW;
- **Area**: Minimized for cost-effective design.

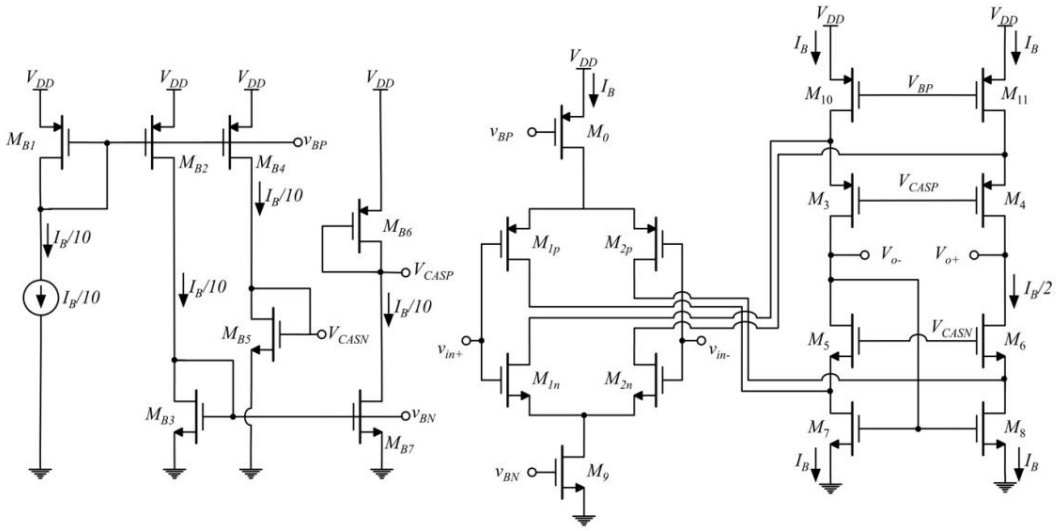

Figure 1 - Schematic of the Folded-Cascode OTA Circuit.

2. Methodology

Design Process:

1. Used Mathcad for dimensioning transistors to achieve optimal trade-offs.
2. Simulated the circuit in Cadence Spectre for electrical validation and iterative refinement.
3. Focused on balancing transistor lengths (L) and V_{DSAT} to meet noise, gain, and bandwidth targets.

Simulation Setup:

- Conducted simulations for DC operating point, gain, bandwidth, and phase performance.
- Validated noise and power metrics.

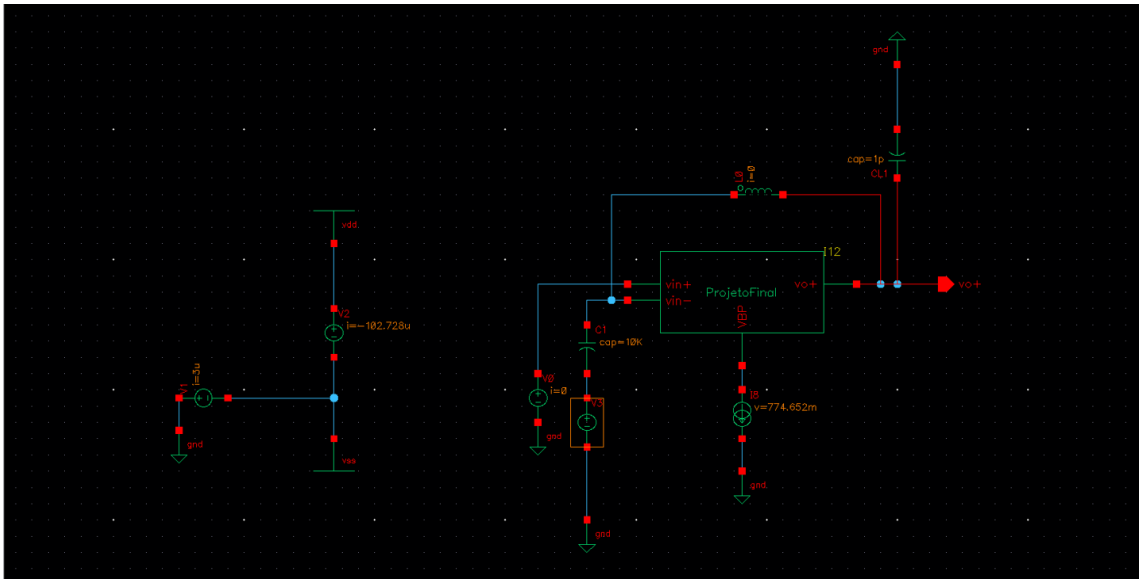

Figure 2 - Cadence Testbench Setup.

3. Results

3.1 Key Simulated Metrics

- **DC Gain**: 66.9dB;
- **GBW**: 115MHz;
- **Second Pole Frequency**: 488.2MHz;
- **Third Pole Frequency**: 1.08GHz;
- **Power Dissipation**: 0.12mW;
- **Area**: 187.05μm^2;
- **FoM**: 940.2.

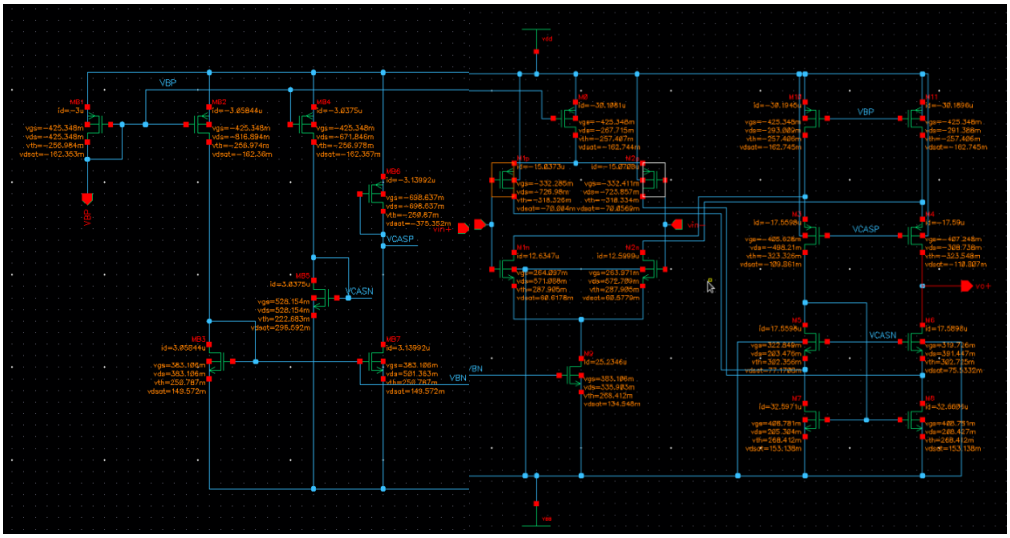

Figure 3 - DC Simulation Results (PFR Analysis).

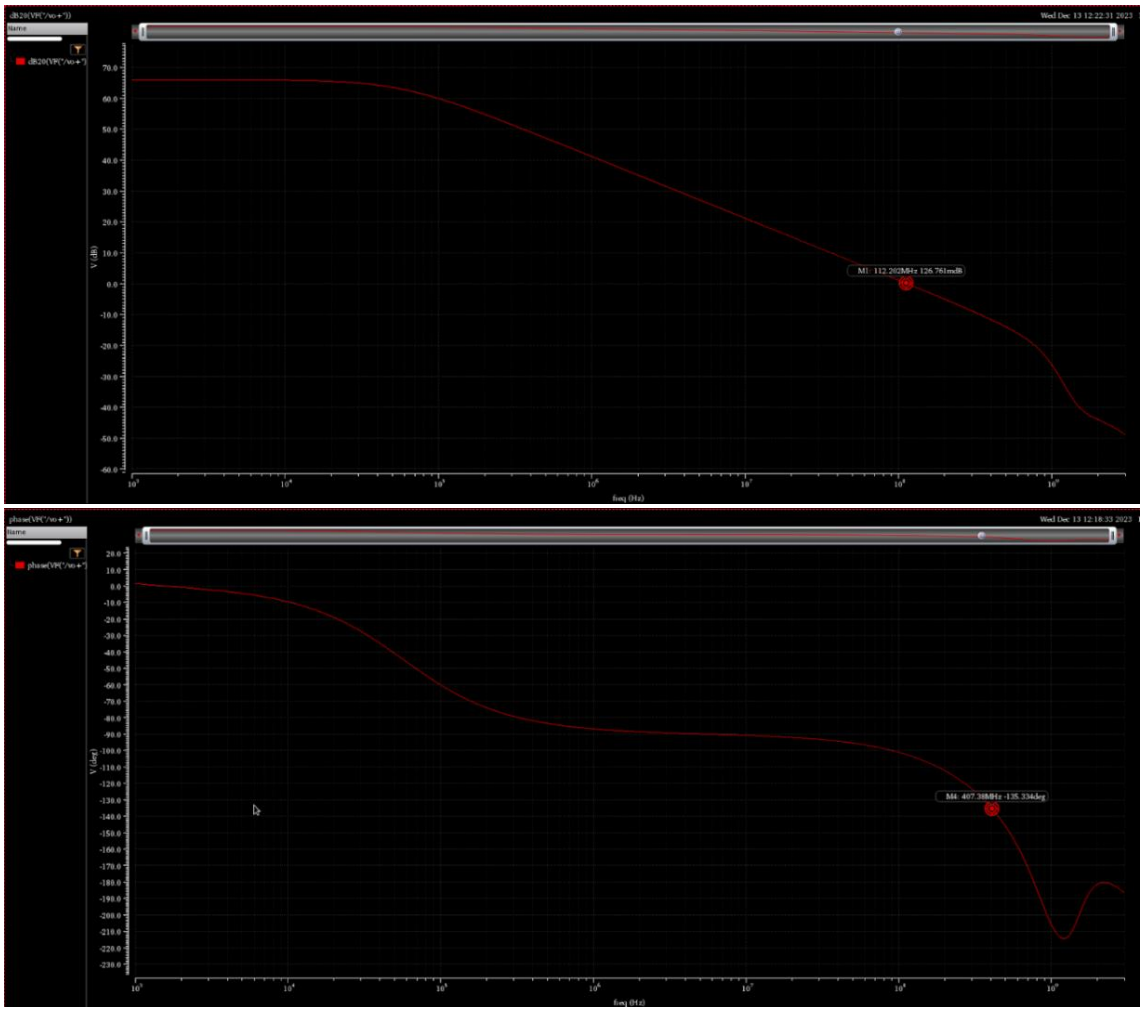

Figure 4 – Simulated Bode Plot.

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4. Discussion

Key Observations:

- Simulation results closely matched theoretical expectations, validating the design methodology.
- Minor discrepancies in noise and gain were attributed to transistor modeling assumptions.

Comparison with Previous Designs:

- +4dB improvement in DC Gain compared to prior lab designs.
- +882% improvement in GBW.
- −40% reduction in area.

Trade-offs:

- Optimizing GBW required adjustments to VDSATV_{DSAT}VDSAT, affecting power efficiency.

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5. Conclusion

Summary:

- The project successfully met objectives for DC gain, GBW, and area, showcasing the efficiency of the design approach.
- Demonstrated the importance of iterative optimization in analog circuit design.

Takeaways:

- Highlights the value of simulation tools like Mathcad and Cadence for achieving real-world performance targets.