Appendix B Internal I/O Register

B.1A Addresses (H8S/2633 Group, H8S/2633F, H8S/2633R)

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FDAC	DADR2									D/A2, D/A3	8
H'FDAD	DADR3										
H'FDAE	DACR23	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FDB0	IrCR	IrE	IrCKS2	IrCKS1	IrCKS0	—	—	—	—	SCI0, IrDA	8
H'FDB4	SCRX	—	IICX1	IICX0	IICE	FLSHE	—	—	—	IIC	8
H'FDB5	DDCSWR	—	—	—	—	CLR3	CLR2	CLR1	CLR0	IIC	8
H'FDB8	DADRAH0/ DACR0	DA13/ TEST	DA12/ PWME	DA11/ —	DA10/ —	DA9/ OEB	DA8/ OEA	DA7/ OS	DA6/ CKS	PWM0	8
H'FDB9	DADRAL0	DA5	DA4	DA3	DA2	DA1	DA0	CFS	—		
H'FDBA	DADRBH0/ DACNTH0	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6		
H'FDBB	DADRBL0/ DACNTL0	DA5	DA4	DA3	DA2	DA1	DA0	CFS	REGS		
H'FDBC	DADRAH1/ DACR1	DA13/ TEST	DA12/ PWME	DA11/ —	DA10/ —	DA9/ OEB	DA8/ OEA	DA7/ OS	DA6/ CKS	PWM1	8
H'FDBD	DADRAL1	DA5	DA4	DA3	DA2	DA1	DA0	CFS	—		
H'FDBE	DADRBH1/ DACNTH1	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6		
H'FDBF	DADRBL1/ DACNTL1	DA5	DA4	DA3	DA2	DA1	DA0	CFS	REGS		
H'FDC0	TCR2	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR2, TMR3	16
H'FDC1	TCR3	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0		
H'FDC2	TCSR2	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0		
H'FDC3	TCSR3	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0		
H'FDC4	TCORA2										
H'FDC5	TCORA3										
H'FDC6	TCORB2										
H'FDC7	TCORB3										
H'FDC8	TCNT2										
H'FDC9	TCNT3										
H'FDD0	SMR3	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI3, Smart card interface	8
	SMR3	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0		
H'FDD1	BRR3										
H'FDD2	SCR3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FDD3	TDR3										

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FDD4	SSR3	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	SCI3, Smart card interface	8
	SSR3	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT		
H'FDD5	RDR3										
H'FDD6	SCMR3	—	—	—	—	SDIR	SINV	—	SMIF		
H'FDD8	SMR4	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI4, Smart card interface	8
	SMR4	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0		
H'FDD9	BRR4										
H'FDDA	SCR4	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FDDB	TDR4										
H'FDDC	SSR4	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT		
	SSR4	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT		
H'FDDD	RDR4										
H'FDDE	SCMR4	—	—	—	—	SDIR	SINV	—	SMIF		
H'FDE4	SBYCR	SSBY	STS2	SYS1	STS0	OPE	—	—	—	System	8
H'FDE5	SYSCR	MACS	—	INTM1	INTM0	NMIEG	MRESE	—	RAME		
H'FDE6	SCKCR	PSTOP	—	—	—	STCS	SCK2	SCK1	SCK0		
H'FDE7	MDCR	—	—	—	—	—	MDS2	MDS1	MDS0		
H'FDE8	MSTPCRA	MSTPA7	MSTPA6	MSTPA5	MSTPA4	MSTPA3	MSTPA2	MSTPA1	MSTPA0		
H'FDE9	MSTPCRB	MSTPB7	MSTPB6	MSTPB5	MSTPB4	MSTPB3	MSTPB2	MSTPB1	MSTPB0		
H'FDEA	MSTPCRC	MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0		
H'FDEB	PFCR	CSS07	CSS36	BUZZE	LCASS	AE3	AE2	AE1	AE0		
H'FDEC	LPWRCR	DTON	LSON	NESEL	SUBSTP	RFCUT	—	STC1	STC0		
H'FE00	BARA	—	—	—	—	—	—	—	—	PBC	8
H'FE01		BAA23	BAA22	BAA21	BAA20	BAA19	BAA18	BAA17	BAA16		
H'FE02		BAA15	BAA14	BAA13	BAA12	BAA11	BAA10	BAA9	BAA8		
H'FE03		BAA7	BAA6	BAA5	BAA4	BAA3	BAA2	BAA1	BAA0		
H'FE04	BARB	—	—	—	—	—	—	—	—		
H'FE05		BAA23	BAA22	BAA21	BAA20	BAA19	BAA18	BAA17	BAA16		
H'FE06		BAA15	BAA14	BAA13	BAA12	BAA11	BAA10	BAA9	BAA8		
H'FE07		BAA7	BAA6	BAA5	BAA4	BAA3	BAA2	BAA1	BAA0		
H'FE08	BCRA	CMFA	CDA	BAMRA2	BAMRA1	BAMRA0	CSELA1	CSELA0	BIEA		
H'FE09	BCRB	CMFB	CDB	BAMRB2	BAMRB1	BAMRB0	CSELB1	CSELB0	BIEB		
H'FE12	ISCRH	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA	Interrupt controller	8
H'FE13	ISCRL	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA		
H'FE14	IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E		
H'FE15	ISR	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FE16	DTCERA	DTCEA7	DTCEA6	DTCEA5	DTCEA4	DTCEA3	DTCEA2	DTCEA1	DTCEA0	DTC	8
H'FE17	DTCERB	DTCEB7	DTCEB6	DTCEB5	DTCEB4	DTCEB3	DTCEB2	DTCEB1	DTCEB0		
H'FE18	DTCERC	DTCEC7	DTCEC6	DTCEC5	DTCEC4	DTCEC3	DTCEC2	DTCEC1	DTCEC0		
H'FE19	DTCERD	DTCED7	DTCED6	DTCED5	DTCED4	DTCED3	DTCED2	DTCED1	DTCED0		
H'FE1A	DTCERE	DTCEE7	DTCEE6	DTCEE5	DTCEE4	DTCEE3	DTCEE2	DTCEE1	DTCEE0		
H'FE1B	DTCERF	DTCEF7	DTCEF6	DTCEF5	DTCEF4	DTCEF3	DTCEF2	DTCEF1	DTCEF0		
H'FE1E	DTCERI	DTCEI7	DTCEI6	DTCEI5	DTCEI4	DTCEI3	DTCEI2	DTCEI1	DTCEI0		
H'FE1F	DTVECR	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0		
H'FE26	PCR	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0	PPG	8
H'FE27	PMR	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV		
H'FE28	NDERH	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8		
H'FE29	NDERL	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0		
H'FE2A	PODRH	POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8		
H'FE2B	PODRL	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0		
H'FE2C	NDRH	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8		
H'FE2D	NDRL	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0		
H'FE2E	NDRH	—	—	—	—	NDR11	NDR10	NDR9	NDR8		
H'FE2F	NDRL	—	—	—	—	NDR3	NDR2	NDR1	NDR0		
H'FE30	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	Port	8
H'FE32	P3DDR	P37DDR	P36DDR	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FE36	P7DDR	P77DDR	P76DDR	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR		
H'FE39	PADDR	—	—	—	—	PA3DDR	PA2DDR	PA1DDR	PA0DDR		
H'FE3A	PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR		
H'FE3B	PCDDR	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR		
H'FE3C	PDDDR	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR		
H'FE3D	PEDDR	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR		
H'FE3E	PFDDR	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR		
H'FE3F	PGDDR	—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR		
H'FE40	PAPCR	—	—	—	—	PA3PCR	PA2PCR	PA1PCR	PA0PCR		
H'FE41	PBPCR	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR		
H'FE42	PCPCR	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR		
H'FE43	PDPCR	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR		
H'FE44	PEPCR	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR		
H'FE46	P3ODR	P37ODR	P36ODR	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR		
H'FE47	PAODR	—	—	—	—	PA3ODR	PA2ODR	PA1ODR	PA0ODR		
H'FE48	PBODR	PB7ODR	PB6ODR	PB5ODR	PB4ODR	PB3ODR	PB2ODR	PB1ODR	PB0ODR		
H'FE49	PCODR	PC7ODR	PC6ODR	PC5ODR	PC4ODR	PC3ODR	PC2ODR	PC1ODR	PC0ODR		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FE80	TCR3	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU3	16
H'FE81	TMDR3	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FE82	TIOR3H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE83	TIOR3L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FE84	TIER3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FE85	TSR3	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FE86	TCNT3										
H'FE87											
H'FE88	TGR3A										
H'FE89											
H'FE8A	TGR3B										
H'FE8B											
H'FE8C	TGR3C										
H'FE8D											
H'FE8E	TGR3D										
H'FE8F											
H'FE90	TCR4	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU4	16
H'FE91	TMDR4	—	—	—	—	MD3	MD2	MD1	MD0		
H'FE92	TIOR4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE94	TIER4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FE95	TSR4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FE96	TCNT4										
H'FE97											
H'FE98	TGR4A										
H'FE99											
H'FE9A	TGR4B										
H'FE9B											
H'FEA0	TCR5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU5	16
H'FEA1	TMDR5	—	—	—	—	MD3	MD2	MD1	MD0		
H'FEA2	TIOR5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FEA4	TIER5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FEA5	TSR5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FEA6	TCNT5										
H'FEA7											
H'FEA8	TGR5A										
H'FEA9											
H'FEAA	TGR5B										
H'FEAB											

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FEB0	TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU	16
H'FEB1	TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0		
H'FEC0	IPRA	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	Interrupt controller	8
H'FEC1	IPRB	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC2	IPRC	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC3	IPRD	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC4	IPRE	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC5	IPRF	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC6	IPRG	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC7	IPRH	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC8	IPRI	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC9	IPRJ	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECA	IPRK	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECB	IPRL	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECE	IPRO	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FED0	ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	Bus controller	8
H'FED1	ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0		
H'FED2	WCRH	W71	W70	W61	W60	W51	W50	W41	W40		
H'FED3	WCRL	W31	W30	W21	W20	W11	W10	W01	W00		
H'FED4	BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMST0		
H'FED5	BCRL	BRLE	BREQOE	—	OES	DDS	RCTS	WDBE	WAITE		
H'FED6	MCR	TPC	BE	RCDM	CW2	MXC1	MXC0	RLW1	RLW0		
H'FED7	DRAMCR	RFSHE	CBRM	RMODE	CMF	CMIE	CKS2	CKS1	CKS0		
H'FED8	RTCNT										
H'FED9	RTCOR										
H'FEDB	RAMER	—	—	—	—	RAMS	RAM2	RAM1	RAM0	FLASH	8
H'FEE0	MAR0AH	—	—	—	—	—	—	—	—	DMAC	16
H'FEE1											
H'FEE2	MAR0AL										
H'FEE3											
H'FEE4	IOAR0A										
H'FEE5											
H'FEE6	ETCR0A										
H'FEE7											
H'FEE8	MAR0BH	—	—	—	—	—	—	—	—		
H'FEE9											
H'FEEA	MAR0BL										
H'FEEB											

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FEEC	IOAR0B									DMAC	16
H'FEED											
H'FEEE	ETCR0B										
H'FEEF											
H'FEF0	MAR1AH	—	—	—	—	—	—	—	—		
H'FEF1											
H'FEF2	MAR1AL										
H'FEF3											
H'FEF4	IOAR1A										
H'FEF5											
H'FEF6	ETCR1A										
H'FEF7											
H'FEF8	MAR1BH	—	—	—	—	—	—	—	—		
H'FEF9											
H'FEFA	MAR1BL										
H'FEFB											
H'FEFC	IOAR1B										
H'FEFD											
H'FEFE	ETCR1B										
H'FEFF											
H'FF00	P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR	Port	8
H'FF01	—	—	—	—	—	—	—	—	—		
H'FF02	P3DR	P37DR	P36DR	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR		
H'FF04	—	—	—	—	—	—	—	—	—		
H'FF05	—	—	—	—	—	—	—	—	—		
H'FF06	P7DR	P77DR	P76DR	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR		
H'FF07	—	—	—	—	—	—	—	—	—		
H'FF09	PADR	—	—	—	—	PA3DR	PA2DR	PA1DR	PA0DR		
H'FF0A	PBDR	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR		
H'FF0B	PCDR	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR		
H'FF0C	PDDR	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR		
H'FF0D	PEDR	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR		
H'FF0E	PFDR	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR		
H'FF0F	PGDR	—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR		
H'FF10	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU0	16
H'FF11	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FF12	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	TPU0	16
H'FF13	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FF14	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FF15	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FF16	TCNT0										
H'FF17											
H'FF18	TGR0A										
H'FF19											
H'FF1A	TGR0B										
H'FF1B											
H'FF1C	TGR0C										
H'FF1D											
H'FF1E	TGR0D										
H'FF1F											
H'FF20	TCR1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU1	16
H'FF21	TMDR1	—	—	—	—	MD3	MD2	MD1	MD0		
H'FF22	TIOR1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FF24	TIER1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FF25	TSR1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FF26	TCNT1										
H'FF27											
H'FF28	TGR1A										
H'FF29											
H'FF2A	TGR1B										
H'FF2B											
H'FF30	TCR2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU2	16
H'FF31	TMDR2	—	—	—	—	MD3	MD2	MD1	MD0		
H'FF32	TIOR2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FF34	TIER2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FF35	TSR2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FF36	TCNT2										
H'FF37											
H'FF38	TGR2A										
H'FF39											
H'FF3A	TGR2B										
H'FF3B											

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FF60	DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A	DMAC	8
H'FF61	DMATCR	—	—	TEE1	TEE0	—	—	—	—		
H'FF62	DMACR0A	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0		16
H'FF63	DMACR0B	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0		
H'FF64	DMACR1A	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0		
H'FF65	DMACR1B	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0		
H'FF66	DMABCRH	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A		
H'FF67	DMABCRL	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A		
H'FF68	TCR0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR0, TMR1	16
H'FF69	TCR1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0		
H'FF6A	TCSR0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0		
H'FF6B	TCSR1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0		
H'FF6C	TCORA0										
H'FF6D	TCORA1										
H'FF6E	TCORB0										
H'FF6F	TCORB1										
H'FF70	TCNT0										
H'FF71	TCNT1										
H'FF74 (write)	TCSR0/ TCNT0	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT0	16
H'FF75 (read)	TCNT0										
H'FF76 (write)	RSTCSR	WOVF	RSTE	RSTS	—	—	—	—	—		
H'FF77 (read)	RSTCSR	WOVF	RSTE	RSTS	—	—	—	—	—		
H'FF78	SMR0	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI0, IIC0, Smart card interface	8
	SMR0	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0		
	ICCR0	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP		
H'FF79	BRR0										
	ICSR0	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB		
H'FF7A	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF7B	TDR0										
H'FF7C	SSR0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT		
	SSR0	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT		
H'FF7D	RDR0										

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FF7E	SCMR0	—	—	—	—	SDIR	SINV	—	SMIF	SCI0, IIC0, Smart card interface	8
	ICDR0/ SARX0	ICDR7/ SVAX6	ICDR6/ SVAX5	ICDR5/ SVAX4	ICDR4/ SVAX3	ICDR3/ SVAX2	ICDR2/ SVAX1	ICDR1/ SVAX0	ICDR0/ FSX		
H'FF7F	ICMR0/ SAR0	MLS/ SVA6	WAIT/ SVA5	CKS2/ SVA4	CKS1/ SVA3	CKS0/ SVA2	BC2/ SVA1	BC1/ SVA0	BC0/FS		
H'FF80	SMR1	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI1, IIC1, Smart card interface	
	SMR1	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0		
	ICCR1	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP		
H'FF81	BRR1										
	ICSR1	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB		
H'FF82	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF83	TDR1										
H'FF84	SSR1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT		
	SSR1	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT		
H'FF85	RDR1										
H'FF86	SCMR1	—	—	—	—	SDIR	SINV	—	SMIF		
	ICDR1/ SARX1	ICDR7/ SVARX6	ICDR6/ SVARX5	ICDR5/ SVARX4	ICDR4/ SVARX3	ICDR3/ SVARX2	ICDR2/ SVARX1	ICDR1/ SVARX0	ICDR0/ FSX		
H'FF87	ICMR1/ SAR1	MLS/ SVA6	WAIT/ SVA5	CKS2/ SVA4	CKS1/ SVA3	CKS0/ SVA2	BC2/ SVA1	BC1/ SVA0	BC0/FS	IIC1	8
H'FF88	SMR2	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI2, Smart card interface	8
	SMR2	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0		
H'FF89	BRR2										
H'FF8A	SCR2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF8B	TDR2										
H'FF8C	SSR2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT		
	SSR2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT		
H'FF8D	RDR2										
H'FF8E	SCMR2	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF90	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D	8
H'FF91	ADDRAL	AD1	AD0	—	—	—	—	—	—		
H'FF92	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF93	ADDRBL	AD1	AD0	—	—	—	—	—	—		
H'FF94	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF95	ADDRCL	AD1	AD0	—	—	—	—	—	—		
H'FF96	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF97	ADDRDL	AD1	AD0	—	—	—	—	—	—		
H'FF98	ADCSR	ADF	ADIE	ADST	SCAN	CH3	CH2	CH1	CH0		
H'FF99	ADCR	TRGS1	TRGS0	—	—	CKS1	CKS0	—	—		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width (bits)
H'FFA2 (write)	TCSR1/ TCNT1	OVF	WT/$\overline{IT}$	TME	PSS	RST/ $\overline{NMI}$	CKS2	CKS1	CKS0	WDT1	16
H'FFA3 (read)	TCNT1										
H'FFA4	DADR0									D/A0, D/A1	8
H'FFA5	DADR1										
H'FFA6	DACR01	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FFA8	FLMCR1	FWE	SWE1	ESU1	PSU1	EV1	PV1	E1	P1	FLASH	8
H'FFA9	FLMCR2	FLER	—	—	—	—	—	—	—		
H'FFAA	EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0		
H'FFAB	EBR2	—	—	—	—	EB11	EB10	EB9	EB8		
H'FFAC	FLPWCR	PDWND	—	—	—	—	—	—	—		
H'FFB0	PORT1	P17	P16	P15	P14	P13	P12	P11	P10	Port	8
H'FFB2	PORT3	P37	P36	P35	P34	P33	P32	P31	P30		
H'FFB3	PORT4	P47	P46	P45	P44	P43	P42	P41	P40		
H'FFB6	PORT7	P77	P76	P75	P74	P73	P72	P71	P70		
H'FFB8	PORT9	P97	P96	P95	P94	P93	P92	P91	P90		
H'FFB9	PORTA	—	—	—	—	PA3	PA2	PA1	PA0		
H'FFBA	PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0		
H'FFBB	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0		
H'FFBC	PORTD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0		
H'FFBD	PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
H'FFBE	PORTF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		
H'FFBF	PORTG	—	—	—	PG4	PG3	PG2	PG1	PG0		

Note: Undefined and reserved addresses are for use in future functional expansion or have test registers, etc., assigned to them. These registers must not be accessed, since operation in the event of such access, and subsequent operation, cannot be guaranteed .