S6A0069

40 SEG / 16 COM DRIVER & CONTROLLER FOR DOT MATRIX LCD

June. 2000.

Ver. 0.0

INTRODUCTION

S6A0069 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 1, 2-line with 5 x 8 or 5 x 11 dots format.
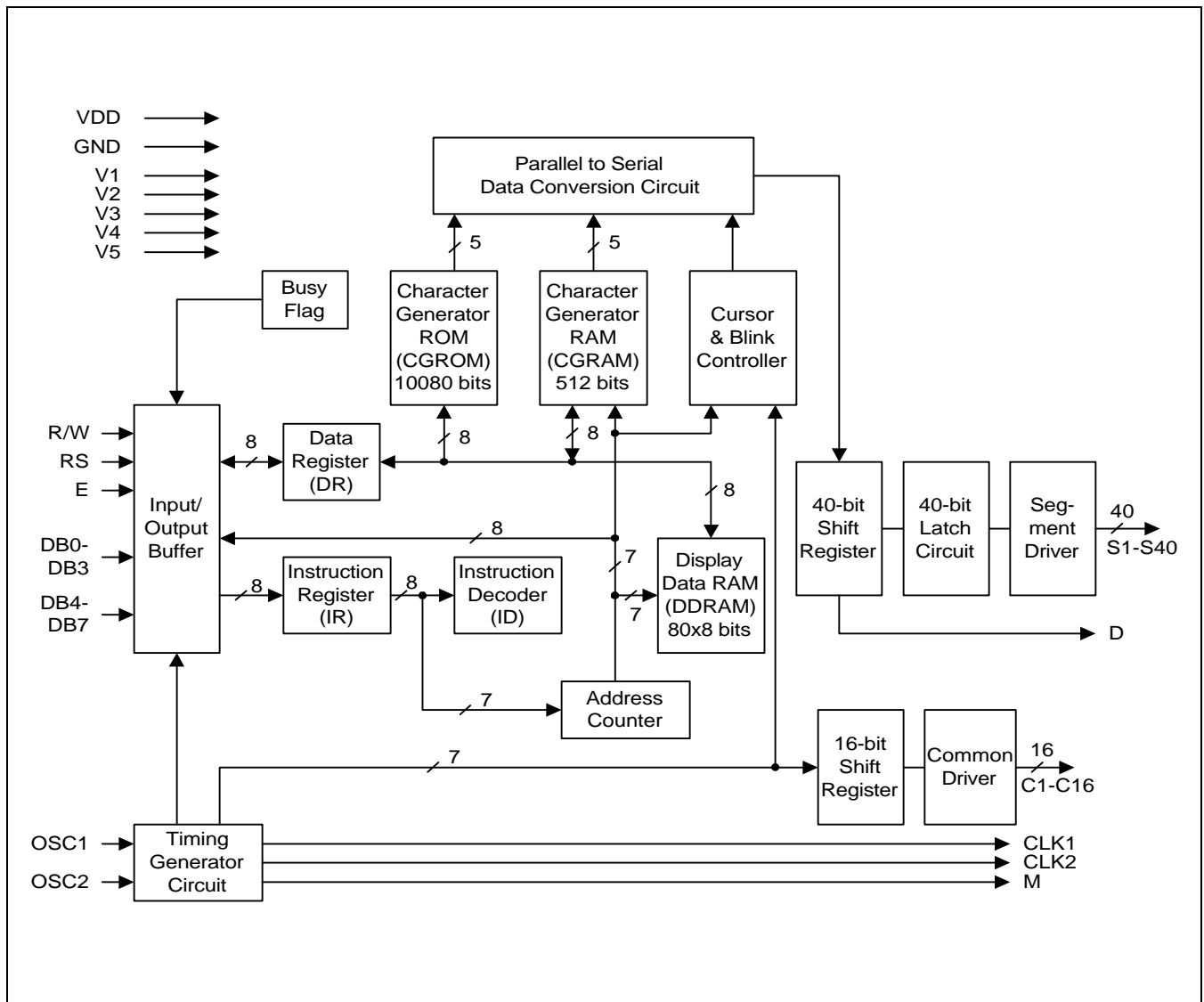
FUNCTIONS

- Character type dot matrix LCD driver & controller.

- Internal driver: 16 common and 40 segment signal output.

- Easy interface with 4-bit or 8-bit MPU

- Display character pattern : 5 x 8 dots format (204 kinds), 5 x 11 dots format (32 kinds)

- The special character pattern can be programmable by Character Generator RAM directly.

- A customer character pattern can be programmable by mask option.

- It can drive a maximum 80 characters by using the S6A0065 or S6A2067 externally.

- Various instruction functions

- Automatic power on reset

FEATURES

- Internal Memory

  - Character Generator ROM (CGROM): 10,080 bits (204 characters x 5 x 8 dot) & (32 characters x 5 x 11 dot)

  - Character Generator RAM (CGRAM): 64×8 bits (8 characters $\times 5 \times 8$ dot)

  - Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)

- Low Power Operation

  - Power supply voltage range: 2.7 to 5.5V (V_{DD})

  - LCD drive voltage range: 3.0 to 13.0V (V_{DD} - V5)

- CMOS process

- Programmable duty cycle: 1/8, 1/11, 1/16

- Internal oscillator with an external resistor

- Low power consumption

- Bare chip available

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BLOCK DIAGRAM

PAD CONFIGURATION

S22 1		64 S39
S21 2	**S6A0069**	63 S40
S20 3		62 C16
S19 4		61 C15
S18 5		60 C14
S17 6		59 C13
S16 7		58 C12
S15 8	Y	57 C11
S14 9		56 C10
S13 10		55 C9
S12 11	X	54 C8
S11 12	(0, 0)	53 C7
S10 13		52 C6
S9 14		51 C5
S8 15		50 C4
S7 16	Chip size: 4060 × 3840	49 C3
S6 17	Pad size: 100 × 100	48 C2
S5 18	Unit: μm	47 C1
S4 19		46 DB7
S3 20		45 DB6
S2 21		44 DB5
S1 22		43 DB4
GND 23		42 DB3
OSC1 24		41 DB2

Top pads (left to right): 80 S23, 79 S24, 78 S25, 77 S26, 76 S27, 75 S28, 74 S29, 73 S30, 72 S31, 71 S32, 70 S33, 69 S34, 68 S35, 67 S36, 66 S37, 65 S38

Bottom pads (left to right): 25 OSC2, 26 V1, 27 V2, 28 V3, 29 V4, 30 V5, 31 CLK1, 32 CLK2, 33 VDD, 34 M, 35 D, 36 RS, 37 R/W, 38 E, 39 DB0, 40 DB1

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PAD CENTER COORDINATES

Unit: um

PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y
1	S22	-1864	1465	28	V3	-670	-1754	55	C9	1864	335
2	S21	-1864	1340	29	V4	-520	-1754	56	C10	1864	460
3	S20	-1864	1215	30	V5	-370	-1754	57	C11	1864	585
4	S19	-1864	1090	31	CLK1	-220	-1754	58	C12	1864	710
5	S18	-1864	965	32	CLK2	-70	-1754	59	C13	1864	835
6	S17	-1864	840	33	VDD	80	-1754	60	C14	1864	960
7	S16	-1864	715	34	M	230	-1754	61	C15	1864	1085
8	S15	-1864	590	35	D	380	-1754	62	C16	1864	1210
9	S14	-1864	465	36	RS	518	-1754	63	S40	1864	1341
10	S13	-1864	340	37	R/W	642	-1754	64	S39	1864	1466
11	S12	-1864	215	38	E	768	-1754	65	S38	886	1754
12	S11	-1864	90	39	DB0	894	-1754	66	S37	760	1754
13	S10	-1864	-35	40	DB1	1018	-1754	67	S36	636	1754
14	S9	-1864	-160	41	DB2	1864	-1488	68	S35	510	1754
15	S8	-1864	-285	42	DB3	1864	-1362	69	S34	386	1754
16	S7	-1864	-410	43	DB4	1864	-1238	70	S33	260	1754
17	S6	-1864	-535	44	DB5	1864	-1112	71	S32	136	1754
18	S5	-1864	-660	45	DB6	1864	-988	72	S31	10	1754
19	S4	-1864	-785	46	DB7	1864	-862	73	S30	-114	1754
20	S3	-1864	-910	47	C1	1864	-665	74	S29	-240	1754
21	S2	-1864	-1034	48	C2	1864	-540	75	S28	-364	1754
22	S1	-1864	-1159	49	C3	1864	-415	76	S27	-490	1754
23	GND	-1864	-1285	50	C4	1864	-290	77	S26	-614	1754
24	OSC1	-1864	-1414	51	C5	1864	-165	78	S25	-740	1754
25	OSC2	-1120	-1754	52	C6	1864	-40	79	S24	-864	1754
26	V1	-970	-1754	53	C7	1864	85	80	S23	-989	1754
27	V2	-820	-1754	54	C8	1864	210				

PIN DESCRIPTION

PIN	No	I/O	NAME	DESCRIPTION	INTERFACE
VDD	33	-	Supply Voltage	Supply Voltage for logical circuit (+3V ± 10%,+5V ±10%)	Power Supply
GND	23			0V (GND)	
V1 - V5	26- 30			Bias voltage level for LCD driving.	
S1 - S40	1-22, 63- 80	O	Segment output	Segment signal output for LCD drive.	LCD
C1 - C16	47-62	O	Common output	Common signal output for LCD drive.	LCD
OSC1	24	I	Oscillator	When use internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External Resistor/ Oscillator OSC1
OSC2	25	O	Oscillator		
CLK1	31	O	Extension driver Latch clock	extension driver latch clock.	Extension driver
CLK2	32	O	Extension driver Shift clock	extension driver shift clock.	
M	34	O	Alternated signal for LCD driver output	Outputs the alternating signal to convert LCD driver waveform to AC.	Extension driver
D	35	O	Display data interface	Outputs extension driver data (the 41th dot's data)	Extension driver
RS	36	I	Register select	Used as register selection input. When RS = "High", Data register is selected. When RS = "Low", Instruction register is selected.	MPU
R/W	37	I	Read/Write	Used as read/write selection input. When R/W = "High", read operation. When R/W = "Low", write operation.	MPU
E	38	I	Read/write enable	Read/write enable signal.	MPU
DB0-DB3	39-42	I/O	Data bus 0-7	When 8-bit bus mode, used as low order bidirectional data bus. In 4-bit bus mode open these pins.	MPU
DB4-DB7	43-46			When 8-bit bus mode, used as high order bidirectional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 is used for Busy Flag output.	MPU

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FUNCTION DESCRIPTION

System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. During read or write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register(IR). The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically. The instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS input pin in 4-bit/8-bit bus mode.

Table 1. Various Kinds of Operations according to RS and R/W Bits

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag (DB7) and address counter (DB0 - DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6 ports.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure1.)
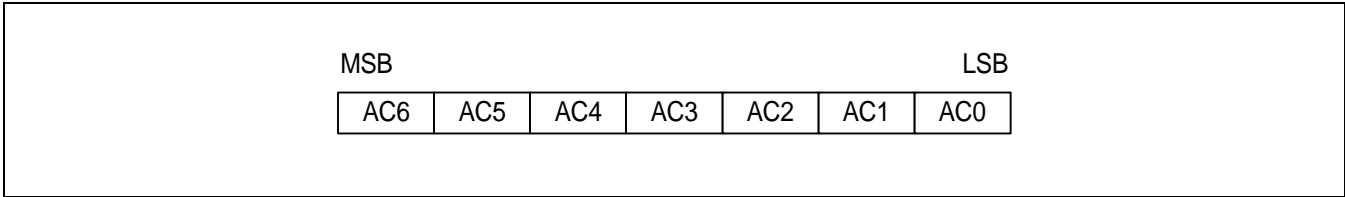
MSB   LSB

AC6	AC5	AC4	AC3	AC2	AC1	AC0

Figure 1. DDRAM Address

1) 1-line Display

In case of 1 line display, the address range of DDRAM is 00H - 4FH. Extension driver will be used. Fig-2 shows the example that 40 segment extension driver is added.
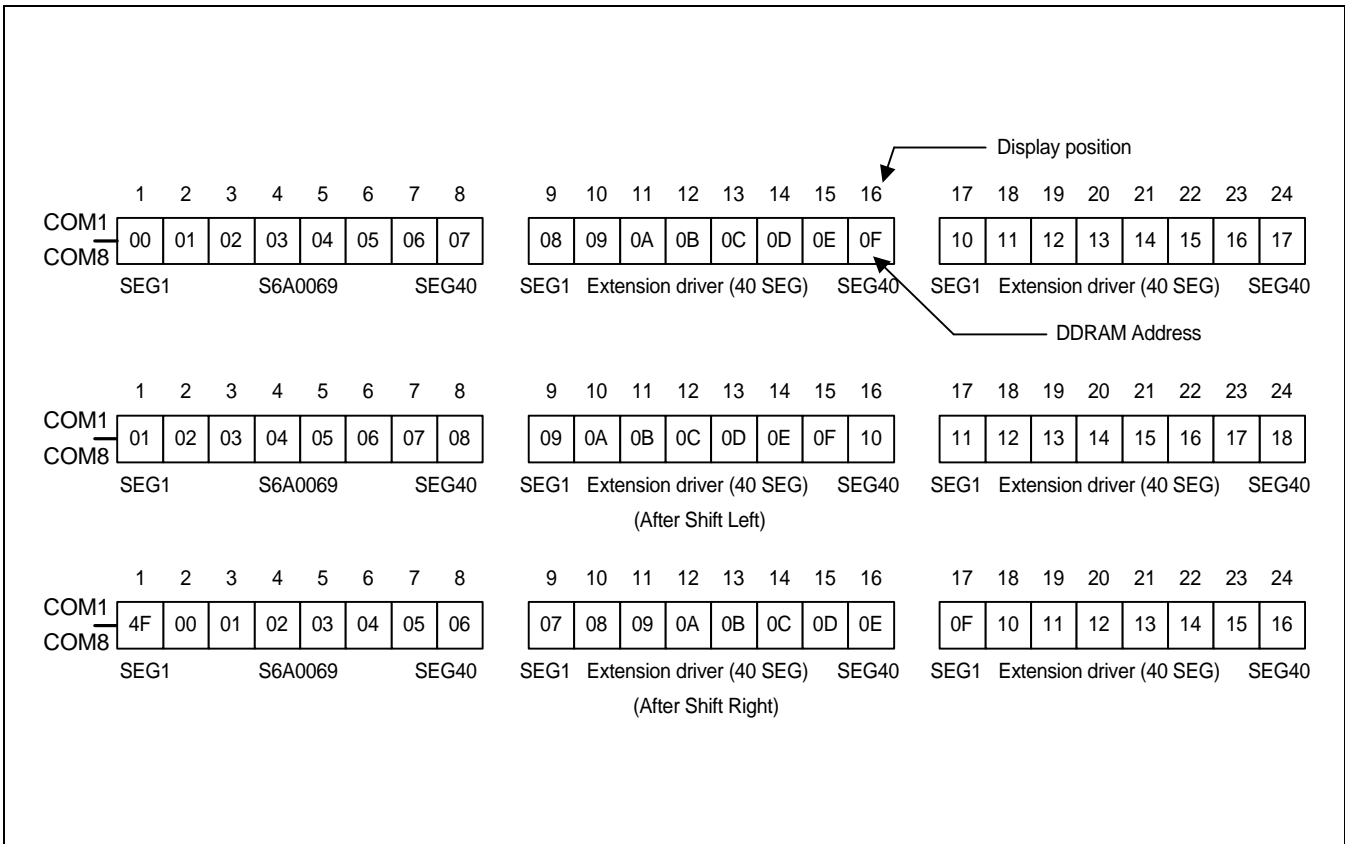

Figure 2. 1-line x 24 Character Display with 40 Segment Extension Driver

2) 2-line Display

In case of 2 line display, the address range of DDRAM is 00H - 27H, 40H - 67H. Extension driver will be used. Figure 3 shows the example that 40 segment extension driver is added.
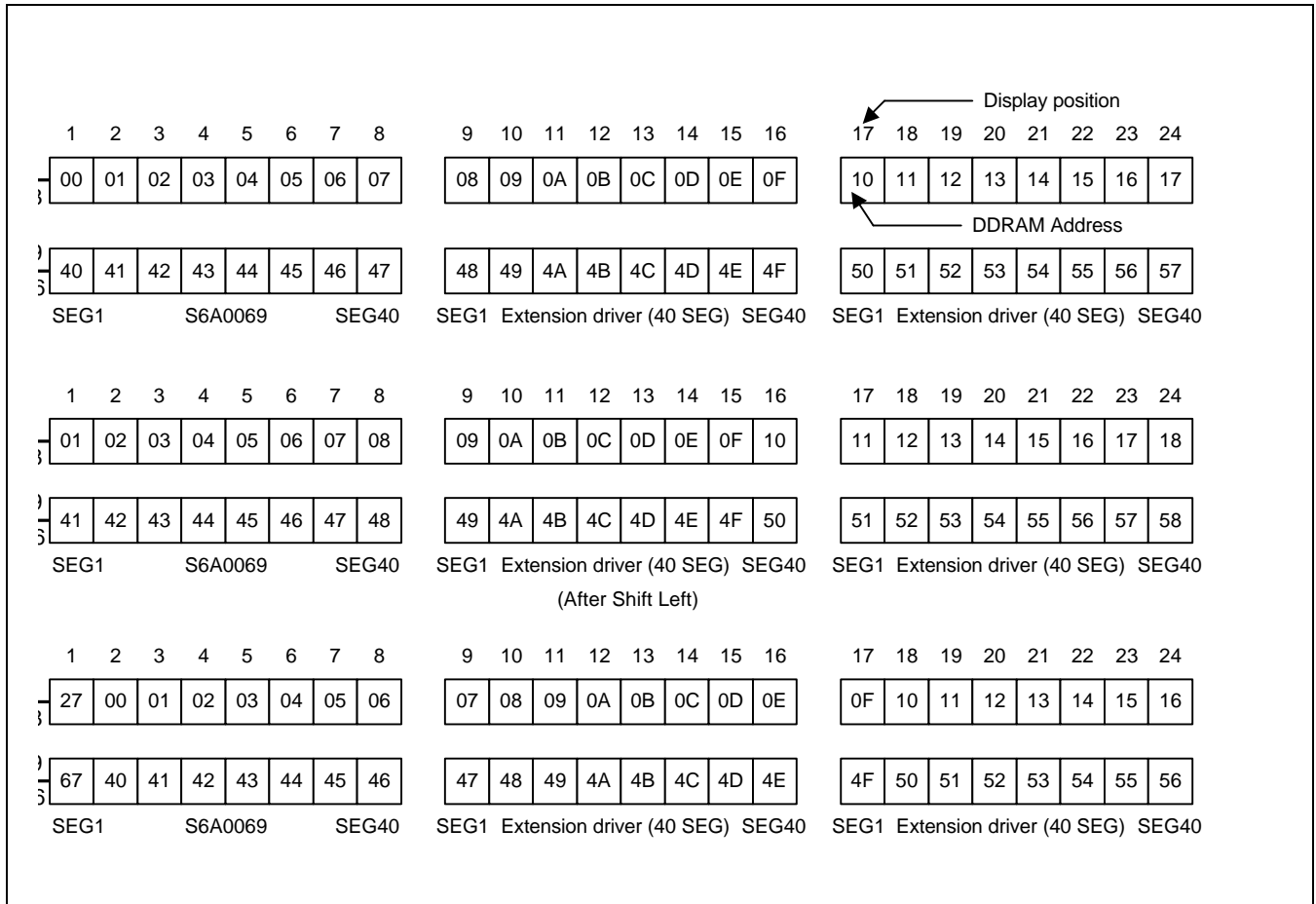

Figure 3. 2-line x 24 Character Display with 40 Segment Extension Driver

CGROM (Character Generator ROM)

CGROM has a 5 x 8 dots 204 characters pattern and a 5 x 10 dots 32 characters pattern. CGROM has 204 character patterns of 5 x 8 dots, and 32 character patterns of 5 x 11 dots.

CGRAM (Character Generator RAM)

CGRAM has up to 5×8 dot, 8 characters. By writing font data to CGRAM, user defined characters can be used (refer to Table 5)

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch. In case of 1-line display mode, COM1- COM8 have 1/8 duty or COM1 — COM11 have 1/11duty, and in 2-line mode, COM1 - COM16 have 1/16 duty ratio.

Cursor / Blink Control Circuit

It controls cursor/blink ON / OFF at cursor position.

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Table 5. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	Pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
				.						.	0	1	1			.	1	1	1	1	1	
				.						.	1	0	0			.	1	0	0	0	1	
				.						.	1	0	1			.	1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
			.								.						.					.
			.								.						.					.
			.								.						.					.
0	0	0	0	x	1	1	1	0	0	0	0	0	0	x	x	x	1	0	0	0	1	Pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
				.						.	0	1	1			.	1	1	1	1	1	
				.						.	1	0	0			.	1	0	0	0	1	
				.						.	1	0	1			.	1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between internal clock of S6A0069 and MPU clock, S6A0069 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 5) Instruction can be divided largely four kinds,

(1) S6A0069 function set instructions (set display methods, set data length, etc.)

(2) Address set instructions to internal RAM

(3) Data transfer instructions with internal RAM

(4) Others.

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read High. Busy Flag check must precede the next instruction. When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "LOW".

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

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3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display

When DDRAM read (CGRAM read/write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

4) Display ON / OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF Control Bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF Control Bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF Control Bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (Refer to table 6). During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

Table 6. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL : Interface Data Length Control Bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display Line Number Control Bit
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.

F : Display Font Type Control Bit
When F = "Low", it means 5×8 dots format display mode
When F = "High", 5×11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether S6A0069 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

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10) Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

Table 7. Instruction Table

Instruction	Instruction Code										Description Instruction Code	Execution time (fsoc=270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable.	39μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	39μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type(F : 5 X 8 dots/ 5 X 11 dots)	39μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

NOTE: When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "LOW".

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INTERFACE WITH MPU

1) Interface with 8-bit MPU

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.
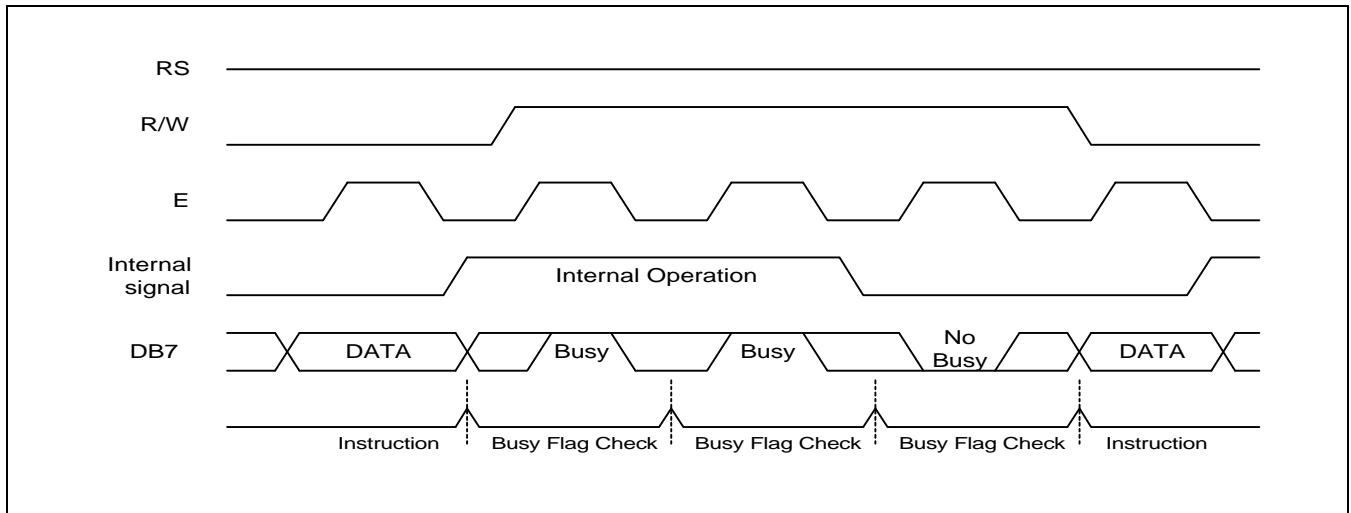

Figure 4. Example of 8-bit Bus Mode Timing Diagram

2) Interface with 4-bit MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended. Example of timing sequence is shown below.
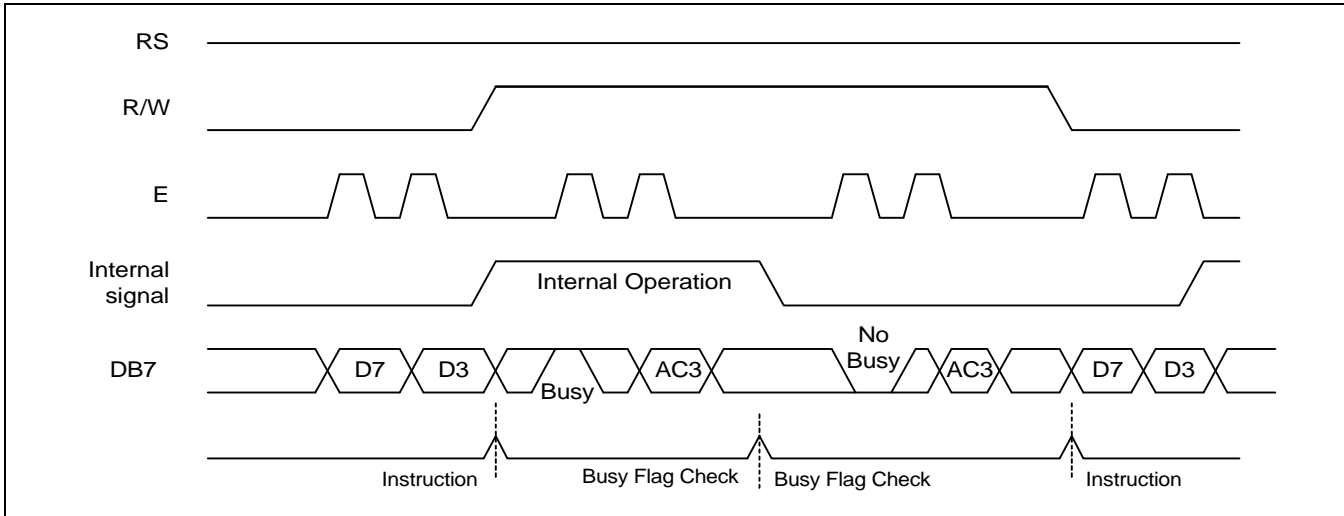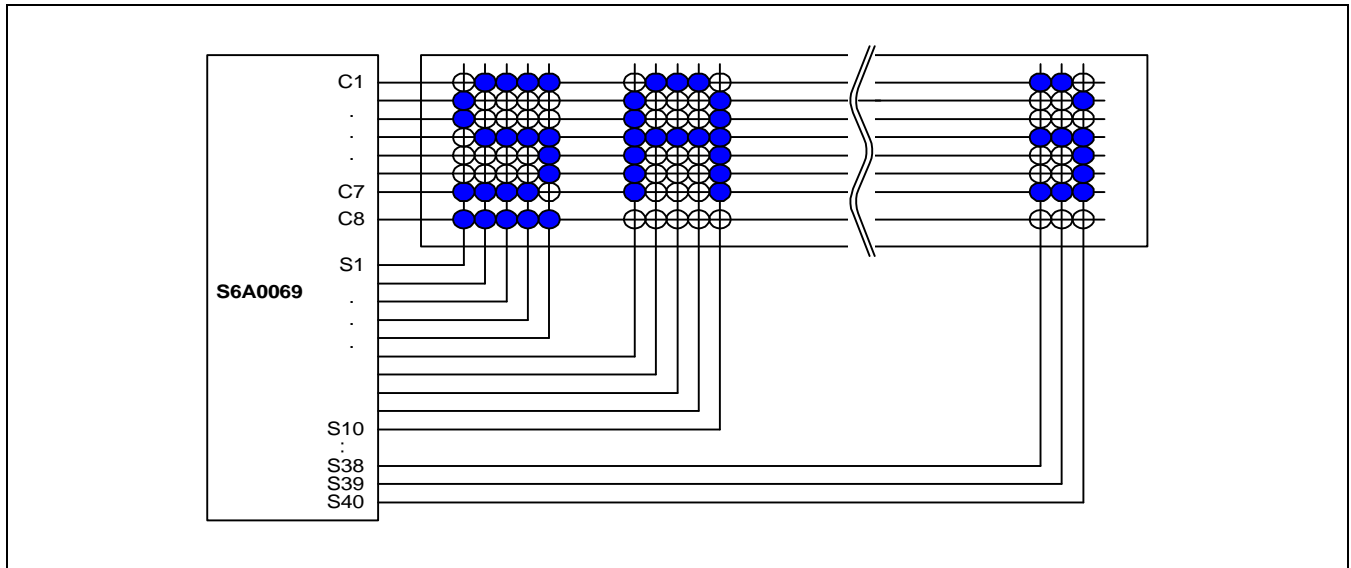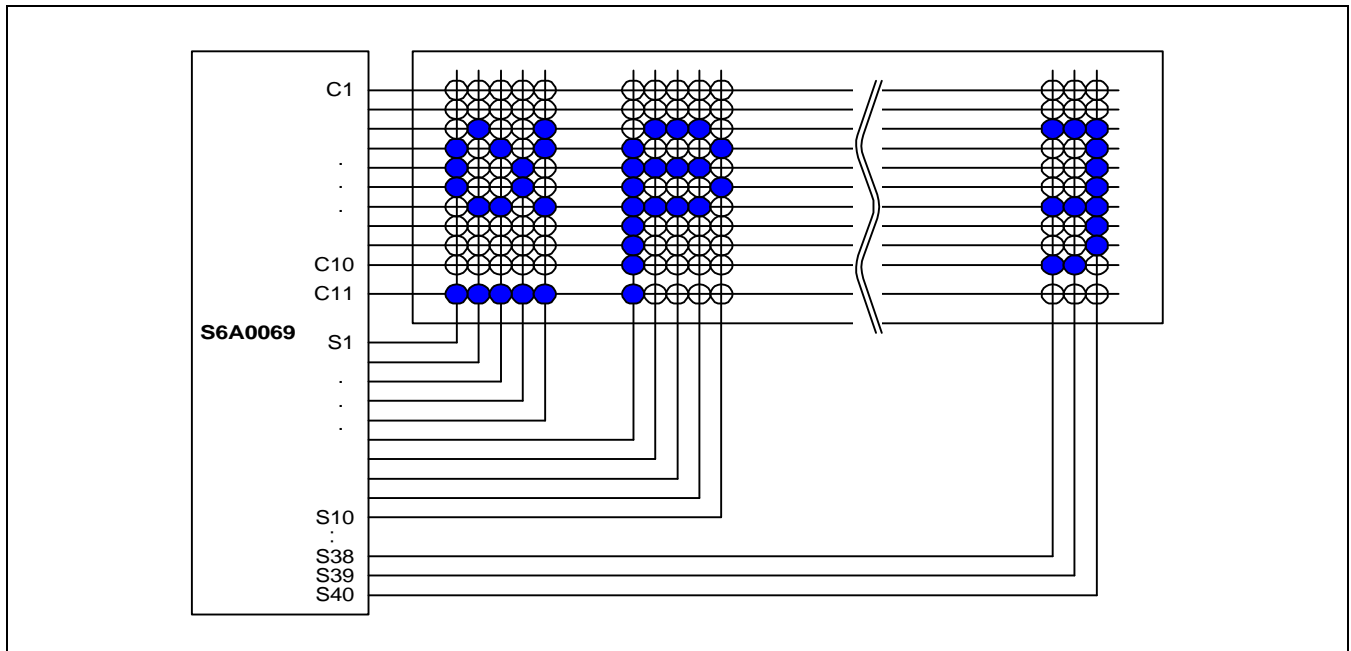

Figure 5. Example of 4-bit Bus Mode Timing Diagram

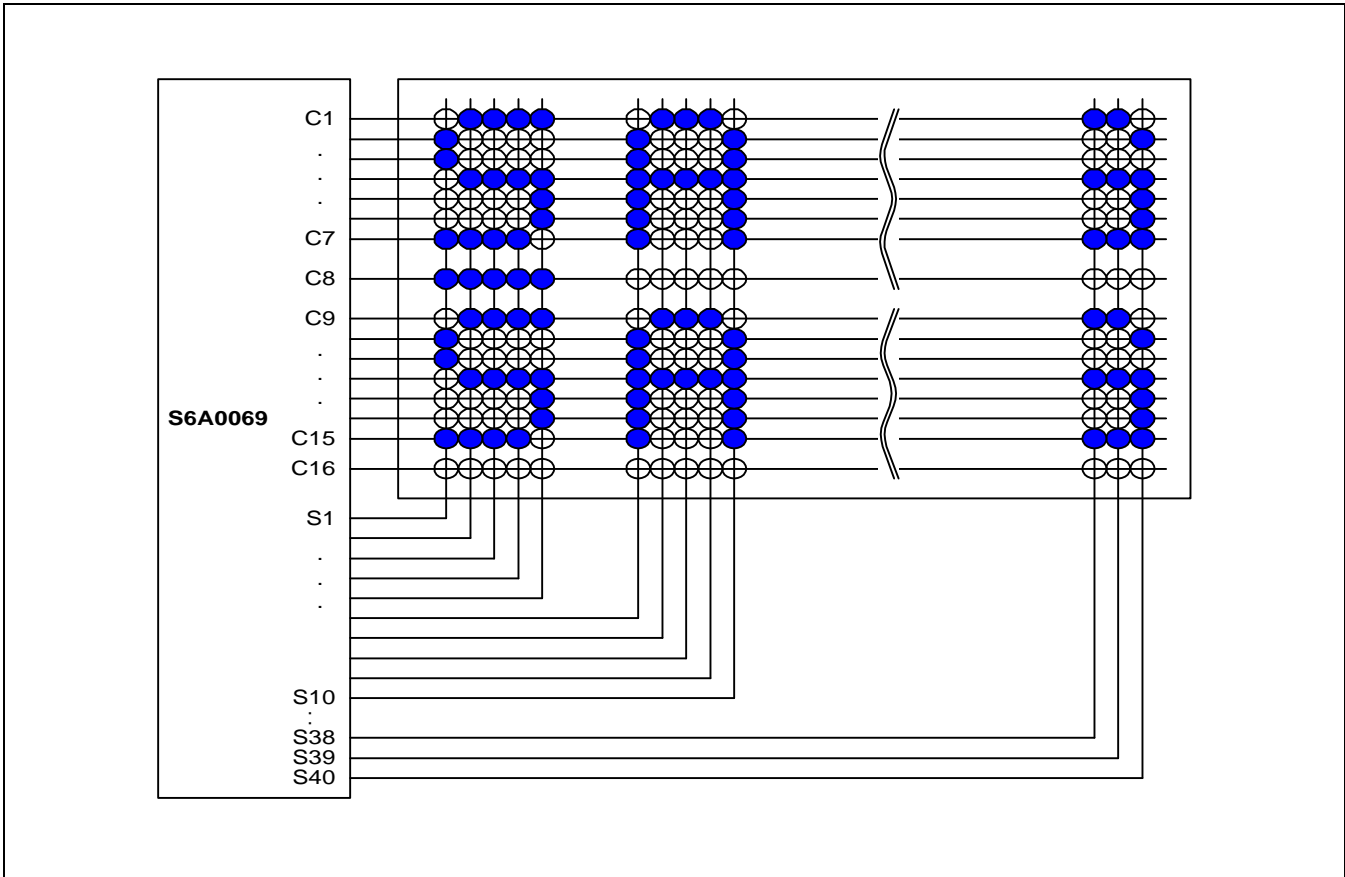## APPLICATION INFORMATION ACCORDING TO LCD PANEL

1) LCD Panel: 8 Character × 1-line Character Format; 5 × 7 dots + 1-cursor line (1/4 Bias, 1/8 Duty)

2) LCD Panel: 8 Character × 1-line Character Format; 5 × 10 dots + 1 cursor line (1/4 Bias, 1/11 Duty)

3) LCD Panel: 8 Character × 2-line Character Format; 5 × 7 dots + 1-cursor line (1/5 Bias, 1/16 Duty)
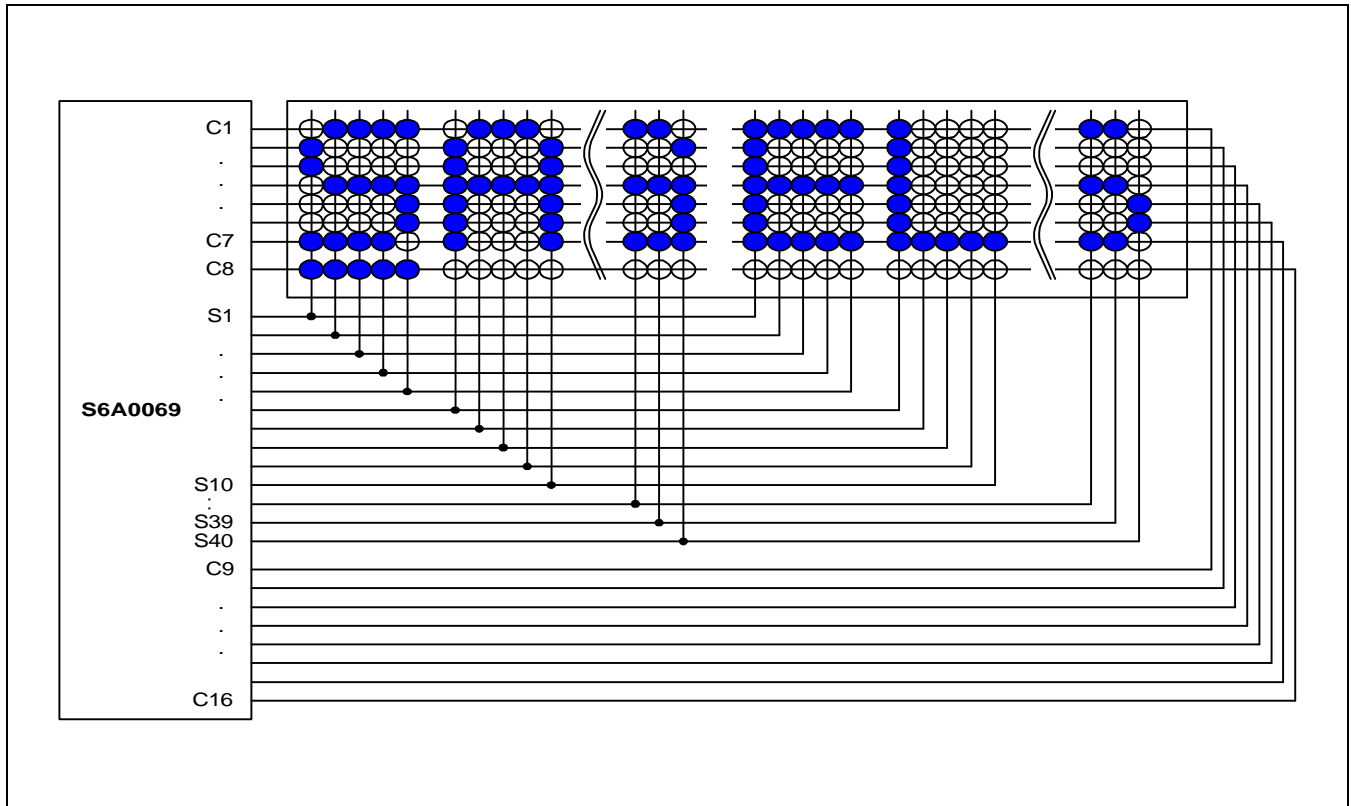
4) LCD Panel: 16 Character ×1-line Character Format; 5×7 dots + 1-cursor line (1/5 Bias, 1/16 Duty)

5) LCD Panel: 4 Character × 2-line Character Format; 5 × 7 dots + 1-cursor line (1/4 Bias, 1/8 Duty)

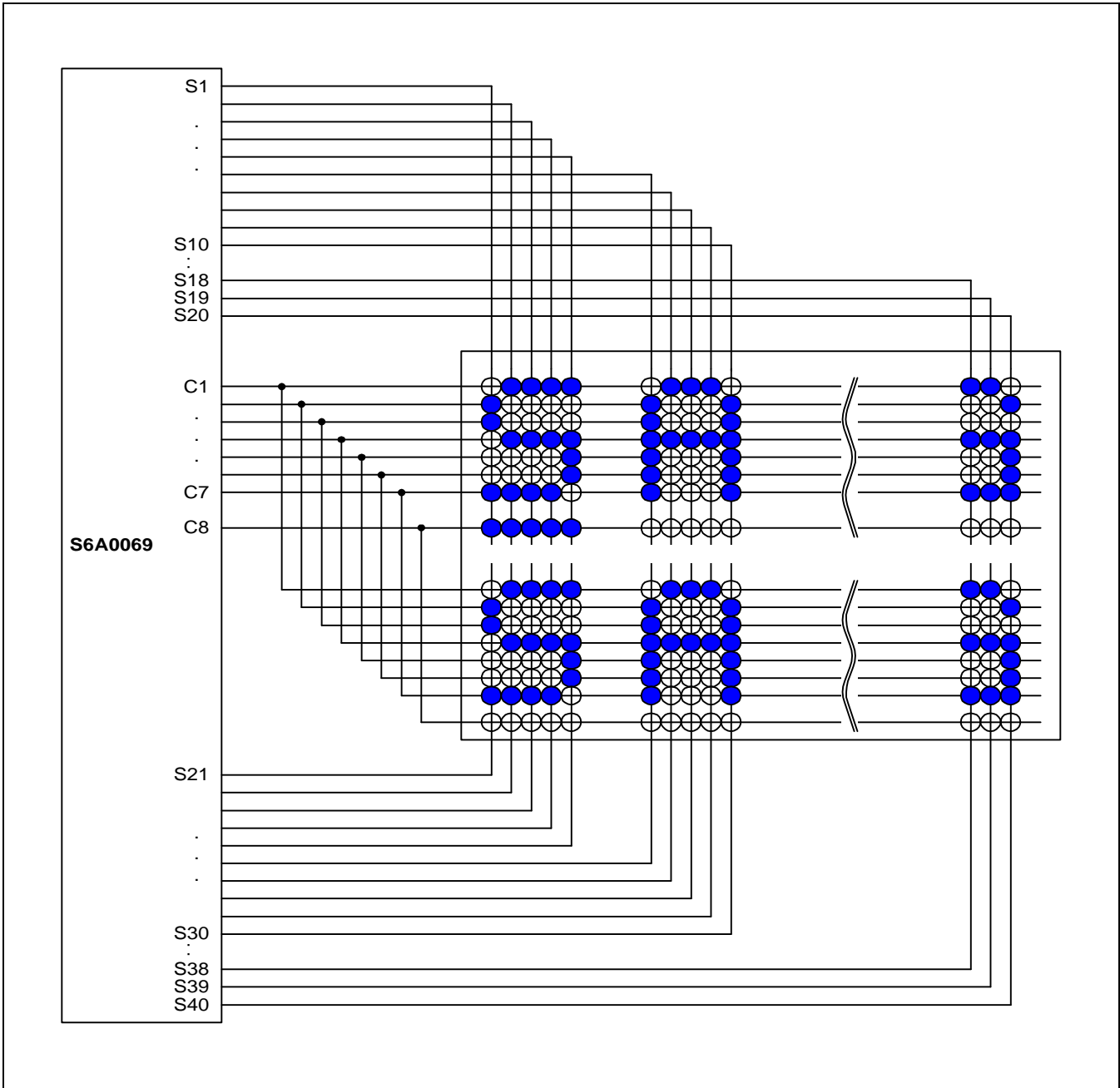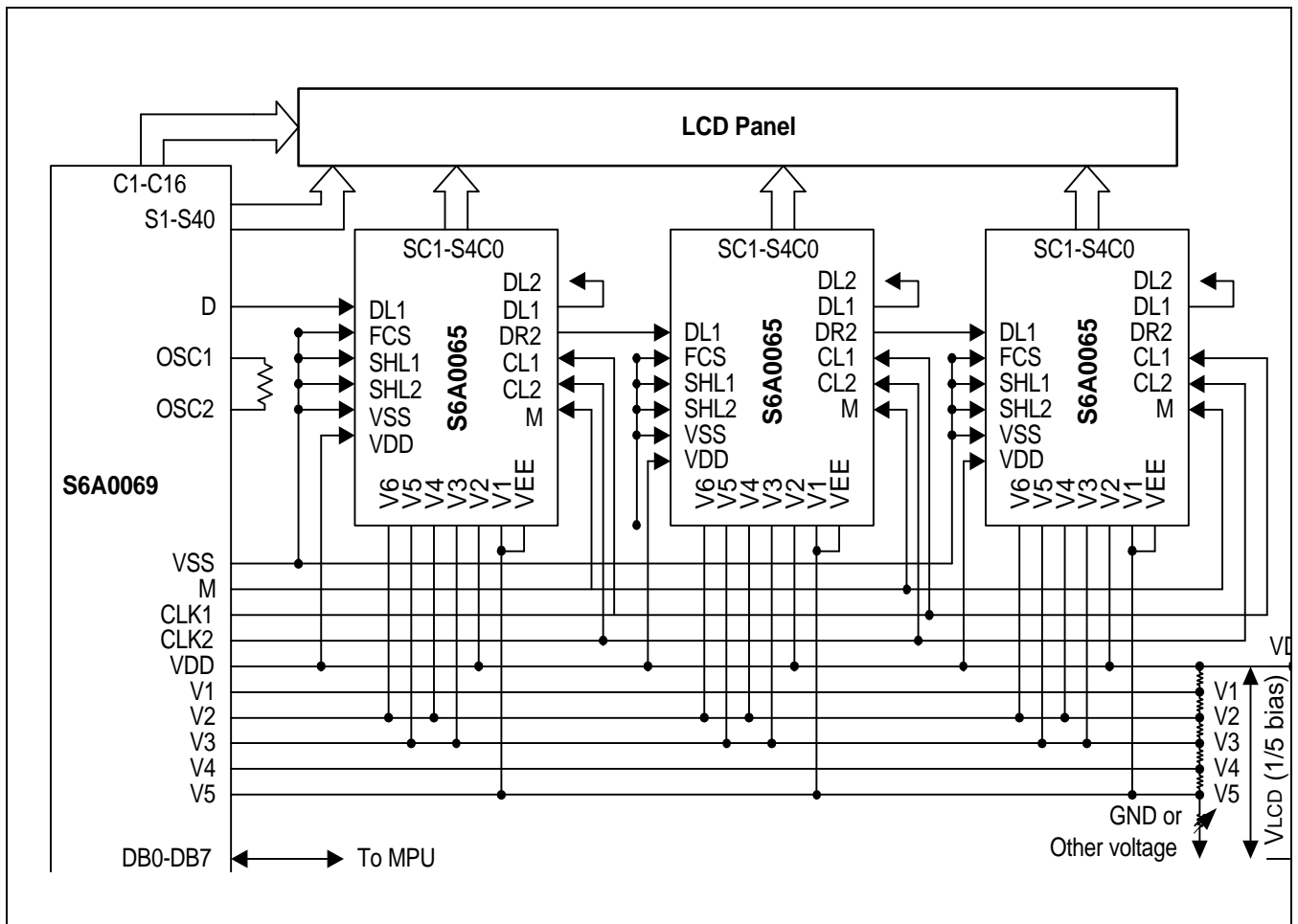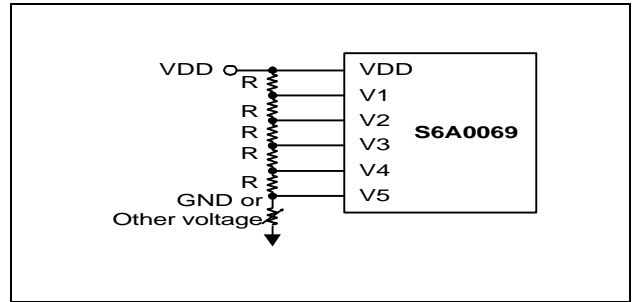## 6) APPLICATION CIRCUIT

NOTE: When S6A0065 is externally connected to the S6A0069, you can increase the number of display digits up to 80 characteristics.

BIAS VOLTAGE DIVIDE CIRCUIT

1) 1/4 bias, 1/8 or 1/11 duty

2)   1/5 bias, 1/16 duty
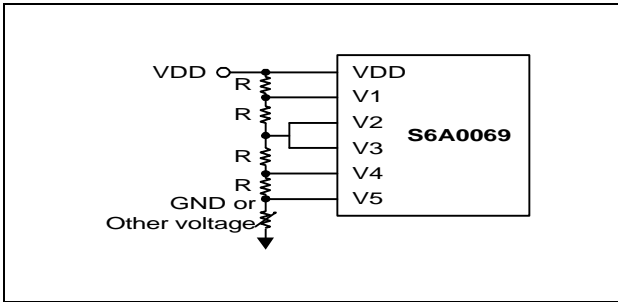
INITIALIZING

When the power is turned on, S6A0069 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

(1) Display Clear instruction: Write "20H" to all DDRAM

(2) Set Functions instruction
        DL = 1 : 8-bit bus mode
        N = 1 : 2-line display mode
        F = 0 : 5 X 8 font type

(3) Control Display ON/OFF instruction
        D = 0 : Display OFF
        C = 0 : Cursor OFF
        B = 0 : Blink OFF

(4) Set Entry Mode instruction
        I/D = 1 : Increment by 1
        SH = 0 : No entire display shift

FRAME FREQUENCY

Programmable Driving Method by the same font mask option: Display waveform A-Type, B-Type

1) 1/8 Duty Cycle

A) A-Type Waveform
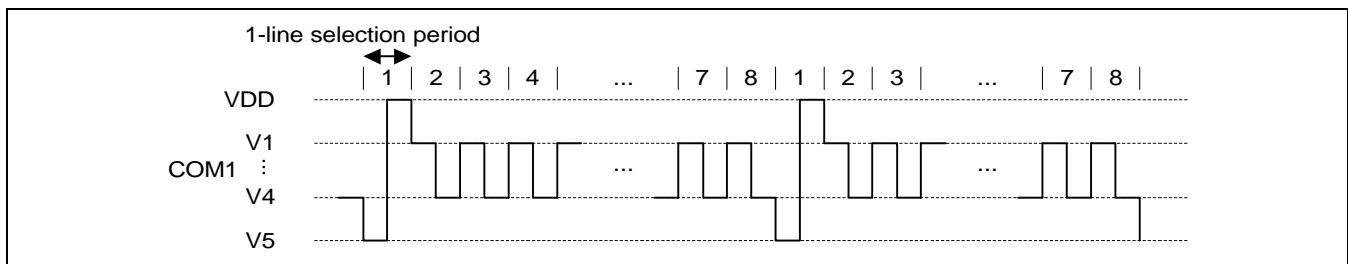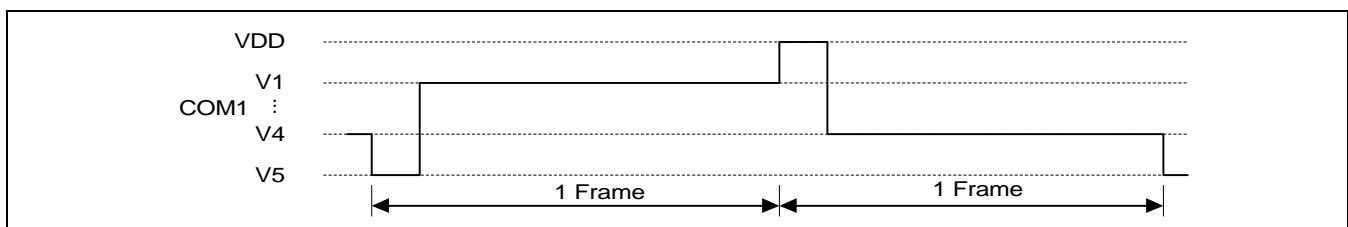
B) B-Type Waveform

Line selection period   = 400 clocks
One Frame   = 400 x 8 x 3.7μs = 11850 μs = 11.9 ms (1 clock = 3.7 μs, fosc = 270kHz)
Frame frequency   = 1 / 11.9ms = 84.3Hz

2) 1/11 duty cycle

A) A-type Waveform
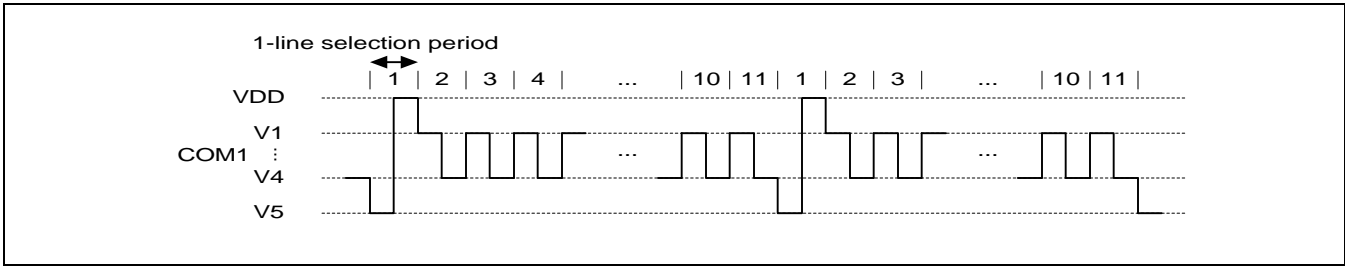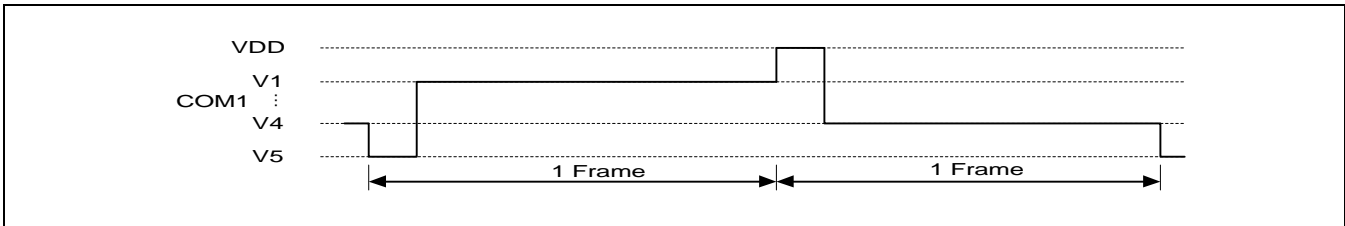
B) B-type Waveform

Line selection period = 400 clocks
One Frame = 400 x 11 x 3.7μs = 16300μs = 16.3ms (1 clock = 3.7μs , fosc = 270kHz)
Frame frequency = 1 / 16.3 ms = 61.4 Hz

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3) 1/16 duty cycle

A) A-type Waveform
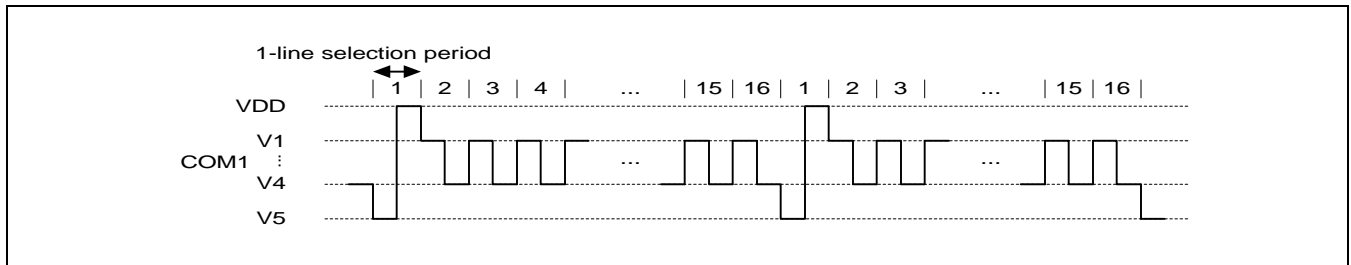
B) B-type Waveform
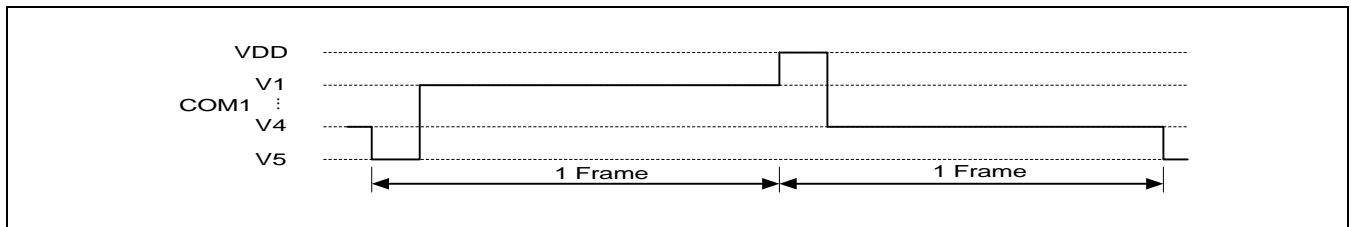
Line selection period = 200 clocks
One Frame = 200 x 16 x 3.7µs = 11850 µs = 11.9 ms (1 clock = 3.7µs, fosc = 270kHz)
Frame frequency = 1 / 11.9ms = 84.3Hz

INITIALIZING BY INSTRUCTION

1) 8-bit Interface Mode (Condition: fosc = 270kHz)

Power On

↓

Wait for more than 30ms after V_{DD} rises to 4.5 V.
Wait for more than 40ms after V_{DD} rises to 2.7 V.

↓

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	X	X

↓

Wait for more than 39 μs

↓

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

↓

Wait for more than 39 μs

↓

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

↓

Wait for more than 1.53ms

↓

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

↓

Initialization End

N	0	1-line mode
	1	2-line mode

F	0	Display OFF
	1	Display ON

D	0	Display OFF
	1	Display ON

C	0	Cursor OFF
	1	Cursor ON

B	0	Blink OFF
	1	Blink ON

I/D	0	Decrement mode
	1	Increment mode

SH	0	Entire shift off
	1	Entire shift on

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2) 4-bit Interface Mode (Condition: fosc = 270kHz)

Power On

↓

Wait for more than 30ms after V$_{DD}$ rises to 4.5 V.
Wait for more than 40ms after V$_{DD}$ rises to 2.7 V.

↓

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

D/L	0	4-bit mode
	1	8-bit mode

N	0	1-line mode
	1	2-line mode

F	0	Display off
	1	Display on

↓

Wait for more than 39µs

↓

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

D	0	Display off
	1	Display on

C	0	Cursor off
	1	Cursor on

B	0	Blink off
	1	Blink on

↓

Wait for more than 39µs

↓

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

↓

Wait for more than 1.53ms

↓

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	SH	X	X	X	X

I/D	0	Decrement mode
	1	Increment mode

SH	0	Entire shift off
	1	Entire shift on

↓

Initialization End

MAXIMUM ABSOLUTE LIMIT

Maximum Absolute Power Ratings

Characteristic	Symbol	Unit	Value
Power Supply Voltage	V_{DD}	V	-0.3 to +7.0
LCD Drive Voltage	V_{LCD}	V	V_{DD}-15.0 to V_{DD}+0.3
Input Voltage	V_{IN}	V	-0.3 to V_{DD}+ 0.3

.Voltage greater than above may damage the circuit ($V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

Temperature Characteristics

Characteristic	Symbol	Unit	Value
Operating Temperature	T_{OPR}	$^\circ$C	-30 to +85
Storage Temperature	T_{STG}	$^\circ$C	-55 to +125

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ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD} = 4.5V to 5.5V, Ta = -30 to +85°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-	4.5	-	5.5	V
Operating Current	I_{DD}	Internal oscillation or external clock (V_{DD} = 5.0V, fosc = 270kHz)	-	0.35	0.6	mA
Input Voltage (1)	V_{IH1}	-	2.2	-	V_{DD}	V
(except OSC1)	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (2)	V_{IH2}	-	V_{DD}-1.0	-	V_{DD}	V
(OSC1)	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (1)	V_{OH1}	I_{OH} = -0.205mA	2.4	-	-	V
(DB0 to DB7)	V_{OL1}	I_{OL} = 1.2mA	-	-	0.4	
Output Voltage (2)	V_{OH2}	I_O = -40µA	$0.9V_{DD}$	-	-	V
(except DB0 to DB7)	V_{OL2}	I_O = 40µA	-	-	$0.1V_{DD}$	
Voltage Drop	Vd_{COM}	I_O = ±0.1mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{LKG}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
Input Low Current	I_{IL}	V_{IN} = 0V, V_{DD} = 5V (pull up)	-50	-125	-250	
Internal Clock (external Rf)	f_{OSC1}	Rf = 91kΩ ±2% (V_{DD} = 5V)	190	270	350	kHz
External Clock	f_{OSC}	-	125	270	350	kHz
	duty		45	50	55	%
	t_R, t_F		-	-	0.2	µA
LCD Driving Voltage	V_{LCD}	V_{DD}-V5 (1/5, 1/4 bias)	3.0	-	13.0	V

DC Characteristics (V_{DD} = 2.7V to 4.5V, Ta = -30 to +85°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-	2.7	-	4.5	V
Operating Current	I_{DD}	Internal oscillation or external clock (V_{DD} = 3.0V, fosc = 270kHz)	-	0.15	0.3	mA
Input Voltage (1)	V_{IH1}	-	0.7 V_{DD}	-	V_{DD}	V
(except OSC1)	V_{IL1}	-	-0.3	-	0.55	
Input Voltage (2)	V_{IH2}	-	0.7V_{DD}	-	V_{DD}	V
(OSC1)	V_{IL2}	-	-	-	0.2 V_{DD}	
Output Voltage (1)	V_{OH1}	I_{OH} = -0.1mA	0.75 V_{DD}	-	-	V
(DB0 to DB7)	V_{OL1}	I_{OL} = 0.1mA	-	-	0.2 V_{DD}	
Output Voltage (2) (except DB0 to DB7) Voltage Drop	V_{OH2}	I_O = -40µA	0.8V_{DD}	-	-	V
	V_{OL2}	I_O = 40µA	-	-	0.2V_{DD}	
	Vd_{COM}	I_O = ± 0.1mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{LKG}	V_{IN} = 0V — V_{DD}	-1	-	1	µA
Input Low Current	I_{IL}	V_{IN} = 0V, V_{DD} = 3V (pull up)	-10	-50	-120	
Internal Clock (external Rf)	f_{OSC1}	Rf = 75kΩ ±2% (V_{DD} = 3V)	190	270	350	kHz
External Clock	f_{OSC2}		125	270	410	kHz
	duty	-	45	50	55	%
	t_R, t_F		-	-	0.2	µS
LCD Driving Voltage	V_{LCD}	V_{DD}-V5 (1/5, 1/4 bias)	3.0	-	13.0	V

NOTE: LCD Driving Voltage

Power	Duty	1/8, 1/11 Duty	1/16 Duty
	Bias	1/4 Bias	1/5 Bias
V_{DD}		V_{DD}	V_{DD}
V_1		V_{DD} - V_{LCD}/4	V_{DD} - V_{LCD}/5
V_2		V_{DD} - V_{LCD}/2	V_{DD} - 2V_{LCD}/5
V_3		V_{DD} - V_{LCD}/2	V_{DD} - 3V_{LCD}/5
V_4		V_{DD} - 3V_{LCD}/4	V_{DD} - 4V_{LCD}/5
V_5		V_{DD} - V_{LCD}	V_{DD} - V_{LCD}

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AC Characteristics

(V_{DD} = 4.5 to 5.5V, Ta = -30 to +85°C)

Mode	Characteristics	Symbol	Min	Typ	Max	Unit
Write Mode (refer to Figure-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (refer to Figure-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	tD	-	-	120	
	Data Hold Time	tDH	5	-	-	

(V_{DD} = 2.7 to 4.5V, Ta = -30 to +85°C)

Mode	Characteristic	Symbol	Min	Typ	Max	Unit
Write Mode (refer to Figure-6)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (refer to Figure-7)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

(V_{DD} = 2.7 to 4.5V, Ta = -30 to +85°C)

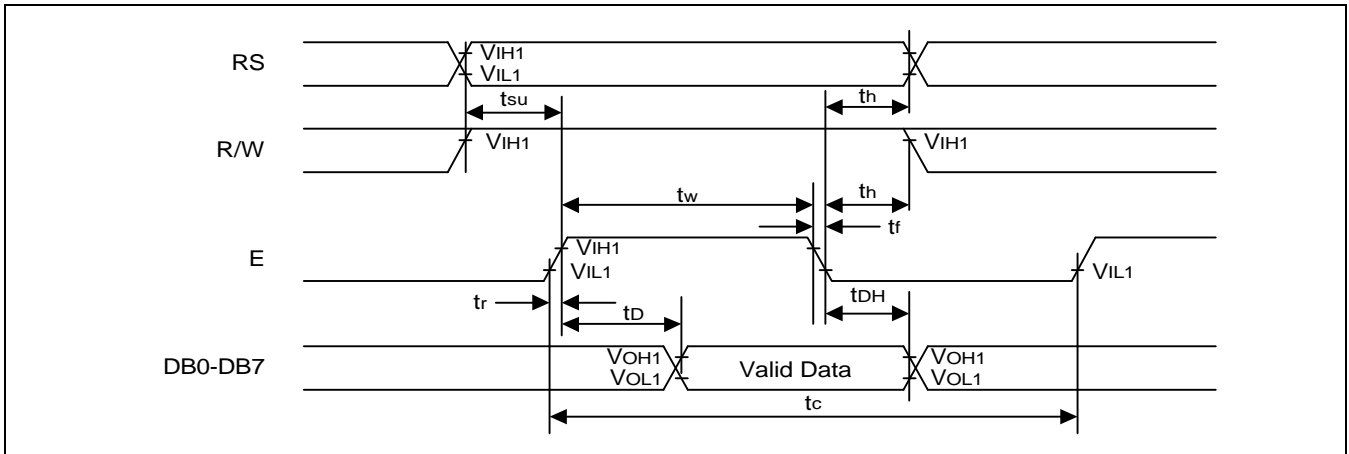| Mode	Characteristic	Symbol	Min	Typ	Max	Unit
Interface Mode with Extension Driver (refer to Figure-8)	Clock Pulse Width (High, Low)	tw	800	-	-	ns
	Clock Rise / Fall Time	t_R, t_F	-	-	25	
	Clock Setup Time	tsu1	500	-	-	
	Data Setup Time	tsu2	300	-	-	
	Data Hold Time	t_{DH}	300	-	-	
	M Delay Time	t_{DM}	-1000	-	1000	
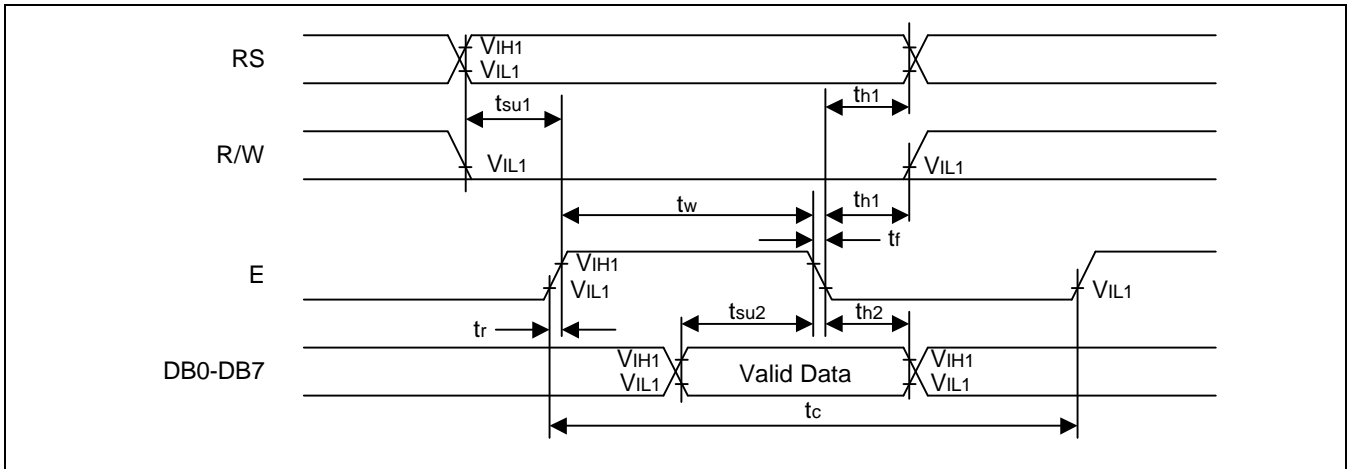
Figure 6. Write Mode Timing Diagram
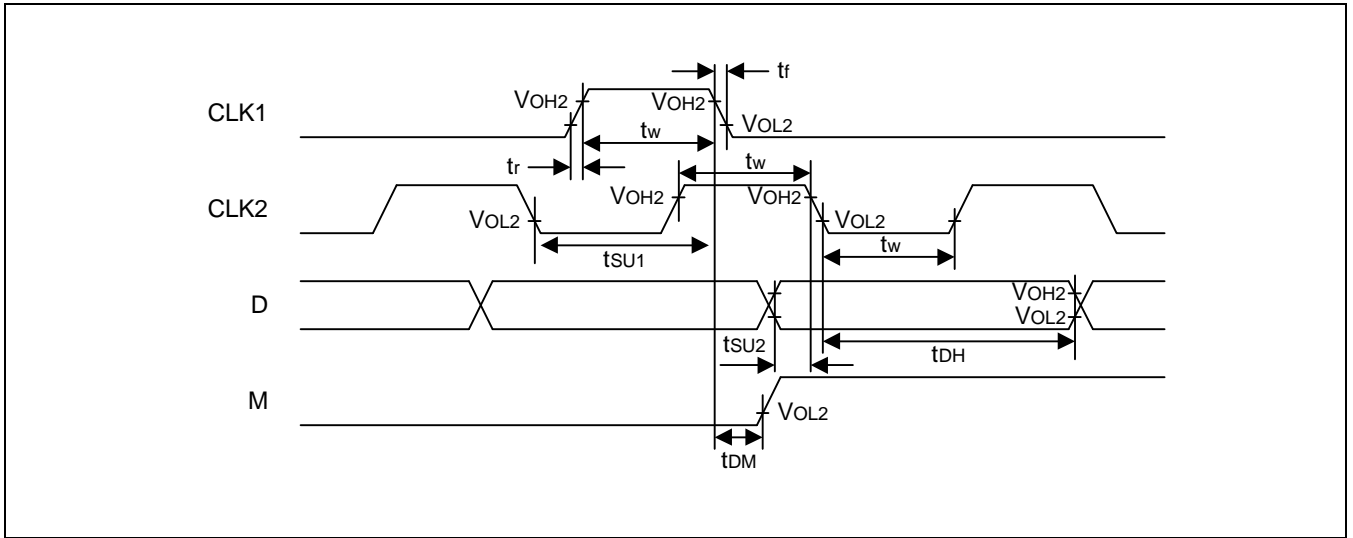

Figure 7. Read Mode Timing Diagram

Figure 8. Interface Mode with Extension Driver Timing Diagram