Homework 7

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Summary

To implement this module, I broke down the problem into a couple of smaller aspects and approached each aspect individually. The first aspect was designing the top-level modules for each of the modules to understand what signals we want for each module. From there each module was created individually based on the functionality focusing on which ones are majority asynchronous logic, versus synchronous logic.

Testing Process

The testing process was a little tricky for this portion mainly due to the fact that it would be nearly impossible to check for signal accuracy using a test bench. For testing I simply utilized a test pattern of checkerboard which helps to showcase the size and then counted the boxes to ensure that no portion of the test-pattern was cutoff. There was no real debugging since the system operated as expected after all syntax issues were fixed.

Clock

Pixel Clock

Calculated: $PixelClock = (HorizontalSize) * (VerticalSize) * (RefreshRate) = 800 * 525 * 60 = 25.2MHz$

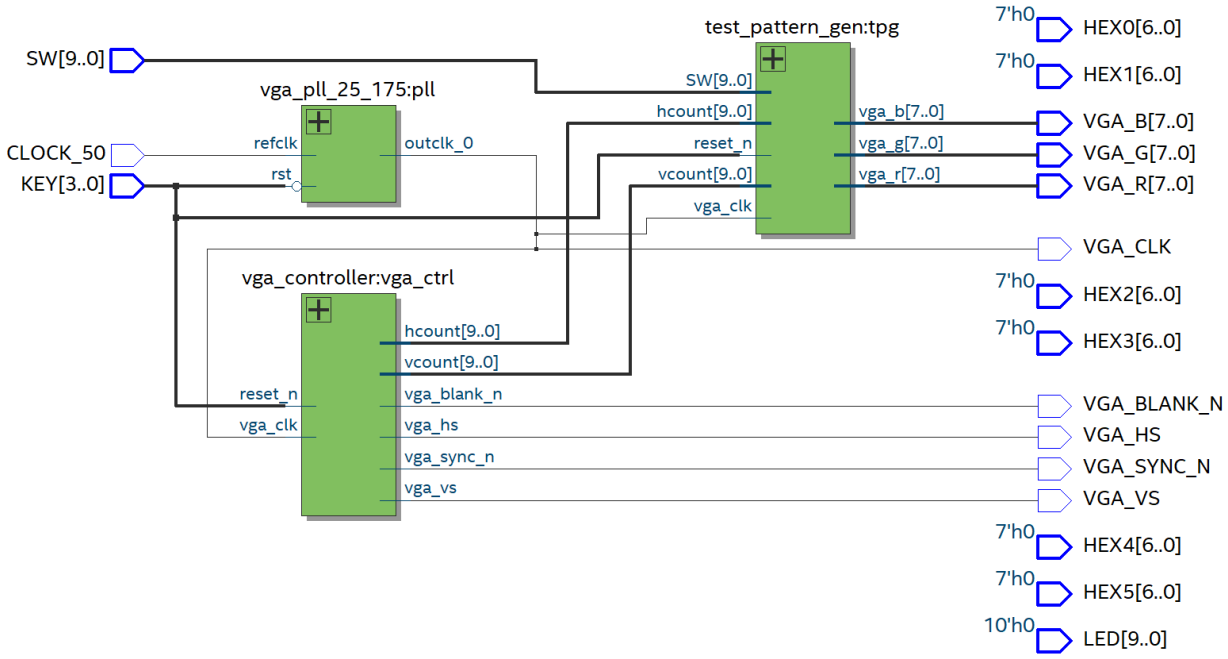
Industry Standard: 25.175MHz [1]

The pixel clock is a reference to the clock used to send over pixel information via the VGA cable. At each clock information for one pixel is sent over, and that rate is determined based on the pixel clock. By changing the pixel clock frequency, we don't see any noticeable difference between our calculated version and the industry standard. This is because we are simply changing the refresh rate. Theoretically if you change the clock frequency to be really slow you will see the monitor refresh in real time each pixel at a time. When put into practice the monitor was unable to recognize the signal and through nothing was connected. This may be due to the fact that a newer monitor was used instead of the classic CRTs. It could also be due to a clock that was too slow for the system to properly operate.

Frame Clock

Frame clock is a reference to the rate at which the entire screen is updated. This can typically also be referenced as the refresh rate. For our system this would be roughly 60 FPS (dependent on if the industry standard or our calculated clock frequency is used for the pixel clock). The pixel clock and frame clock are directly related to one another. Lower frame clock means the screen is updated less. If it is too low the eye will start to see the refresh happening.

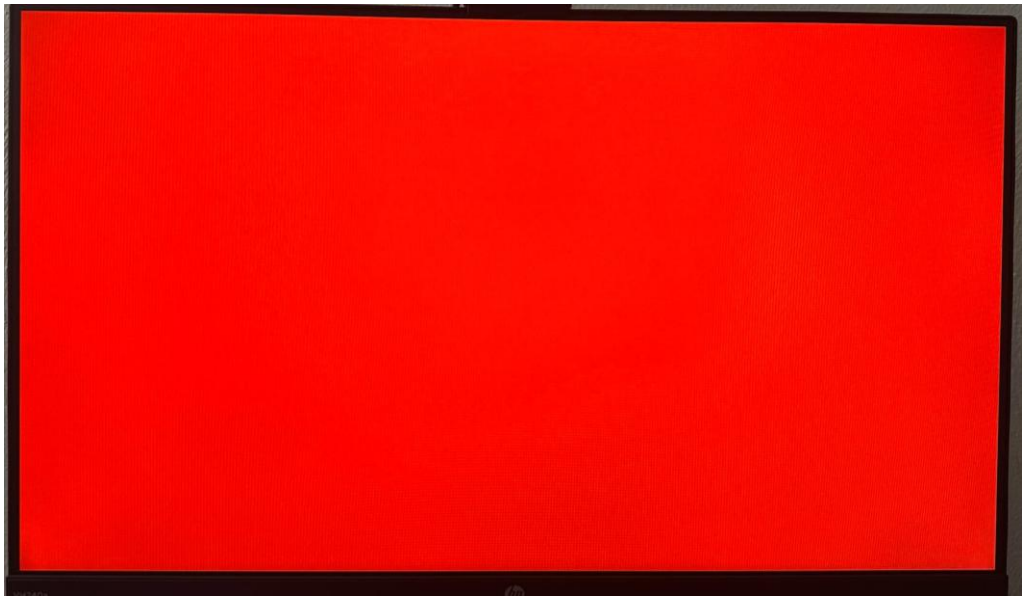
RTL Schematic



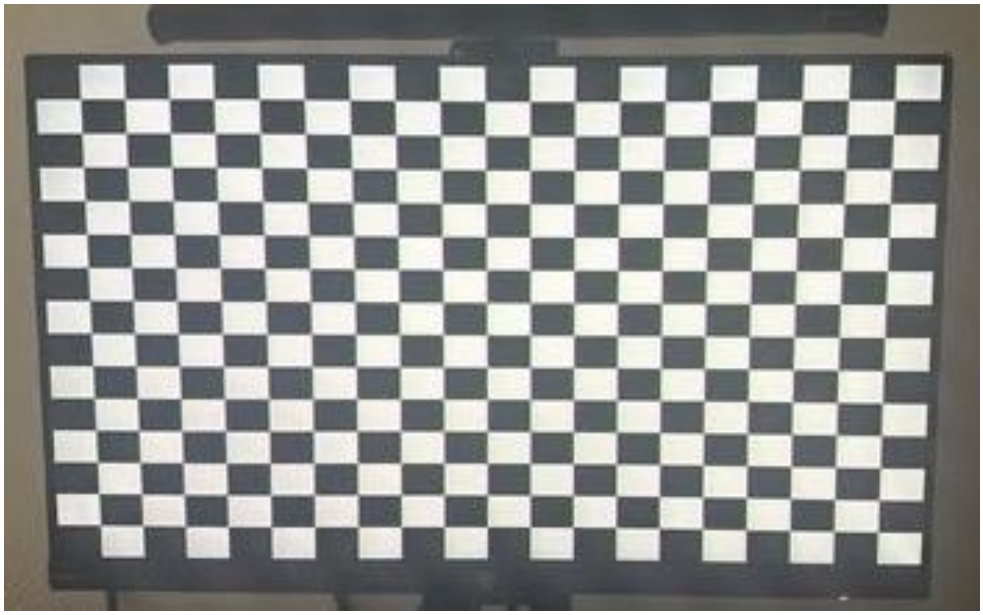
High level RTL schematic showing the overall design for the vga system.

Test Pattern

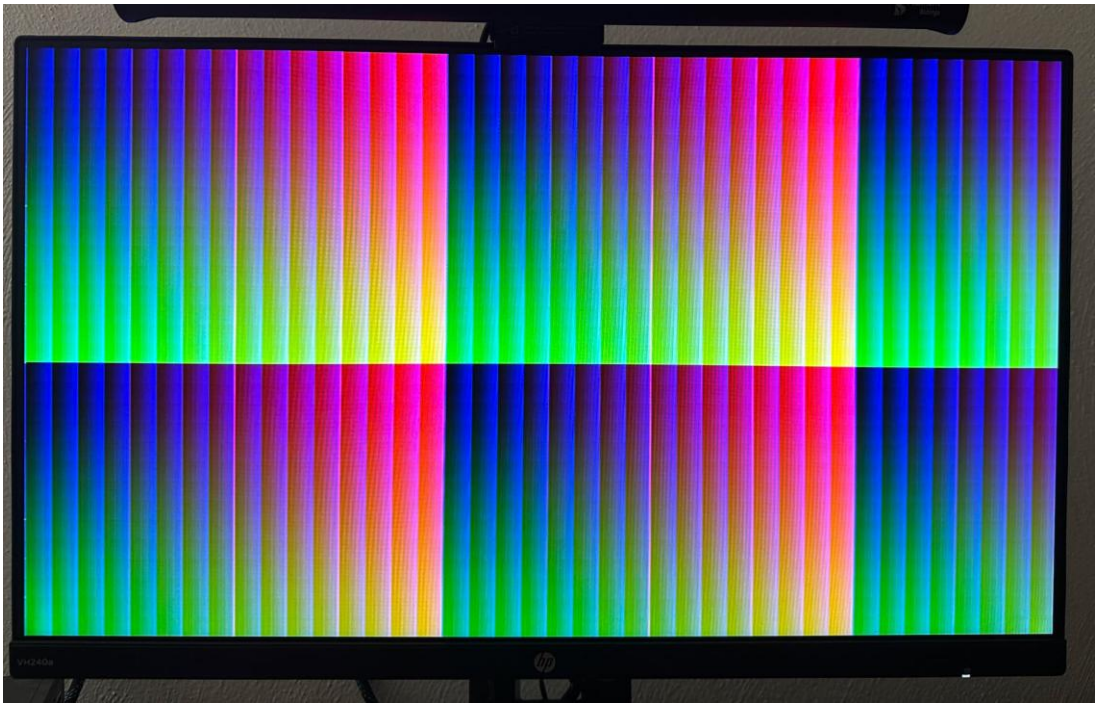
The test patterns use a priority encoder schema with SW[0] having the highest priority. The patterns are shown below.



SW[0] is high



SW[1] is high



SW[2] is high

Default (SW 0-2 not high)

The test cases are used to help ensure different patterns can be displayed as well as different color patterns.

Sources

1. http://www.tinyvga.com/vga-timing