EE 330
Homework Assignment 4
Fall 2019 (Due Friday Sept 20)

Problem 1 3.1 of Weste and Harris (WH)

Problem 2 3.2 of WH

Problem 3 If a transistor of length 7nm and width 14nm has a gate oxide thickness of 25A°, how many silicon dioxide molecules will be needed for the gate oxide?

Problem 4 What is the resistance in an aluminum interconnect that is 200μm long, 60nm wide, and 60nm thick.

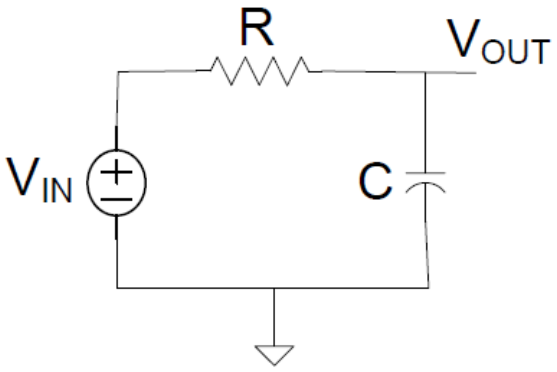
Problem 5 3.5 of WH

Problem 6 How many 12 inch wafers can be obtained from a 2m silicon pull? Assume the kerf width when a wire saw is used is to cut the wafers is 150μm. In solving this problem, state and use a typical value for the wafer thickness.

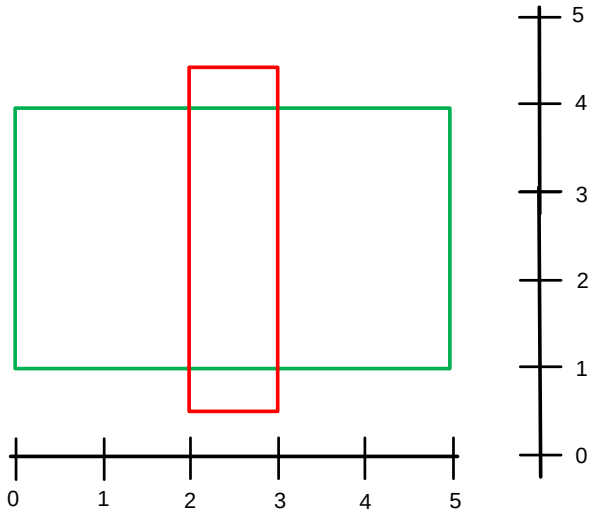
Problem 7 A first-order RC filter is shown. The 3-dB band edge of this filter is given by $\omega_{3dB} = \frac{1}{RC}$. Assume Poly 1 with a silicide block is used to make the resistor and the capacitor is a Poly Insulator Substrate capacitor. This filter is to be fabricated in the ON 0.5μ CMOS process that is characterized by the parameters attached to this assignment.

a) Design this circuit and estimate the area required to implement this filter in your design if the 3dB band edge is to be located at 2K Hz and the capacitor value is 2 pF.

b) If the resistor is too big or the capacitor is too big, the area required to realize this filter becomes very large. Determine the value of R and C that will minimize the total area and compare the area required for the "minimal area" design with that you required in part a). Use a serpentine layout for the resistor.



Problem 8 Consider the layout of a transistor shown below where red is polysilicon and green is n-active. Rulers with dimensions in µm are shown.



a) What is the drawn length and width of the transistor?
b) Assume positive photoresist is used pattern the polysilicon region to protect it during the polysilicon etch. If the photoresist is under-exposed so that the edges move by 0.1µm from the desired location and the photoresist development is perfect, and the polysilicon is under-etched so that the edges move by 0.1µm, what will be the actual length and width of the transistor? (neglect any lateral diffusion that may occur)
c) Repeat part b) if negative photoresist is used.

Problem 9 An aluminum interconnect 250µm long and 2µm wide has a measured resistance of 25Ω. Determine the thickness of the aluminum interconnect and the sheet resistance.

Problem 10 If a copper interconnect has the same thickness and the same width as the aluminum interconnect in Problem 9, how long could it be if it also had the same resistance?

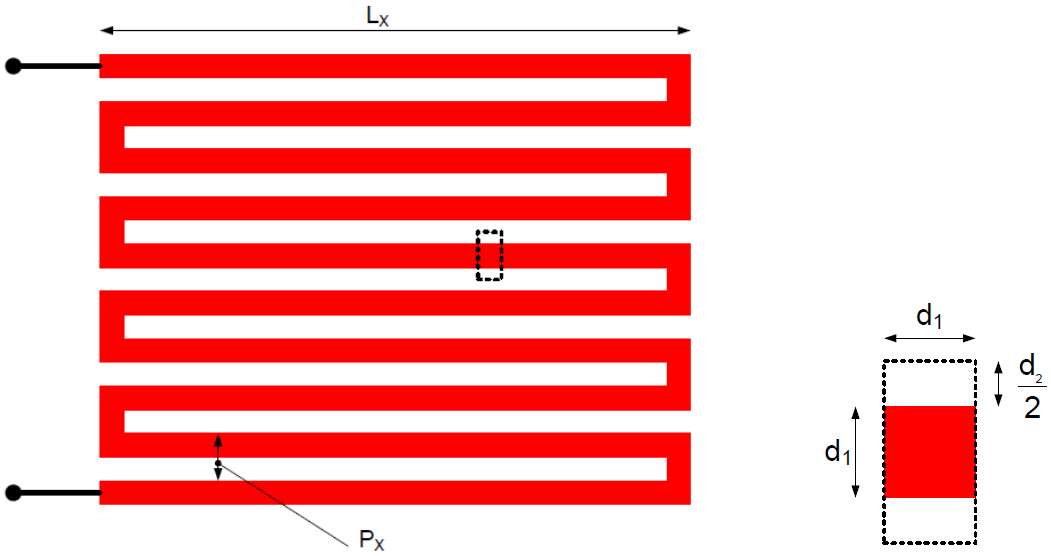
Problem 11 Thermal oxide growth of field oxide causes the wafer surface to become somewhat nonplanar. If 5000Å of field oxide is thermally grown, what is the difference in the thickness of the wafer between regions where field oxide is present and where it is absent. In solving this problem, state and use a typical value for the wafer thickness.

Problem 12 **Compare the area required** for the layout of a 5K resistor using Poly 1 to that required using p+ diffusion in the ON 0.5µ CMOS process. Use a serpentine

layout with minimum width and minimum spacing for the resistive elements and be sure that you meet the design rules of the process.

Serpentine layout:

A serpentine (sometimes termed "meander")layout is shown below. For large valued resistors, the length L_X is generally much larger than the pitch, P_X. The dashed box which includes exactly one square of resistance is expanded below. The dimension d_1 corresponds to the minimum width of the "one-square" resistor and d_2 to the minimum spacing between the serpentine resistor stripes.



Problem 13 and 14 Use Modelsim to create a Thermometer Decoder very similar to last week. The Thermometer Decoder will have 15 inputs and 4 decoded outputs. Create a test bench to verify your design. Include screenshots of your Verilog code and simulation waveforms. Use the truth table below as a guide. Also, give at least one example of how this Thermometer Decoder could be used in Analog Design.

Input														
t14	t13	t12	t11	t10	t9	t8	t7	t6	t5	t4	t3	t2	t1	t0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Decoded Output			
b3	b2	b1	b0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

MOSIS WAFER ELECTRICAL TESTS

RUN: V37P — VENDOR: AMIS (ON-SEMI)
TECHNOLOGY: SCN05 — FEATURE SIZE: 0.5 microns
Run type: SHR

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SMSCN3ME06_ON-SEMI

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.76	-0.90	volts
SHORT	20.0/0.6			
Idss		466	-255	uA/um
Vth		0.65	-0.88	volts
Vpt		13.1	-12.2	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.67	-0.94	volts
Vjbkd		10.9	-11.8	volts
Ijlk		242.7	<50.0	pA
Gamma		0.49	0.56	V^0.5
K' (Uo*Cox/2)		57.8	-18.9	uA/V^2
Low-field Mobility		472.03	154.35	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

COMMENTS:

PROCESS PARAMETERS	N+	P+	N_W	_U	POLY	PLY2_HR	POLY2	M1	UNITS
Sheet Resistance	82.4	106.7	814.1	23.2	1076		40.8	0.09	ohms/sq
Contact Resistance	59.6	152.5		16.0			26.0		ohms
Gate Oxide Thickness	141								angstrom

PROCESS PARAMETERS	M2	M3	N_W	UNITS
Sheet Resistance	0.09	0.05	808	ohms/sq
Contact Resistance	0.84	0.82		ohms

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	416	710	86		29	12	8	91	aF/um^2
Area (N+active)			2456		37	17	12		aF/um^2
Area (P+active)			2362						aF/um^2
Area (poly)				922	64	16	9		aF/um^2
Area (poly2)					58				aF/um^2
Area (metal1)						32	12		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	345	236			51	34	26		aF/um
Fringe (poly)					70	39	28		aF/um
Fringe (metal1)						49	33		aF/um
Fringe (metal2)							55		aF/um
Overlap (N+active)			191						aF/um
Overlap (P+active)			234						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.29	volts
Vol (100 uA)	2.0	0.47	volts
Voh (100 uA)	2.0	4.48	volts
Vinv	2.0	2.47	volts
Gain	2.0	-17.59	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		103.03	MHz
D256_WIDE (31-stg,5.0V)		158.86	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.48	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		0.99	uW/MHz/gate

COMMENTS: SUBMICRON

V37P SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

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* DATE: Oct 17/13
* LOT: v37p                  WAF: 1003
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 1.41E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = 0.6176544
+K1      = 0.9137986      K2      = -0.1071877     K3      = 22.288867
+K3B     = -9.7485086     W0      = 2.658488E-8    NLX     = 1E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.8309419      DVT1    = 0.3317542      DVT2    = -0.5
+U0      = 460.0124125    UA      = 2.759471E-13   UB      = 1.603084E-18
+UC      = 3.089014E-12   VSAT    = 1.840576E5     A0      = 0.5615191
+AGS     = 0.1204319      B0      = 1.941274E-6    B1      = 5E-6
+KETA    = -2.797385E-3   A1      = 2.420581E-5    A2      = 0.3164714
+RDSW    = 1.115544E3     PRWG    = 0.0828351      PRWB    = 0.0311852
+WR      = 1              WINT    = 2.526685E-7    LINT    = 7.469087E-8
+XL      = 1E-7           XW      = 0              DWG     = -1.032244E-8
+DWB     = 1.914595E-8    VOFF    = -6.986376E-5   NFACTOR = 0.8533219
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.045973E-3    ETAB    = -3.21453E-4
+DSUB    = 0.0833302      PCLM    = 2.3615569      PDIBLC1 = 9.500103E-5
+PDIBLC2 = 1.863456E-3    PDIBLCB = 0.0644698      DROUT   = 1.39184E-3
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+PSCBE1  = 3.853855E8     PSCBE2  = 4.115782E-6    PVAG    = 0
+DELTA   = 0.01           RSH     = 82.4           MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 1.91E-10       CGSO    = 1.91E-10       CGBO    = 1E-9
+CJ      = 4.131634E-4    PB      = 0.8399766      MJ      = 0.4305505
+CJSW    = 3.400072E-10   PBSW    = 0.809471       MJSW    = 0.1977865
+CJSWG   = 1.64E-10       PBSWG   = 0.8            MJSWG   = 0.2019414
+CF      = 0              PVTH0   = -0.028514      PRDSW   = 114.6437024
+PK2     = -0.0768747     WKETA   = -0.0138828     LKETA   = 1.62687E-3      )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 1.41E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.9152268
+K1      = 0.553472       K2      = 7.871921E-3    K3      = 8.5645893
+K3B     = 0.5506188      W0      = 1E-8           NLX     = 1.006451E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.4716221      DVT1    = 0.1854949      DVT2    = -0.3
+U0      = 201.3603195    UA      = 2.48572E-9     UB      = 1.005454E-21
+UC      = -1E-10         VSAT    = 1.578444E5     A0      = 0.8192884
+AGS     = 0.1111278      B0      = 5.743519E-7    B1      = 6.088988E-8
+KETA    = -4.865785E-3   A1      = 5.800723E-4    A2      = 0.3229711
+RDSW    = 3E3            PRWG    = -0.0219603     PRWB    = -0.0910566
+WR      = 1.01           WINT    = 2.247043E-7    LINT    = 9.979797E-8
+XL      = 1E-7           XW      = 0              DWG     = 2.080226E-9
+DWB     = -1.38669E-8    VOFF    = -0.0295318     NFACTOR = 0.5872216
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 4.979072E-4    ETAB    = -0.2
+DSUB    = 1              PCLM    = 2.3970968      PDIBLC1 = 0.0961044
+PDIBLC2 = 4.073922E-3    PDIBLCB = -0.0315594     DROUT   = 0.2897615
+PSCBE1  = 8E10           PSCBE2  = 8.966681E-8    PVAG    = 0.0149129
+DELTA   = 0.01           RSH     = 106.7          MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.34E-10       CGSO    = 2.34E-10       CGBO    = 1E-9
+CJ      = 7.086018E-4    PB      = 0.8698912      MJ      = 0.4856488
+CJSW    = 2.340641E-10   PBSW    = 0.8329387      MJSW    = 0.2034305
+CJSWG   = 6.4E-11        PBSWG   = 0.8            MJSWG   = 0.2261452
+CF      = 0              PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 0.0120657      LKETA   = -0.0104163      )
*
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