EE330 Lab 12
Section 5, 8:00 am

Design and Simulation of Digital Circuits using
Hardware Description Languages

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1.1 Simulating Behavioral Code

This section focused on creating a verilog program that mirrors a schematic made in cadence, using it to compare the effort taken to create this one vs one in cadence.

```verilog
//----------------------------------------
//
// Boolean function for lab 12
// Implementing function:
// !ABC + A!BC +AB!C
//
//----------------------------------------

module boolean_function(
      i_A,
      i_B,
      i_C,
      o_F
);

      input i_A, i_B, i_C;
      output o_F;
      wire s_gate1, s_gate2, s_gate3;

      and (s_gate1, !i_A, i_B, i_C);
      and (s_gate2, i_A, !i_B, i_C);
      and (s_gate3, i_A, i_B, !i_C);

      or  (o_F, s_gate1, s_gate2, s_gate3);
endmodule
```
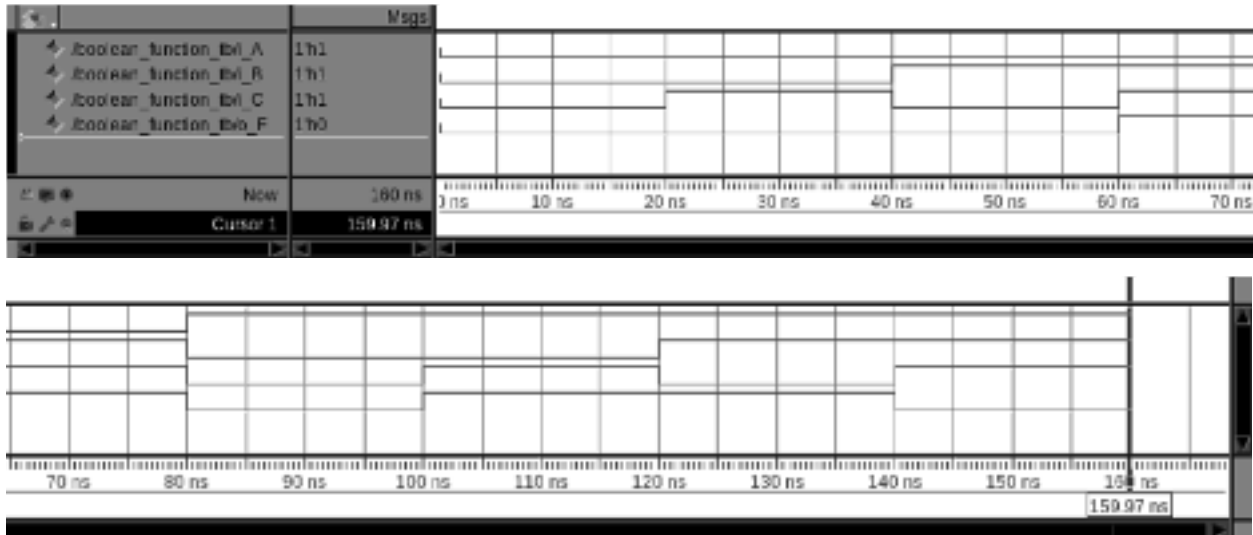
```verilog
`timescale 1 ns/10 ps
module boolean_function_tb;

    reg i_A, i_B, i_C;
    wire o_F;

    localparam period = 20;

    boolean_function DUT(.i_A(i_A), .i_B(i_B), .i_C(i_C),
.o_F(o_F));

    initial
    begin
        i_A = 0;
        i_B = 0;
        i_C = 0;
        #period;

        i_A = 0;
        i_B = 0;
        i_C = 1;
        #period;

        i_A = 0;
        i_B = 1;
```

```verilog
        i_C = 0;
        #period;

        i_A = 0;
        i_B = 1;
        i_C = 1;
        #period;


        i_A = 1;
        i_B = 0;
        i_C = 0;
        #period;

        i_A = 1;
        i_B = 0;
        i_C = 1;
        #period;

        i_A = 1;
        i_B = 1;
        i_C = 0;
        #period;

        i_A = 1;
        i_B = 1;
        i_C = 1;
        #period;
    end
endmodule
```
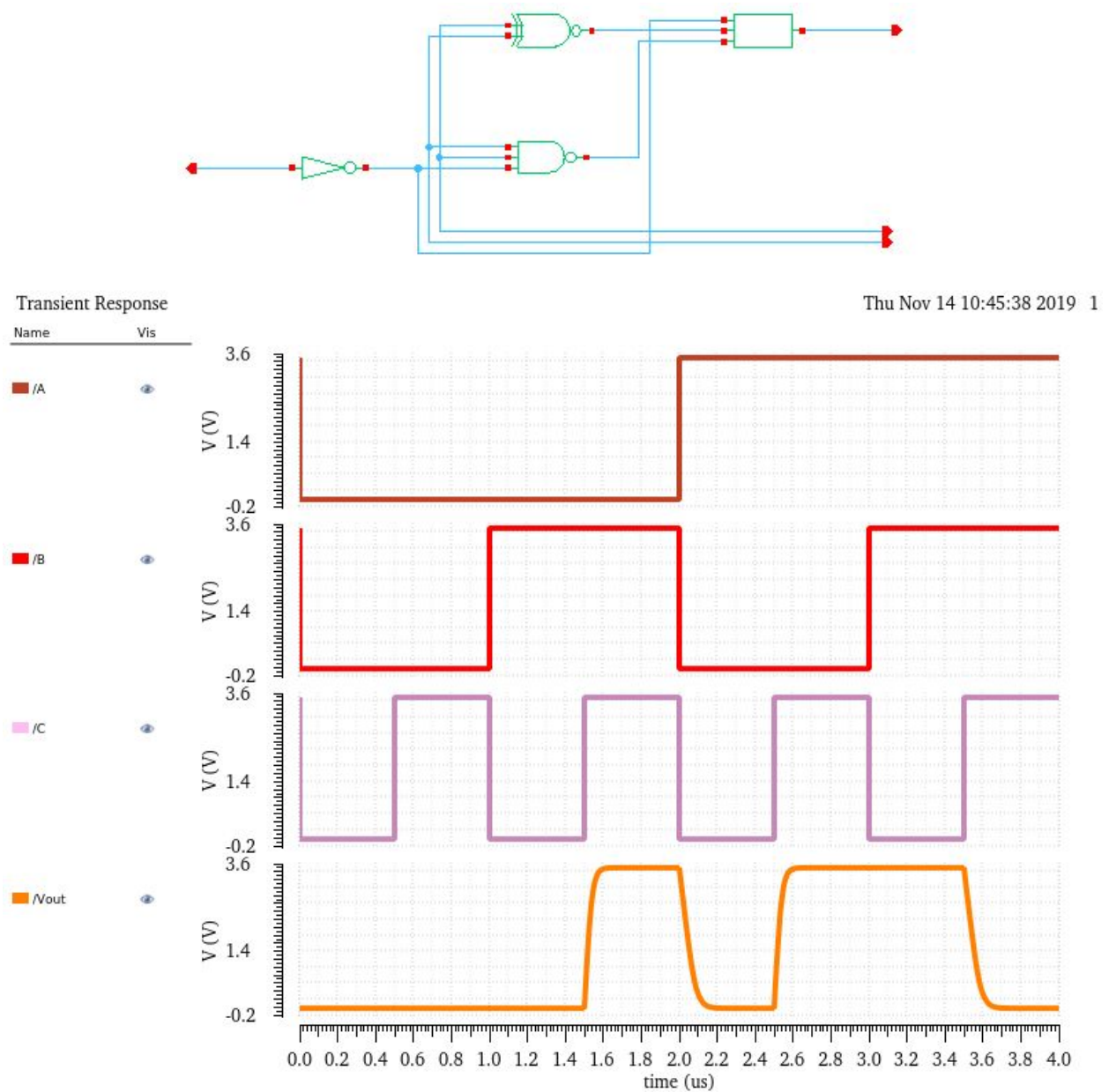
# Part 2: Verilog Synthesis with RTL Compiler

After importing the necessary libraries, we imported the created verilog into cadence and used it to create a schematic.

The created schematic with its test waveform is shown below:

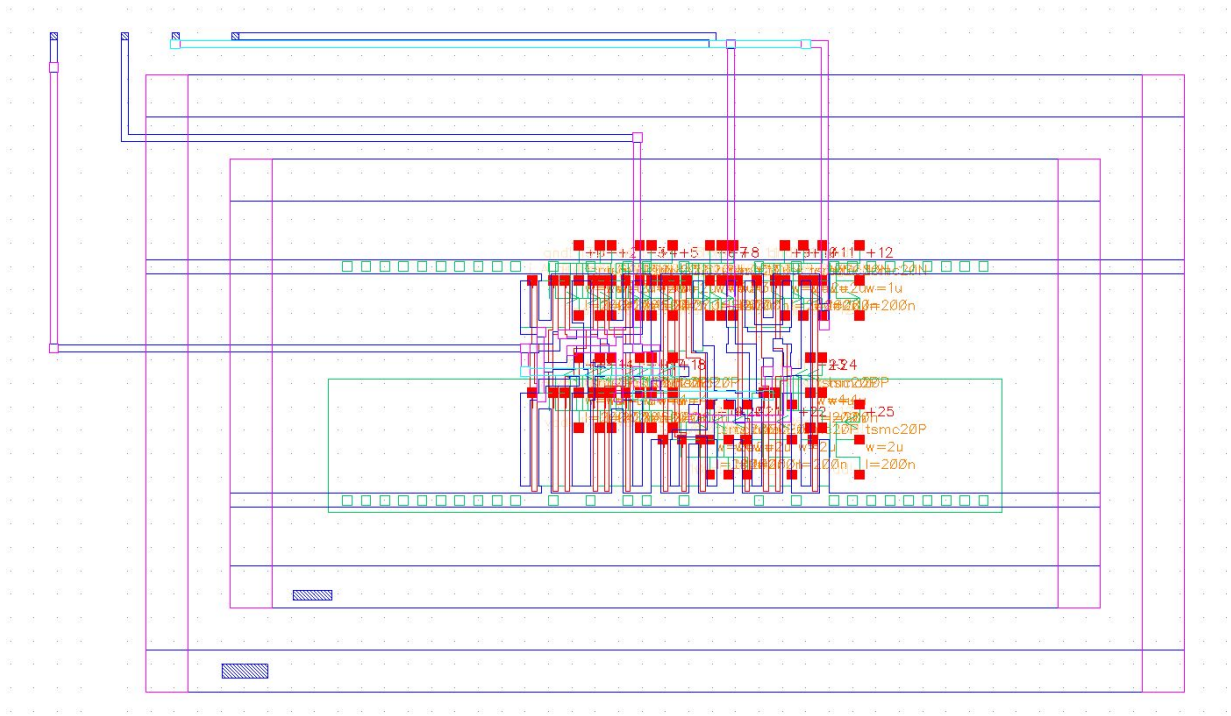# Part 3: Layout of Digital Circuits with Innovus

This section showed the simplicity of using Innovus to convert a schematic into a layout. Using some pretty fancy settings, we set two rings for power, then connected pins.
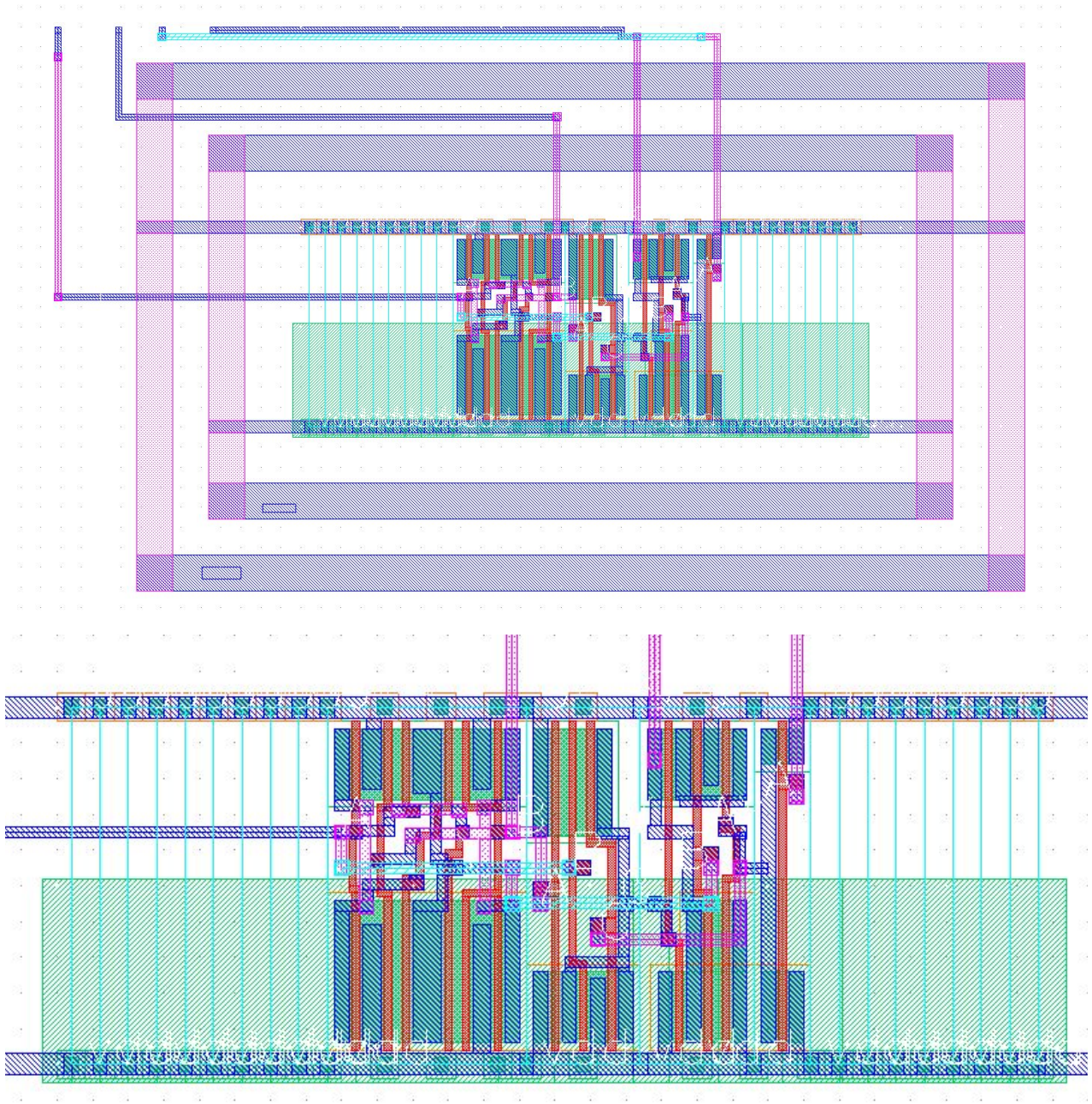
Part 4: Import the layout into Cadence.

Once everything was set up, we extracted the previous layout and ensured it conformed to DRC and LVS.


```
DRC started at Thu Nov 14 11:21:03 2019

Validating hierarchy instantiation for:
library: boolean_function
cell:    boolean_function
view:    layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu Nov 14 11:21:03 2019
   completed ....Thu Nov 14 11:21:03 2019
   CPU TIME = 00:00:00   TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "boolean_function layout"   *********
   Total errors found: 0
```

```
Compiling Diva LVS rules...

    Net-list summary for /home/sgordon4/ee330/LVS/layout/netlist
       count
        19                nets
        6                 terminals
        13                pmos
        13                nmos

    Net-list summary for /home/sgordon4/ee330/LVS/schematic/netlist
       count
        19                nets
        6                 terminals
        13                pmos
        13                nmos


    Terminal correspondence points
    N13         N1          gnd!
    N18         N8          i_A
    N17         N7          i_B
    N15         N6          i_C
    N16         N2          o_F
    N14         N0          vdd!

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout   schematic
                               instances
          un-matched            0         0
          rewired               0         0
          size errors           0         0
          pruned                0         0
          active                26        26
          total                 26        26

                                 nets
          un-matched            0         0
          merged                0         0
          pruned                0         0
          active                19        19
          total                 19        19

                              terminals
          un-matched            0         0
          matched but
          different type        0         0
          total                 6         6


Probe files from /home/sgordon4/ee330/LVS/schematic
```