EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _

Exam 2
Spring 2018

Instructions: This is a 50-minute exam. Students may bring 2 pages of notes (front and back) to this exam. There are 6 short question is worth 2 points each, two short questions worth 4 points each, and 5 problems worth 16 points each. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$ and $V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$ and $V_{Tp} = -0.5V$. Correspondingly, assume all npn BJT transistors have model parameters $J_S = 10^{-14}A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S = 10^{-14}A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. If parameters are needed for CMOS process characterization beyond what is given, use the measured parameters from the TSMC 0.18μ process given below as model parameters. Assume all diodes are characterized by the model parameters $J_{SX}=0.5A/\mu m^2$, $V_{G0}=1.17V$, and $m=2.3$.

1. (2 pts) How many small-signal parameters are required for the small-signal model of a nonlinear one-port circuit?

2. (2 pts) The diode equation is much more difficult to work with than the simpler piecewise-linear diode model (open circuit when not conducting and a dc voltage source of 0.6V when conducting). What is a quick way to check and see if the simpler piecewise-linear model can be used when analyzing a diode circuit?

3. (2pts) The parameters {$\mu$, $C_{OX}$, $V_{TH}$, $\lambda$, $\gamma$, and $\varphi$ } were used to characterize the operation of a MOSFET. Which of these parameters corresponds to the Early Voltage parameter, $V_{AF}$, in the bipolar transistor?

4. (2 pts) In a CMOS process that has a single polysilicon layer, it can be observed that after processing, polysilicon appears either on top of thin oxide or on top of thick oxide. What must the designer do to place polysilicon on top of thin oxide?

5. (2 pts) The base in a vertical npn transistor is very thin. What is the major reason that the based region is intentionally made very thin?

6. (2pts) The isolation diffusion is used to provide electrical separation of devices in a bipolar process. What is the counterpart method in a bulk CMOS process for providing electrical separation of devices?

7. (4 pts) An inexperienced designer was told that if Metal and Polysilicon in a CMOS process overlap, the metal will always appear on top of polysilicon. He also observed that during layout it was common to first layout the polysilicon and then do the interconnects with metal thus placing metal on top of the polysilicon. This inexperienced designer figured out a clever way to place metal under polysilicon that he thought others had overlooked and that this could be done during layout without any changes in the process flow. What he proposed was to first layout the metal and then layout the polysilicon this placing polysilicon on top of metal. He indicated that this process was more tedious because more planning needed to go into the layout process to be sure that the metal was in the right place when polysilicon was added later. After spending a lot of time following this method of layout where all metal was placed before any polysilicon was placed, a design was completed. After fabrication, will the circuit have metal under polysilicon as planned by the clever but inexperienced designer? If not, what will be observed?

8 (4 pts) If a BJT is operating in the Forward Active region and it is observed that the emitter current is 5mA and the base current is 1mA, what is the "β" for the transistor?

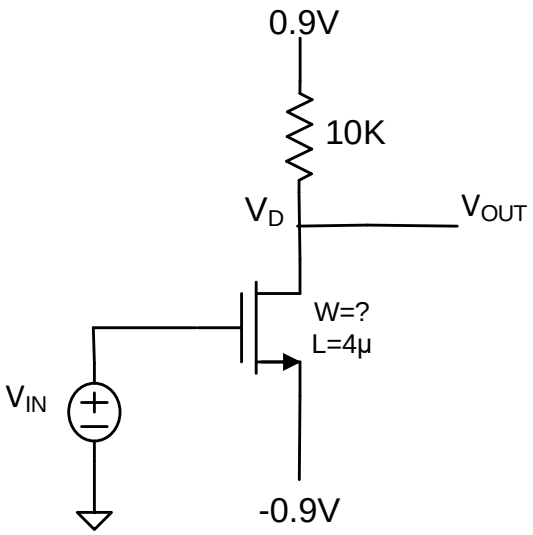
**Problem 1** (16 pt) Consider the following circuit.

a) Draw the small signal equivalent circuit assuming the MOS transistor is operating in the saturation region

b) Give the small-signal voltage gain in terms of the small-signal model parameters assuming the MOS transistor is operating in the saturation region

c) Determine W so that the quiescent output voltage is 0V

d) Determine the small-signal voltage gain with the value of W determined in part c)



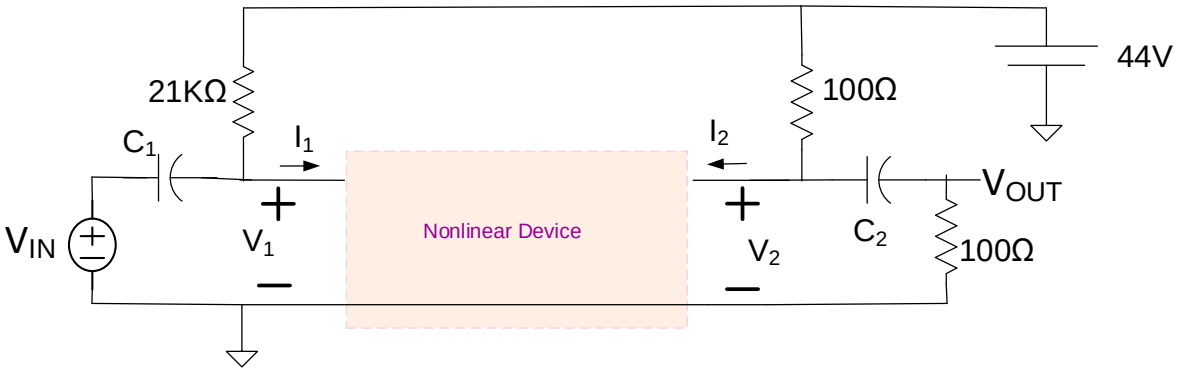
**Problem 2** Consider the circuit shown below. Assume the capacitors are large and also assume that $V_{IN}$ is a small-signal input. Assume further that the nonlinear device (depicted in the box below) that is characterized by the equations

$$I_1 = 10^{-3} V_1$$

$$I_2 = \begin{cases} 10^{-2} V_1 & for\ V_1 < 1V \quad (termed\ region\ 1) \\ 10^{-2} V_1^3 \left(1 + \dfrac{V_2}{10}\right) & for\ V_1 > 1V \quad (termed\ region\ 2) \end{cases}$$

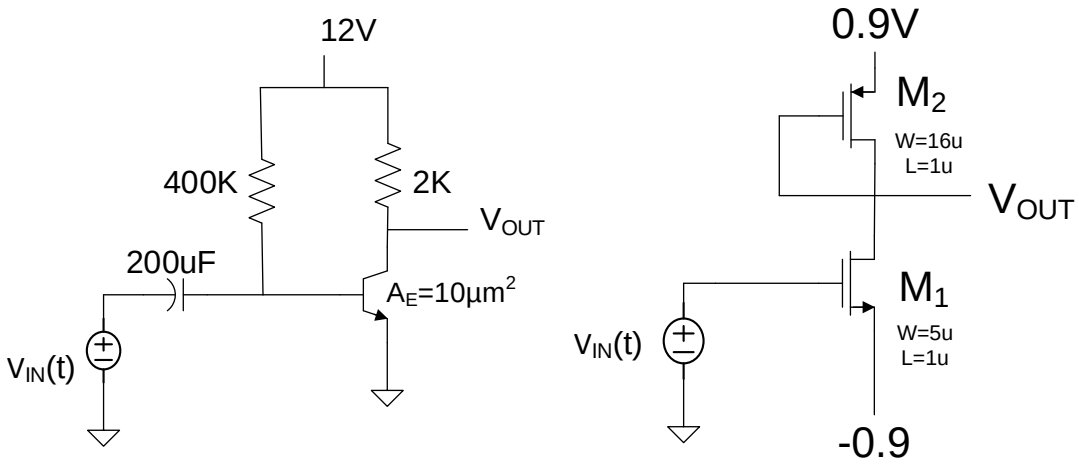
(the numerical coefficients in the model have dimensions to make the expressions shown consistent but are not shown for notational convenience)

a) Develop a small-signal model of this nonlinear device in terms of the "y" parameters when operating in region 2 in terms of the quiescent values for $V_1$ and $V_2$.
b) Give an equivalent circuit for the small-signal model
c) Determine $V_{1Q}$ and $V_{OUTQ}$
d) Determine the small-signal voltage gain in terms of the circuit components and the y parameters of the nonlinear device
e) (extra credit) Determine the numerical value of the voltage gain.



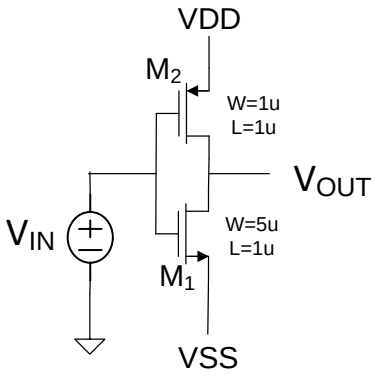
**Continue solution to Problem 2 here if additional space is needed**

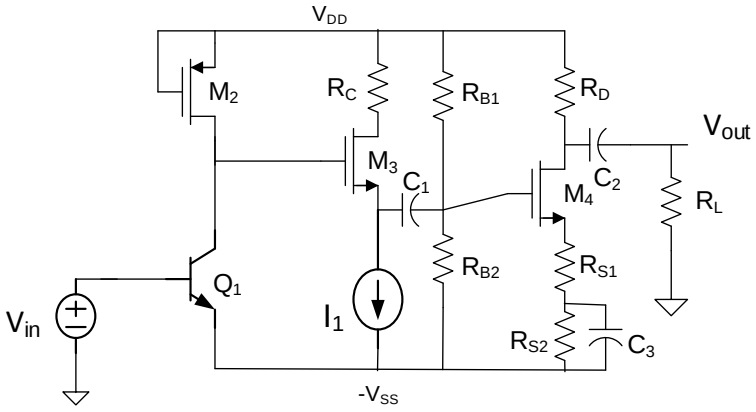
**Problem 3** (16 pts) Determine the quiescent output voltage for the following two circuits. Assume the small-signal inputs are very small. Use the model parameters for the devices given at the top of this exam.



**Problem 4** (16 pts) Design a circuit using only MOS transistors that has an output voltage of 2V. You have available any number of MOS transistors and a single DC 5V dc power supply. Be sure to give the sizes of all transistors. Assume the MOS transistors are from a 5V process and have model parameters $\mu_n C_{OX} = 100\mu A/V^2$ and $V_{Tn} = 0.75V$, and all p-channel transistors have model parameters $\mu_p C_{OX} = 30\mu A/V^2$ and $V_{Tp} = -0.75V$.

**Problem 5** (16 pts) Draw the small-signal equivalent circuit for the following two amplifier structures. Assume the capacitors are large, all MOS transistors are operating in the Saturation region, and all bipolar transistors are operating in the Forward Active region. Do not solve.



MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

| TRANSISTOR PARAMETERS | W/L | N-CHANNEL | P-CHANNEL | UNITS |
|---|---|---|---|---|
| MINIMUM | 0.27/0.18 | | | |
| Vth | | 0.50 | -0.51 | volts |
| SHORT | 20.0/0.18 | | | |
| Idss | | 547 | -250 | uA/um |
| Vth | | 0.51 | -0.51 | volts |
| Vpt | | 4.8 | -5.6 | volts |
| WIDE | 20.0/0.18 | | | |
| Ids0 | | 14.4 | -4.7 | pA/um |
| LARGE | 50/50 | | | |
| Vth | | 0.43 | -0.42 | volts |
| Vjbkd | | 3.1 | -4.3 | volts |
| Ijlk | | <50.0 | <50.0 | pA |
| K' (Uo*Cox/2) | | 175.4 | -35.6 | uA/V^2 |
| Low-field Mobility | | 416.52 | 84.54 | cm^2/V*s |

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

| Design Technology | XL (um) | XW um) |
|---|---|---|
| SCN6M_DEEP (lambda=0.09) | 0.00 | -0.01 |
| thick oxide | 0.00 | -0.01 |
| SCN6M_SUBM (lambda=0.10) | -0.02 | 0.00 |
| thick oxide | -0.02 | 0.00 |

| FOX TRANSISTORS | GATE | N+ACTIVE | P+ACTIVE | UNITS |
|---|---|---|---|---|
| Vth | Poly | >6.6 | <-6.6 | volts |

| PROCESS PARAMETERS | N+ | P+ | POLY | N+BLK | PLY+BLK | M1 | M2 | UNITS |
|---|---|---|---|---|---|---|---|---|
| Sheet Resistance | 6.7 | 7.8 | 8.0 | 59.7 | 313.6 | 0.08 | 0.08 | ohms/sq |
| Contact Resistance | 10.6 | 11.0 | 10.0 | | | | 4.79 | ohms |
| Gate Oxide Thickness | 41 | | | | | | | angstrom |

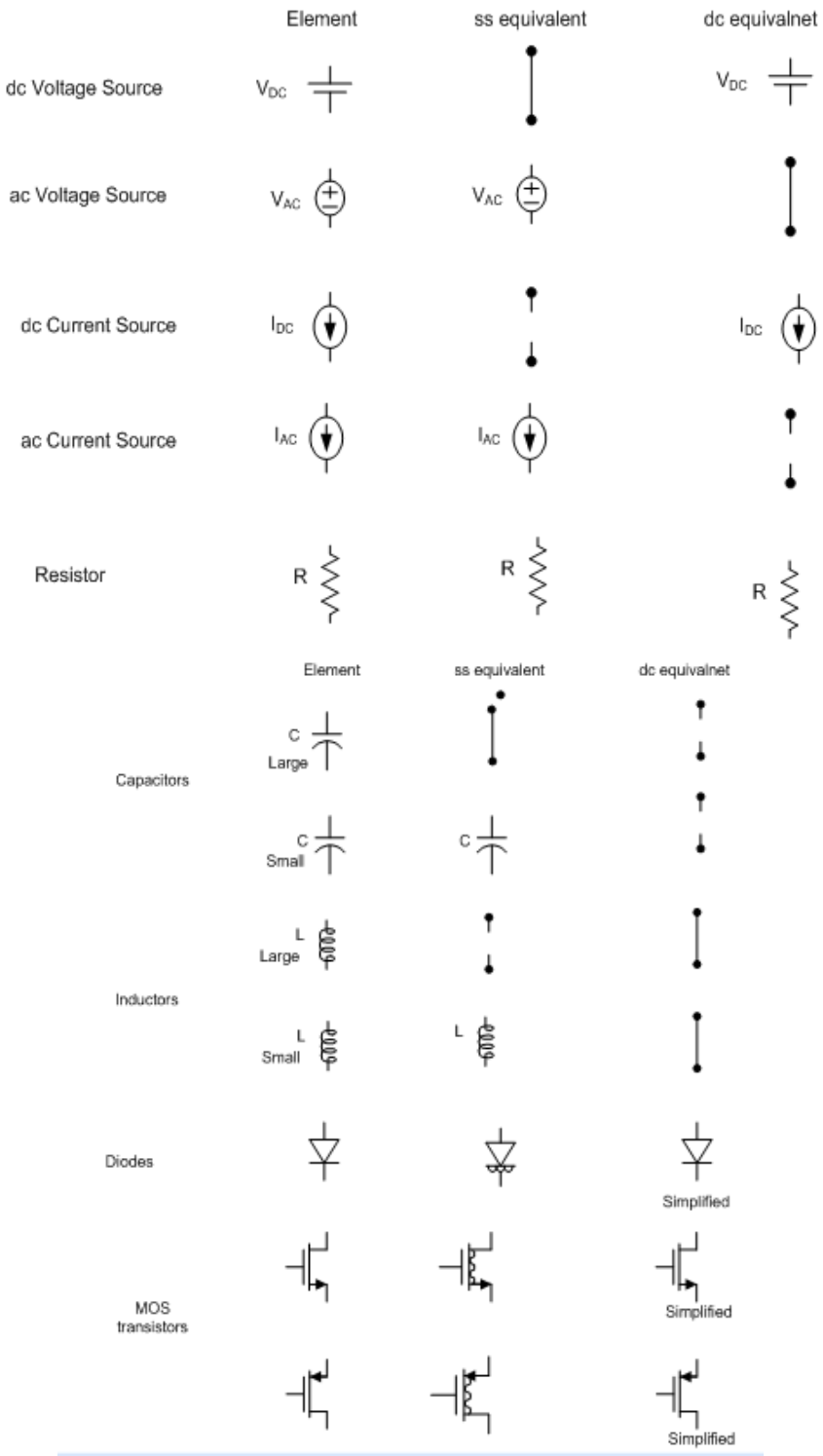
| PROCESS PARAMETERS | M3 | POLY_HRI | M4 | M5 | M6 | N_W | UNITS |
|---|---|---|---|---|---|---|---|
| Sheet Resistance | 0.08 | | 0.08 | 0.08 | 0.03 | 930 | ohms/sq |
| Contact Resistance | 9.24 | | 14.05 | 18.39 | 20.69 | | ohms |

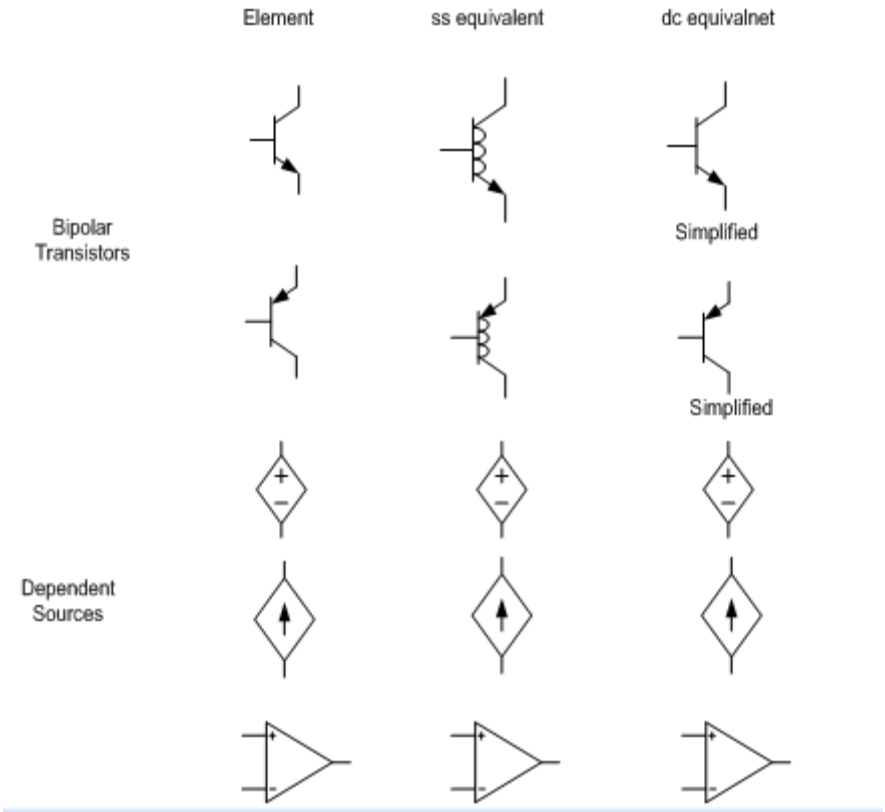
COMMENTS: BLK is silicide block.

| CAPACITANCE PARAMETERS | N+ | P+ | POLY | M1 | M2 | M3 | M4 | M5 | M6 | R_W | D_N_W | M5P | N_W | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Area (substrate) | 942 | 1163 | 106 | 34 | 14 | 9 | 6 | 5 | 3 | | 123 | | 125 | aF/um^2 |
| Area (N+active) | | | 8484 | 55 | 20 | 13 | 11 | 9 | 8 | | | | | aF/um^2 |
| Area (P+active) | | | 8232 | | | | | | | | | | | aF/um^2 |
| Area (poly) | | | | 66 | 17 | 10 | 7 | 5 | 4 | | | | | aF/um^2 |
| Area (metal1) | | | | | 37 | 14 | 9 | 6 | 5 | | | | | aF/um^2 |
| Area (metal2) | | | | | | 35 | 14 | 9 | 6 | | | | | aF/um^2 |
| Area (metal3) | | | | | | | 37 | 14 | 9 | | | | | aF/um^2 |
| Area (metal4) | | | | | | | | 36 | 14 | | | | | aF/um^2 |
| Area (metal5) | | | | | | | | | 34 | | | | 984 | aF/um^2 |
| Area (r well) | 920 | | | | | | | | | | | | | aF/um^2 |
| Area (d well) | | | | | | | | | | 582 | | | | aF/um^2 |
| Area (no well) | 137 | | | | | | | | | | | | | aF/um^2 |
| Fringe (substrate) | 212 | 235 | 41 | 35 | 29 | 21 | 14 | | | | | | | aF/um |
| Fringe (poly) | | | 70 | 39 | 29 | 23 | 20 | 17 | | | | | | aF/um |
| Fringe (metal1) | | | | 52 | 34 | | 22 | 19 | | | | | | aF/um |
| Fringe (metal2) | | | | | 48 | 35 | 27 | 22 | | | | | | aF/um |
| Fringe (metal3) | | | | | | 53 | 34 | 27 | | | | | | aF/um |
| Fringe (metal4) | | | | | | | 58 | 35 | | | | | | aF/um |
| Fringe (metal5) | | | | | | | | 55 | | | | | | aF/um |
| Overlap (N+active) | | | 895 | | | | | | | | | | | aF/um |
| Overlap (P+active) | | | 737 | | | | | | | | | | | aF/um |

| CIRCUIT PARAMETERS | | | UNITS |
|---|---|---|---|
| Inverters | K | | |
| Vinv | 1.0 | 0.74 | volts |
| Vinv | 1.5 | 0.78 | volts |
| Vol (100 uA) | 2.0 | 0.08 | volts |
| Voh (100 uA) | 2.0 | 1.63 | volts |
| Vinv | 2.0 | 0.82 | volts |
| Gain | 2.0 | -23.72 | |
| Ring Oscillator Freq. | | | |
| D1024_THK (31-stg,3.3V) | | 300.36 | MHz |
| DIV1024 (31-stg,1.8V) | | 363.77 | MHz |
| Ring Oscillator Power | | | |
| D1024_THK (31-stg,3.3V) | | 0.07 | uW/MHz/gate |
| DIV1024 (31-stg,1.8V) | | 0.02 | uW/MHz/gate |

## Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Bipolar Transistors
Simplified
Simplified
Dependent Sources