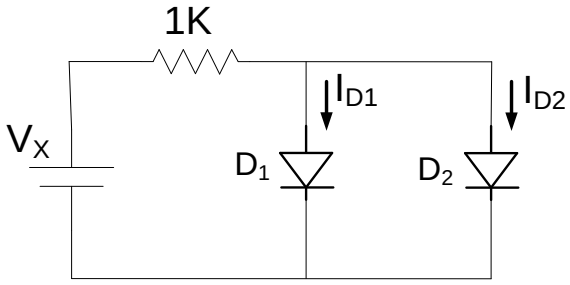
EE 330
Homework Assignment 6
Spring 2018 (Due Wed Feb 14 at 9:00 a.m. – no late assignments accepted)

Each problem is worth 10 points except Problem 17 which is worth 20 points. Solve Problems 15,16, and 17 and any remaining problems that total 60 points. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 100\mu A/V^2$ and $V_{Tn} = 1V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 33\mu A/V^2$ and $V_{Tp} = -1V$. If parameters are needed for process characterization beyond what is given, use the measured parameters from the ON 0.5μ process given below as model parameters.

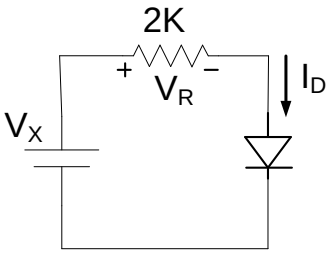
Problem 1 Size an n-channel transistor in the ON 0.5μ CMOS process so that the impedance in the switch-level model is 3500Ω when operating with a 3.5V power supply. Repeat for an n-channel transistor in the IBM 0.13μ CMOS process when operating with a 1.5V supply.

Problem 2 If a minimum-sized inverter designed in the ON 0.5μ CMOS process could directly drive a minimum-sized inverter designed in the IBM 0.13μ CMOS process, what would be t_{HL} and t_{LH} for the ON 0.5μ inverter? Assume a supply voltage of 1.5V. Neglect any interconnect parasitics.

Problem 3 Assume the junction area of D_1 is $50\mu^2$ and that of D_2 is 5 times as large. Determine the current I_{D1} if V_X=1.6V. Assume J_S for the process where the diodes are fabricated is $5fA/\mu^2$.



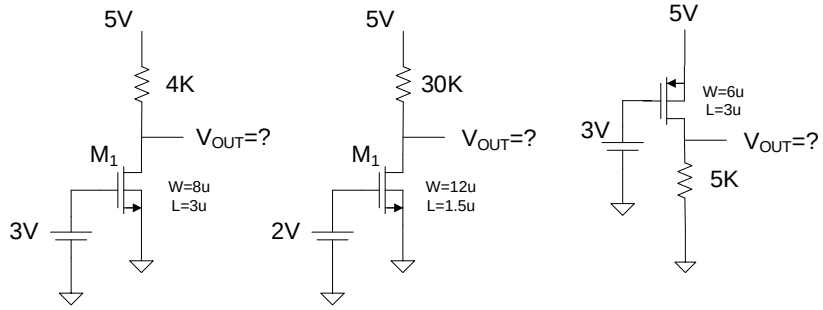
Problem 4 Determine the current I_D (within ±5%) if V_X=15V for the following circuit. Assume the area of the diode is $100\mu^2$ and $J_S=10^{-15}A/u^2$.



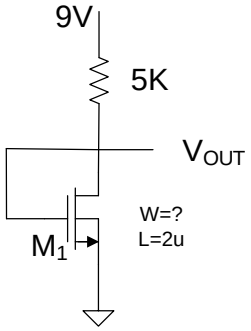
Problem 5 Repeat Problem 4 if V_X=580mV.

Problem 6 If the voltage of a forward-biased pn junction is varied between 0.55V and 0.65V, what is the range in the diode current. Assume the junction area of the diode is $100\mu^2$ and $J_S=10^{-15}A/\mu^2$.

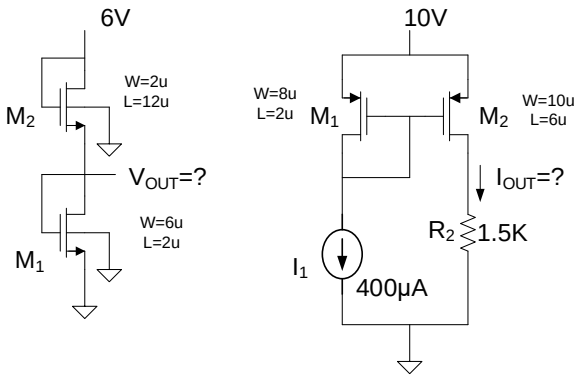
Problem 7 Analytically determine the variable indicated by a ? in the following circuits. Assume the devices are in a process with $V_{TN}=1V$, $V_{TP}=-1V$, $\mu_nC_{OX}=100\mu AV^{-2}$ and $\mu_pC_{OX}=33\mu AV^{-2}$.



Problem 8 Determine W so that V_{OUT} = 3V



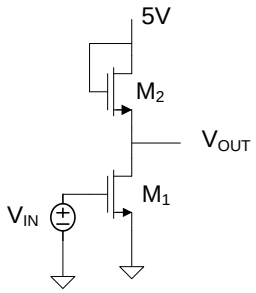
Problem 9 Analytically determine the variable indicated by a ? in the following circuits. Assume the devices are in a process with $V_{TN}=1V$, $V_{TP}=-1V$, $\mu_nC_{OX}=100\mu AV^{-2}$ and $\mu_pC_{OX}=33\mu AV^{-2}$



Problem 10 Consider the following circuit.

a) If V_{IN}=2V, determine the dimensions of M_1 that will result in an output voltage of 3.5V. Assume that the dimensions of M_2 are W_2=8µ and L_2=2µ. The relevant model parameters of the devices are V_{TN}=1V, V_{TP}=-1V, $\mu_n C_{OX}$=100µAV^{-2} and $\mu_p C_{OX}$=33µAV^{-2}.

b) Repeat part a) if the goal is to have an output voltage of 0.8V.



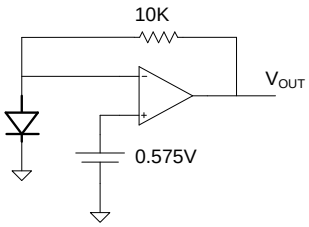
Problem 11

Assume the op amp is ideal and biased with VDD=20Vand VSS=-20V and the diode is characterized by model parameters: J_{SX}=0.5A/µ^2, V_{G0}=1.17V, m=2.3. Assume the area of the junction is 100µ^2.

a) Determine V_{OUT} if T= -20^{o}C

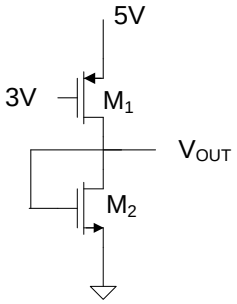
b) Repeat part a) if T= 40^{o}C.

c) Repeat part a) if T=120^{o}C



Problem 12

Determine V_{OUT} for the following circuit. Assume the devices M_1 and M_2 are identically sizes with W=L=5u. The relevant model parameters of the devices are V_{TN}=1V, V_{TP}=-1V, $\mu_n C_{OX}$=100µAV^{-2} and $\mu_p C_{OX}$=33µAV^{-2}.

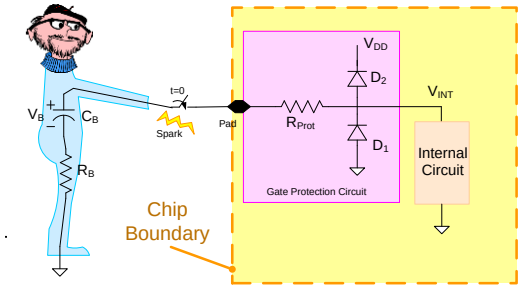


Problem 13

Assume a junction capacitor has a capacitance of 200fF with zero volts bias. What will be the value of this capacitor with a reverse bias of 3V? With a forward bias of 250mV?

Problem 14

Gate protection circuits are used to protect the sensitive gate oxide of devices connected to the input of an integrated circuit from modest short-duration over voltages. Although no input protection circuit can protect from all unknown over-voltages, the Human Body Model (HBM) is often used to model the type of over-voltages that are commonly experienced when humans might become statically charged during normal activities. Such a model is shown below with a connection to one pad on the integrated circuit. In this model, R_B is the body resistance, C_B is the body capacitance, and V_B is the charge on the body capacitance. Touching of the circuit while the person is "charged" is modeled by closing the switch in this model. At a time designated as t=0 it is assumed that the switch is closed and this inserts a voltage into the input pad of the integrated circuit. In the absence of the gate protection circuit, the pad voltage will appear directly on the voltage V_{INT} of the internal integrated circuit if the input impedance to the Internal Circuit is high.



Assume the Internal Circuit has an input that is four parallel-connected minimum sized inverters that are designed in the ON 0.5μ CMOS process. Assume that the diodes D_1 and D_2 can be modeled as an ideal diode with $J_S=10^{-20}A/\mu^2$ and that the area of each of the two diode junctions is $1000\mu^2$.

Consider two HBMs. One is termed a low voltage model and the other a high voltage model. These are characterized respectively by

HBM_1: V_B =250V, C_B=150pF, R_B=1.5K
HBM_2: V_B =2KV, C_B=150pF, R_B=1.5K

a) What will be the peak value of the voltage V_{INT} when the switch is closed if the gate protection circuit is absent (i.e. the Pad is directly connected to the Internal Circuit) with each of the models?

b) What will be the peak value of the voltage V_{INT} when the switch is closed if the gate protection circuit is present with each of the models? Assume R_{PROT}=10K.

c) What will be the peak current in D_2 with each of the models? Assume R_{PROT}=10K.

d) What is the purpose of including the resistor R_{PROT} and what are the disadvantages of including this resistor in the gate protection circuit?

Problem 15 Design a voltage programmable capacitor that varies between 2pF at 0V bias and 2.5pf at a bias of 3.8V.

Problem 16 Design a circuit using only MOS transistors that has an output voltage of 2.0V. In addition to the transistors, you have a single dc power supply of 6V available. You may use as many MOS transistors as you want and can specify any size for the devices.

Problem 17 (weighted as two problems) Use Modelsim to create a positive edge triggered JK Flip-flop. Include screenshots of your Verilog code, and simulation waveforms.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T86S VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		463	-248	uA/um
Vth		0.67	-0.91	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.8	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.49	0.57	V^0.5
K' (Uo*Cox/2)		57.8	-19.1	uA/V^2
Low-field Mobility		475.38	157.09	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

AMI 0.5u Process Description
Continued

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	84.4	109.2	22.9	1102	41.9	0.09	0.09	ohms/sq
Contact Resistance	60.9	150.6	15.8		26.8		0.81	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	818	808	ohms/sq
Contact Resistance	0.81			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	426	724	85		30	15	9	37	aF/um^2
Area (N+active)			2434		34	17	12		aF/um^2
Area (P+active)			2351						aF/um^2
Area (poly)				899	56	16	9		aF/um^2
Area (poly2)					46				aF/um^2
Area (metal1)						33	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	361	241			71	49	33		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						46	34		aF/um
Fringe (metal2)							54		aF/um
Overlap (N+active)			292						aF/um
Overlap (P+active)			387						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.04	volts
Vinv	1.5	2.29	volts
Vol (100 uA)	2.0	0.12	volts
Voh (100 uA)	2.0	4.86	volts
Vinv	2.0	2.47	volts
Gain	2.0	-18.26	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		98.75	MHz
D256_WIDE (31-stg,5.0V)		153.47	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.00	uW/MHz/gate

COMMENTS: SUBMICRON

MOSIS WAFER ACCEPTANCE TESTS

RUN: T85X (8WL_8LM_OL) VENDOR: IBM-BURLINGTON
TECHNOLOGY: SIGE013 FEATURE SIZE: 0.13 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SIGE8WL_IBM-BU

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.16/0.12			
Vth		0.41	-0.42	volts
SHORT	20.0/0.12			
Idss		406	-178	uA/um
Vth		0.43	-0.42	volts
Vpt		3.6	-3.6	volts
WIDE	20.0/0.12			
Ids0		155.2	-127.9	pA/um
LARGE	20.0/20.0			
Vth		0.12	-0.23	volts
Vjbkd		2.7	-3.2	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.28	0.23	V^0.5
K' (Uo*Cox/2)		308.0	-48.8	uA/V^2
Low-field Mobility		553.02	87.62	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	UNITS
Sheet Resistance	6.7	6.3	6.6					ohms/sq
Sheet Resistance				78	51	50	50	mohms/sq
Contact Resistance	9.4	9.2	8.3		0.68	1.37	2.00	ohms
Gate Oxide Thickness	31							angstrom

PROCESS PARAMETERS	M5	M6	M7	M8	N_W	PPLY+BLK	N+BLK	POLY_NON	POLY_NON TaN	UNITS
Sheet Resistance	41	44	7	7.4						mohms/sq
Sheet Resistance					327	321.2	73.4	231.6	1547.4 58.9	ohms/sq
Contact Resistance	2.19	2.51	2.51	2.53						ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	M7	M8	TaN	MiM	UNITS
Area (substrate)	973	1203	109	57	41	32	27	23	20	17	14	24		aF/um^2
Area (N+active)		11176												aF/um^2
Area (P+active)		10496												aF/um^2
Area (r well)	605													aF/um^2
Area (N+ HA varactor)		2390												aF/um^2
Area (M1)			128											aF/um^2
Area (M2)				171										aF/um^2
Area (M3)					182									aF/um^2
Area (M4)						176								aF/um^2
Area (M5)							82							aF/um^2
Area (M6)								81						aF/um^2
Area (M7)									45					aF/um^2
Area (M8)										85				aF/um^2
Area (MiM)													4100	aF/um^2
Fringe (substrate)	60	68												aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.50	volts
Vinv	1.5	0.52	volts
Vol (100 uA)	2.0	0.01	volts
Voh (100 uA)	2.0	1.18	volts
Vinv	2.0	0.53	volts
Gain	2.0	-18.48	
Ring Oscillator Freq.			
DIV1024 (31-stg,1.2V)		376.81	MHz
D1024_THK (31-stg,2.5V)		279.93	MHz
Ring Oscillator Power			
DIV1024 (31-stg,1.2V)		5.13	nW/MHz/gate
D1024_THK (31-stg,2.5V)		26.50	nW/MHz/gate
Operational Amplifier			
Gain		10	

COMMENTS: DEEP_SUBMICRON