EE 330
Homework Assignment 2
Fall 2019   Due Monday Sept 9

On this and subsequent HW assignments there will be problems that require a Verilog or VHDL solution. It will be assumed that students either have a background in Verilog or VHDL or that they will study what is needed to develop this background. There are numerous sources for material on Hardware Description Languages available on line. The text for the course also has a short discussion on HDL in Sec. 1.8 and a more extensive discussion in Appendix A.

Problem 1 1.1 of Weste and Harris (WH) but project to 2020 instead of to 2016.

Problem 2 1.5 of WH but for a 3-input NOR gate instead.

Problem 3 Assume a 300mm wafers cost \$3200. If the defect density on this wafer is 1.5/cm^2, determine the cost per good die if the die is square with a side dimension of 8 mm. Assume the soft yield is 100%.

Problem 4 Assume the specified offset voltage for each of the 2 amplifiers in a "dual" op amp is 5mV (that is, $|V_{OS}|<5\text{mV}$). Determine the soft yield for the "dual" op amp integrated circuit (i.e. both op amps must meet the V_{OS} specification) if the standard deviation of the offset voltage for each op amp is 3 mV and the mean is 0V. Assume the offset voltage for each of the 2 amplifiers are uncorrelated and that the distribution of the offset voltages are Gaussian.

Problem 5 Assume the offset voltage of an operational amplifier is a random variable and that the input offset voltage has a Gaussian distribution with a mean of 0V and a standard deviation of $\sigma = \frac{A_{VT0}}{\sqrt{A}}$ where A is the gate area of two input transistors of the op amp and A_{VT0} = 20mVμm (the units are mV times a micrometer). Determine the area required for the two input transistors if the input offset voltage is to be at most 1.5mV if a soft yield of 97% is required.

Problem 6 Assume a particular function in a 65nm process being used today requires a die area of 0.5cm^2 and that it is fabricated on 300mm wafers that cost \$3200. Predictions now suggest that in a few years, high-end processes will have 7nm feature sizes on 450mm wafers. If the 450mm wafers cost \$10000 each, what will be the approximate cost per good die of the same function if fabricated in the new high-end process with feature sizes of 7nm? When solving this problem, assume the circuit schematic does not change but the transistor sizes scale with the feature size. Neglect the bonding pad areas. Assume the defect density in both processes is the same and is 1.4/cm^2 and that the soft yield is 100%.

Problem 7 Using the switch-level model of n-channel and p-channel transistors, design a logic circuit comprised of only n-channel and p-channel transistors that implements the function

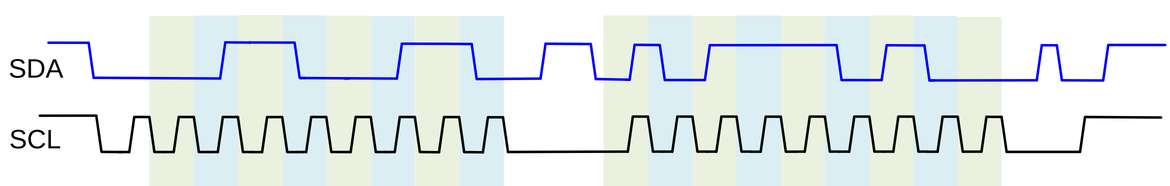
$$F = A + \overline{C}$$

Assume the input variables you have available are A and C (the + symbol denotes the Boolean "OR" operation).

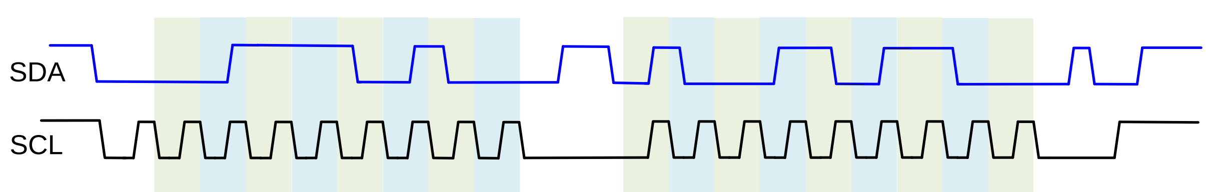
Problem 8 Using the switch-level model of the n-channel and p-channel transistors and assuming that V_{DD}=3V, determine the output voltage of a 2-input NOR gate if

a) Both inputs are 0V
b) One input is 0V and the other input is 3V
c) Both inputs are 3V

Problem 9 There are several different protocols used for communicating between devices on a chip, between chips on a PCB, or between different systems. Some are serial and some are parallel. Included in the communication protocols are SPI, UART, USB, and I^2C. This problem will focus on I^2C. I^2C is a 2-wire (plus ground) open-drain protocol where one or more devices are designated as a Master and the remaining devices are designated as slaves. The 2 wires connecting the devices can be referred to as an I^2C bus. With this protocol, communications ports of the devices are placed in parallel on the 2-wire bus. The two nodes in the I^2C bus are designated as SDA and SCL. In standard I^2C protocol there can be up to 128 slave devices each with unique addresses of <A6,A5,A4,A3,A2,A1,A0>. Assume in a system with a single Master, the following two data sequences on these two nodes were obtained (shading has been added to better visualize the relationship between SDA and SCL)where high levels on both nodes are 1.2V and low values are 0V.



Data Sequence 1



Data Sequence 2

a) Describe what Data Sequence 1 represents
b) Describe what Data Sequence 2 represents
c) What does the term "open-drain" mean?
d) The I^2C protocol is noted for not having logic contention. What does this mean?
e) Why can devices with modestly different logic levels coexist on the same I^2C bus?

Problem 10 Create in Verilog the following Boolean function. Use only the NOR gate you created in the last homework assignment. Create a test bench to test the Boolean function. Include screenshots of your Verilog code and simulation results.

$$F = \overline{A} \bullet B \bullet C + A \bullet B \bullet \overline{C}$$

(The + symbol denotes the Boolean "OR" operation and the $\bullet$ symbol denotes the Boolean "AND" operation. In future designations of Boolean operations, the "$\bullet$ " symbol will be suppressed and the same function F will be designated as
$F = \overline{A}BC + A\overline{B}C + AB\overline{C}$).