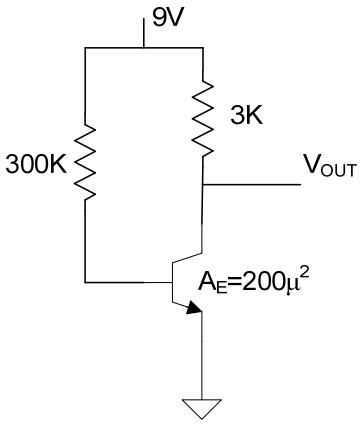
EE 330 Fall 2012
Homework 7

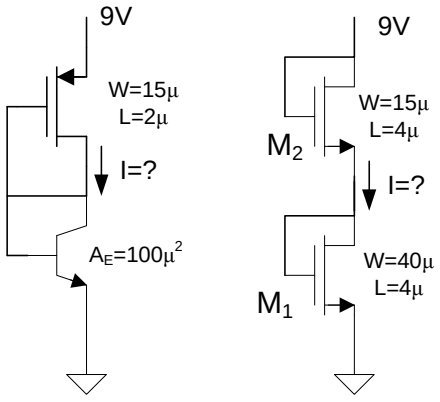
Due Friday October 5 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 100\mu A/V^2$ and $V_{Tn} = 1V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 33\mu A/V^2$ and $V_{Tp} = -1V$. Correspondingly, assume all npn BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is 100 μ^2. If parameters are needed for process characterization beyond what is given, use the measured parameters from the ON 0.5μ process.

Problem 1 (10 points):
Determine the output voltage for the following circuit



Problem 2 (10 points):
Determine the currents labeled with a "?"



Problem 3 (10 points):
Design a circuit using only MOS transistors that has an output voltage of 3V. In addition to the transistors, you have a single dc power supply of 6V available. You may use as many MOS transistors as you want and can specify any size for the devices.

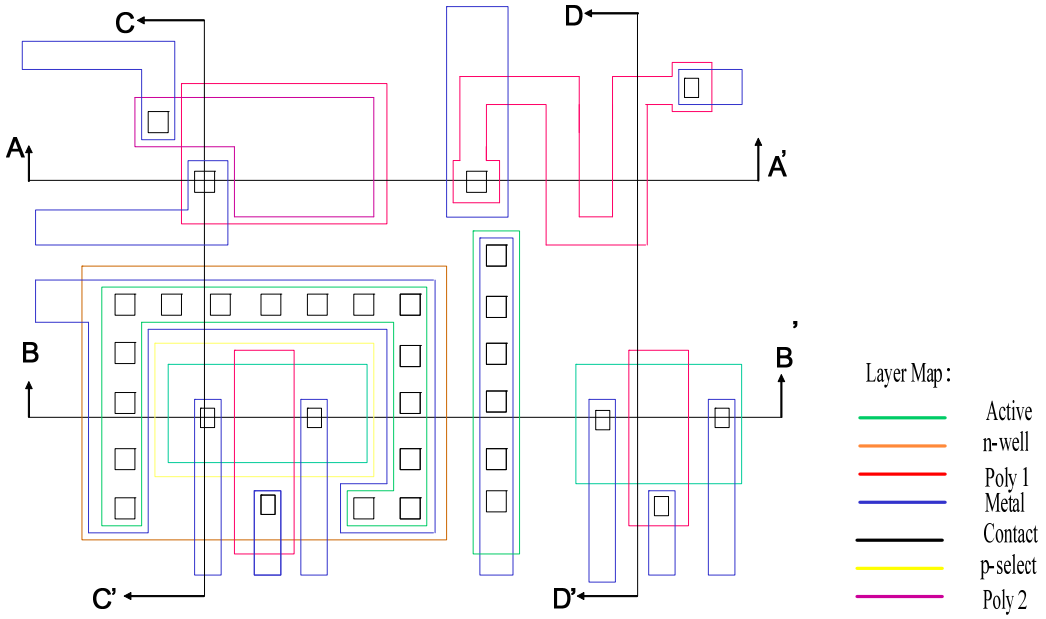
Problem 3' (Extra Credit of 10 points):
Repeat problem 3 if instead of using MOS transistors, you have available only BJTs.

Problem 4 (10 points):
Assume a junction capacitor has a capacitance of 500fF with zero volts bias. What will be the value of this capacitor with (a) reverse bias of 3V, and (b) forward bias of 250mV?

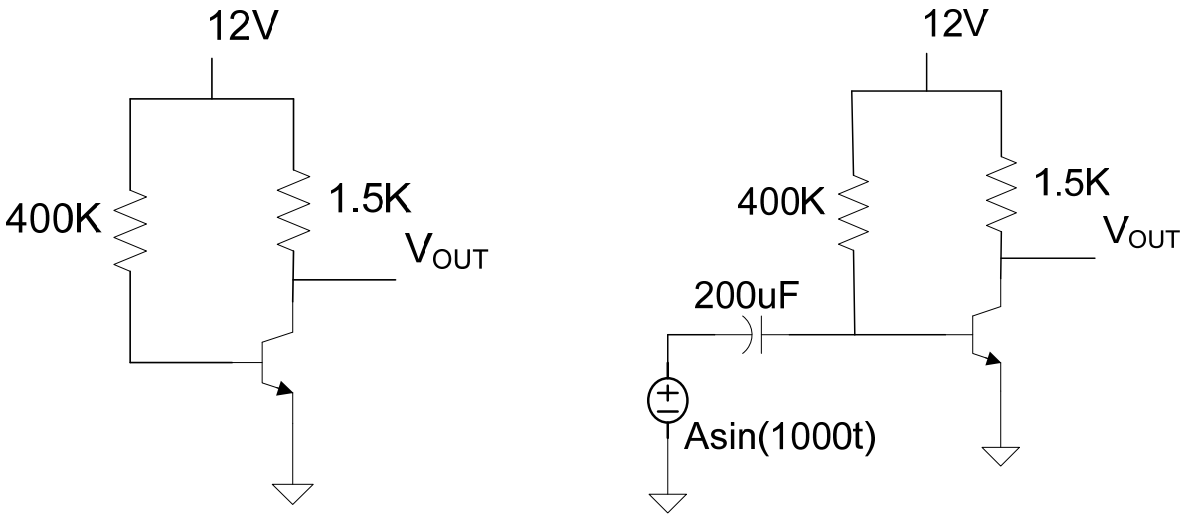
Problem 5 (10 points):
Design a voltage programmable junction capacitor that varies between 2pF to 3pF at a reverse bias between 0V to 4V respectively.

Problem 6 (10 points):
Sketch a cross-sectional view along the AA' cross-section for the CMOS layout shown below. Assume a basic CMOS process in which the n-select mask is generated from the compliment of the p-select mask.

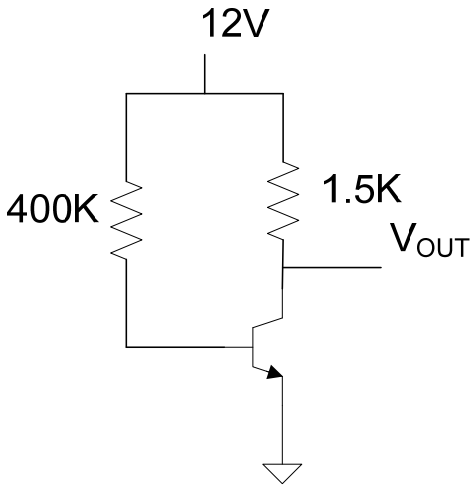
Problem 6' (Extra Credit of 10 points):
Repeat Problem 6 along the CC' cross-section



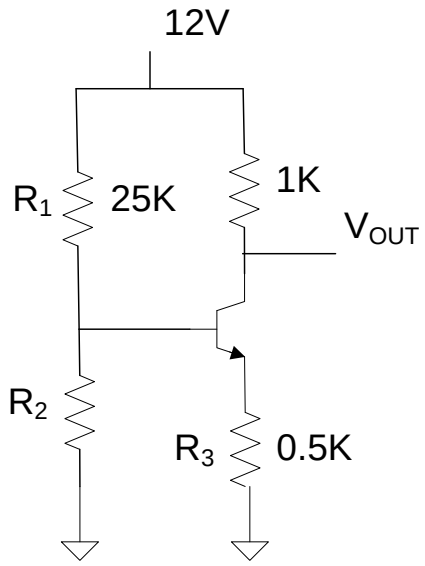
Problem 7 (10 points):
Assume the emitter area for the BJT is $200\mu^2$, the base area is 500 μ^2, β=100, and J_S=50fA/μ^2. Determine the output voltage V_{OUT} for the two circuits shown if A=0.01V.



Problem 8 (10 points):
The process parameter β for a BJT is quite variable from one process run to another. If the β in a process varies between 85 and 125, what is the corresponding variation in the output voltage V_{OUT} for the circuit shown?



Problem 9 (10 points):
The 400k resistor in problem 7 is termed a biasing resistor since it is used to establish the desired value of the quiescent output voltage. This scheme where this single resistor is used to establish the base current is termed a self-bias scheme. An alternative biasing scheme is shown below. In this circuit, the resistor R_1 has been set to 25K. This scheme is often termed a fixed-bias scheme. In this circuit, determine R_2 so that the quiescent output voltage is the same as that for the circuit of Problem 7 when the value of β is 100.



Problem 10 (10 points):
Using the value of R_2 determined in the problem 9, compare the variation in the output voltage of the self-bias circuit in problem 8 to that of the fixed-bias circuit in problem 9 if β varies between 85 and 125.

Problem 11 (Extra Credit for 15 points):
Using Verilog, build a 3-8 bit binary to thermometer decoder. For an input of 000 to 111, it should decode into an 8-bit number with a single one in the position noted by the decimal equivalent of the 3-bit binary number. For example, 100 will correspond to 00010000, and 101 corresponds to 00100000. Your design should be verified with a computer simulation.