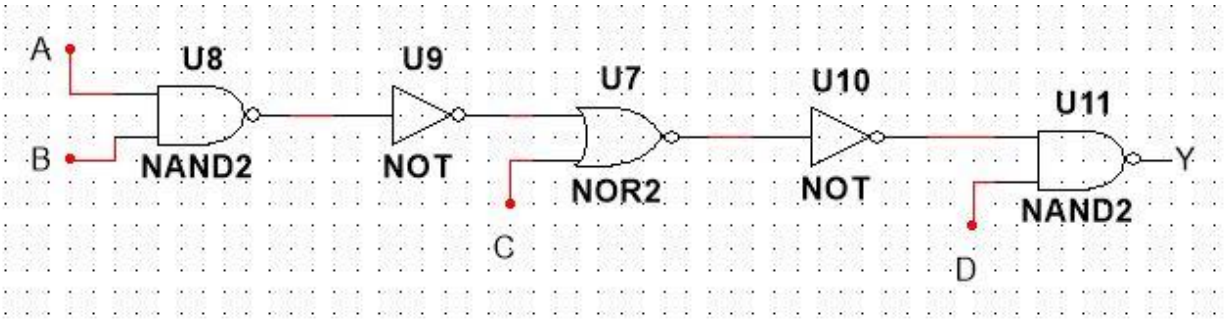
Homework 3 Fall 2017 TA: Joseph Aymond

Problem 1:

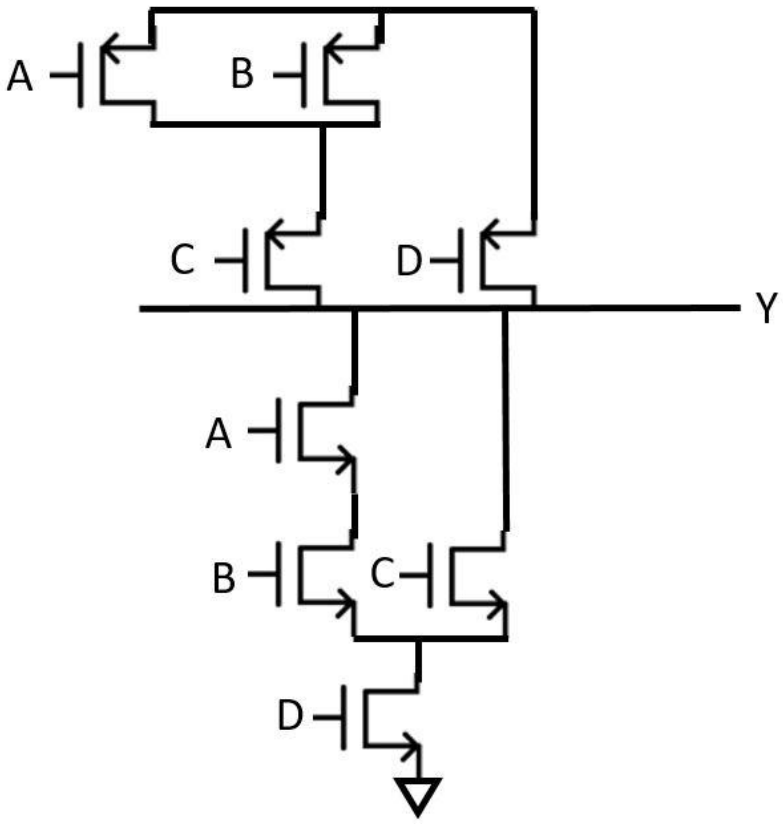
$Y = \overline{(AB + C)D}$

One possible design with static CMOS gates,



This design uses 16 transistors.

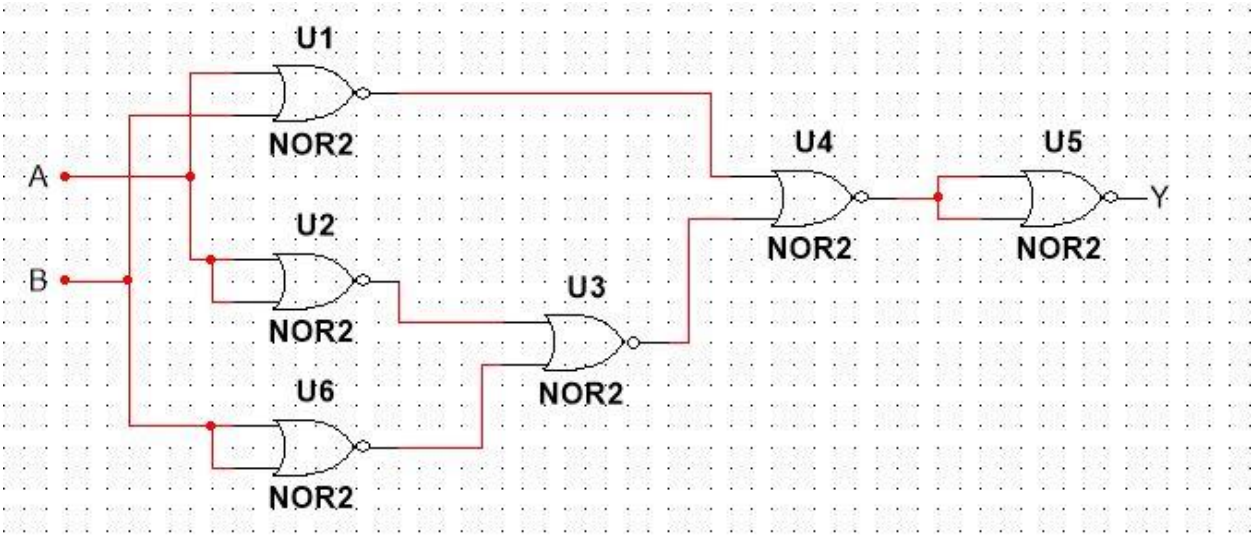
The below is one design for a compound CMOS gate



This design uses 8 transistors

Problem 2:

Y = $\bar{A}\bar{B} + AB$



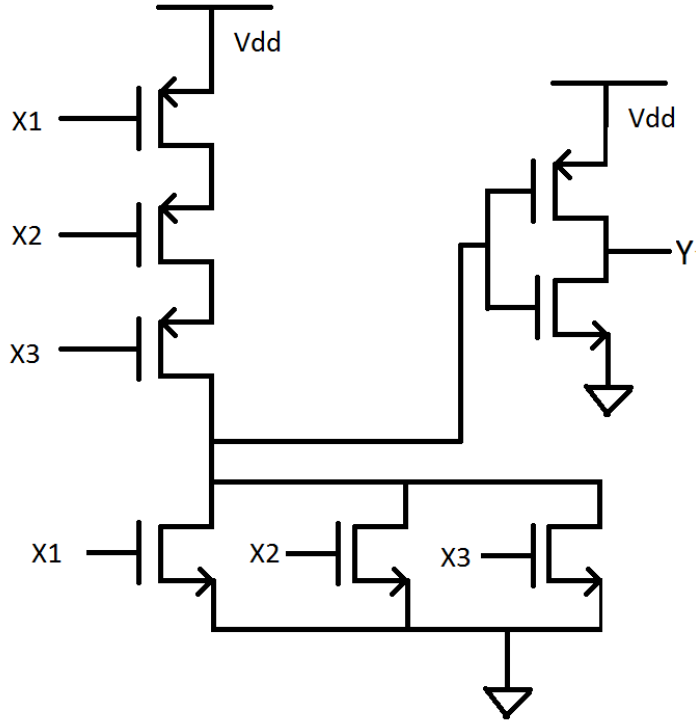
Problem 3:

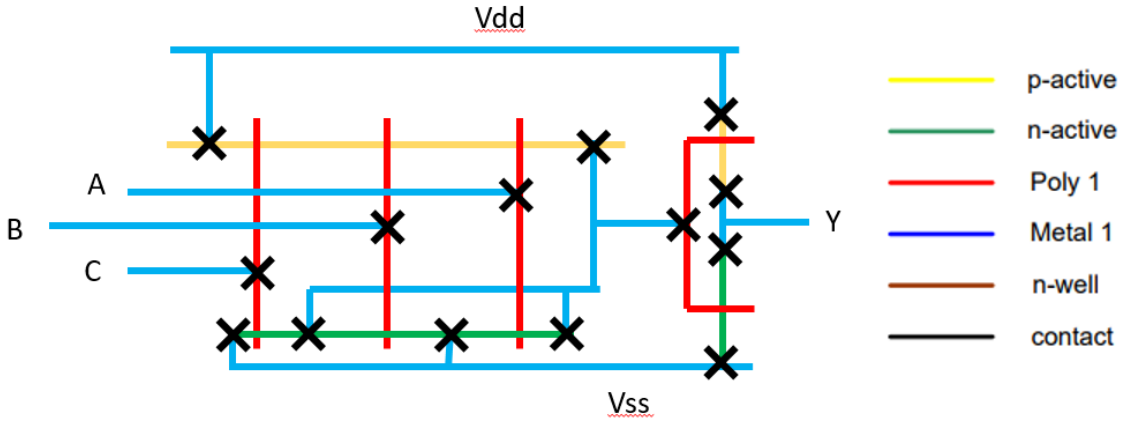
For minimum sized 2 input NAND,

$R_{SWN} = 2k\Omega, R_{SWP} = 6k\Omega, C = 40fF$

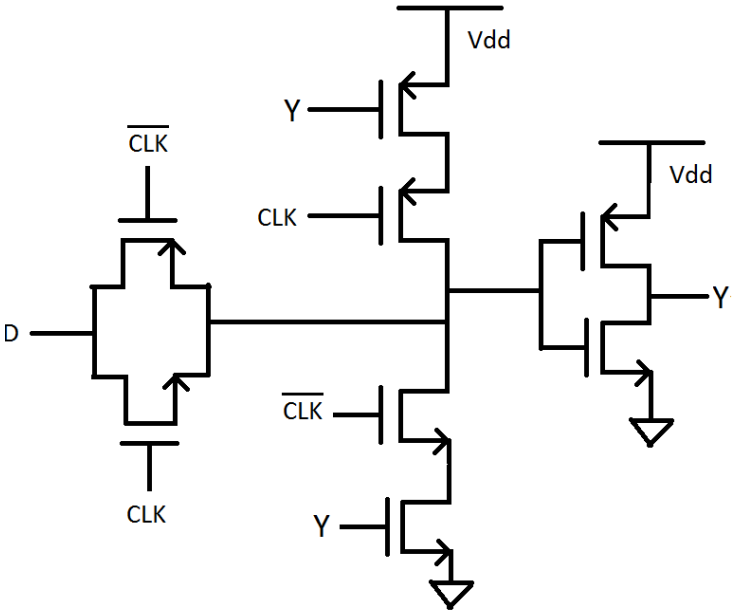
$T_{HL} = 2 * R_{SWn} * C = 4k * 40f = 160 * 10^{-12} seconds = 160\ pS$

Problem 4


Vdd
X1
X2
X3
Vdd
Y
X1
X2
X3

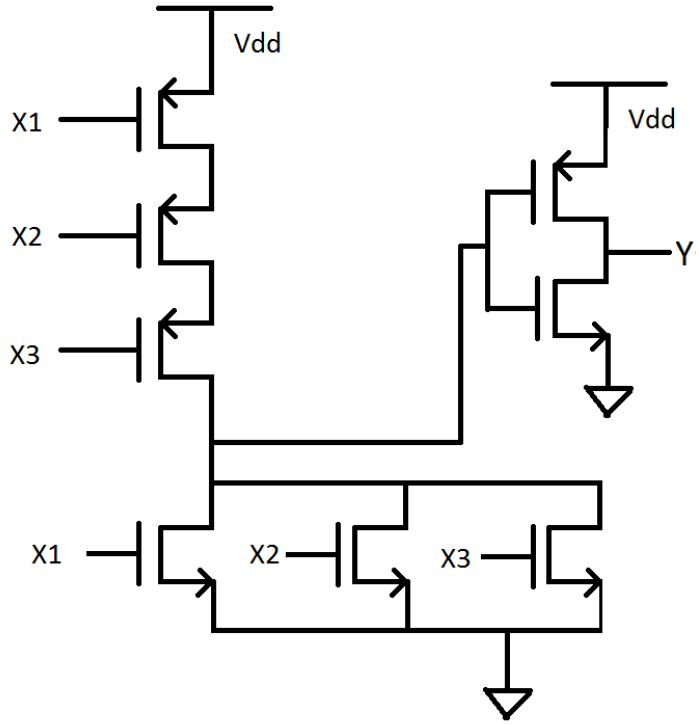

Vdd
A
B
C
Y
Vss
p-active
n-active
Poly 1
Metal 1
n-well
contact

Problem 5



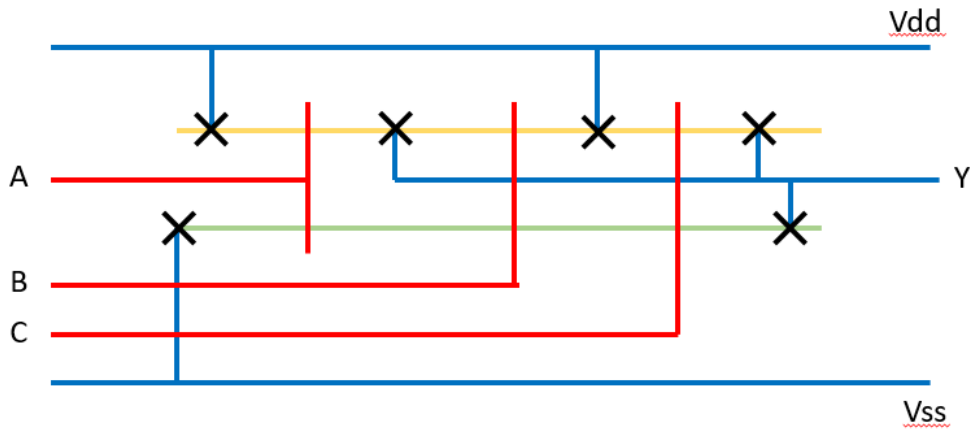
The second inverter is combined with the transmission gate, rather than two separate components.

Problem 6



Problem 7

There should not be a contact between B and N_{active}
N_{active} region is missing one contact with V_{SS}
There should be a contact between Y and P_{active}
The metal contact between A and B that connects N_{active} and V_{SS} needs to be removed.



Problem 8

a) $R_{W\_Aluminum} = \frac{2.8*10^{-8}}{0.2*10^{-6}} * \frac{180}{5} + \frac{2.8*10^{-8}}{0.2*10^{-6}} * \frac{40-5}{5} = 6.02\Omega$

$$V_{wire} = 5 * \frac{6.02}{100 + 6.02} = 283.9\ mV$$

$$V_{Resistor} = 5V - V_{wire} = 5 - 0.2839 = 4.716\ V$$

b) $R_{W_{Copper}} = 3.655\ \Omega$

$$V_{wire} = 5 * \frac{3.655}{100 + 3.655} = 0.176\ V$$

$$V_{Resistor} = 5 * \left(\frac{100}{100 + 3.655}\right) = 4.824\ V$$

c) $V_{RW} < 5V * 5\% = 0.25V$

$$5V * \left(\frac{R_W}{100 + R_W}\right) < 0.25V \rightarrow R_W < 5.263\ \Omega$$

$$R_W = 6.02 * \frac{5\mu m}{Width_{wire}} \rightarrow Width_{Wire} \geq 5.72\ \mu m$$

Problem 9:

Each inverter has $C_L = 1.5\ fF + 1.5\ fF = 3fF$
total load capacitance $C = 3\ pF * 16 = 48\ fF$
$R_{SWp} = 6k\Omega \rightarrow T_{LH} = 6\ k * 48\ f =$ $288 * 10^{-12} S = 288\ pS$

Problem 10

Mux4to1 code

/home/jaaymond/ee330/verilog/EE330Homework/4to1MUX.v (/M

```
Ln#
 1  `timescale 1ns/1ps
 2  module MUX4to1(A, B, C, D, s1, s2, out);
 3    input [3:0] A, B, C, D;
 4    input  s1, s2;
 5    output [3:0] out;
 6    reg [3:0] o;
 7
 8    assign out = o;
 9
10    always @(*) begin
11      if(s1 == 0) begin
12        if(s2 == 0) begin
13          o <= A;
14        end
15        else begin
16          o <= C;
17        end
18       end
19       else begin
20        if(s2 == 0) begin
21          o <= B;
22        end
23        else begin
24          o <= D;
25        end
26      end
27    end
28  endmodule
```

Test bench Code

/home/jaaymond/ee330/verilog/EE330Homework/MUX_tb.v (/M

```
Ln#
 1  `timescale 1ns/1ps
 2
 3  module MUX_tb();
 4
 5    reg [3:0] A, B, C, D;
 6    reg s1, s2;
 7    wire [3:0] out;
 8
 9    MUX4to1 mux(.A(A), .B(B), .C(C), .D(D),
10      .s1(s1), .s2(s2), .out(out));
11
12    initial begin
13     A = 4'b0001;
14     B = 4'b0010;
15     C = 4'b0100;
16     D = 4'b1000;
17     s1 = 0;
18     s2 = 0;
19    end
20
21    always #20 s1 <= ~s1;
22    always #40 s2 <= ~s2;
23
24  endmodule
```

Simulation results