CprE 381, Computer Organization and Assembly-Level Programming, Spring 2019

Lab 3 Report

Lab Partners _____Sean Gordon_____

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Section/Lab Time _____

Refer to the highlighted language in the lab 3 instruction for the context of the following questions.

a. [Part 0] At the end of Chapter 5, answer question 5. At the end of Chapter 7, answer exercise 2.

5.5)
```
process(A, B, C, D, E, F, G, H)
    begin
        org <= A or B or C or D or E or F or G or H;
    end process;
```

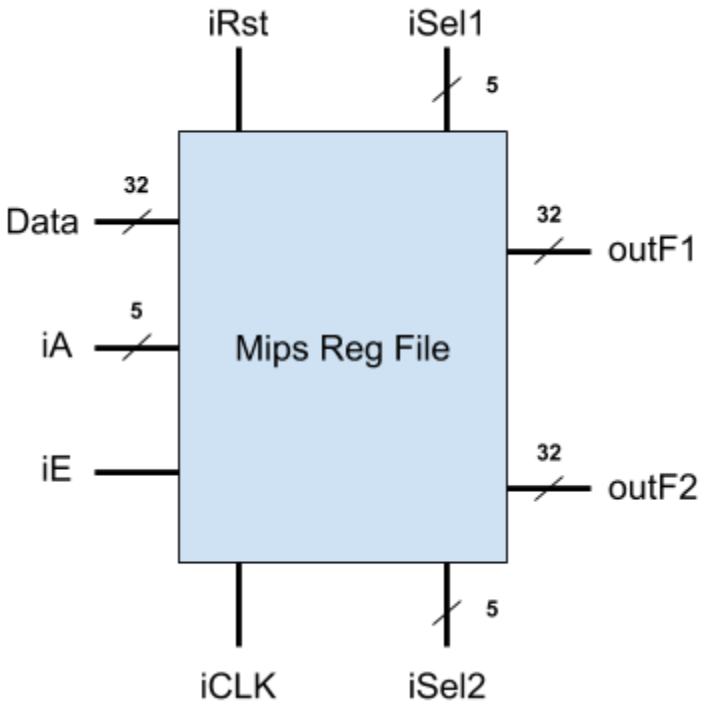
7.2)
```
entity dff is
    port( Clk     : in std_logic;
          D, S, R : in std_logic;
          Q       : out std_logic);
end dff;

architecture behavior of dff is
begin
        dff_proc: process(Clk, S, R)
        begin
            if(S='0') then
                Q <= '1';
            elsif(R = '0') then
                Q <= '0';
            elsif(rising_edge(clk)) then
                Q <= D;
            end if;
        end process dff_proc;
end behavior;
```

b. [Part 0] In your Lab #3 report PDF, provide the Canvas group name for your project team (see assignment page for group creation), and a listing of its members. On a scale of 1-10, how comfortable with VHDL does each team member currently feel

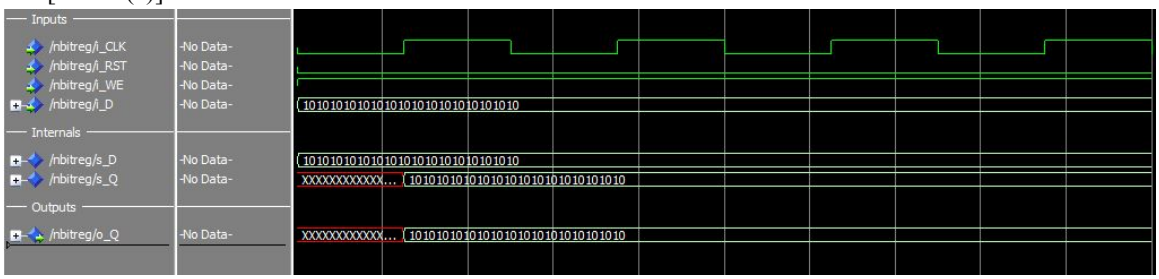
Term project 8
Sean Gordon - 7
Xuewen Jiang - ?

c. [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?



d. [Part 1 (b)] Create an N-bit register using this flip-flop as your basis.

e. [Part 1 (c)] Waveform.



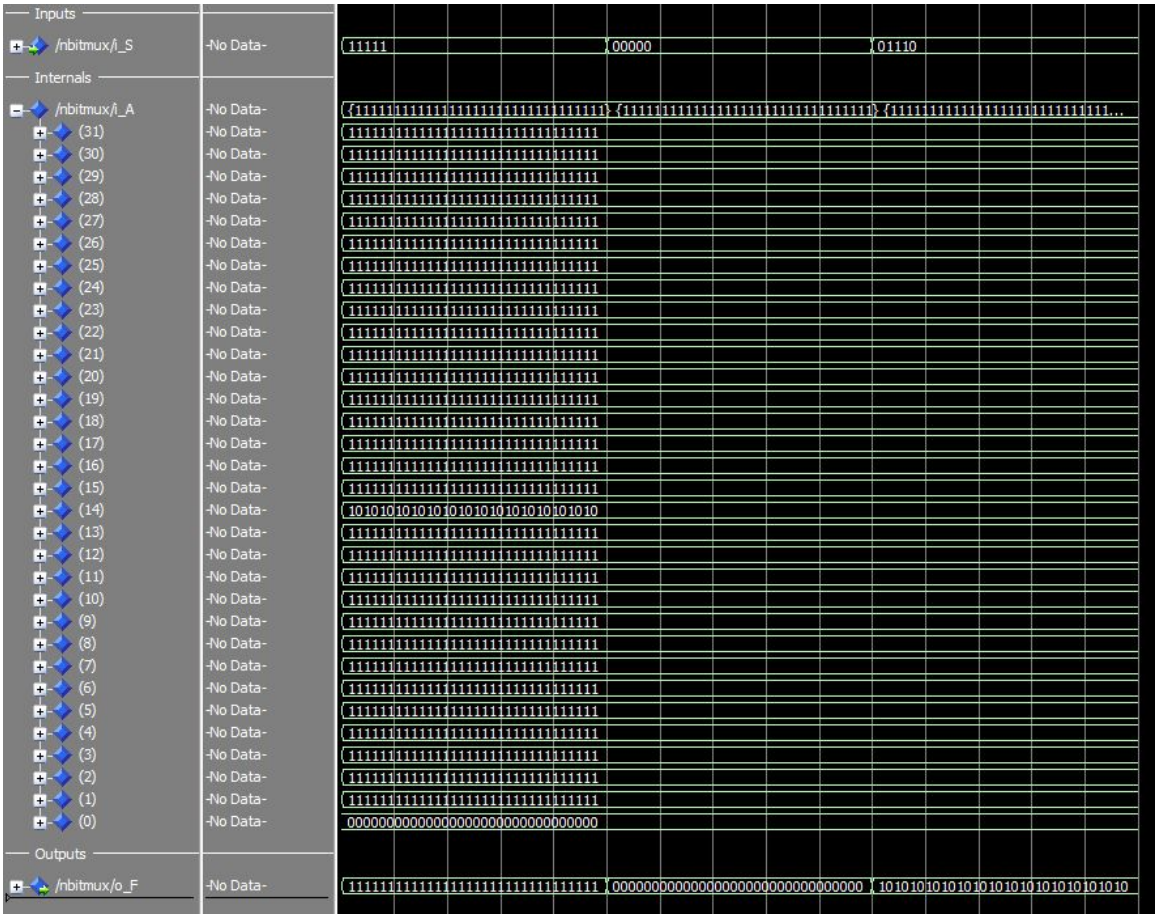
f. [Part 1 (d)] What type of decoder would be required by the MIPS register file and why? □
The register file requires a 5:32 bit decoder because there are 32 registers, and to output 32 signals the decoder needs 5 input signals.

g. [Part 1 (e)] Waveform.

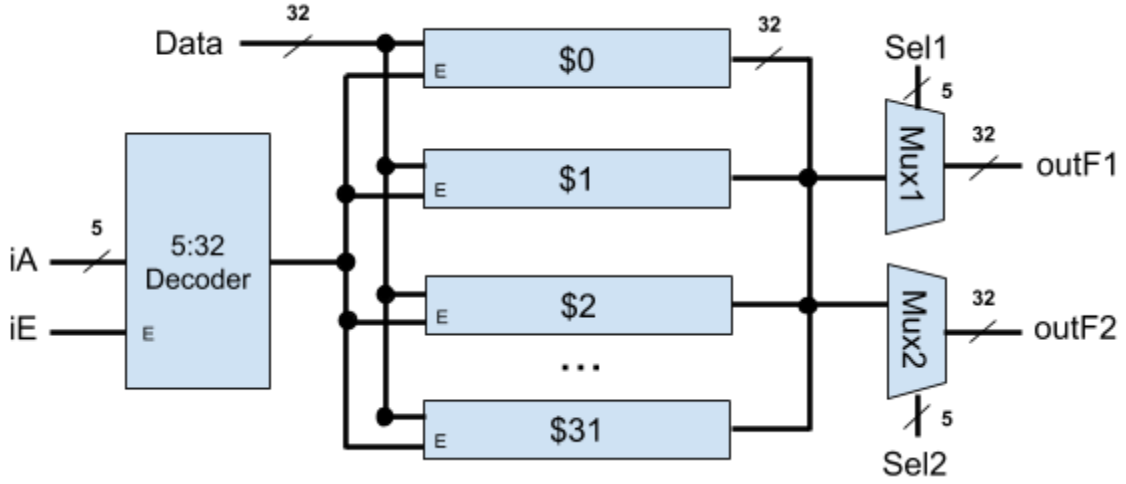
h. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

I will create an W-wide multiplexor with N-bit bundle width using dataflow type architecture, as dataflow is vastly easier to implement and to debug, as well as simulating faster.

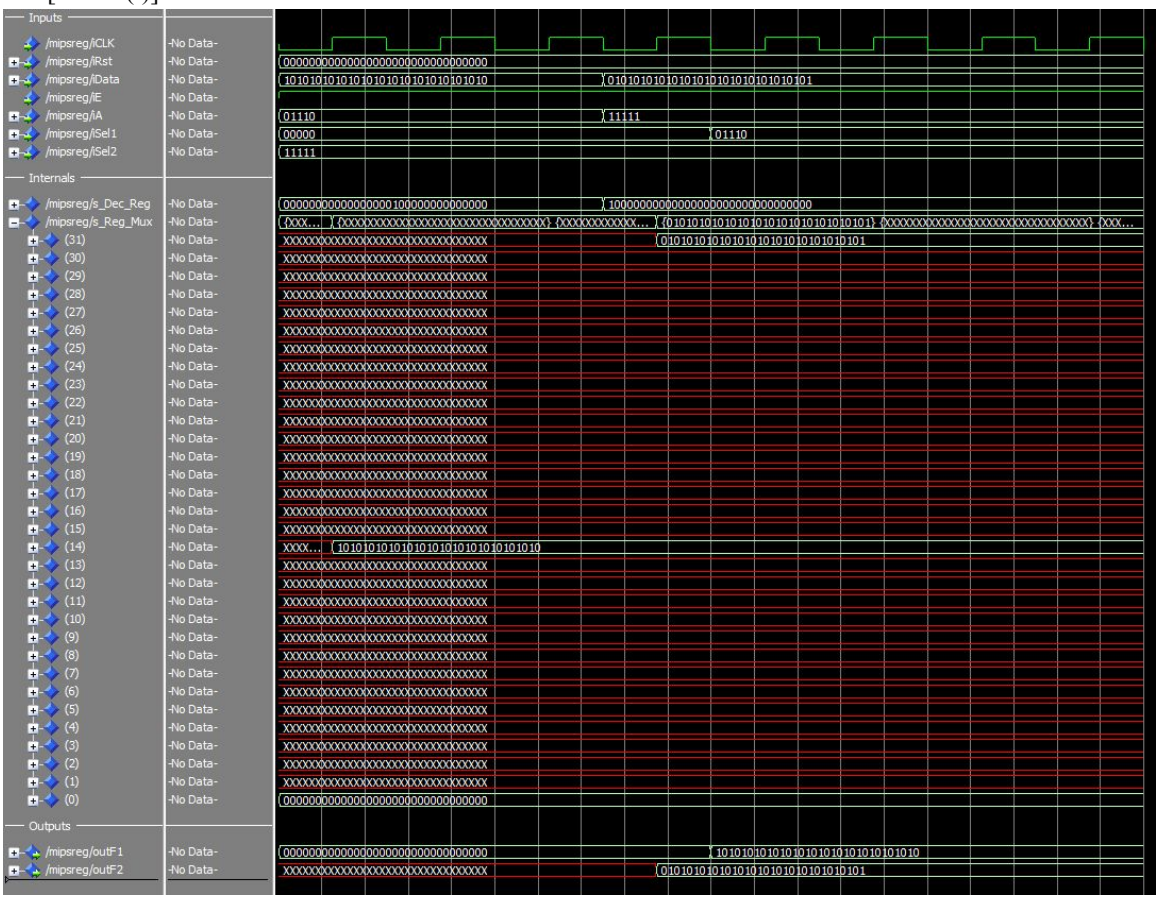
i. [Part 1 (g)] Waveform.



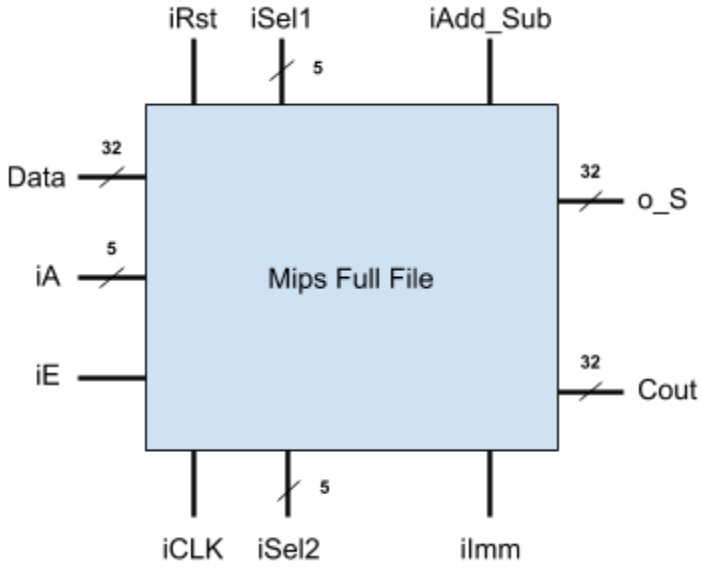
j. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).



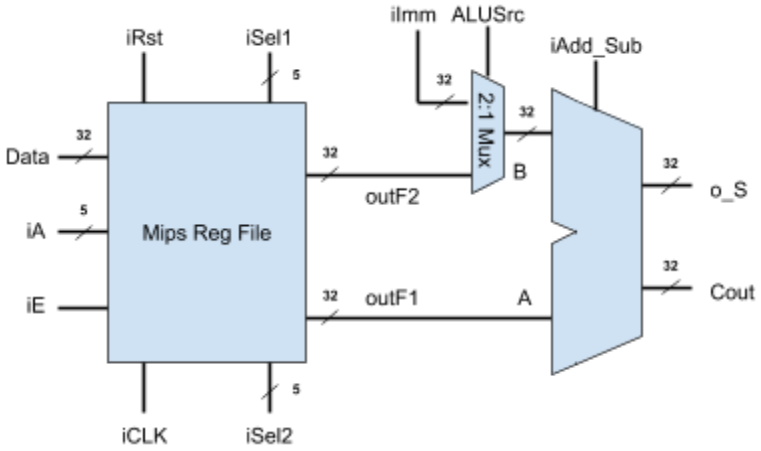
k. [Part 1 (i)] Waveform.



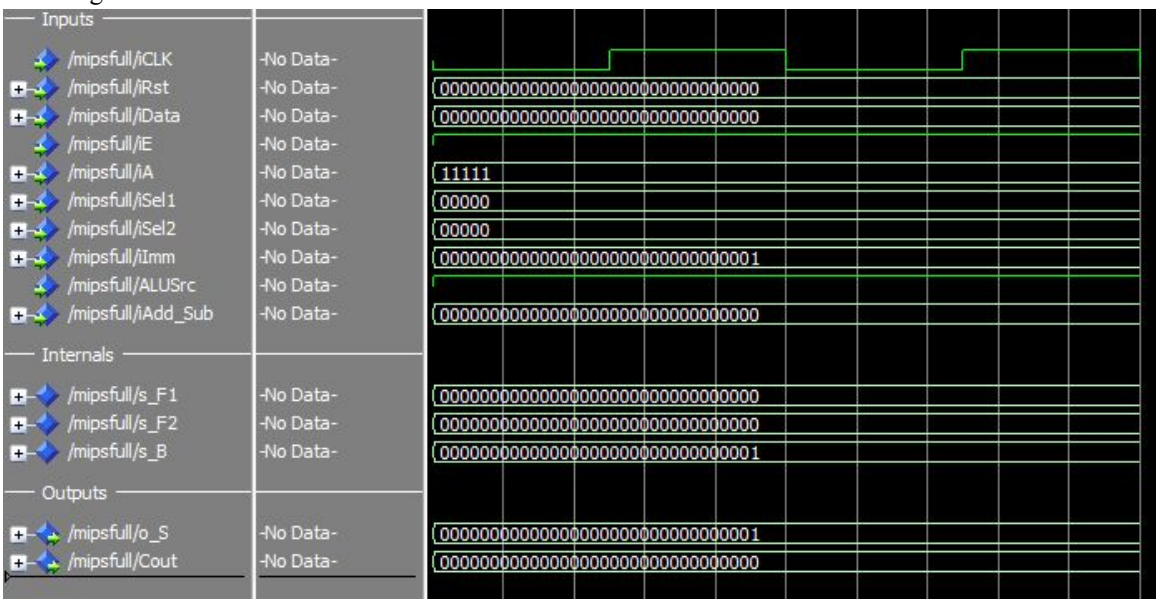
l. [Part 2 (b)] Draw the interface description for this MIPS-like datapath.



m. [Part 2 (c)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).



n. [Part 2 (d)] Include in your report waveform screenshots that demonstrate your properly functioning design.



o. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

p.

1. How many hours did you spend on this lab?

Too many to be acceptable

Task	During lab time	Outside of lab time
Reading lab	0:30	0:20
Pencil/paper design	0:15	0:15
VHDL design	1:00	5:00
Assembly coding	0	0
Simulation	15:00	0:30
Debugging	15:00	2:00
Report writing	0	0:45
Other:		
Total	2:00	8:50

2. If you could change one thing about the lab experience, what would it be? Why?
   Get rid of part 2. The length of these labs is absurd.

3. What was the most interesting part of the lab?
   Finishing the lab so I could finally work on other classes. These labs are horrendously inefficient as teaching mediums.