EE330
Homework 8
Fall 2018
Solutions – TA: Robert Buckley

Problem 1

Assume BJT works in forward active region

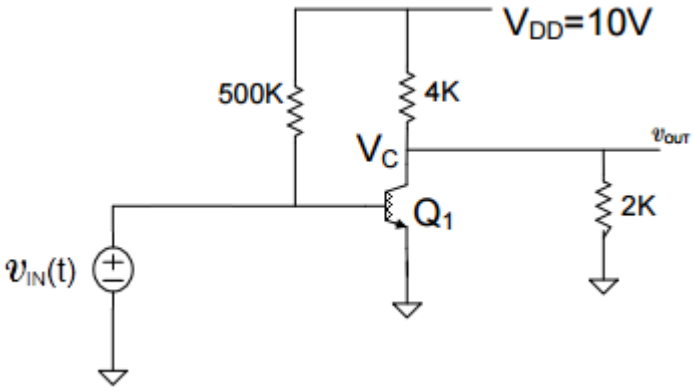
$I_B = \left(\frac{10 - 0.6}{500k}\right) = 18.8\mu A$

$I_C = \beta I_B = 100 * 18.8\mu A = 1.88mA$

$V_C = 10 - 4000 * 0.00188 = 2.48V$

$V_{out} = 0V$ (there is a capacitor creating an open circuit in DC.)

Small signal equivalent circuit:



Problem 2

For the MOSFET to be in saturation $V_{DS} \geq V_{GS} - V_T$

$V_{out} + 2 \geq 2 - 0.5 \rightarrow V_{out} \geq -0.5$

$I_D = \frac{\mu_n C_{OX} W}{2L}(V_{GS} - V_T)^2 = \frac{4 - V_{out}}{R_1}$

$300 * 10^{-6} * \left(\frac{12}{4}\right) * (0 - (-2) - 0.5)^2 = \frac{4 - V_{out}}{R_1}$

$V_{out} = 4 - 0.002025 * R_1 \geq 0.5V$

$\rightarrow R_1 \leq 1728.4\Omega$

Problem 3

$\frac{R_1}{2} = 864.2k\Omega$

$A_V = \frac{2I_{DQ}R}{V_{SS} + V_T} = \frac{3.5\ V}{-1.5\ V} = -2.33\text{V/V}$

Problem 4

Assuming that M_1 and M_2 are in saturation

$$I_{D_1} = I_{D_2} \rightarrow \frac{\mu_n C_{OX} W_n}{2L_n}(V_{GS} - V_T)^2 = \frac{\mu_p C_{OX} W_p}{2L_p}(V_{GS} - V_T)^2$$

$$\rightarrow \frac{300 * 10^{-6} * 10}{2 * 2}(0 - (-1) - 0.5)^2 = \frac{75 * 10^{-6} * 50}{2 * 1}\left(V_{out} - 1 - (-0.5)\right)^2$$

$\rightarrow V_{out} = 0.183$ or 0.816. Since $0.816 - 1 > -0.5$ this would put the transistor in ohmic region so the voltage is $0.183V$.

Problem 5

For quiescent values that capacitors act as open circuits, so the voltage is simply,

$$I_B = \frac{32 - V_B}{90\text{K}} - \frac{V_B}{10\text{K}} = \frac{32 - 10 * V_B}{90\text{K}}$$

$$I_E = (\beta + 1)I_B = (101) * \frac{32 - 10 * (V_E + 0.6)}{90\text{K}} = \frac{V_E}{1.5\text{K}} \rightarrow V_E = 2.454\ \text{V} \rightarrow V_B = 3.054\ \text{V}$$

$I_C = 101 * 16.222\ \mu\text{A} \rightarrow V_C = 32 - 3000 * I_C = 27.085\ \text{V}$

$V_{out} = 0V$

Problem 6

$$V_{out} = 1 - \left(4000 * i_{DQ}\right)$$

$$I_{DQ} = 300 * 10^{-6} * \left(\frac{6}{2 * 4}\right) * (0 - (-1) - 0.5)^2$$

$I_{DQ} = 56.25\mu A$

$V_{out} = 0.775V$

Problem 7

a) $I_{DQ} = 300 * 10^{-6} * \left(\frac{6}{2*3}\right)(4 - 0.5)^2$

$I_{DQ} = 75\ \mu A$

$V_{outq} = 4 + 75\ \mu * 60k = 8.5V$

b) When $V_{in} = 0V, V_{out1} = V_{outQ} = 6V$

When $V_{in} = 25mV, V_{out2} = V_{outQ} + \Delta\text{V}$

$$g_m = 300 * 10^{-6}\left(\frac{6}{3}\right)(1) = 600\frac{\mu A}{V}$$

$\Delta V = (g_m * \Delta V_{in}) * 20k = 0.9V$

$V_{out2} = 9.4V$

Problem 8

$$R_{FET} = \frac{1}{\mu_n C_{OX}}\left(\frac{L}{W}\right)(2-1)$$

$$\frac{V_{out} - V_{in}}{R_F} = \frac{V_{in}}{R_{FET}}$$

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_F}{R_{FET}} = 1 + \left(\frac{1}{R_{fet}}\right)\mathrm{R_F} = \mu_n C_{OX}\left(\frac{W}{L}\right)R_F$$

$$\frac{V_{out}}{V_{in}} = 1 + 300 * 10^{-6} * \left(\frac{4}{1}\right) * R_F = 1 + \frac{3R_F}{2500}$$

Problem 9

a) $\frac{I_{B1}}{I_{B2}} = \frac{A_{E1}}{A_{E2}} = \frac{1}{4}$

$$I_B = I_{B1} + I_{B2} = 5\, I_{B1}$$

$$I_{IN} = I_{C1} + \beta I_B = \beta I_{B1} + 5 I_{B1}$$

$$I_{B1} = I_{in}\left(\frac{1}{\beta + 5}\right) -> I_{out} = \beta I_{B2} = \beta * 4 I_{B1} = I_{in}\left(\frac{4}{1 + \frac{5}{\beta}}\right)$$

Assuming that β is large $\rightarrow I_{out} = 4 * I_{in} = 4\ mA$

b)

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = \frac{10}{20} = \frac{1}{2}$$

$$I_{out} = 2 I_{in} = 2\ mA$$

Problem 10

$$BJT: I_{out} = \frac{A_{E2}}{A_{E1}} I_{in}$$

$$MOSFET: I_{out} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} I_{in}$$

Problem 11

At the basics, $I_d = \mu C_{ox}\left(\frac{w}{2L}\right)\left(V_{gs} - V_T\right)^2$, and all three have the same total length and width. Becuase the length/width is the one degree of freedom we have to modify the MOSFET, they should behave the same.

Problem 12

```
1   module and4bit(i_A,i_B,o_F);
2     input [3:0] i_A, i_B;
3     output [3:0] o_F;
4
5     assign o_F = i_A & i_B;
6
7   endmodule
8
```

```
1   module Mux4_2_1 (i_A, i_B, i_S, o_F);
2     input [3:0] i_A, i_B;
3     input i_S;
4     output [3:0] o_F;
5
6       Mux_2_1 mux0(.i_A(i_A[1:0]), .i_B(i_B[1:0]), .i_S, .o_F(o_F[1:0]));
7       Mux_2_1 mux1(.i_A(i_A[3:2]), .i_B(i_B[3:2]), .i_S, .o_F(o_F[3:2]));
8
9   endmodule
```

```
1   module dff(i_A,o_F,clk);
2     input i_A, clk;
3     output o_F;
4     reg o_F;
5
6     always @ (posedge clk)
7       o_F = i_A;
8
9     endmodule
10
11  module register(i_A,o_F,clk);
12    input  [3:0] i_A;
13    input  clk;
14    output [3:0] o_F;
15
16    dff flip0(.i_A(i_A[0]), .clk(clk), .o_F(o_F[0]));
17    dff flip1(.i_A(i_A[1]), .clk(clk), .o_F(o_F[1]));
18    dff flip2(.i_A(i_A[2]), .clk(clk), .o_F(o_F[2]));
19    dff flip3(.i_A(i_A[3]), .clk(clk), .o_F(o_F[3]));
20
21  endmodule
```

```
module halfadder(i_A,i_B,i_C,o_C,o_S);
  input i_A, i_B, i_C;
  output o_C, o_S;

  assign o_S = i_A ^ i_B ^ i_C;
  assign o_C = (i_A & i_B) | (i_A & i_C) | (i_B & i_C);

endmodule

module fulladder(i_A,i_B,i_C,o_C,o_S);
  input  [3:0] i_A, i_B;
  input   i_C;
  output  o_C;
  output [3:0] o_S;
  wire   [2:0] w_C;

  halfadder adder0(.i_A(i_A[0]), .i_B(i_B[0]), .i_C(i_C), .o_C(w_C[0]), .o_S(o_S[0]));
  halfadder adder1(.i_A(i_A[1]), .i_B(i_B[1]), .i_C(i_C), .o_C(w_C[1]), .o_S(o_S[1]));
  halfadder adder2(.i_A(i_A[2]), .i_B(i_B[2]), .i_C(i_C), .o_C(w_C[2]), .o_S(o_S[2]));
  halfadder adder3(.i_A(i_A[3]), .i_B(i_B[3]), .i_C(i_C), .o_C(o_C),    .o_S(o_S[3]));


endmodule
```

```
module andadder(i_A, i_B, o_F, clk, i_S);
  input  [3:0] i_A, i_B;
  input  clk, i_S;
  output [3:0] o_F;
  wire   [3:0] w_R0, w_R1, w_AND, w_ADD, w_MUX, o_C;

  register reg0(.i_A(i_A), .o_F(w_R0), .clk(clk));
  register reg1(.i_A(i_B), .o_F(w_R1), .clk(clk));

  and4bit   and0(.i_A(w_R0), .i_B(w_R1), .o_F(w_AND));
  fulladder add0(.i_A(w_R0), .i_B(w_R1), .i_C(0), .o_C(o_C), .o_S(w_ADD));
  Mux4_2_1  mux0(.i_A(w_AND), .i_B(w_ADD), .i_S(i_S), .o_F(w_MUX));

  register reg3(.i_A(w_MUX), .o_F(o_F), .clk(clk));


endmodule
```

```
1   module andadder_TB();
2     reg [3:0] i_A, i_B;
3     reg clk, i_S;
4     wire [3:0] o_F;
5
6     andadder TB(.i_A(i_A), .i_B(i_B), .o_F(o_F), .clk(clk), .i_S(i_S));
7
8     initial
9     begin
10      i_A = 4'b0000;
11      i_B = 0;
12      clk = 0;
13      i_S = 0;
14    end
15
16    always
17    #1 clk = ~clk;
18    always
19    #5 i_S = ~i_S;
20
21    always
22    #10 i_A = i_A+1;
23    always
24    #20 i_B = i_B+1;
25
26    endmodule
```