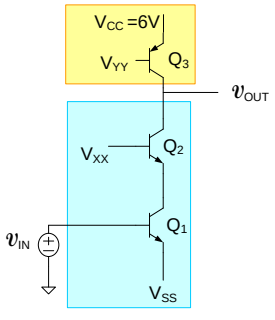
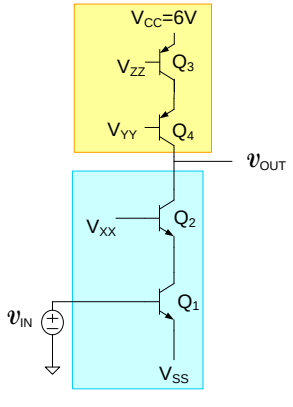
EE 330
Assignment 13
Fall 2019
Solve Problems 1-7. Since there will be an in-class exam on Friday Nov 22, problems 8-11 will not be collected and this assignment will be due at noon time on Wednesday Nov. 20. No late assignments will be accepted after noon on the 20th.

If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $L_{MIN}=W_{MIN}=0.5\mu$, and $V_{DD}=3.5V$ and a bipolar process is available with model parameters $J_S= 10^{-14}A/u^2$, $\beta_n=100$ and $\beta_p= 40$. The output conductance of the BJT and the MOSFET are characterized, respectively, by $V_{AF}=100V$ and $\lambda=.01V^{-1}$.

Problem 1 Assume the biasing voltages have been selected so that the quiescent output voltage is 3V and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume $A_{E1}=A_{E2}=50\mu^2$ and $A_{E3}=20\mu^2$.



Problem 2 Assume the biasing voltages have been selected so that the quiescent output voltage is 3V and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume $A_{E1}=A_{E2=}50\mu^2$and $A_{E3}=A_{E4}=20\mu^2$.

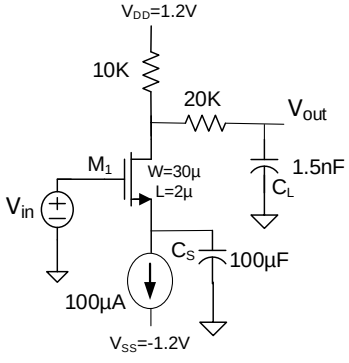


Problem 3 If a DC input voltage of 2uV is placed in series with v_{IN} in the previous circuit, how much change in the output voltage from the quiescent value of 3V can be expected? Comment on

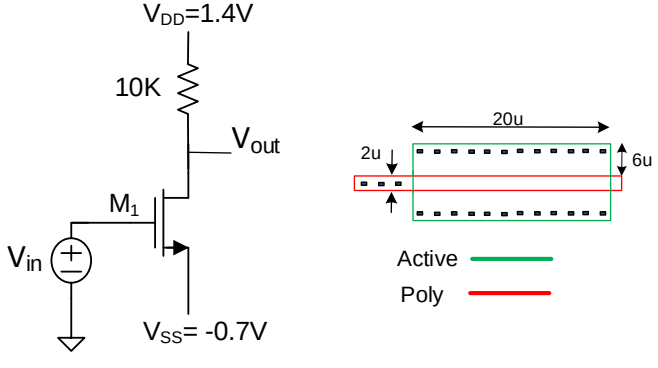
the implications of this observation.

Problem 4 Consider the following amplifier. You may neglect any parasitic capacitances in the transistor M_1.

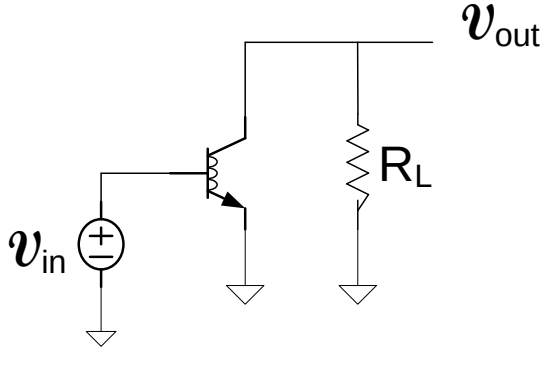
a) Determine the quiescent drain voltage of M_1
b) Determine an expression for the small-signal voltage gain valid throughout the audio frequency range (hint: C_L is not negligible)
c) Determine the 3db bandwidth of the amplifier



Problem 5 At high frequencies the gain of an amplifier drops off due to the parasitic capacitances in the transistor. A dominant contributor to the drop in gain is often the parasitic drain-substrate (or termed the drain-bulk) capacitance of the transistor. Determine the 3dB bandwidth of the following amplifier (assume all parasitic capacitances except C_{DB} can be neglected). A layout of the transistor is sketched. Relevant model parameters are included in the model information attached at the end of this assignment.



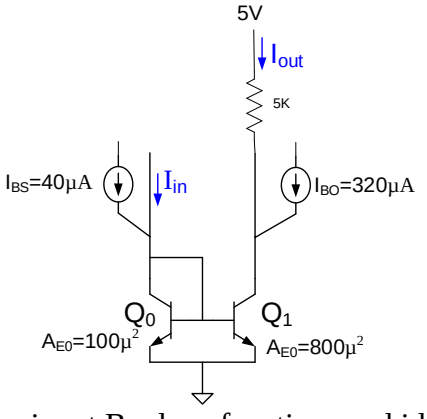
Problem 6 The small-signal equivalent circuit of a common emitter amplifier is shown below. If the emitter area of the BJT is $100\mu^2$ and the load resistor R_L is 10K, bias this circuit so that the quiescent output voltage is 3V and the DC voltage across R_L is also 3V while maintaining the same small signal gain that this circuit has. You have one dc power supply available of any value you choose and any number of resistors and capacitors.



Problem 7 Consider the following circuit.

a) Determine an analytical expression that relates I_{OUT} to I_{IN}

b) With a computer simulation, plot the relationship between I_{OUT} and I_{IN} as I_{IN} is varied between -40uA and +40uA .

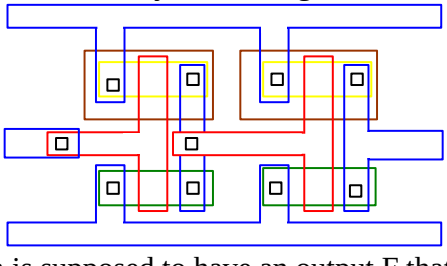


Problem 8 Give all of the two-input Boolean functions and identify which of those are useful or are actually used.

Problem 9 A physical layer implementation of a circuit at the layout level is shown below where blue denotes metal, red polysilicon, green n-active, yellow p-active, brown n-well and black contacts. Assume the upper metal rail is a VDD pin, the lower metal rail is ground, the middle left metal is Boolean input A, and the middle right metal is Boolean output B.

a) Give a physical layer view of this layout at the circuit schematic level. Assume the contact sizes are 2λ x 2λ.

b) Give a structural layer view of this layout at the gate level.



Problem 10 A Boolean System is supposed to have an output F that is high when the Boolean inputs A and B are high or when the inputs C and D are high and E is low or when the input A is low and the input E is high.

a) Give a behavioral description of this system in terms of the input/output variables A,B,C,D,E, and F.

b) Write Verilog code describing this system at the behavioral level

c) Give a gate-level structural description of this system if the only gates that are NOR gates with any number of inputs

d) Write Verilog code describing this system at the gate level

e) Give a transistor-level physical description of this system. You may use any logic style you are familiar with. You need not size the devices

Problem 11 Give two distinct structural implementations at the gate level of a system with the following Behavioral Description: The output F is high when A is high and B is high or when C is high and B is low. Otherwise the F output is low.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON