EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Final Exam
Spring 2017

Instructions: Students may bring 3 pages of notes (3 front + 3 back) to this exam. There are 10 questions and 8 problems. There are two points allocated to each question. All problems are worth 10 points. Please solve problems in the space provided on this exam. Attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/V^2$, $\mu_p C_{OX}= \mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=4fF/\mu^2$, $\lambda = 0.01V^{-1}$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters for an npn transistor of $J_S=10^{-15}A/\mu^2$, $\beta_n=100$ and $V_{AFn} = \infty$ and those for a pnp transistor are $J_S=10^{-15}A/\mu^2$, $\beta_p=20$ and $V_{AFp} = \infty$. If any other process parameters are needed, use the process parameters associated with the process described in the attachments to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters. Several tables that may be of use are appended at the end of the exam.

1. (2pts) An SCR is formed by a stacking of alternate p and n diffused regions. How many diffused regions are needed to form a basic SCR?

2. (2pts). What is the fundamental difference between an SCR and a Triac?

3. (2 pts) Delay calculations using the Elmore delay model are said to be "faithful". In the context of timing in logic circuits, what does it mean to be "faithful"?

4. (2 pts) What is the major purpose of a pad driver?

5. (2 pts) Some logic is termed "ratio logic". What is the key feature characterizing ratio logic?

6. (2 pts) Why is the capacitance density of Metal 3 to substrate considerably lower than the capacitance density of Metal 1 to substrate in a standard CMOS process?

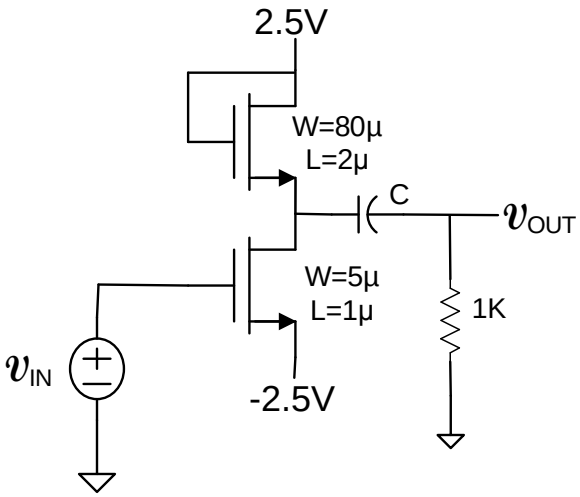
7. (2 pts) What parameter in a JFET corresponds to the threshold voltage in a MOSFET?

8. (2 pts) What are the two major limitations of pass transistor logic?

9. (2 pts) Compound gates (sometimes referred to as Complex Logic Gates) are often used as an alternative to static CMOS NAND and NOR gates to implement Boolean functions. What is the major advantage of using Compound Gates?

10. If a CMOS inverter in the process described on the top of this exam is designed with an n-channel transistor sized with $W=W_{min}$ and a p-channel transistor with $W=20W_{min}$ what will be the trip-point voltage? Assume both transistors have a length of L_{min}.

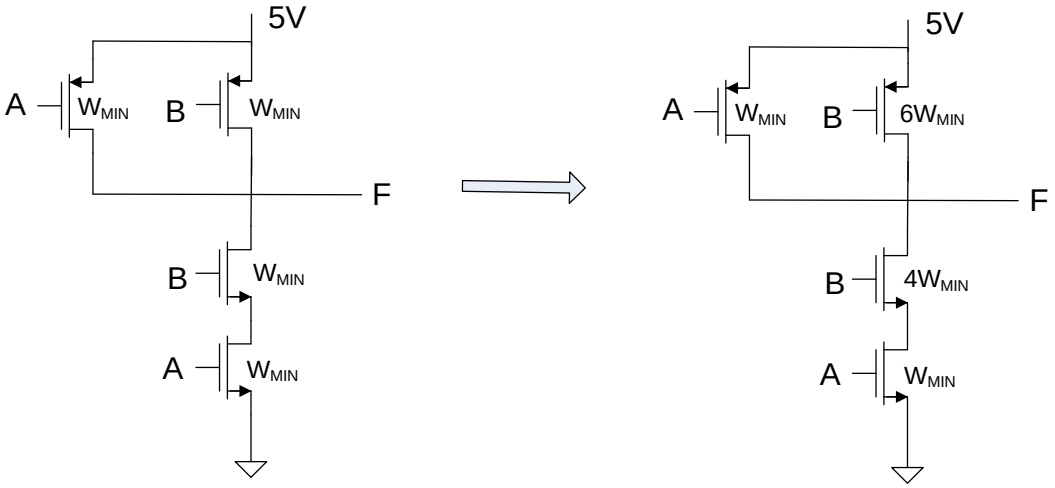
Problem 1 Consider the amplifier below. Determine the small signal voltage gain from the input to the output. Assume the capacitor C is large.

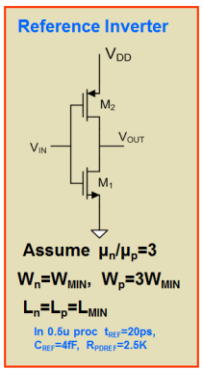


Problem 2 Design a voltage amplifier using any number of MOS transistors that has a nominal dc gain of +5 and that drives a 10KΩ load that is connected to ground. You may use at most 2 DC power supplies, any number of dc current sources, any number of resistors, and any number of capacitors in your design. Your design should include an indication of the values of all components, the dimensions of all transistors, and should include any biasing needed for your circuit to meet the specifications given.

Problem 3 A design engineer determined that a change in sizing of a minimum-sized 2-input NOR gate with inputs A and B was needed. The resized gate is to be an equal worst-case rise and fall structure with an OD of 2. So, before lunch the sizing of the gates for the A input were changed to the correct value but after lunch the designer forgot to change the sizing of the gates for the B input. The original circuit and the changed circuit are shown below. A reference inverter is also shown.

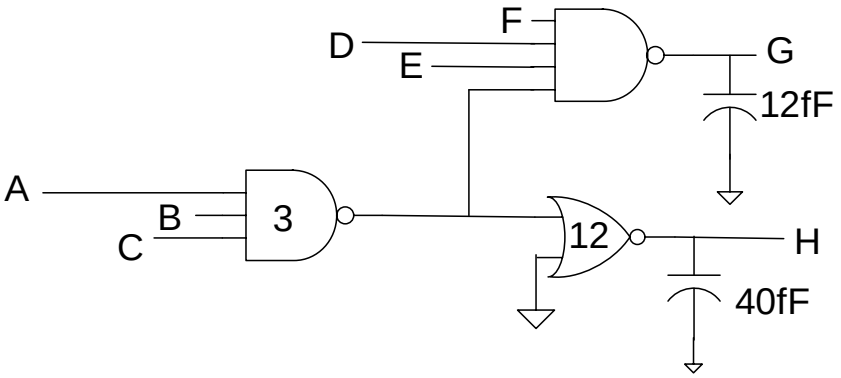
a) Determine the desired t_{HL} for the correctly sized gate with an overdrive of 2 if it is loaded on the output with a capacitor of $10C_{REF}$. (Assume length of all devices is L_{MIN})
b) Determine the actual t_{HL} for the incorrectly-sized gate assuming the same $10C_{REF}$ load
c) Determine the worst-case t_{LH} for the incorrectly-sized gate with the same $10C_{REF}$ load

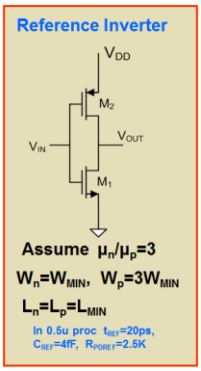




Problem 4 Consider the following circuit. Assume the Boolean inputs B and C are 1 and the supply voltage is 3.5V. A reference inverter is shown below.

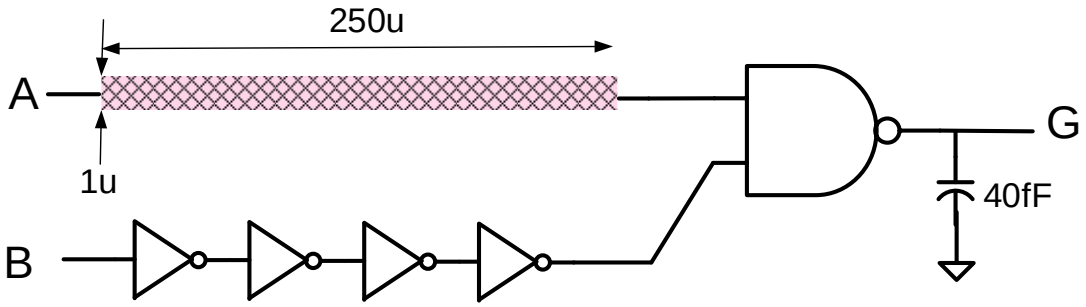
a) Determine the dynamic power dissipation in the 3-input NAND gate with an OD of 3 if the A input is a 100MHz clock signal
b) Repeat part a) if the sizing of the 3-input NAND gate is minimum sized

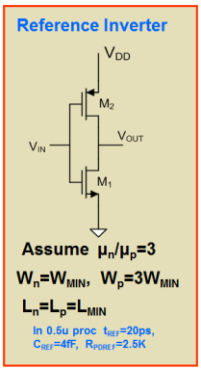




Problem 5 A poly 1 interconnect designed using the process described in the attachment to this exam connects the Boolean input A into a 2-input NOR gate. The dimensions of the interconnect are shown.

a) Determine the propagation delay from A to G assuming the boolean input B=1.
b) If the boolean inputs A and B both transition from 0 to 1 at the same time, determine t_{HL} at the G output



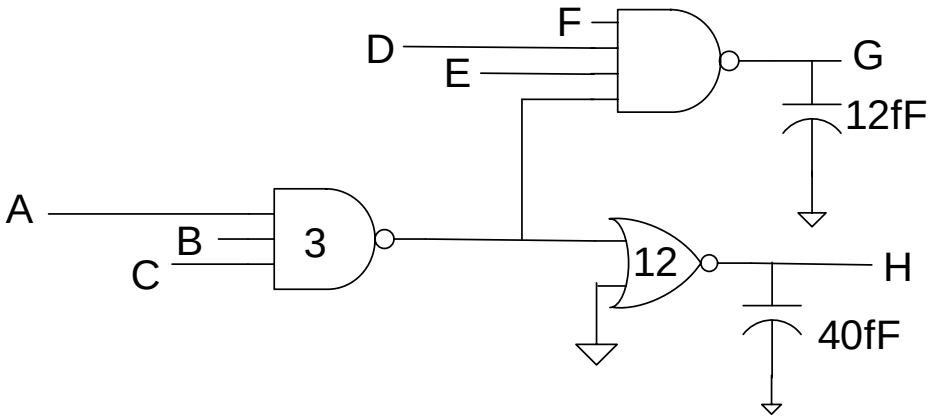


Problem 6 A segment of a logic block is shown below. Assume the lengths of all devices are L_{MIN}. Assume the overdrive factors of all gates, relative to that of an equal rise/fall reference inverter, are as indicated. Gates with no overdrive factor shown have an overdrive of 1. Assume that the process in which these gates are fabricated is characterized by a minimum length equal rise/fall reference inverter with

t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

a) Determine the worst-case propagation delay from **A** to**G**

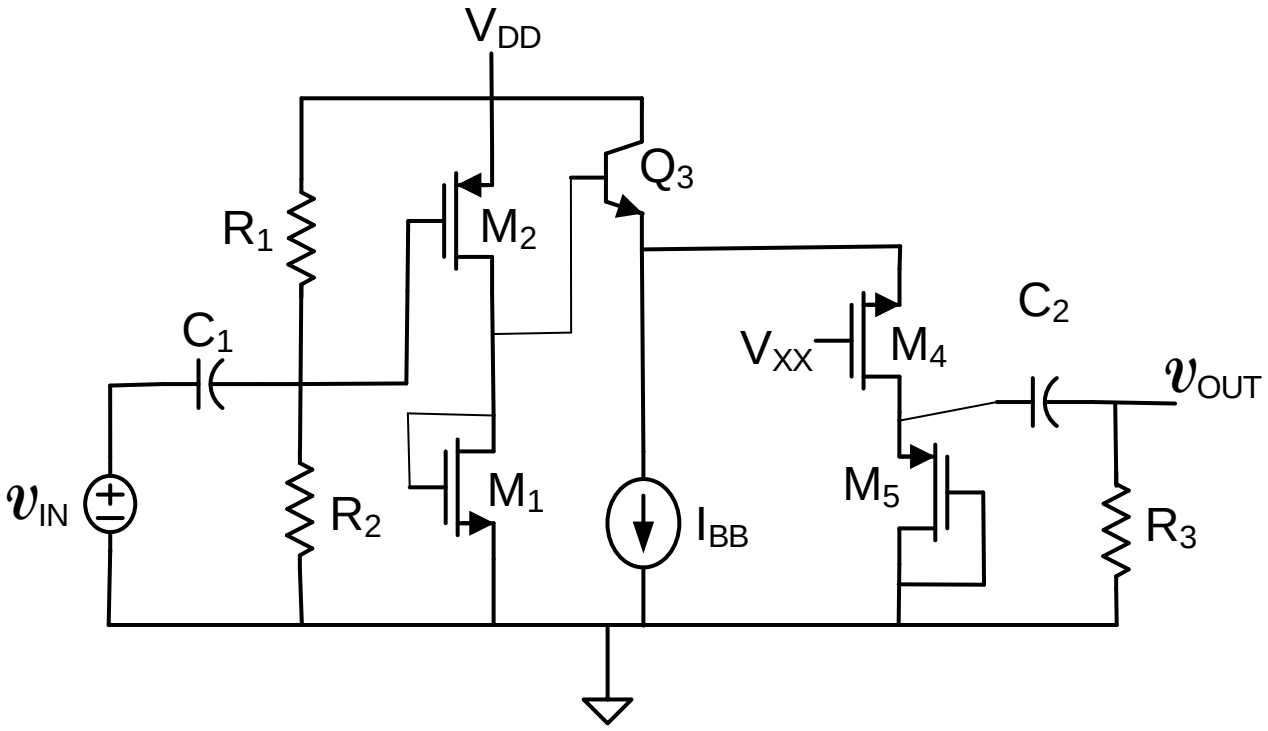
b) Repeat part a) if all gates are all minimum sized



Problem 7 Consider the amplifier block shown below. Assume the capacitors are large and the current gain β of the BJT is also large.

a) Draw the small-signal equivalent circuit of this amplifier assuming the BJT is operating in the forward active region and the MOSFETs are operating in the saturation region

b) Determine the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the components in the circuit



Problem 8 Design, at the transistor level, a circuit using static CMOS gates that implements the Boolean function $F=A+B\bar{C}D$ Assume the inputs **A,B,C** and **D** are available. Size the gates for equal worst-case rise and fall times. The overdrive on all gates should be 1 except for the last stage which should have an overdrive of 5.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

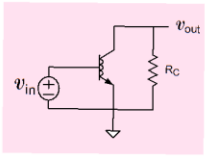
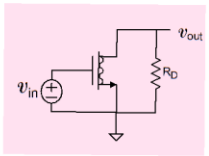
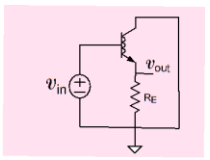
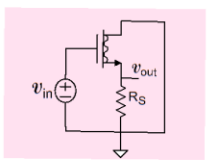
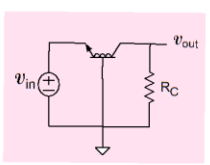
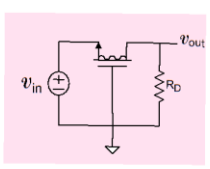
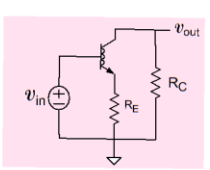
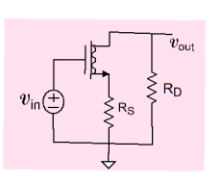
PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

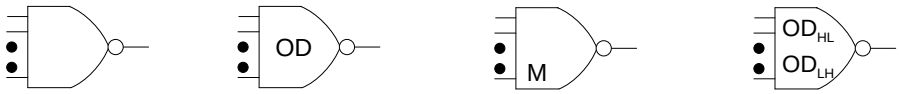
COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

Basic Amplifier Gain Table

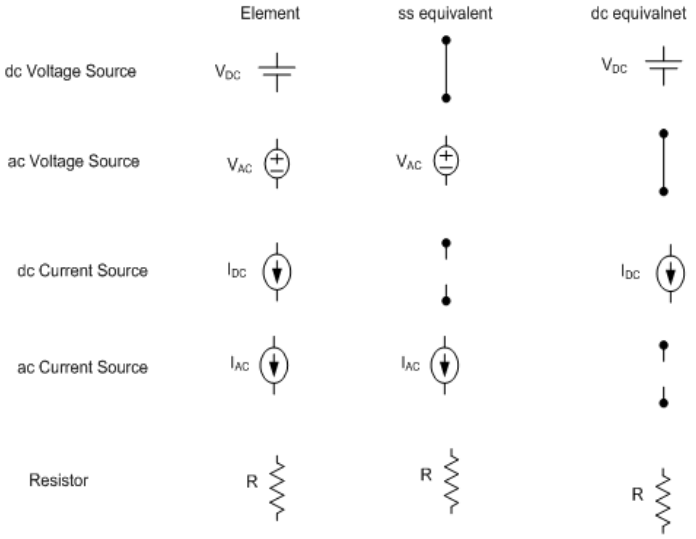
	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
								
A_V	$-g_mR_C$		$\frac{g_m}{g_m+g_E}$		g_mR_C		$-\frac{R_C}{R_E}$	
	$-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$	$\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	$\frac{I_{CQ}R_C}{V_t}$	$\frac{2I_{DQ}R_C}{V_{EB}}$		
R_{in}	r_π		$r_\pi+\beta R_E$		g_m^{-1}		$r_\pi+\beta R_E$	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞
R_{out}	R_C		g_m^{-1}		R_C		R_C	
			$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$				

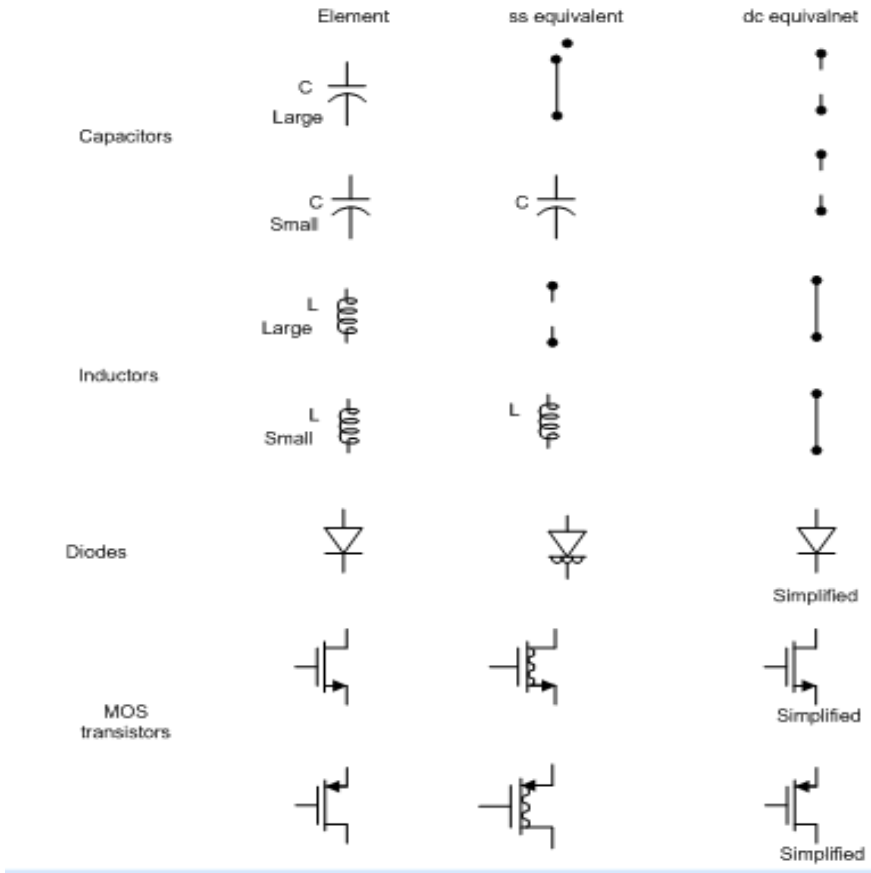
Propagation Delay in Logic Circuits with OD and Asymetry



	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{i(k+1)}$	$\sum_{k=1}^{n} \frac{F_{i(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{i(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{i(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Capacitors
C
Large
C
Small
C
Inductors
L
Large
L
Small
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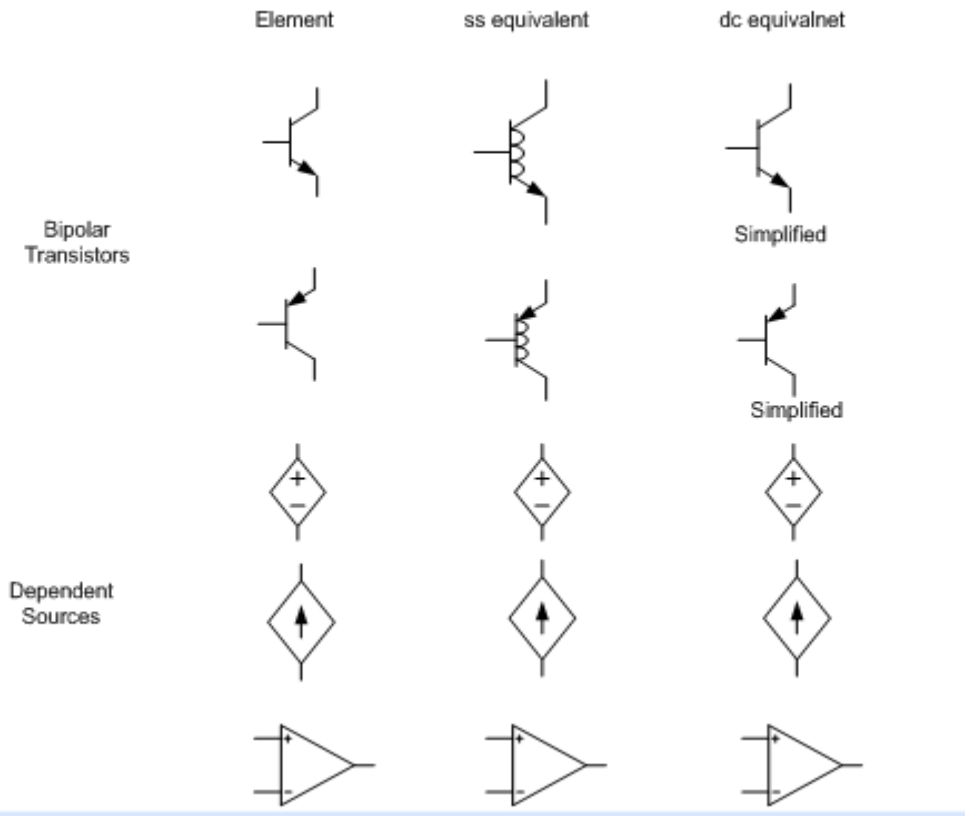
Diodes
Simplified
MOS
transistors
Simplified
Simplified


Element
ss equivalent
dc equivalnet
Bipolar
Transistors
Simplified
Simplified
Dependent
Sources