EE 330 Fall 2012
Homework 9

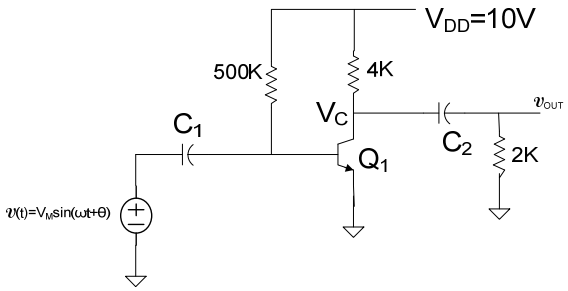
Due Friday October 19 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

There is 16 problems and one extra credit problem. Solve any number of problems such that the total is 100 (excluding the extra credit problem). If you solve more problems than a 100, please indicate which problems you would like to be graded. Otherwise, the grader will arbitrarily choose which problems he/she will grade. Unless stated to the contrary, assume all MOS transistors have model $\mu nCOX=100\mu A/V^2$, $V_{Tn}=1V$, $\mu_n/\mu_p=3$, $V_{Tp}=-1V$ and all BJT transistors have model parameters $J_SA=10^{-12}A$, $\beta n=100$, and , $\beta p=30$.

Problem 1 (10 points):

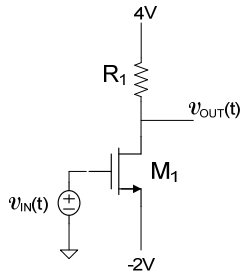
Assume the capacitors are very large.

a) Draw the small signal equivalent circuit for the amplifier shown
b) Determine the quiescent value of V_C and V_{OUT}
c) Obtain the small-signal voltage gain
d) Determine the small-signal output voltage v_{OUT} if $V_M=200mV$

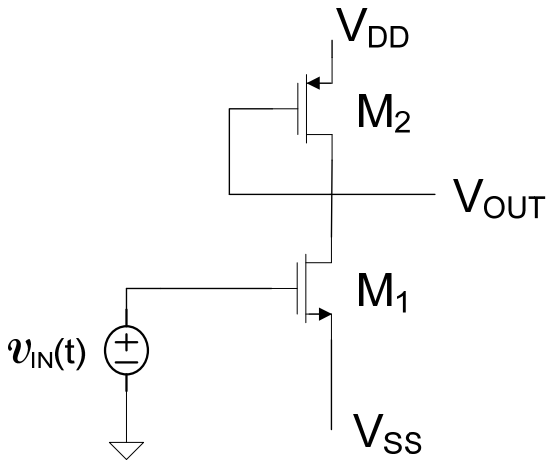


Problem 2 (10 points):

a) Determine the maximum value of R_1 that will keep M_1 in saturation. M_1 has dimensions W=12u and L=2u and $\mu_nC_{OX}=100\mu A/v^2$, $\mu_pC_{OX}=30\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}=-0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda=0$, $\gamma=0$.
b) If R_1 is 1/3 of the value determined in Part a), determine the small signal voltage gain of this circuit.
c) With the value of R_1 used in part b), determine the total output voltage if $v_{IN}(t)=.001\sin(5000t+75^o)$.

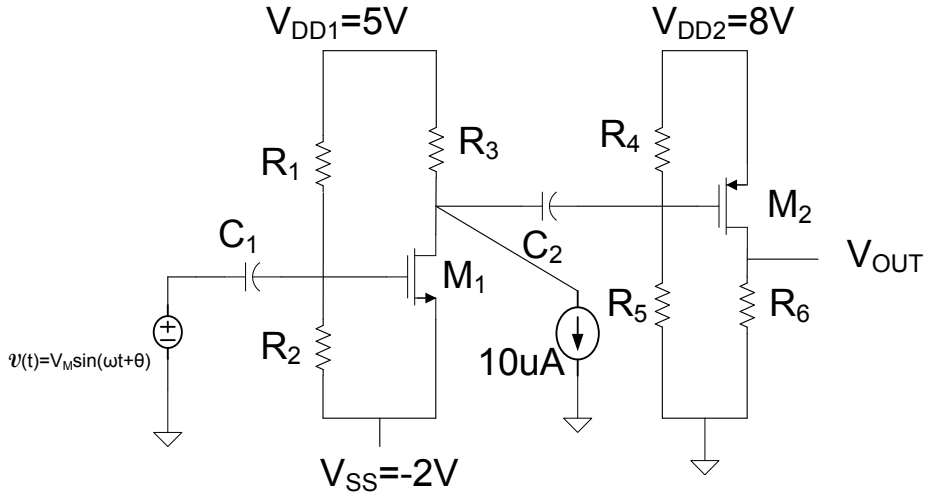


Problem 3 (10 points):
Obtain an expression for the small signal output voltage in terms of the small signal parameters if the input is given by the expression $v_{IN}(t)=V_M\cos(\omega t+\theta)$. Assume M_1 is operating in the saturation region.



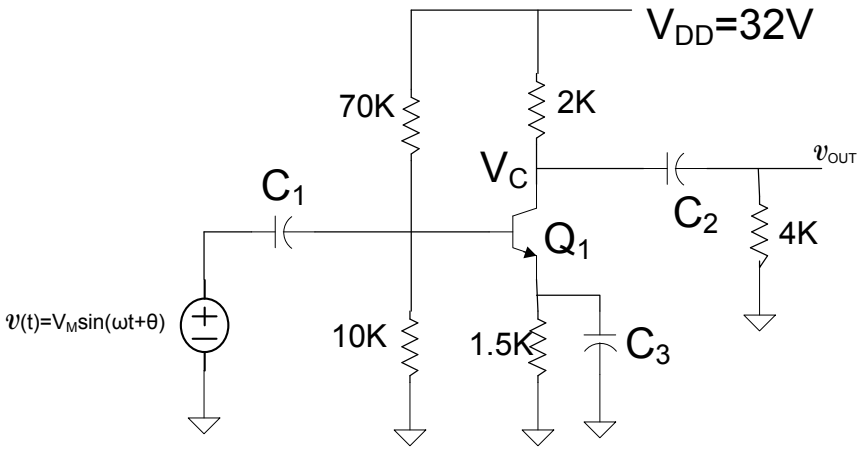
Problem 4 (5 points):
Determine the total output voltage for the circuit in Problem 3 if V_{DD}=5V, V_{SS}=-2V, W_1=15u, L_1=2u, W_2=4.5u and L_2=1u. Assume the process is with parameters $\mu_n C_{OX}=100\mu A/v^2$, $\mu_p C_{OX}=30\mu A/v^2$, V_{TNO}=0.5V, V_{TPO}= - 0.5V, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$.

Problem 5 (5 points):
Obtain the AC equivalent and the DC equivalent circuit for the following network. Assume the transistors are operating in the saturation region and all capacitors are large. You need not solve the circuit.

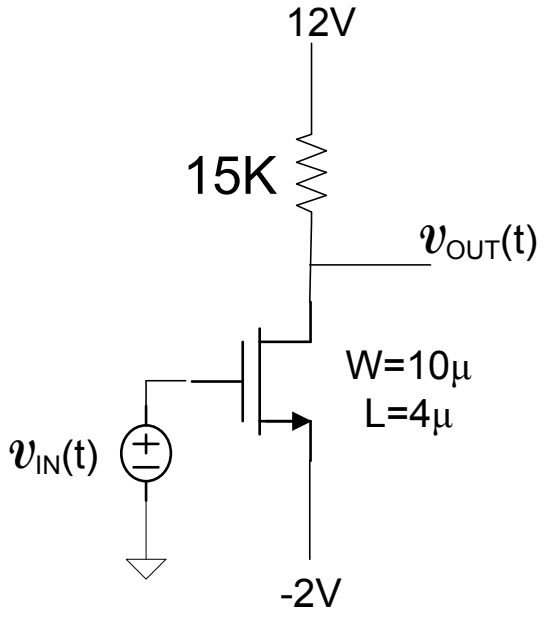


Problem 6 (10 points):
Assume the capacitors are all very large.

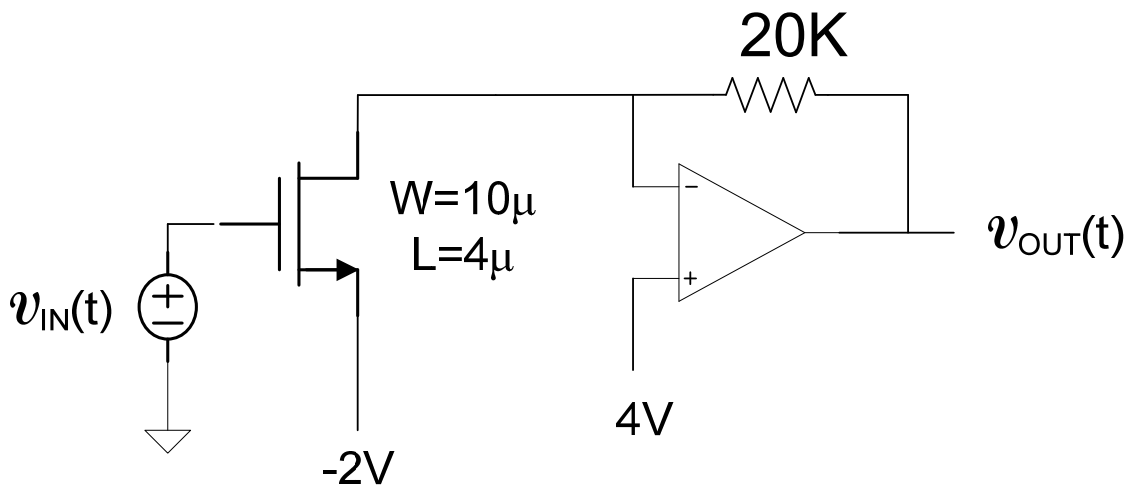
e) Draw the small signal equivalent circuit for the amplifier shown
f) Determine the quiescent value of V_C and V_{OUT}
g) Obtain the small-signal voltage gain
h) Determine the small-signal output voltage v_{OUT} if V_M=200mV



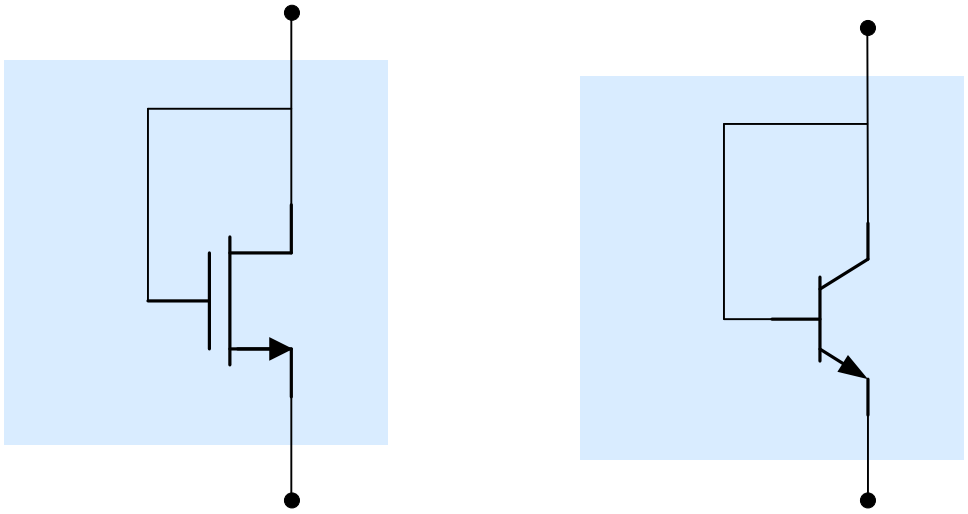
Problem 7 (10 points):
Obtain the quiescent output voltage and the small signal voltage gain.



Problem 8 (10 points):
Determine the small signal output voltage if the small signal input voltage is a sinusoidal 1kHz signal with P-P amplitude of 25mV.



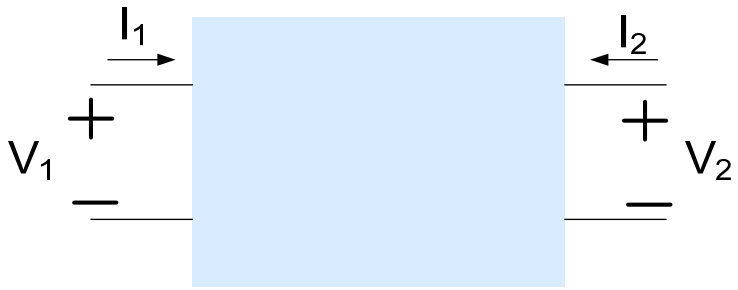
Problem 9 (5 points):
Obtain the small signal impedance between the two terminals exiting the box. Assume the MOSFET is operating in the Saturation region and the BJT in the Forward Active region and that the quiescent currents are both 1mA.



Problem 10 (15 points):
Consider a device characterized by the equations

$$I_1 = V_1^2 V_2^2$$

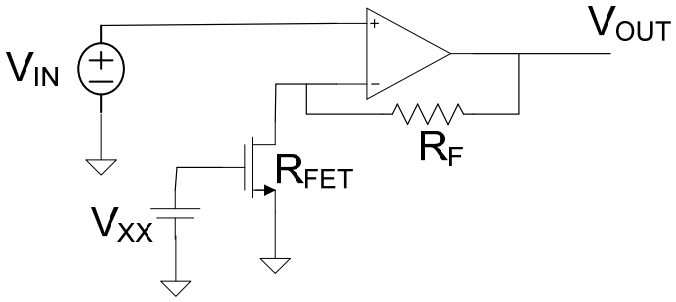
$$I_2 = 0.1e^{0.2V_1 V_2}$$



a. Determine the small signal model for the three-terminal device characterized by the equations given above
b. Determine the numerical values for the small signal model parameters if the quiescent value of the port voltages are V_2=1V, V_1=5V.
c. Determine the quiescent currents at the Q-point established in part b.
d. Determine the small signal currents i_1 and i_2 if the small signal voltages v_1 and v_2 were measured to be $1mV_{RMS}$ and $2mV_{RMS}$ respectively. Assume the same Q-point as established in part b.

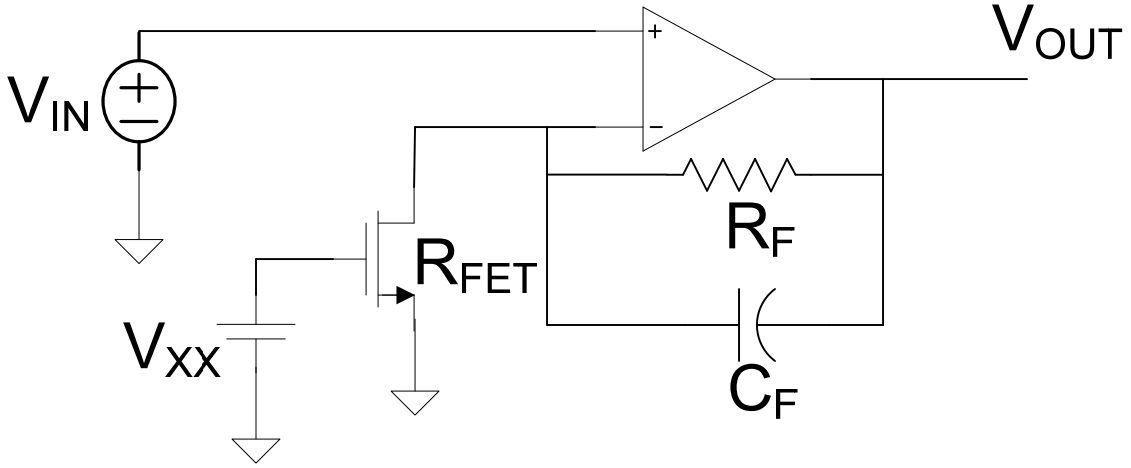
Problem 11 (10 points):
Assume V_{IN} is a low frequency nearly sinusoidal waveform that is below 25mV P-P and that W=12μm, L=1μm for the MOSFET.

a. Determine the voltage gain of this circuit if V_{XX}=2V.
b. How does the voltage gain change if V_{XX} is swept between 1.5V and 4V?



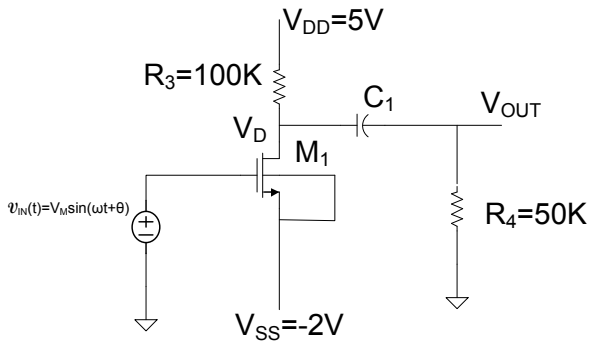
Problem 12 (10 points):
In the circuit shown, R_F=40K, C_F=0.1uF and the MOSFET has dimensions W=6μm, L=2μm. Assume the op amp is ideal.

a) Determine the sinusoidal steady state response if V_{XX}=1.5V and V_{IN}=0.02sin1000t.
b) On the same axis, plot the transfer function V_{OUT}/V_{IN} for V_{XX}=1.5V, 14, and 4V.
c) Obtain an expression for the poles and zeros of the transfer function as a function of V_{XX} and plot as V_{XX} varies between 1.5V and 4V.



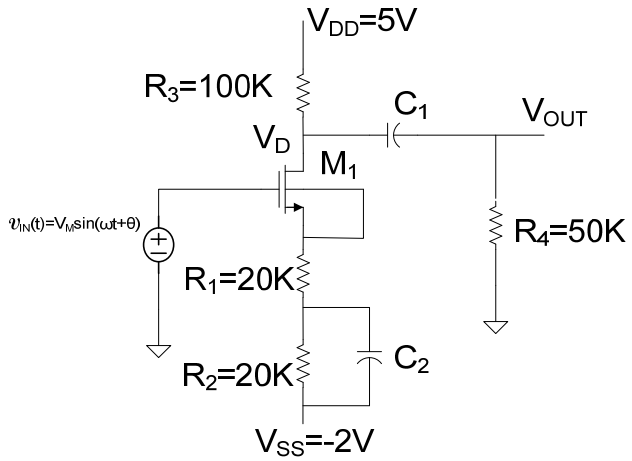
Problem 13 (10 points):
In the circuit shown, the dimensions of the transistor are W=8u and L=10u. Assume C_1 is very large.

a) Draw the small signal equivalent circuit for the amplifier
b) Determine the quiescent value of V_D and V_{OUT}
c) Obtain the small-signal voltage gain
d) Determine the small-signal output voltage v_{OUT} if V_M=20mV

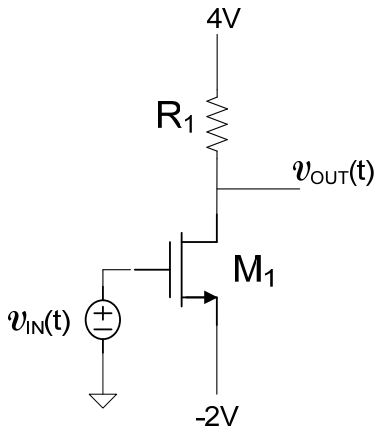


Problem 14 (10 points):
In the circuit shown the dimensions of the transistor are W=10u and L=1u. Assume C_1 and C_2 are very large.

a) Draw the small signal equivalent circuit for the amplifier
b) Determine the quiescent value of V_D and V_{OUT}
c) Obtain the small-signal voltage gain
d) Determine the small-signal output voltage v_{OUT} if V_M=200mV



Problem 15 (10 points):
If R_1=10K, size the device so that the amplifier has a voltage gain of -8.



Problem 16 (15 points):
Design an amplifier using only BJT transistors, resistors, capacitors and voltage sources that has a voltage gain of -20 when driving a 2K resistor.

Problem 17 (Extra Credit of 20 points):
Using Verilog, design a serial-to-parallel converter. The converter should take in a serial input from an external source and output an 8-bit parallel result stored in a register file (just a multi-bit group of flip flops that each store one bit of data). Assume the serial input arrives prior to each rising clock edge from a microcontroller using the same clock signal. Thus, a new bit of serial data is available on each clock pulse to be stored in the register file. In addition to the serial input and clock signal, two other inputs to the system are the active low reset and conversion enable. When reset is low, the parallel register is loaded with 0's. When high, the system resumes normal operation. The conversion enable signal must be set high in order for serial-to-parallel conversions to take place. Otherwise, the incoming serial data is ignored. Finally, when writing the testbench, assume the clock period is 20ns. Please submit the module code, testbench code, and simulation waveform to receive full credit.