

Grades for Sean Gordon

Course

Arrange By



CPR E 381 Spring 2019



Assignment Group



Apply

NAME	DUE	STATUS	SCORE	OUT OF	
Lab 1 Labs	Jan 25, 2019 by 10am	LATE	100%	100	 

SCORE DETAILS

CLOSE

Mean: 95

High: 100

Low: 0



COMMENTS

CLOSE

In the future, include screenshots in the lab report, and a 2 sentence ish explanation of how you know it's working.

Trenton Allison, Jan 26, 2019 at 12:13pm

Lab 3 Labs	Feb 8, 2019 by 10am	LATE	77%	100	 
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SCORE DETAILS



CLOSE



Mean: 76.3

High: 100



Low: 0



NAME	DUE	STATUS	SCORE	OUT OF	
COMMENTS					CLOSE
<p>The zip file contains the updated evaluation form.</p> <p>Lab #3</p> <p>Prelab (10/15 points)</p> <p>10/10 points for Prelab all or nothing</p> <p>0/5 points for team formation; -5 points if the team-related questions are not answered in their reports.</p> <p>Problem 1 (40/40 points)</p> <p>5/5 points for a) interface description</p> <p>5/5 points for b) code</p> <p>5/5 points for c) testing</p> <p>5/5 points for d) & e) description/implementation/testing</p> <p>5/5 points for f) defense of design</p> <p>5/5 points for g) mux design/test</p> <p>5/5 points for h) reg file schematic</p> <p>5/5 points for i) reg file test</p> <p>Problem 2 (27/45 points)</p> <p>3/5 points for interface description of simplified MIPS datapath (-2 o_S should be connected to Data of the reg file, aka not be in the top level diagram)</p> <p>9/10 points for schematic of simplified MIPS datapath (-1 o_S should go to data)</p> <p>15/15 points for correct implementation</p> <p>0/15 points for waveform screenshots that demonstrate the design's operation (-15 waveform doesn't show any functionality)</p> <p>Total: 77/100</p>					<p>Sean Gordon, Feb 8, 2019 at 10:24am</p> <p>Trenton Allison, Feb 8, 2019 at 3:45pm</p>
Lab 2	Feb 1, 2019 by 10am	LATE	90%	100	 
SCORE DETAILS					CLOSE
Mean: 82.1 High: 100 Low: 0					<input type="text"/> <input type="button" value=""/>

NAME	DUE	STATUS	SCORE	OUT OF	
COMMENTS CLOSE					
<p> <i>Prelab 10/10</i> <i>Problem 1 (20/20 points)</i> <i>5/5 a) structural code</i> <i>5/5 b) dataflow code</i> <i>10/10 ModelSim simulation</i> <i>Problem 2 (20/20 points)</i> <i>3/3 a) description</i> <i>4/4 b) structural code</i> <i>4/4 c) structural nbit code use 1 sel bit</i> <i>4/4 d) dataflow code use 1 sel bit</i> <i>5/5 e) simulation code and output</i> <i>Problem 3 (14/20 points)</i> <i>3/3 a) description</i> <i>4/4 b) structural code</i> <i>2/4 c) structural nbit code -2 Cout should carry to next cin of adder</i> <i>2/4 d) dataflow code -2 Cout should carry to next cin of adder</i> <i>3/5 e) simulation code and output -2 Cout should carry to next cin of adder</i> <i>Problem 4 (26/30 points)</i> <i>10/10 a) description</i> <i>6/10 b) structural code -4 not ripple carry</i> <i>10/10 a thorough test</i> <i>Total: 90/100</i> </p>					<p>Trenton Allison, Feb 4, 2019 at 11:57pm</p>
Lab 4 Labs	Feb 15, 2019 by 10am	LATE	52%	100	 

SCORE DETAILS CLOSE				
Mean: 71.8	High: 100	Low: 0	<div> <div></div> <div></div> </div>	

NAME	DUE	STATUS	SCORE	OUT OF	
COMMENTS					CLOSE
<p><i>Prelab</i></p> <p><i>Lab #4 (100 points)</i></p> <p><i>Prelab (10/10 points)</i></p> <p><i>Problem 1 (20/20 points)</i></p> <p><i>5/5 points for a) correct examples/types for immediate extended instructions</i></p> <p><i>10/10 points for b) code for each extender component (16-bit, signed/zero)</i></p> <p><i>5/5 points for c) test for each extender component</i></p> <p><i>Problem 2 (22/30 points)</i></p> <p><i>15/15 points for a) correctly modified dmem.hex file</i></p> <p><i>7/15 points for b) test/simulation of dmem testbench (-5 did not move vales from mem into 256, -3 very few test cases)</i></p> <p><i>Problem 3 (8/40 points) (not demoed)</i></p> <p><i>8/10 points for a) description of new control signals for the simple processor (-2 need mem/alu signal for reg data in)</i></p> <p><i>0/10 points for b) schematic of simple processor with extenders and data memory (-2 missing alu/mem mux, -4 missing memory, -2 missing sign extend, -2 o_s should go to mem address and reg data)</i></p> <p><i>0/20 points for c) test simple processor.</i></p> <p><i>Total = 52/ 100</i></p>					<p><i>Sean Gordon, Feb 8, 2019 at 9:20am</i></p> <p><i>Trenton Allison, Feb 15, 2019 at 6:24pm</i></p>
HW0					
Homework	Jan 23, 2019 by 11:59pm		89%	100	 
SCORE DETAILS					CLOSE
Mean: 83.7	High: 100	Low: 0	<input type="text"/> <input type="button" value=""/>		

NAME	DUE	STATUS	SCORE	OUT OF
COMMENTS				CLOSE

1. Review

- a. 10/10 points:
- b. 3/5 points: -2 not supporting 2 bit wide data
- c. 7/10 points: -2 zero needed a not gate,-1 "0000" lights positive (label inputs next time)
- d. 2/5 points: -3 no work
- e. 7/10 points: -3 no work

2. Introduction to computers

Trenton Allison, Jan 25, 2019 at 1:04pm

3. Canvas

- a. 10/10 points

Total 39/50

2. Introduction to computers

- a. 16/16
- b. 16/16
- c. 18/18

Ashraf Shaikh-Mohammed, Jan 26, 2019 at 9:53am

Total 50/50

HW1

Homework

Jan 28, 2019 by 11:59pm

81%

100



SCORE DETAILS				CLOSE
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Mean: 78.8

High: 100

Low: 0

Assessment by Rohit Sahu

[Close Rubric](#)

NAME	DUE	STATUS	SCORE	OUT OF
HW1 RUBRIC				
CRITERIA	RATINGS			PTS
ISA Part a view longer description	6 pts Full Marks	0 pts No Marks		5 / 6 pts
	Comments ii. Memory-memory operations (correct is CISC-like) so -1			

NAME DUE STATUS SCORE OUT OF

HW1 RUBRIC

CRITERIA	RATINGS		PTS
ISA Part b view longer description	12 pts Full Marks	0 pts No Marks	6 / 12 pts
	Comments i. Number of named registers (correct is ISA)so -1 ii. Number of cycles an instruction takes to execute (correct is uArch) so -1 iii. Whether or not immediate operands can be used directly in arithmetic instructions (correct is ISA) so +1 iv. Which register number is the stack pointer (correct is ABI, ISA) so +1 v. Which, if any, registers numbers produce constants (e.g., 0 or -1) (correct is ISA) so +1 vi. Which register numbers pass arguments to function calls (correct is ABI) so -1 vii. Which register numbers are temporary or saved (correct is ABI) so -1 viii. Addressable address range for memory operations (correct is ISA) so -1 ix. Type of adder used in the ALU (correct is uArch) so +1 x. Which instructions update the PC (correct is ISA) so -1 xi. Which bits of an instruction correspond to the opcode or an operand (correct is ISA) so +1 xii. Number of functional units in the processor (correct is uArch) so +1		
MIPS Part a view longer description	9 pts Full Marks	0 pts No Marks	9 / 9 pts

NAME DUE STATUS SCORE OUT OF

HW1 RUBRIC

CRITERIA	RATINGS		PTS
MIPS Part b view longer description	14 pts Full Marks	0 pts No Marks	9 / 14 pts
	Comments -5: Missing explanation for absence of MOV		
MIPS Part c view longer description	5 pts Full Marks	0 pts No Marks	5 / 5 pts
MIPS Part d view longer description	25 pts Full Marks	0 pts No Marks	23 / 25 pts
	Comments -2: You should be using addi for remainder		
Mars Part a view longer description	5 pts Full Marks	0 pts No Marks	5 / 5 pts
	Comments MARS effectively simulates the MIPS ISA and some small amount of the ABI (e.g., syscalls and named registers). It certainly does not simulate microarchitectural characteristics where operations may take multiple cycles, etc. Although MARS does understand the ABI, it certainly is faithful to the ISA where pseudo instructions can be broken down into their composite parts and simulated as individual steps.		
Mars Part b view longer description	14 pts Full Marks	0 pts No Marks	14 / 14 pts

NAME	DUE	STATUS	SCORE	OUT OF
HW1 RUBRIC				
CRITERIA	RATINGS			PTS
Mars Part c view longer description	10 pts Full Marks	0 pts No Marks		5 / 10 pts
	Comments -5: Minor error: Your program returns floor instead of ceil. For e.g. input of 3 and 4 gives 3 not 4 (ceil[3.5]). Reason is that you missed to add one before division and when I change that your code works perfectly.			
Total Points: 81				

HW2

Homework

Feb 4, 2019 by 11:59pm

LATE

0%

100

×



SCORE DETAILS

CLOSE

Mean: 63.1

High: 100



Low: 0

COMMENTS

CLOSE

Wrong homework submitted

Ashraf Shaikh-Mohammed, Feb 6, 2019 at 6:51am

NAME	DUE	STATUS	SCORE	OUT OF	
HW3 Homework	Feb 11, 2019 by 11:59pm		36%	100	×  

SCORE DETAILS

[CLOSE](#)

Mean: 46.8

High: 100

Low: 0

COMMENTS

[CLOSE](#)

Part2: 5/53

a. (5/15)

-10: saturating and abs logic missing...instead of add you should be using subu to subtract unsigned values...abs is a pseudo instruction i.e it must be implemented. Saturation is the process of assigning the maximum unsigned value when the subtraction of unsigned input values i.e. a signed value overflows.

Rohit Sahu, Feb 13, 2019 at 12:55am

b. (0/15)

c. (0/15)

d. (0/8):

Part1:

a. 15/15



Ashraf Shaikh-Mohammed, Feb 13, 2019 at 8:29am

b. 21/32: Couple minor mistakes but no hex and decimal given

Subtotal: 36/47

a. 5/15 (Revised): Major Logical flaw, goal to make number same as immediate. How do you loop?

Ashraf Shaikh-Mohammed, Mar 4, 2019 at 1:11pm

NAME	DUE	STATUS	SCORE	OUT OF	
HW4	Feb 25, 2019 by 11:59pm		98%	100	 
Homework					

SCORE DETAILS

CLOSE

Mean: 91.5

High: 100



Low: 0

COMMENTS

CLOSE

2a: a byte is 8 bits; 18 implies decimal and not hexadecimal

Henry Duwe, Feb 28, 2019 at 2:49pm

HW5	Mar 4, 2019 by 11:59pm		78%	100	 
Homework					

SCORE DETAILS

CLOSE

Mean: 50.8

High: 95

Low: 0

+

NAME	DUE	STATUS	SCORE	OUT OF
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COMMENTS

[CLOSE](#)

1.

Quality: 13/15

Test #2:

-2 incorrect assembly format, "FFFF" needs to be "0xFFFF"

Test #3:

-0 same as above

Formatting: 15/15

Completeness: 15/15

Ryan Toepfer, Mar 12, 2019
at 11:58am

subtotal: 43/45

2. Processor Implementation Details (8/25 points)

a. 3/15 points: (-2 missing PC, -2 missing I_Mem, -2 missing RT/Imm MUX, -2 missing ALU_MEM MUX, -2 missing ALU_MEM MUX, -2 missing control)

b. 0/5 points: (-2 don't extra read ports, -3 dont need extra alu outputs)

c. 5/5 points: ()

3. Processor Cycle Time Determination (27/30 points)

a. 5/5 points r type: ()

4/5 points lw : (-1 for added mux before ALU (that mux already has its value)

3/5 points cond : (-1 for added mux before ALU(that mux already has its value), -1 for missing and)

b. 6/6 points for the correct ranking ()

9/9 points for justification ()

Trenton Allison, Mar 30, 2019
at 6:30pm

subtotal: 35/55

HW6

Homework

Mar 13, 2019 by 11:59pm

76%

100



SCORE DETAILS



[CLOSE](#)

Mean: 37.1



High: 99

Low: 0



NAME	DUE	STATUS	SCORE	OUT OF
COMMENTS				CLOSE
Performance Analysis:				
A.) Average CPI (20/20):				Ashraf Shaikh- Mohammed, Mar 19, 2019 at 12:06pm
B.) Better Performance (15/20): Breakeven frequency calculation is not apt.				
Total: 35/40				
2. Amdahl's Law (41/60 points)				
a. 13/20				Rohit Sahu, Mar 23, 2019 at 4:11pm
5/5 points for using Mars				
5/5 points for a reasonable estimation of total number of clock cycles				
3/5 points for reasonable estimation of fraction of cycles that software multiplier requires..-2 not quite correct see soln..you can calculate this by subtracting the total clock cycles for software to total clock cycles by hardware to get the difference. if you see the assembly code for multiply in prob2softfloat.s it consists of much more than 14 inst. Though your approach is correct!				
0/5 points for reasonable assumptions. -5 No assumptions stated. a big assumption here is that the hardware multiplier has no effect on the clock frequency in the assumed single cycle processor.				
b. 13/20				
5/5 points for identifying correct portion that can be accelerated by hardware multiplier.				
5/5 points for calculating reasonable speed up factor and improvement factor				
3/5 points for calculating reasonable maximum speed up possible...-2 because of incorrect f value				
0/5 points for reasonable assumptions. -5 No assumptions stated..a big assumption here is that the hardware multiplier has no effect on the clock frequency in the assumed single cycle processor.				
c. 15/20				
7/10 points for correctly scaling the formula..-3 the whole set of instr will be penalized including 1-f fraction..see soln				
8/10 points for reasonable maximum speedup possible...-2 approach is correct but values are off.				
HW7	Mar 27, 2019 by 11:59pm		85%	100
Homework				 

NAME	DUE	STATUS	SCORE	OUT OF
SCORE DETAILS				CLOSE
Mean: 51	High: 100	Low: 0	<div> <div></div> <div></div> </div>	
COMMENTS				CLOSE
<p>1. Pipeline Cycle Time (20 points)</p> <p>a. 5/10 points for correct cycle time; (the PC is a register, and so it breaks up the mux and the i_mem, also dmem is longer)</p> <p>5/5 points for specifying that the longest stage sets the cycle time;</p> <p>0/5 points for some justification of why the memory stage is the longest stage</p> <p>subtotal = 10 / 20</p>				Trenton Allison, Mar 28, 2019 at 5:40pm
<p>2. Pipeline Simulation (35/40):</p> <p>PCSrc MUX 1 values are technically not blank/unknown, they're unused. For instance, 4th cycle, its 0x0000401c. minor errors</p>				Ashraf Shaikh-Mohammed, Apr 8, 2019 at 11:42am
<p>4. Computer architecture in media (15/15):</p> <p>Nicely done!!</p> <p>subtotal: 50/55</p>				
<p>3. Exam question</p> <p>Q 15/15</p> <p>A 10/10</p> <p>subtotal = 25/25</p>				Henry Duwe, Apr 17, 2019 at 3:20pm
Homework 7 Question 3	Mar 27, 2019 by 11:59pm		0%	0
Homework				

NAME	DUE	STATUS	SCORE	OUT OF	
HW8					
Homework	Apr 8, 2019 by 11:59pm		95%	100	 

SCORE DETAILS

CLOSE

Mean: 66.8

High: 100

Low: 0





COMMENTS

CLOSE

2. Pipeline Hazard Test Case Generation (50/50 points)

Rohit Sahu, Apr 16, 2019 at 10:48am
1. -5 address generation is incorrect

Henry Duwe, Apr 18, 2019 at 1:40pm
- subtotal: 45/50

HW9					
Homework	Apr 15, 2019 by 11:59pm		90%	100	 


SCORE DETAILS

CLOSE

Mean: 51.3

High: 100

Low: 0



NAME	DUE	STATUS	SCORE	OUT OF
<div>COMMENTS<div>CLOSE</div></div>				
<div>2. Cache concepts</div> <div>5.2.1 (10/10):</div> <div>5.2.2 (15/15):</div> <div>5.2.3 (15/25): incorrect way of solving, C1 and C2 are not same as 5.2.1 n 5.2.2, C2 is best design though</div> <div>5.2.6 (5/5):</div> <div>Sub-total (45/55)</div> <div>1. Principle of Locality<div>a. 15/15 points:</div><div>b. 15/15 points:</div><div>c. 15/15 points: (note that the problem asked for c code)</div></div> <div>Subtotal: 45/45</div>				
HW10	Apr 22, 2019 by 11:59pm		60%	100
Homework				<div>×</div> <div><div></div><div></div></div>



SCORE DETAILS				CLOSE
Mean: 45.4	High: 100	Low: 0	<div> <div></div> <div><div></div></div> </div>	

NAME	DUE	STATUS	SCORE	OUT OF
<div>COMMENTS</div> <div>CLOSE</div>				
1. 20/20 3. 0/25		Rohit Sahu, Apr 23, 2019 at 7:59pm		
2. Cache config and sim (40/55): a. (12/12): b. (8/8): c. (10/15): d. (10/20):		Ashraf Shaikh-Mohammed, Apr 26, 2019 at 10:49am		
HW11 Homework	Apr 29, 2019 by 11:59pm	32%	100	×



<div>SCORE DETAILS</div> <div>CLOSE</div>				
Mean: 34.1	High: 100	Low: 0		

<div>COMMENTS</div> <div>CLOSE</div>				
a. 0/18 points: 6 points for the results of each command b. 0 points c. 10/20 points: 0/10 points for generating the time vs j plot; 5/5 points for correctly identifying the interesting inflection point; 5/5 points for for justification/reasoning. d. 10/20 points: 0/10 points for generating the time vs j plot; 5/5 points for correctly identifying the interesting inflection point; 5/5 points for for justification/reasoning. e. 0/20 points: 0/10 points for generating the time vs j plot; 0/5 points for correctly identifying the interesting inflection point; 0/5 points for for justification/reasoning. f. 12/22 points: 0/6 points for total data size consistent with previous answers; 8/8 points for identifying processor; 4/4 points for looking up L1 cache values; 0/4 points for confirming their values were correct Total 32 / 100	Trenton Allison, May 8, 2019 at 8:04pm			

NAME	DUE	STATUS	SCORE	OUT OF	
Homework 10 Question 3 Homework	Apr 22, 2019 by 11:59pm		0	0	
Project Part 1 Project	Mar 1, 2019 by 10am	LATE	93%	300	 

SCORE DETAILS

CLOSE


Mean: 261.3High: 300Low: 0

COMMENTS



CLOSE

Previous report pdf was corrupted, re-submitting.

Sean Gordon, Mar 1, 2019 at 10:20am

NAME	DUE	STATUS	SCORE	OUT OF	
COMMENTS					CLOSE
<p>Project Part 1 (100 points)</p> <p>Prelab (10/10 points)</p> <p>Problem 1 (29/30 points)</p> <p>6/6 points for srl vs sra explanation</p> <p>6/6 right shifter vhdl code + explanation (could have reused the right shifter to do signed or undigned)</p> <p>5/6 left shifter vhdl code + explanation (-1 you didn't flip the bits to shift like you said you did in the report)</p> <p>6/6 points for waveforms</p> <p>6/6 points for reasonably helpful explanation of waveform (-3 "we tested" is not enough)</p> <p>Problem 2 (24/25 points)</p> <p>9/10 points for reasonable ALU schematic (-1 overflow should not go high when unsigned)</p> <p>5/5 points for challenges</p> <p>5/5 points for waveforms</p> <p>5/5 reasonably helpful explanation of waveform</p> <p>Problem 3 (30/35 points)</p> <p>10/10 points for a test program that is reasonably comprehensive;</p> <p>5/10 points for a reasonable justification that their testing plan is comprehensive; (-5 points if it is just that every instruction is tested or something similarly short and shallow)</p> <p>15/15 points for waveforms and reasonably helpful explanation (-10 no explanation)</p> <p>Total = 93/100</p>					Trenton Allison, Mar 10, 2019 at 10:35pm
Project Part 1 Individual Feedback	Mar 1, 2019 by 10am		✓	0	
Project					
Project Part 2a	Mar 15, 2019 by 10am	LATE	0%	0	
Project					
COMMENTS					CLOSE

NAME	DUE	STATUS	SCORE	OUT OF
COMMENTS				CLOSE
Submitted late as I was working with Duwe.				Sean Gordon, Mar 15, 2019 at 12:38pm
Please upload the report, bbubblesort.s and your demo sheet.				Trenton Allison, Apr 5, 2019 at 10:57pm
Report:				
Part A (5/25 Points)				
Problem 1 (5/10 points)				
0/5 points for a spreadsheet of control signal values for each of the required instructions.				
5/5 points for a complete control unit				
Problem 2 (0/5 points)				
Problem 3 (0/10 points)				
0/10 points for a test application that makes use of every instruction needed for part a with a helpful explanation.				
Part B (0/45 points)				
Problem 4 (/5 points)				
5 points for updating spreadsheet of control signal values.				
Problem 5 (/10 points)				
5 points for an attempt at a function to control the different control flow-related instructions and for a list of additional control signals need for the schematic.				Trenton Allison, Apr 5, 2019 at 10:58pm
5 points for a schematic of the instruction fetch logic and other modifications needed.				
Problem 6 (/15 points + /10 EC)				
5 point for test program that tests all instructions, with a helpful explanation.				
10 points for bubblesort				
0/10 Extra Credit points fully implemented and simulated merge sort program in their processor (all or nothing).				
Problem 8 (15 points)				
/5 points for demonstrating in some way a correct synthesis by including the synthesis log.				
/5 points for reporting a reasonable critical path that is tracked through their top-level modules (PC -->Memory --> reg file --> ALU --> Memory, etc), if not the specific signals of the design (PC bit 0 --> Memory address 0 --> reg file address A bit 0 --> register file mux select line bit 0, etc).				
/5 points for Fmax				
Report subtotal: --/70				
Need demo sheet for grade				

NAME	DUE	STATUS	SCORE	OUT OF	
Project Part 2b Project	Mar 29, 2019 by 10am	LATE	89.4%	1,000	 

SCORE DETAILS

CLOSE

Mean: 836.9

High: 1,000

Low: 0

COMMENTS



CLOSE

See attached files.

 [Download sub_report.html](#)

Ryan Toepfer, Apr 5, 2019 at 2:10pm

NAME	DUE	STATUS	SCORE	OUT OF
COMMENTS				CLOSE
<p>Correctness: 60/84 * 30% = 21.4/30</p> <p>Report:</p> <p>Part A (25/25 Points)</p> <p>Problem 1 (10/10 points)</p> <p>5/5 points for a spreadsheet of control signal values for each of the required instructions.</p> <p>5/5 points for a complete control unit</p> <p>Problem 2 (5/5 points) (good .do file)</p> <p>Problem 3 (10/10 points)</p> <p>10/10 points for a test application that makes use of every instruction needed for part a with a helpful explanation.</p> <p>()</p> <p>Part B (33/45 points)</p> <p>Problem 4 (5/5 points)</p> <p>5/5 points for updating spreadsheet of control signal values.</p> <p>Problem 5 (5/10 points)</p> <p>0/5 points for an attempt at a function to control the different control flow-related instructions and for a list of additional control signals need for the schematic.</p> <p>5/5 points for a schematic of the instruction fetch logic and other modifications needed.</p> <p>Problem 6 (15/15 points + 0/10 EC)</p> <p>5/5 point for test program that tests all instructions, with a helpful explanation. ()</p> <p>10/10 points for bubblesort</p> <p>0/10 Extra Credit points fully implemented and simulated merge sort program in their processor (all or nothing).</p> <p>Problem 8 (8/15 points)</p> <p>2/5 points for demonstrating in some way a correct synthesis by including the synthesis log. (-3 synthesis did not complete)</p> <p>3/5 points for reporting a reasonable critical path that is tracked through their top-level modules (-2 critical path should not go through reg file and sign extender)</p> <p>3/5 points for Fmax (-2 missing actual Fmax)</p> <p>Report subtotal: 58/70</p> <p>Total: 89.4 / 100 (not all demoed)</p> <p>Need demo sheet for grade</p> <p>Also need Individual project 2 feedback for grade</p>				
				Trenton Allison, Apr 6, 2019 at 10:54pm

NAME	DUE	STATUS	SCORE	OUT OF	
Project Part 2 Individual Feedback Project	Mar 29, 2019 by 10am	LATE	✓	0	
Project Part 3a Project	Apr 12, 2019 by 10am	LATE	0%	0	
Project Part 3b Project	Apr 26, 2019 by 10am	LATE	92.6%	1,000	 

SCORE DETAILS


CLOSE

Mean: 774.6High: 1,000Low: 0

COMMENTS


CLOSE

Part A

Download sub_report.html

Ryan Toepfer, May 4, 2019 at 1:29pm

Part B

Download sub_report.html

Ryan Toepfer, May 5, 2019 at 5:02pm



NAME	DUE	STATUS	SCORE	OUT OF
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<div>COMMENTS</div> <div> <p>Part A (35/35):</p> <p>problem 2 (5/5):</p> <p>problem 3 (20/20):</p> <p>problem 4 (10/10):</p> <p>-----</p> <p>Part B (35/35):</p> <p>problem 5 (5/5):</p> <p>problem 6 (3/5): No test bench, but you can stall</p> <p>problem 7-8 (5/5):</p> <p>problem 10 (10/10):</p> <p>problem 12 (10/10):</p> <p>-----</p> <p>67/70</p> <p>Correctness (30 points):</p> <p>synthetic benchmark (5/5): Part A (2.5/2.5), Part B (2.5/2.5)</p> <p>Bubble sort (5/5) : Part A (2.5/2.5), Part B (2.5/2.5)</p> <p>Fraction of total test case passed (15.6/20): PartA= 65/83 PartB= 64/83</p> <p>Total (25.6/30)</p> </div>				
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Trenton Allison, May 10, 2019 at 11:58pm

<div>Project Part 3 Individual Feedback</div> <div>Project</div>	Apr 26, 2019 by 10am	LATE	✓	0
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<div>Project Part 4</div> <div>Project</div>	May 3, 2019 by 10am		94%	700
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NAME	DUE	STATUS	SCORE	OUT OF
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SCORE DETAILS

CLOSE

Mean: 601.7

High: 700

Low: 0

COMMENTS

CLOSE

This is not the portion that makes all of the effort worth it.

Problem 1 (5/5 points)
Problem 2 (34/36 points) -2 part 2 did not synthisize
Problem 3 (25/25 points)
Problem 4 (5/5 points)
Problem 5 (5/5 points)
Problem 6 (9/12 points) -2 no talk about a program that preforms better on 3b
Problem 7 (10/12 points) -1 no resolution for delta cycles, -1 no resolution for propogating

Total: 94/100

Sean Gordon, May 2, 2019 at 5:59pm











Trenton Allison, May 5, 2019 at 11:07pm

Lec1,2	Jan 16, 2019 by 11:59pm	0%	1	×	📄
Participation					

Lec2,1	Jan 23, 2019 by 10am	1	1		📄
Participation					

Lec2,2	Jan 25, 2019 by 10am	1	1		📄
Participation					



Lec1,3	Jan 18, 2019 by 11:59pm	1	1		📄
Participation					

NAME	DUE	STATUS	SCORE	OUT OF	
Lec3,1 Participation	Jan 28, 2019 by 10am		1	1	
Lec3,3 Participation	Feb 1, 2019 by 10am		1	1	
Lec4,1 Participation	Feb 4, 2019 by 10am		1	1	
Lec4,2 Participation	Feb 6, 2019 by 10am		1	1	
Lec4,3 Participation	Feb 8, 2019 by 10am		1	1	
Lec5,1 Participation	Feb 11, 2019 by 10am		1	1	
Lec5,2 Participation	Feb 13, 2019 by 10am		1	1	
Lec5,3 Participation	Feb 15, 2019 by 10am		100%	1	 
Lec6,1 Participation	Feb 20, 2019 by 10am		1	1	

NAME	DUE	STATUS	SCORE	OUT OF	
Lec10,1 Participation	Mar 25, 2019 by 10am		1	1	
Lec7,2 Participation	Feb 27, 2019 by 10am		1	1	
Lec13,2 Participation	Apr 17, 2019 by 10am		1	1	×
Lec6,2 Participation	Feb 22, 2019 by 10am	MISSING	0	1	×
Lec7,3 Participation	Mar 1, 2019 by 10am		1	1	
Lec8,1 Participation	Mar 4, 2019 by 10am		1	1	
Lec8,2 Participation	Mar 6, 2019 by 10am	MISSING	0	1	×
Lec8,3 Participation	Mar 8, 2019 by 10am		1	1	
Lec7,1 Participation	Feb 25, 2019 by 10am		1	1	

NAME	DUE	STATUS	SCORE	OUT OF		
Lec9,1 Participation	Mar 11, 2019 by 10am		1	1		📝
Lec9,2 Participation	Mar 13, 2019 by 10am	MISSING	0	1	×	📝
Lec9,3 Participation	Mar 15, 2019 by 10am		1	1		📝
Lec10,2 Participation	Mar 27, 2019 by 10am		1	1		📝
Lec10,3 Participation	Mar 29, 2019 by 10am		100%	1	×	📝
Lec15,3 Participation	May 3, 2019 by 10am		100%	1	×	📝
Lec11,1 Participation	Apr 3, 2019 by 10am	MISSING	0	1	×	📝
Lec11,2 Participation	Apr 5, 2019 by 10am	MISSING	0	1	×	📝
Lec12,1 Participation	Apr 8, 2019 by 10am		0.96	1	×	📝

NAME	DUE	STATUS	SCORE	OUT OF	
Lec12,2 Participation	Apr 10, 2019 by 10am		1	1	
Lec12,3 Participation	Apr 12, 2019 by 10am		1	1	
Lec13,1 Participation	Apr 15, 2019 by 10am		1	1	
Lec13,3 Participation	Apr 19, 2019 by 10am	MISSING	0	1	×
Lec14,1 Participation	Apr 22, 2019 by 10am		1	1	
Lec14,2 Participation	Apr 24, 2019 by 10am	MISSING	0	1	×
Lec14,3 Participation	Apr 26, 2019 by 10am		1	1	
Lec15,1 Participation	Apr 29, 2019 by 10am		1	1	
Lec15,2 Participation	May 1, 2019 by 11:59pm	MISSING	0	1	×

NAME	DUE	STATUS	SCORE	OUT OF	
Exam 1					
Exams	Feb 18, 2019 by 9:50am		84%	100	  

SCORE DETAILS

CLOSE



Close Rubric

Assessment by Henry Duwe

NAME	DUE	STATUS	SCORE	OUT OF
RUBRIC				
CRITERIA	RATINGS			PTS
Question 1	25 to >0 pts Points	0 pts No Marks		18 / 25 pts
Question 2	25 to >0 pts Points	0 pts No Marks		5 / 25 pts
Question 3	30 to >0 pts Points	0 pts No Marks		30 / 30 pts
Question 4	5 to >0 pts Points	0 pts No Marks		0 / 5 pts
Question 5	15 to >0 pts Points	0 pts No Marks		15 / 15 pts
				Total Points: 68

Exam 2
 Exams

Apr 1, 2019 by 9:50am

94.96%

100





SCORE DETAILS

CLOSE

Mean: 74.4

High: 98.1

Low: 45.2



Assessment by Henry Duwe

[Close Rubric](#)

RUBRIC (1)			
CRITERIA	RATINGS		PTS
Question 1	15 to >0 pts Points	0 pts No Marks	15 / 15 pts
Question 2	25 to >0 pts Points	0 pts No Marks	19 / 25 pts
Question 3	35 to >0 pts Points	0 pts No Marks	35 / 35 pts
Question 4	25 to >0 pts Points	0 pts No Marks	23 / 25 pts
			Total Points: 92

Exam 3

Exams

May 6, 2019 by 7:30am

94

100

NAME	DUE	STATUS	SCORE	OUT OF
LABS			79.75%	319.00 / 400.00
HOMEWORK			86.5%	692.00 / 800.00
PROJECT			91.9%	2,757.00 / 3,000.00
PARTICIPATION			100%	27.00 / 27.00
IMPORTED ASSIGNMENTS			N/A	0.00 / 0.00
EXAMS			90.99%	272.96 / 300.00
TEST			N/A	0.00 / 0.00
TOTAL			90.14%	