EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 2
Spring 2017

Instructions: This is a 50-minute exam. Students may bring 2 pages of notes (front and back) to this exam. Each short question is worth 2 points and each problem is worth 16 points. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=1V$,$V_{TPO}= - 1V$, $\gamma =0.4V^{-1/2,}$, $\phi=0.6V$, $C_{OX}=2fF/\mu^2$, and $\lambda = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF} = \infty$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters are needed, use the process parameters associated with the process described on the attachments to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters. Also attached to this exam is a table that has information about large and small signal models of devices.

1. (2 pts) The term "diode connected transistor" is used to describe a particular circuit that can be implemented with either MOS or Bipolar transistors. Give the schematic of a diode-connected NMOS transistor.

2. (2 pts) What are the two major reasons that the "β" for the vertical npn BJT is larger than the "β" for the lateral pnp in a basic bipolar process?

3. (2 pts) Why is C_{OX} the same for n-channel and p-channel transistors in the CMOS process we have been working with?

4. (2 pts) Why is the epitaxial process used to create the collector region of a vertical npn transistor in a bipolar process rather than an n-diffusion?

5. (2pts) What is the purpose of the buried collector in a bipolar process?

6. (2pts) Thyristors (Triacs and SCRs) are widely used to switch large loads (large currents) yet the power dissipation is usually very small. What key characteristic of the thyristors is necessary for the power dissipation in the thyristor to be small?

7. (2pts) If an amplifier circuit has a power gain in the signal path from the input to the output, what part of the circuit provides the energy necessary to have a power gain?

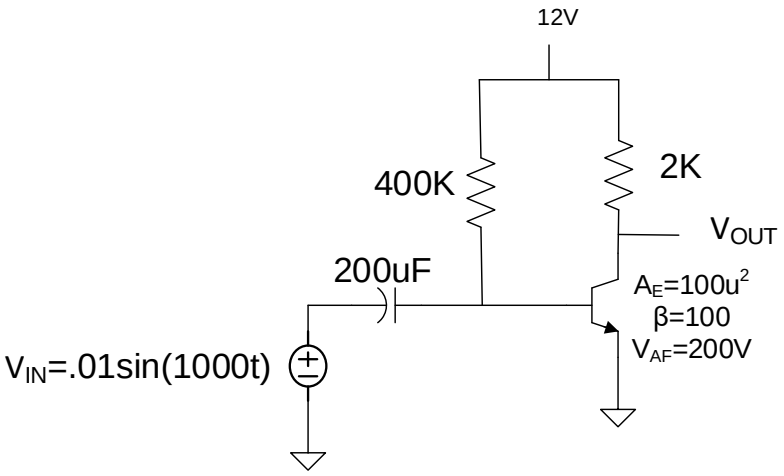
8. (2pts) What parameter in the JFET model corresponds to the threshold voltage in a MOSFET?

9 (2pts) What feature is a bipolar process that has been discussed in class is the dominant contributor to the large area required for a vertical npn transistor?

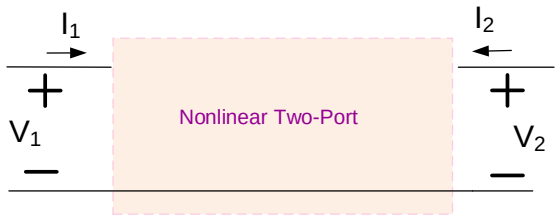
10 (2pts) Give the two-port model for a unilateral amplifier in terms of the standard amplifier parameters.

Problem 1 (16 pt) Consider the following circuit.

a) Determine the quiescent value of V_{OUT}
b) Determine the small-signal voltage gain in terms of the small-signal model parameters
c) Determine $V_{OUT}(t)$



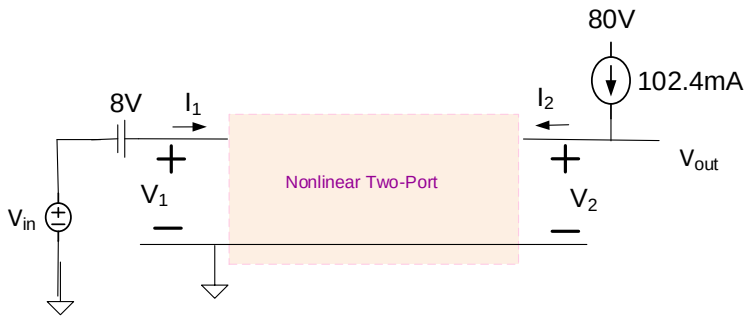
Problem 2 (16 pts) Consider a nonlinear device characterized by the following equations:



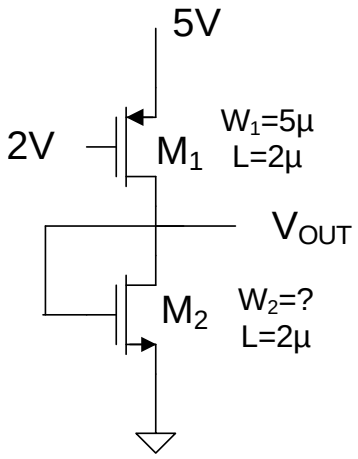
$$I_1 = \begin{cases} 0 & V_1 < 2V \quad V_2<2V \\ 10^{-4}(V_1-2)^2 & 2V < V_1 < 4V \quad V_2<2V \\ 10^{-4}\left(3+\frac{V_1^2}{16}\right) & V_1 > 4V \quad V_2>2V \end{cases}$$

$$I_2 = \begin{cases} 10^{-4}V_1^2V_2 & V_1<2V \quad V_2 < 2V \\ \frac{1}{5000}V_1V_2^3 & V_1>2V \quad V_2 >2V \end{cases}$$

a) Derive the small-signal equivalent circuit for V_1>4V and V_2>4V in terms of the operating point of the circuit
b) If the circuit is biased as shown below, numerically determine the quiescent output voltage
c) If the circuit is biased as shown below, determine the small signal voltage gain



Problem 3 (16 pts) Consider the following circuit. The relevant model parameters of the devices are $V_{TN}=1V$, $V_{TP}=-1V$, $\mu_n C_{OX}=100\mu AV^{-2}$ and $\mu_p C_{OX}=33\mu AV^{-2}$.

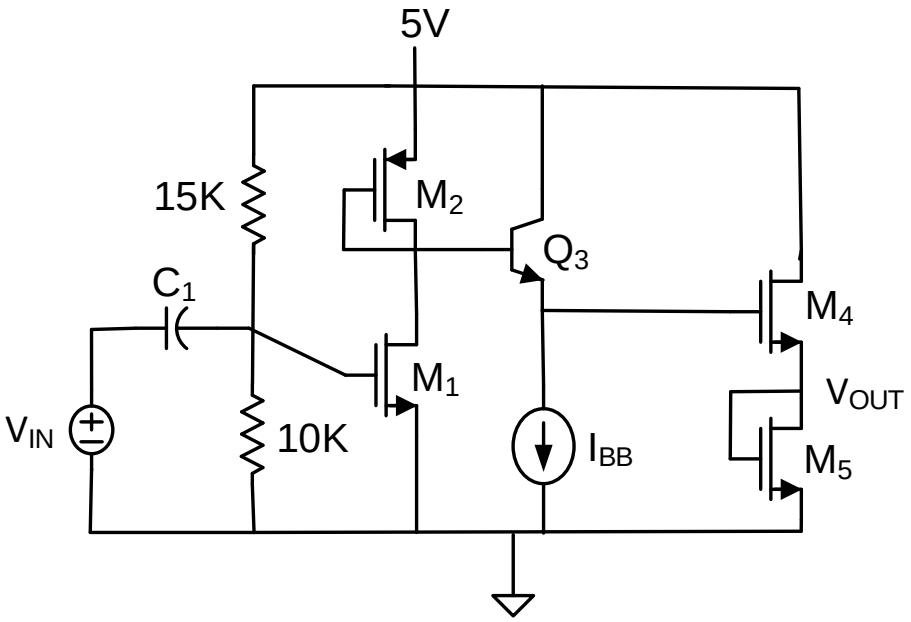


a) Determine W_2 so that $V_{OUTQ}=2V$

b) Determine the power dissipation of the 5V voltage source

Problem 4 (16 pts) Design a circuit using only MOS transistors that has an output voltage of 6V. In addition to the transistors, you have a single dc power supply of 10V available. You may use as many MOS transistors as you want and can specify any sizes for the devices.

Problem 5 (16 pts) Draw the small-signal equivalent circuit for the following amplifier structure. Assume the capacitor is large, all MOS transistors are operating in the Saturation region, and all bipolar transistors are operating in the Forward Active region. Do not solve.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

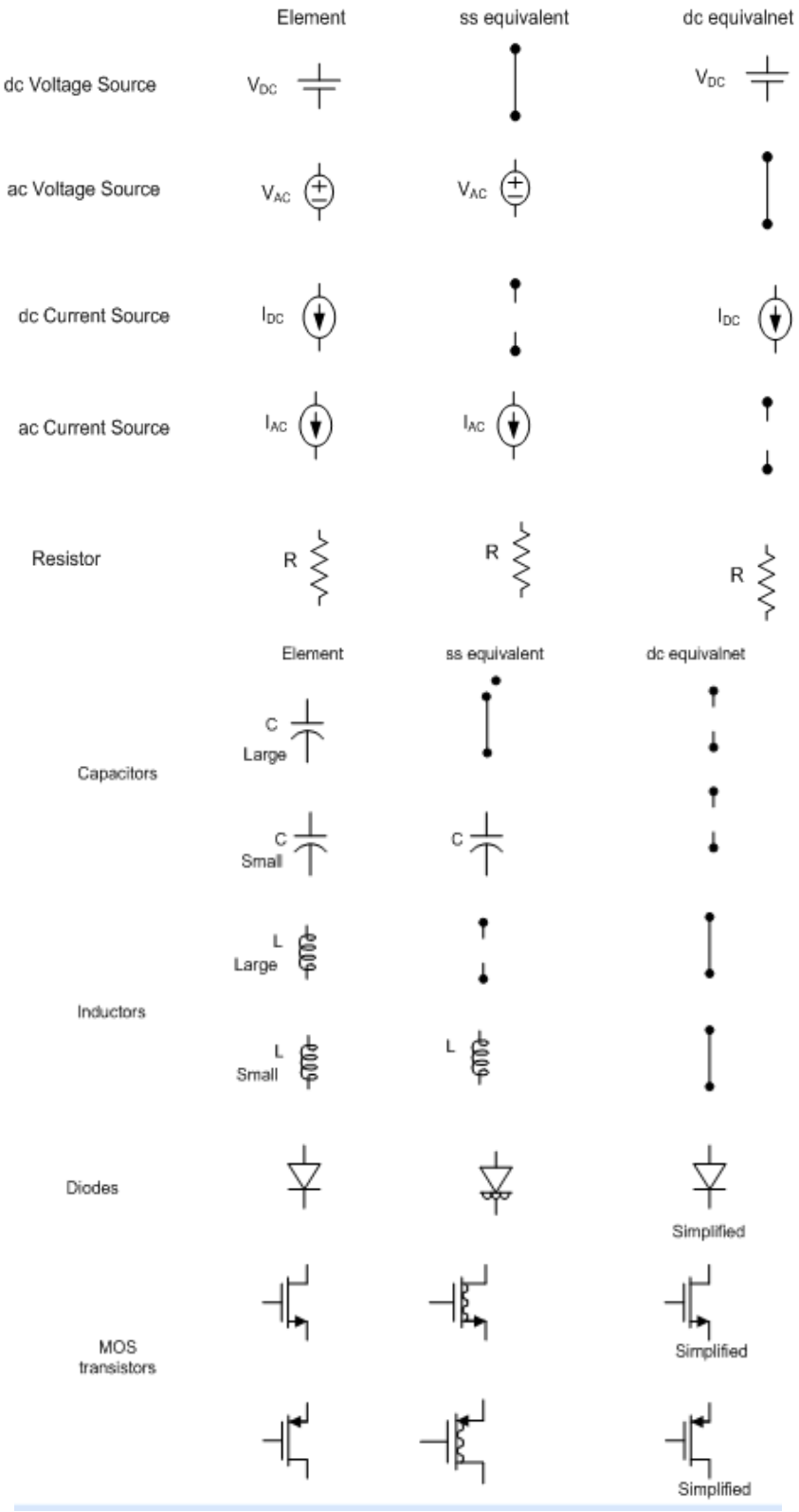
PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

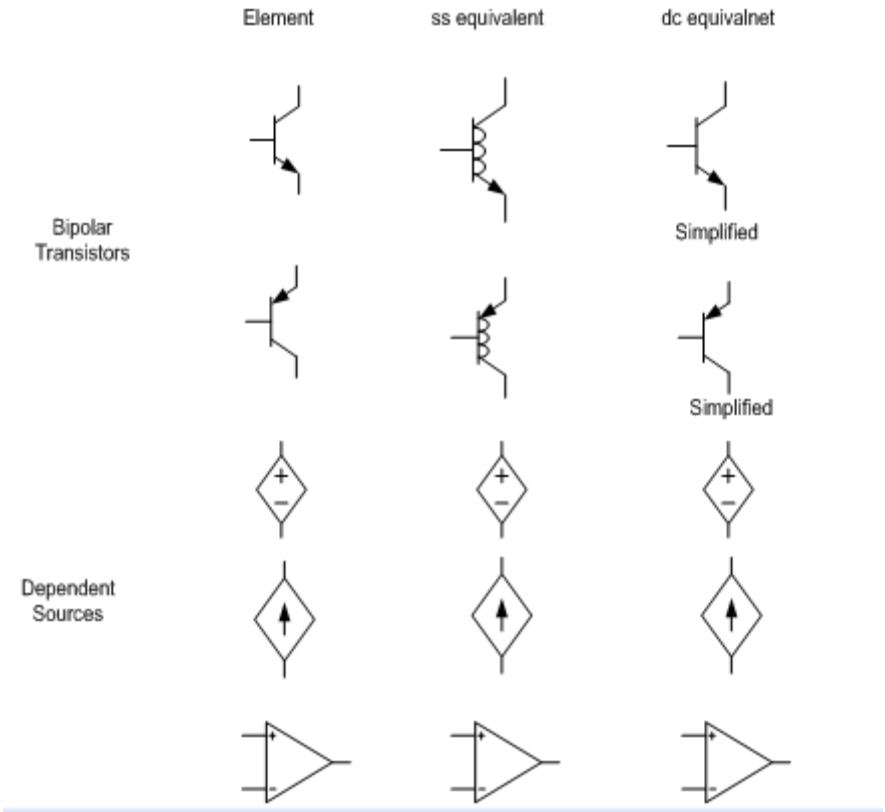
PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Bipolar Transistors
Simplified
Simplified
Dependent Sources