EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 1
Fall 2017

Instructions: Students may bring 1 page of notes (front and back) to this exam and a calculator but the use of any device that has wireless communication capability is prohibited. There are 9 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$ ,$\mu_p C_{OX}=\mu_n C_{OX}/3$ ,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$; if reference to a diode is made, assume the process parameter; $J_S=10^{-17}A/\mu^2$ ; and if reference to a bipolar process is made assume process parameters; $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF}=\infty$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

1. (2pts) What is the major reason the semiconductor industry was interested in replacing aluminum interconnects with copper interconnects?

2. (2pts) Though most design rules specify minimum feature sizes, design rules for contacts give sizing rules as "exactly" meaning that contact sizes must all be the same size. What is the major reason that designers can not make contacts larger?

3. (2pts) If a silicon dioxide gate layer is 50A thick, about how many $SiO_2$ molecules will be stacked on top of each other to create this layer?

4. (2pts) $SiO_2$ is typically thermally grown to form a gate oxide. But if $SiO_2$ is placed on top of metal, a different process is used to form the $SiO_2$ layer. What process is typically used to form $SiO_2$ on top of metal?

5. (2pts) Two individuals working independently at different companies are both credited with inventing the integrated circuit. Give the name of one of them.

6. (2pts) Boron is widely used as a dopant for creating p-type silicon. What is the key characteristic of Boron that makes it well suited for creating p-type impurities?

7. (2pts) Why are contacts to polysilicon not allowed on top of the channel of transistors in most semiconductor processes?

8. (2pts) In logic circuits (gates) constructed with n-channel pull-down networks and p-channel pull-up networks where for any input either the n-channel or p-channel network is conducting and the other is nonconducting, it was observed with an ideal switch-level model of the MOS transistors that

   a) Logic levels were $V_{DD}$ and 0
   b) Static power dissipation was 0 in both the logic high and logic low states
   c) Propagation delays for either HL or LH output transitions were 0

   But upon examining these circuits in more detail with better device models, it was observed that one of these 3 properties is not really achieved. Which one of these properties was not really achieved when better models were used?

9. (2pts) The term MOSFET is an abbreviation for Metal-Oxide-Semiconductor-Field-Effect-Transistor. Though this term was descriptive of how early MOSFETs were formed, one of the words is no longer descriptive of how most modern MOSFETs are constructed. What word is not descriptive and why is it no longer descriptive?

10. (2pts) What is the main difference between positive photoresist and negative photoresist?

**Problem 1 (16 pts)** Consider a process where the fabrication cost of 8" wafers is \$900 and the defect density is 1.4/cm$^2$.

**a)** If an integrated circuit designed in this process has a die area of 0.75cm$^2$, what is the fabrication cost per good die?

**b)** What percent reduction in die costs (for the same circuit) would be realized if the defect density were reduced to 1.2/cm$^2$?

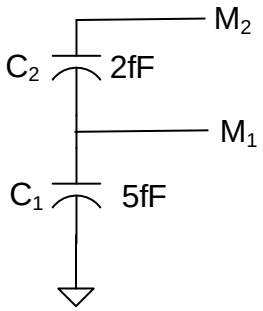
**Problem 2 (16 pts)** Consider a Boolean system with three inputs, **A, B**, and **C**, and output **F** defined by the function

$$F = A \bullet \left( \overline{B} + C \right)$$

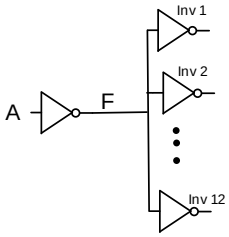
a) Design a CMOS circuit, at the transistor level, that implements the Boolean system described using only NAND and NOR logic gates. Assume the inputs that are available are **A, B**, and **C**.

b) Repeat part a) but use compound logic gates instead of NAND and NOR logic.

**Problem 3 (16 pts)** Design a circuit (sketch the layout including a labeling of feature sizes) that creates two capacitors, a capacitor $C_1$ from Metal 1 to substrate of value 5fF and a capacitor $C_2$ from Metal 2 to Metal 1 of 2fF as shown in the schematic below.



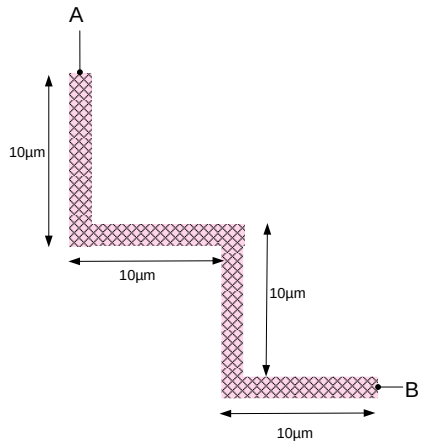
**Problem 4 (16 pts)** Assume a CMOS inverter designed in the ON 0.5μm CMOS process drives 12 identical devices and the supply voltage is 3.5V. If a step input from 0V to 3.5V is applied at the input, what is the corresponding HL output transition time of the inverter? Assume minimum-sized devices are used and also assume $V_{DD}$=3.5V.



**Problem 5 (16 pts)** Consider a polysilicon interconnect with dimensions shown below where the width of the rectangular segments are all 2μm. Assume the sheet resistance at room temperature (300K) is 20Ω/□, the TCR is 1200ppm/$^{o}$C, and the VCR is 150ppm/V.

Determine the resistance of this interconnect at 350K if the voltage across the resistor is small.

Extra credit (5 pts) Determine the resistance of this interconnect at 350K if the voltage across the resistor is 5V.



| TRANSISTOR PARAMETERS | W/L | N-CHANNEL | P-CHANNEL | UNITS |
|---|---|---|---|---|
| MINIMUM | 3.0/0.6 | | | |
| Vth | | 0.78 | -0.93 | volts |
| SHORT | 20.0/0.6 | | | |
| Idss | | 439 | -238 | uA/um |
| Vth | | 0.69 | -0.90 | volts |
| Vpt | | 10.0 | -10.0 | volts |
| WIDE | 20.0/0.6 | | | |
| Ids0 | | < 2.5 | < 2.5 | pA/um |
| LARGE | 50/50 | | | |
| Vth | | 0.70 | -0.95 | volts |
| Vjbkd | | 11.4 | -11.7 | volts |
| Ijlk | | <50.0 | <50.0 | pA |
| Gamma | | 0.50 | 0.58 | V^0.5 |
| K' (Uo*Cox/2) | | 56.9 | -18.4 | uA/V^2 |
| Low-field Mobility | | 474.57 | 153.46 | cm^2/V*s |

COMMENTS: XL_AMI_C5F

| FOX TRANSISTORS | GATE | N+ACTIVE | P+ACTIVE | UNITS |
|---|---|---|---|---|
| Vth | Poly | >15.0 | <-15.0 | volts |

| PROCESS PARAMETERS | N+ACTV | P+ACTV | POLY | PLY2_HR | POLY2 | MTL1 | MTL2 | UNITS |
|---|---|---|---|---|---|---|---|---|
| Sheet Resistance | 82.7 | 103.2 | 21.7 | 984 | 39.7 | 0.09 | 0.09 | ohms/sq |
| Contact Resistance | 56.2 | 118.4 | 14.6 | | 24.0 | | 0.78 | ohms |
| Gate Oxide Thickness | 144 | | | | | | | angstrom |

| PROCESS PARAMETERS | MTL3 | N\PLY | N_WELL | UNITS |
|---|---|---|---|---|
| Sheet Resistance | 0.05 | 824 | 815 | ohms/sq |
| Contact Resistance | 0.78 | | | ohms |

COMMENTS: N\POLY is N-well under polysilicon.

| CAPACITANCE PARAMETERS | N+ACTV | P+ACTV | POLY | POLY2 | M1 | M2 | M3 | N_WELL | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Area (substrate) | 429 | 721 | 82 | | 32 | 17 | 10 | 40 | aF/um^2 |
| Area (N+active) | | | 2401 | | 36 | 16 | 12 | | aF/um^2 |
| Area (P+active) | | | 2308 | | | | | | aF/um^2 |
| Area (poly) | | | | 864 | 61 | 17 | 9 | | aF/um^2 |
| Area (poly2) | | | | | 53 | | | | aF/um^2 |
| Area (metal1) | | | | | | 34 | 13 | | aF/um^2 |
| Area (metal2) | | | | | | | 32 | | aF/um^2 |
| Fringe (substrate) | 311 | 256 | | | 74 | 58 | 39 | | aF/um |
| Fringe (poly) | | | | | 53 | 40 | 28 | | aF/um |
| Fringe (metal1) | | | | | | 55 | 32 | | aF/um |
| Fringe (metal2) | | | | | | | 48 | | aF/um |
| Overlap (N+active) | | | 206 | | | | | | aF/um |
| Overlap (P+active) | | | 278 | | | | | | aF/um |