EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Exam 1

Spring 2017

Instructions: Students may bring 1 page of notes (front and back) to this exam and a calculator but the use of any device that has wireless communication capability is prohibited. There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$; if reference to a diode is made, assume the process parameter; $J_S=10^{-17}A/\mu^2$; and if reference to a bipolar process is made assume process parameters; $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF} = \infty$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

1. (2pts) What is the difference between n-active and p-active?

2. (2pts) What is the major difference between an epitaxial layer and a polysilicon layer?

3. (2pts) Why is a barrier metal included under all copper interconnects?

4. (2pts) Why is the ON voltage of a silicon diode often modeled as a 0.6V voltage source?

5. (2 pts) What is the major reason CMOS replaced NMOS as the technology of choice for building most large digital circuits?

6. (2pts) What is the major benefit of using “shallow trench isolation” rather than thermally grown oxide when laterally separating transistors from each other?

7. (2pts) Why is CVD rather than thermal growth used to place SiO_2 on top of a metal layer?

8. (2pts) How many valence-band electrons are there in a Silicon atom?

9. (2pts) What is the major reason the capacitance density of Metal 2 to substrate is considerably less than the capacitance density of Metal 1 to substrate in most semiconductor processes?

10. (2pts) Why are contacts from Metal 1 to Poly usually not allowed on the top of thin gate oxide?

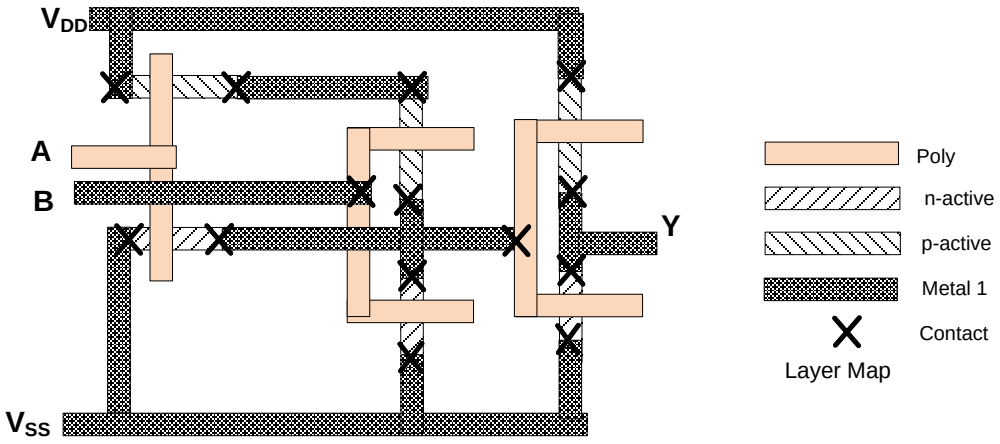
Problem 1 (16 pts) Consider a Boolean system with three inputs, **A, B**, and **C**, and output **F** defined by the function

$$F = \bar{A}B + A\bar{C}\,.$$

a) Design a CMOS circuit, at the transistor level, that implements the Boolean system described using only NAND logic . Assume the inputs that are available are **A, B**, and **C**.
b) Repeat part a) but use compound logic gates instead of NAND logic.

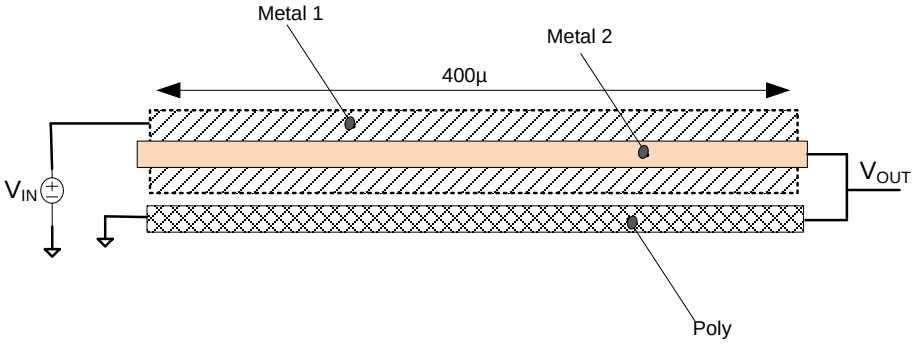
Problem 2 (16 pts) Assume a CMOS inverter designed in the ON 0.5µm CMOS process drives a 1pF load and the supply voltage is 3.5V. If a step change on the input from 0 to 3.5V occurs at time t=0, what is the HL output transition time? Assume V_{DD}=3.5V.

Problem 3 (16 pts) A stick diagram along with a layer map are shown below. Draw the equivalent circuit corresponding to this stick diagram.



Problem 4 (16 pts) An interconnect region is shown where the length of Metal 1, Metal 2, and Poly are all approximately 400µm. The width of Metal 2 and Poly are both 2µm and the width of Metal 1, which lies under Metal 2, is 6µm. On the right side Metal 2 is connected to Poly and on the left an input voltage source drives Metal 1.

a) Draw an equivalent electrical circuit of this layout (including values for all components) that includes all relevant parasitic capacitances associated with Metal 1 and Metal 2 and the relevant resistance of Poly. Neglect any resistance associated with the metal layers and any capacitance associated with the Poly.
b) If the input is a 2V step applied at time t=0, what should the output voltage be if there are no parasitic resistors or capacitors?
c) Give an analytical expression for the actual output voltage if a 2V step is applied at the input.



Problem 5 (16 pts) If the voltage of a forward-biased pn junction is varied between 0.55V and 0.6V, what is the range in the diode current. Assume the junction area of the diode is $200\mu^2$ and $J_S=10^{-15}A/\mu^2$.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um