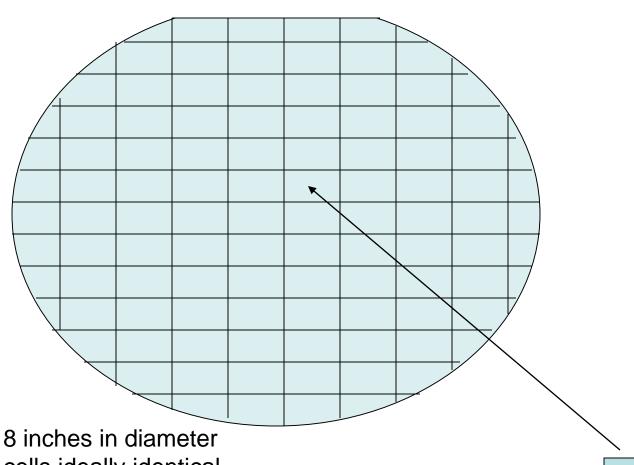
EE 330 Lecture 4

- Yield
- Statistics Review
- Key Historical Developments (continued)
- Some other statistical issues (for fun)

Wafer

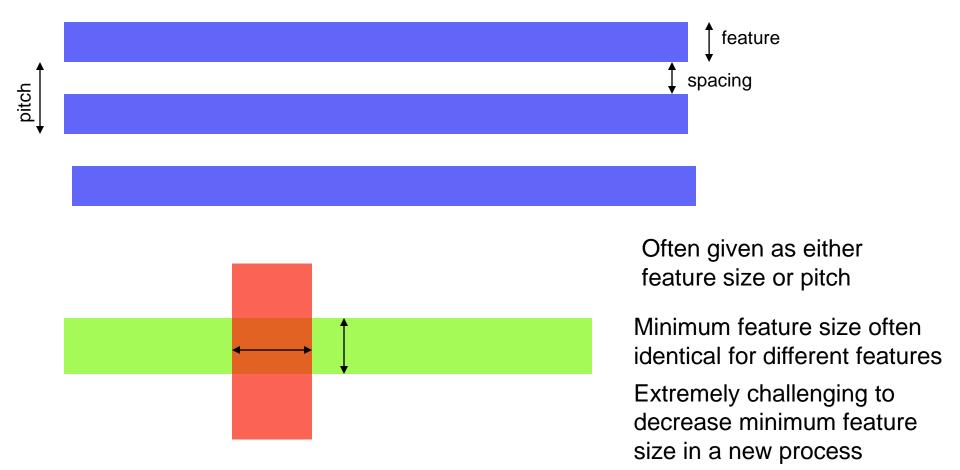


- 6 inches to 18 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small



Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured



What is meant by "reliably"

Yield is acceptable if circuit performs as designed even when a very large number of these features are made

If P is the probability that a feature is good

n is the number of uncorrelated features on an IC

Y is the yield

$$Y = P^{n}$$

$$P = e^{\frac{\log_{e} Y}{n}}$$

Example: How reliable must a feature be?

n=5E3

Y = 0.9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$
 =0.999979

But is n=5000 large enough? is Y large enough?

More realistically n=5E9 (or even 5E10)

Consider n=5E9

20 parts in a trillion or size of a piece of sheetrock relative to area of lowa

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes

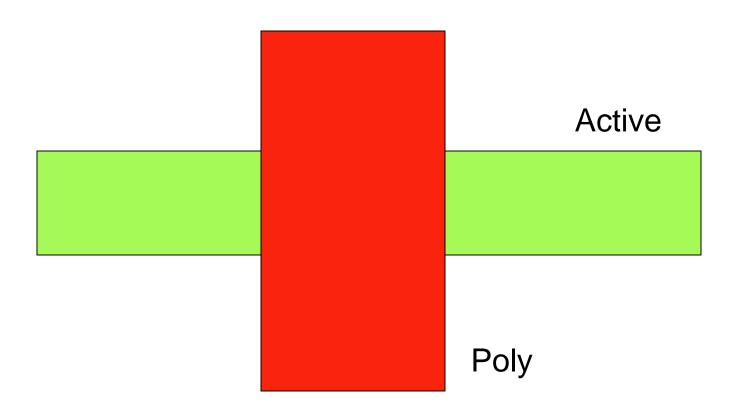
Feature Size

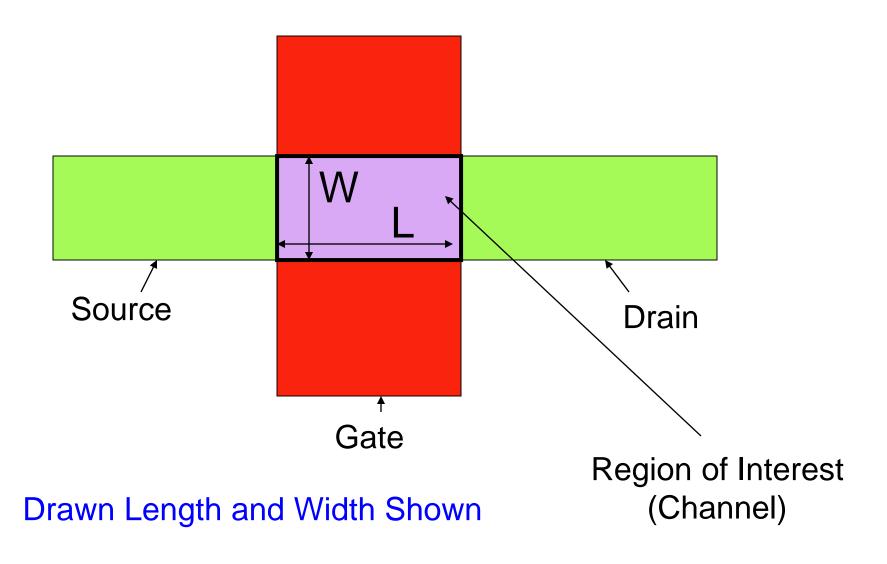
- Typically minimum length of a transistor
- Often minimum width or spacing of a metal interconnect (wire)
- Point of "bragging" by foundries
 - Drawn length and actual length differ
- Often specified in terms of pitch
 - Pitch is sum of feature size and spacing to same feature
 - Pitch approximately equal to twice minimum feature size

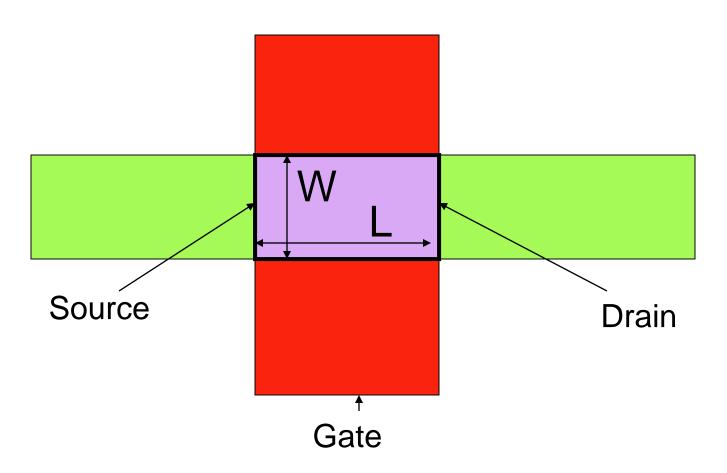
Feature Size Evolution

Mid 70's	25µ
2005	90nm
2010	20nm
2020	7nm

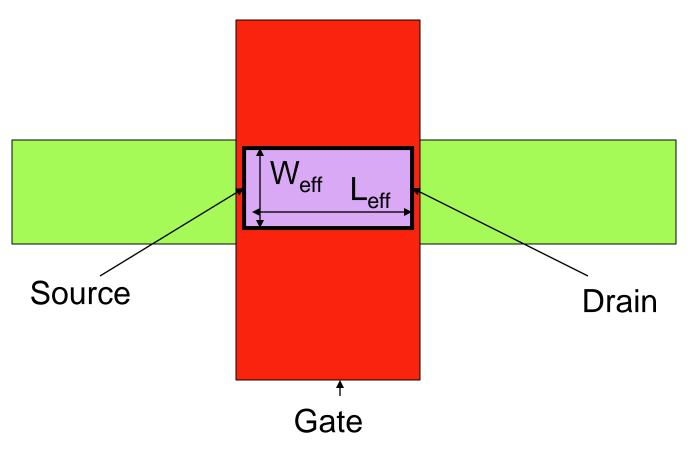
$$1\mu = 10^3 nm = 10^{-6} m = 10^4 \text{ A}$$







Actual Drain and Source at Edges of Channel



Effective Width and Length Generally Smaller than Drawn Width and Length

Device and Die Costs

Characterize the high-volume incremental costs of manufacturing integrated circuits

Example: Assume manufacturing cost of an 8" wafer in a 0.25µ process is \$800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

$$n_{trans} \cong \frac{A_{wafer}}{A_{trans}} = \frac{\pi (4in)^2}{(0.25\mu)^2} = 5.2E11$$
 (520 Billion!) (Trillion, Tera ...10¹²)

$$C_{trans} = \frac{C_{wafer}}{n_{trans}} = \frac{\$800}{5.2E11} = \$15.4E - 9$$

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!

Device and Die Costs

$$C_{per\,unit\,area} \cong \$2.5 / cm^2$$

Example: If the die area of the 741 op amp is 1.8mm², determine the cost of the silicon needed to fabricate this op amp

$$C_{741} = \$2.5 / cm^2 \bullet (1.8mm^2) \cong \$.05$$

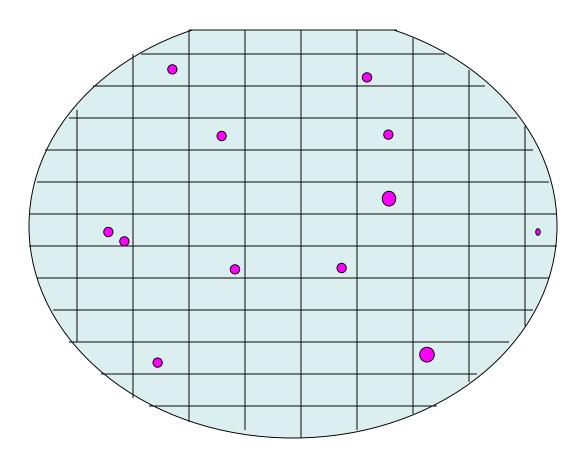
Actual integrated op amp will be dramatically less if bonding pads are not needed

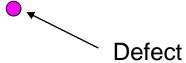
Size of Atoms and Molecules in Semiconductor Processes

Silicon:	Average Atom Spacing	$2.7\mathrm{\mathring{A}}$
	Lattice Constant	5.4 Å
S_iO_2	Average Atom Spacing	3.5 Å
	Breakdown Voltage	5 to $10MV/cm = 5 \text{ to } 10mV/A^{0}$
Air		20KV/cm

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches

Defects in a Wafer





- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss

Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed Hard Faults
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a "gleam in the eye" of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults

Yield Issues and Models

- Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)
- The circuits failures associated with these parametric variations are termed Soft Faults
- Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults

Hard Fault Model

$$Y_H = e^{-Ad}$$

Y_H is the probability that the die does not have a hard fault A is the die area d is the defect density (typically 1cm⁻² < d < 2cm⁻²)

Industry often closely guards the value of d for their process

Other models, which may be better, have the same general functional form

Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

$$\sigma = \frac{\rho}{\sqrt{A_k}}$$

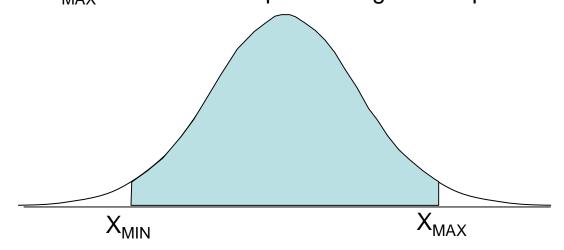
ρ is a constant dependent upon the architecture and the process

A_k is the area of the parameter sensitive area

Soft Fault Model

$$P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x) dx$$

 P_{SOFT} is the soft fault yield f(x) is the probability density function of the parameter of interest X_{MIN} and X_{MAX} define the acceptable range of the parameter of interest



Some circuits may have several parameters that must meet performance requirements

Soft Fault Model

If there are k parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$Y_S = \prod_{j=1}^k P_{SOFT_j}$$

Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

$$Y = Y_H Y_S$$

Cost Per Good Die

The manufacturing costs per good die is given by

$$C_{Good} = \frac{C_{FabDie}}{Y}$$

where C_{FabDie} is the manufacturing costs of a fab die and Y is the yield

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.

Example: Assume a die has no soft fault vulnerability, a die area of 1cm² and a process has a defect density of 1.5cm⁻²

- a) Determine the hard yield
- b) Determine the manufacturing cost per good die if 8" wafers are used and if the cost of the wafers is \$1200

Solution

a)
$$Y_{H} = e^{-Ad}$$

$$Y = e^{-1cm^{2} \cdot 1.5cm^{-2}} = 0.22$$
b)
$$C_{Good} = \frac{C_{FabDie}}{Y}$$

$$C_{FabDie} = \frac{C_{Wafer}}{A_{Wafer}} A_{Die}$$

$$C_{FabDie} = \frac{\$1200}{\pi (4in)^{2}} 1cm^{2} = \$3.82$$

$$C_{Good} = \frac{\$3.82}{0.22} = \$17.37$$

Do you like statistics?

Statistics are Real!

Statistics govern what really happens throughout much of the engineering field!

Statistics are your Friend !!!!

You might as well know what will happen since statistics characterize what WILL happen in the presence of variability in many processes!

Assume x is a random variable of interest

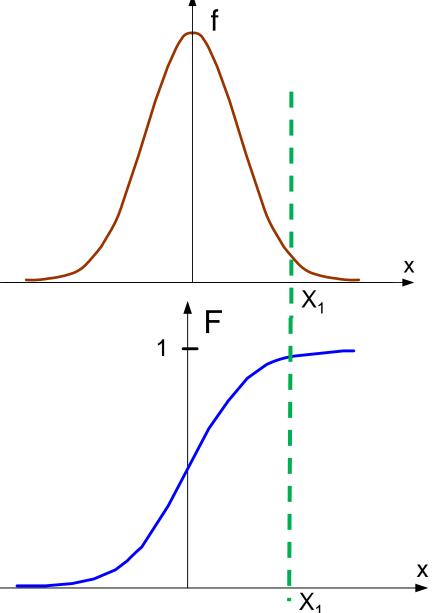
f(x) = Probability Density Function for x

$$\int_{x=-\infty}^{\infty} f(x) dx = 1$$

F(x) = Cumulative Density Function for x

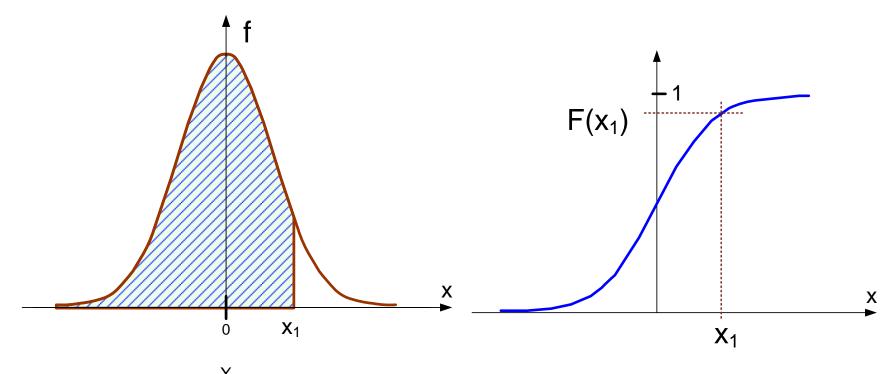
$$F(X_1) = \int_{x=-\infty}^{X_1} f(x) dx$$

$$0 \le F(x) \le 1$$
 $\frac{\partial F(x)}{\partial x} \ge 0$



f(x) = Probability Density Function for x

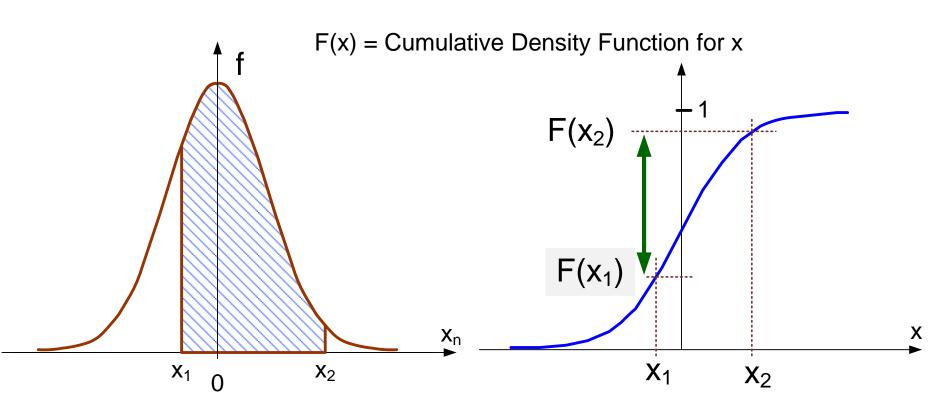
F(x) = Cumulative Density Function for x



$$P\{x \le x_1\} = \int_{x=-\infty}^{X_1} f(x) dx$$

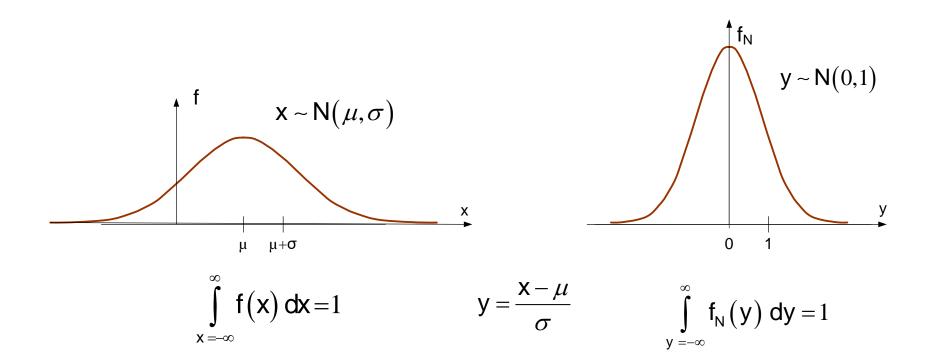
$$P\{x \le X_1\} = F(X_1)$$

f(x) = Probability Density Function for x



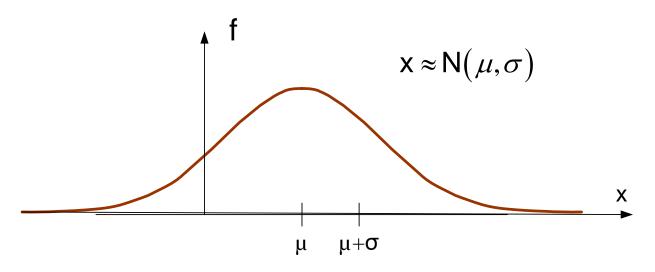
$$P\{X_1 \le x \le X_2\} = \int_{X_1}^{X_2} f(x) dx$$

$$P{X_1 \le x \le X_2} = F(X_2) - F(X_1)$$



Theorem 1: If the random variable x in normally distributed with mean μ and standard deviation σ , then $y = \frac{x - \mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

(Normal Distribution and Gaussian Distribution are the same)



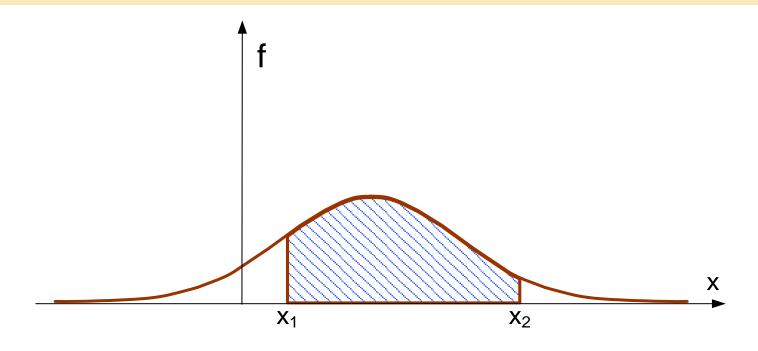
The random part of many parameters of microelectronic circuits is often assumed to be Normally distributed and experimental observations confirm that this assumption provides close agreement between theoretical and experimental results

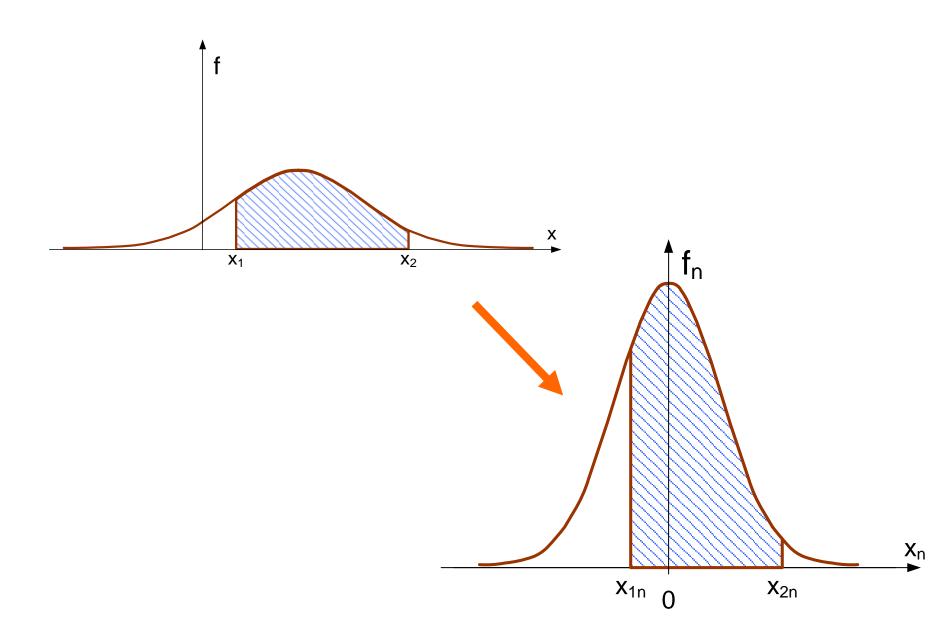
The mapping $y = \frac{x - \mu}{\sigma}$ is often used to simplify the statistical characterization of the random parameters in microelectronic circuits

Theorem 2: If x is a Normal (Gaussian) random variable with mean μ and standard deviation σ , then the probability that x is between x_1 and x_2 is given by

$$p = \int\limits_{x_1}^{x_2} f(x) dx = \int\limits_{x_{1n}}^{x_{2n}} f_n(x) dx \quad \text{where} \quad x_{1n} = \frac{x_1 - \mu}{\sigma} \quad \text{and} \quad x_{2n} = \frac{x_2 - \mu}{\sigma}$$

and where $f_n(x)$ is N(0,1)

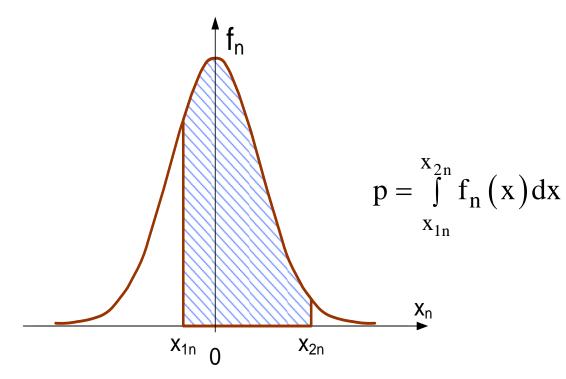




Observation: The probability that the N(0,1) random variable x_n satisfies the relationship $x_{1n} < x_n < x_{2n}$ is also given by

$$p = F_n(x_{2n}) - F_n(x_{1n})$$

where $F_n(x)$ is the CDF of x_n .

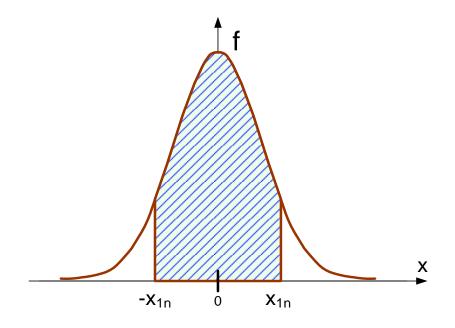


Since the N(0,1) distribution is symmetric around 0, p can also be expressed as

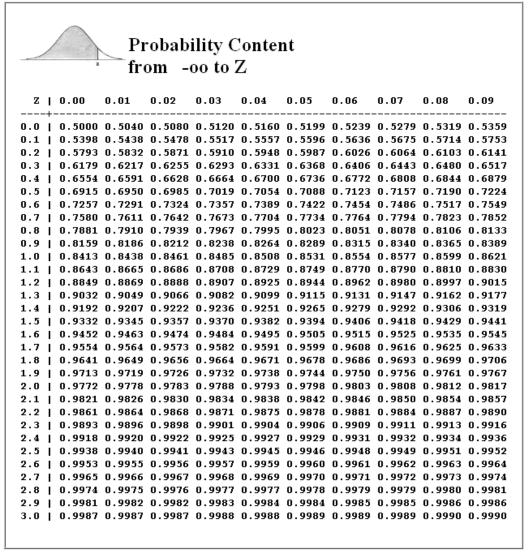
$$p = F_n(x_{2n}) - (1 - F_n(-x_{1n}))$$

Observation: In many electronic circuits, the random variables of interest are 0 mean Gaussian and the probabilities of interest are characterized by a region defined by the <u>magnitude</u> of the random variable. In these cases,

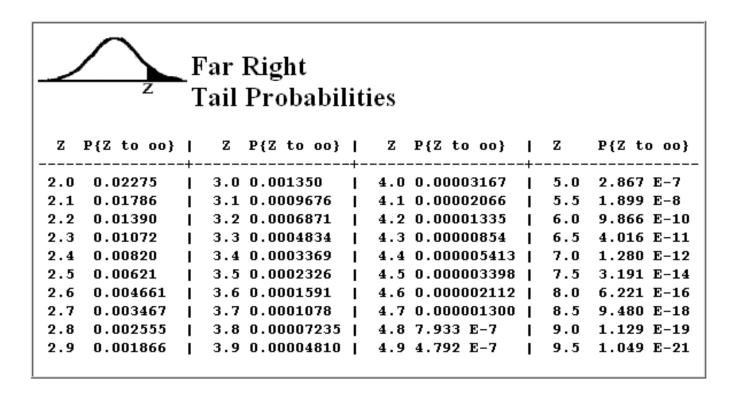
$$p = \int_{-x_{1n}}^{x_{1n}} f_n(x) dx = F_n(x_{1n}) - F_n(-x_{1n}) = 2F_n(x_{1n}) - 1$$



Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

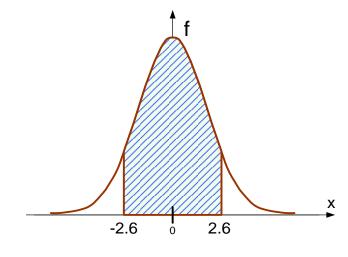


Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.



Example: Determine the probability that the N(0,1) random variable has magnitude less than 2.6

$$p = 2F_n(2.6) - 1$$



From the table of the CDF, $F_n(2.6) = 0.9953$ so p=.9906

End of Lecture 4