Class 23

Sean Gordon

1) a) 8 2-input XNOR gates, 8 not gates, 1 2-input NOR gate, 1 8-input OR gate

1 9-input AND gate, 2 8-input AND gates, 1 7-input AND gate, 1 6 input AND gate

1 5-input AND gate, 1 4-input AND gate, 1 3-input AND gate, 1 2 input AND gate

b) $8 \cdot 8 + 8 \cdot 2 + 1 \cdot 4 + 1 \cdot 18 + 1 \cdot 20 + 2 \cdot 18 + 1 \cdot 16 + 1 \cdot 14 + 1 \cdot 12 + 1 \cdot 10 + 1 \cdot 8 + 1 \cdot 6 = 224$ transistors

2) a) 122 transistors

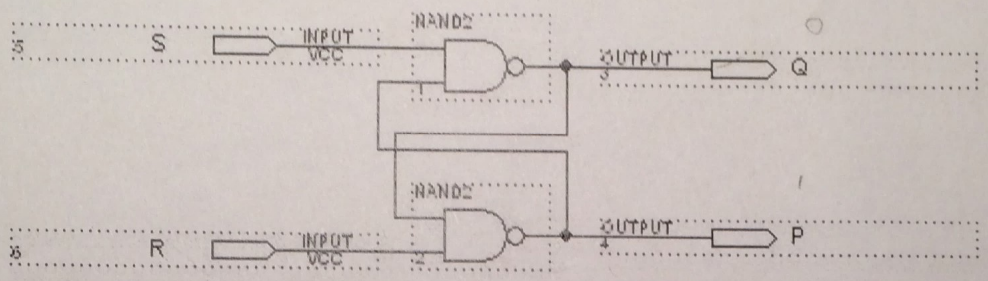
b) 1 8-input NOR gate, 1 2-input NOR gate, 9 not gates

38 transistors

c) $122 + 38 = 160$ transistors

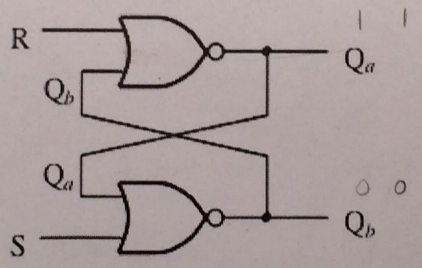
Class 25 (120 points)

1. (50 points) In the circuit below, two NAND gates are used to construct a latch. (Notice that the basic latch presented in Class 25 uses two NOR gates.) Describe what the circuit below does when:
   (a) R = 0, S = 0;
   (b) R = 0, S = 1;
   (c) R = 1, S = 0;
   (d) R = 1, S = 1;

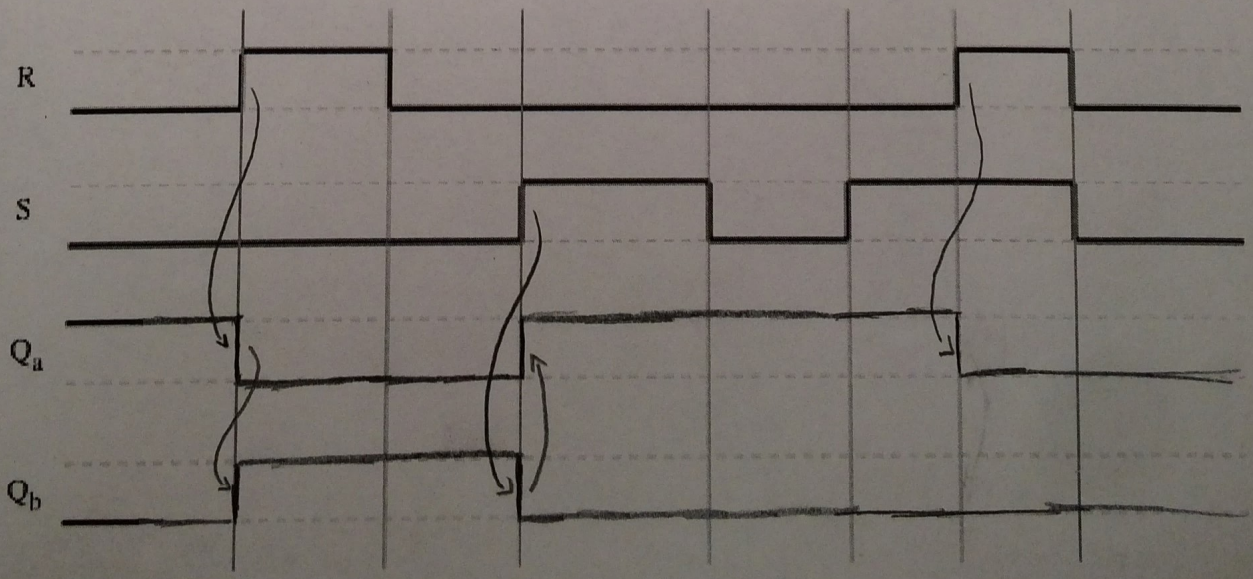


Hint: You may want to use Boolean algebra to transform this latch into the basic latch presented in Class 25 (constructed using NOR gates).

2. (70 points) Consider the basic latch as shown below. Assume that the propagation delay of the NOR gates is negligible. Assume $Q_a = 1$ and $Q_b = 0$ initially.



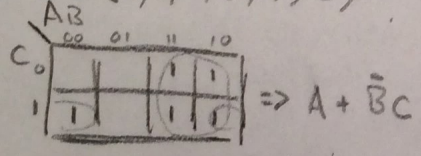
Given the input *R* and *S* signals as shown below, complete the timing diagram. Please use arrows as in Fig. 5.4(c) to indicate the causal relationship of the transitions of signals.
Hint: It would be helpful to go through the animation of Slide 5 of Class 25 Mini-Lecture slides.



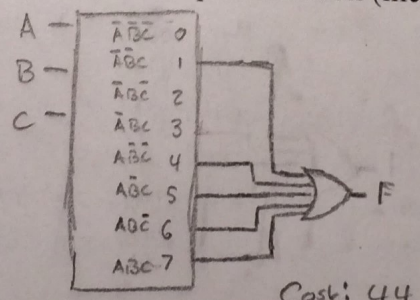
Class 24 (100 points)

1. (100 points) Given a 3-input function $F(A,B,C) = \sum m(1,4,5,6,7)$. Assume that AND gates and OR gates of any number of inputs and NOT gates can be used. Let the cost of a logic circuit be the total number of gates plus the total number of inputs to all gates in the circuit. Show your steps in the following questions.
   (a) (20 points) Implement F using one 3-to-8 decoder without enable and a minimal number of basic gates. Assume the decoder is implemented using the idea in Fig. 4.13 but extended to a 3-to-8 decoder. What is the total cost of your implementation (including the gates inside the decoder)?
   (b) (20 points) Implement F directly as a simplified SOP expression. What is the total cost of your implementation?
   (c) (20 points) Implement F using one 2-to-1 MUX and a minimal number of basic gates. Assume the MUX is implemented as in Fig. 4.1. What is the total cost of your implementation (including the gates inside the MUX)? In this question, you should minimize the cost of your implementation by determining the best input to be used as the select input to the MUX.
   (d) (20 points) Implement F using one 4-to-1 MUX and a minimal number of basic gates. Assume the MUX is implemented as in Fig. 4.2. What is the total cost of your implementation (including the gates inside the MUX)? In this question, you should minimize the cost of your implementation by determining the best inputs to be used as the select inputs to the MUX.
   (e) (20 points) Implement F using one 8-to-1 MUX and a minimal number of basic gates. Assume the MUX is implemented using the idea in Fig. 4.1 and Fig. 4.2 but extend to a 8-to-1 MUX. What is the total cost of your implementation (including the gates inside the MUX)?

$\Sigma m(1,4,5,6,7) \Rightarrow$

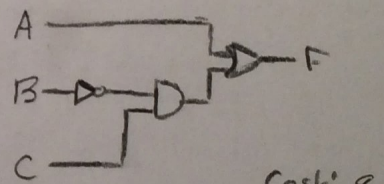


a)



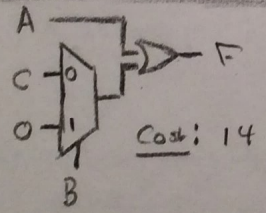
Cost: 44

b)



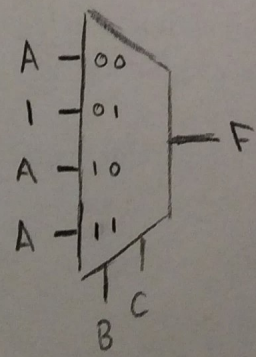
Cost: 8

c)

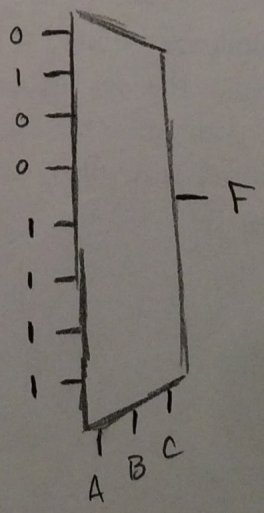


Cost: 14

d)



Cost: 25



Cost: 55