EE 330
Homework Assignment 3

Fall 2018
Due date: Monday Sept 10

Problem 1 Problem 1.6 of WH part b) only. Modify this problem to the design of this function first using the compound gate approach and second, using the static CMOS gate (NAND and NOR gates) approach. Compare the number of levels of logic and the total transistor count in the two approaches.

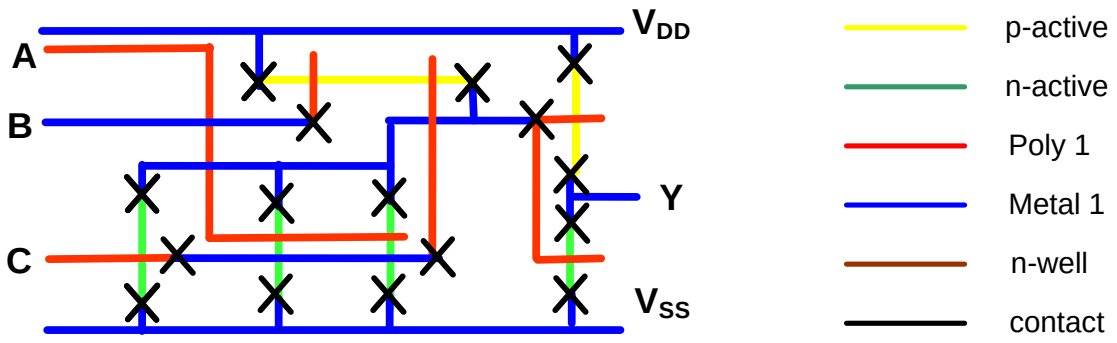
Problem 2 Problem 1.9 part b) only of WH. Restrict the gates you use in this solution to NOR gates only.

Problem 3 Determine the output transitions t_{LH} if a two-input CMOS NOR gate is driving a 60fF load capacitance and both inputs transition from high to low at the same time. Assume all devices are minimum-sized and V_{DD}=3V.

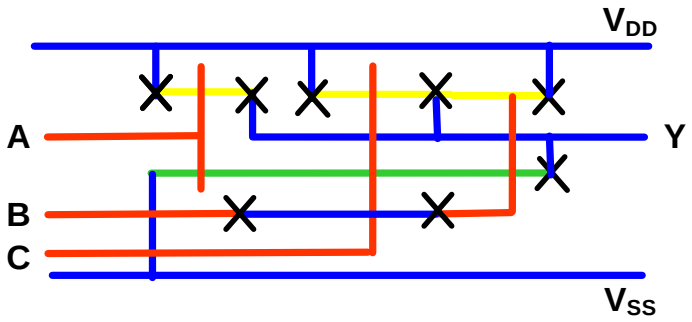
Problem 4 Give a transistor-level circuit schematic and sketch a stick diagram for a CMOS 3-input OR gate designed by following a 3-input NOR gate with an inverter. The three inputs to the gate should be on the left side of the stick diagram and the output on the right side of the diagram. All inputs and the output should be in Metal 1.

Problem 5 Problem 1.15 of WH

Problem 6 The stick diagram of a circuit is shown. Give a circuit schematic for this circuit. The color-code for the stick diagram is shown to the right.

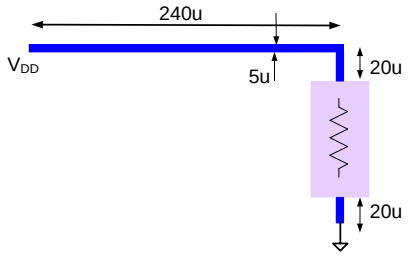


Problem 7 A stick diagram has been put together for a 3-input CMOS NAND gate and is shown below. There are one or more errors in this stick diagram. Identify and correct all errors in the stick diagram. The color-code for the stick diagram is shown in the previous problem.



Problem 8 A Metal-1 interconnect (shown in blue) is used to connect a V_{DD}=5V supply voltage to a resistor. Assume the nominal value of the resistor (shown in the purple box) is 50Ω. Unfortunately there is some resistance in the interconnect and this causes some voltage loss to the load when current is flowing through the interconnect. Assume the interconnect is made of aluminum and is 0.2um thick.

a) What voltage will actually appear across the 50 Ω resistor
b) What voltage would actually appear across the resistor if copper was used instead of aluminum for the interconnect. Assume it is of the same thickness.
c) The voltage drop can be decreased by increasing the width of the interconnect. How wide does an aluminum interconnect need to be guarantee that the voltage drop across the load is no more than 5% below the supply voltage?



Hint: You may find Sec 6.1 and Sec 6.2 of the text useful for solving this problem

Problem 9 Assume a CMOS inverter designed in the ON 0.5µ CMOS process drives 6 identical devices and the supply voltage is 3.5V. If a step input from 3.5V to 0V is applied at the input, what is the LH output transition time? Assume minimum-sized devices are used and also assume V_{DD}=3.5V.

Problem 10 Use Modelsim to create a 2-to-1 multiplexer (MUX) with two 2-bit inputs, 1 select bit, and one 2-bit output (see diagram below). Create a test bench for the code and show the simulation results and waveforms.