EE 330
Assignments 14
Spring 2018
Due Monday April 23

Solve any 10 problems.

If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=350\mu A/v^2$, $\mu_p C_{OX}=70\mu A/v^2$, $V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, $L_{MIN}=W_{MIN}=0.18\mu$, and $V_{DD}=2V$.

Problem 1

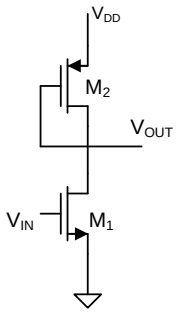
A static CMOS inverter with $W_n=W_p=2\mu$ and $L_n=L_p=1\mu$ designed in a 0.18μ CMOS process is driving a 4pF load. Determine t_{HL} and t_{LH} for the output of this inverter.

Problem 2 If a semiconductor process were available with $V_{Tn}=0.3V_{DD}$ and $V_{Tp}= -0.1V$, determine R_{pd}, R_{pu}, t_{HL}, t_{LH}, and V_{trip} of a minimum-sized inverter if it is driving an 8fF load. Assume $\mu_n C_{OX}=350\mu A/v^2$, $\mu_p C_{OX}=70\mu A/v^2$, and $V_{DD}=2V$.

Problem 3 In the same semiconductor process described in Problem 2, give a sizing strategy needed to place V_{trip} at $V_{DD}/2$.

Problem 4 In the same semiconductor process described in Problem 2, give a sizing strategy needed to achieve $t_{HL}=t_{LH}$.

Problem 5 If the n-channel device is minimum sized ($W_{min}=L_{min}=0.18u$), size the device M_2 so that $V_{TRIP}=V_{DD}/2$. Assume that $V_{DD}=2V$,



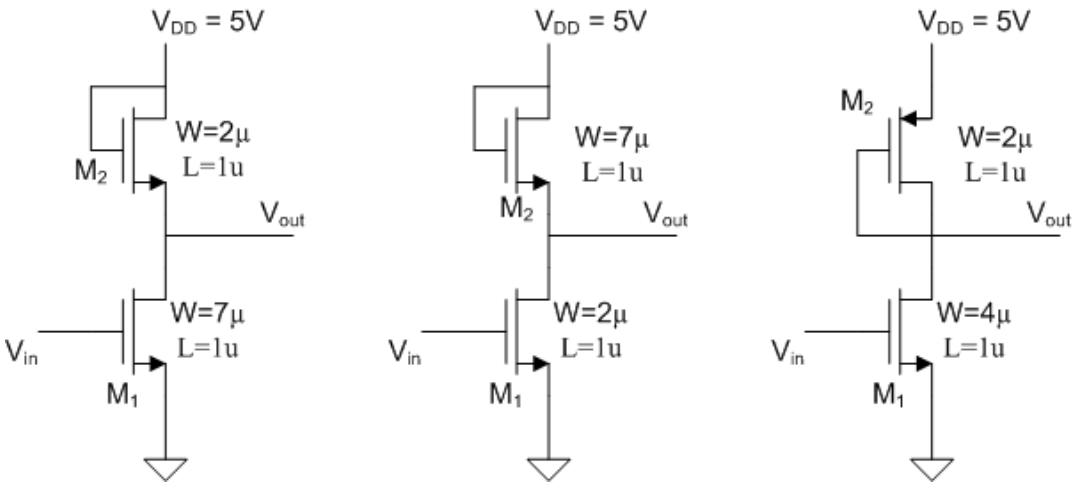
Problem 6 Determine V_H and V_L for the inverter in Problem 5 using the sizing determined in that problem.

Problem 7 Consider a two-input NOR gate sized for equal worst-case rise and fall times that is driving an identical device.

a) Determine the trip points for all combinations of input transitions
b) Determine the fastest and slowest t_{LH} for the output of the first gate in this cascade.

Problem 8 Size the devices in a 4-input NOR gate for equal worst-case rise and fall times.

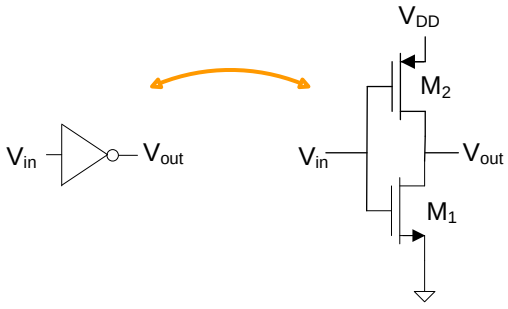
Problem 9 The circuits shown have been proposed as digital inverters. Determine which will behave as digital inverters and which will not. If the circuit performs as a digital inverter, determine V_H and V_L. Assume the devices are all in the process with $\mu C_{OX}=100uA/V^2$, $V_T=1V$, $\gamma = 0$ and $\lambda=0$.



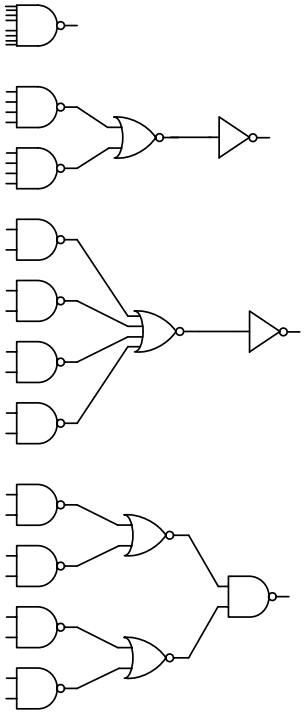
Problem 10 What is the maximum value of W_1 in the circuit (a) of the previous problem that can be used if this circuit is to perform as a digital inverter?

Problem 11 Determine the trip-point, V_H, and V_L of the inverter under the following scenarios and comment on how device dimensions affect these key characteristics. Assume $\mu_n C_{OX}=350uA/V^2$, $V_{Tn}=0.5V$, $V_{Tp}=-0.5V$, $V_{DD}=2V$, $\mu_n/\mu_p=5$, $\gamma=0$ and $\lambda=0$.

a) $W_1=0.18u$, $W_2=0.9u$, $L_1=0.18u$, $L_2=0.18u$
b) $W_1=3u$, $W_2=15u$. $L_1=3u$, $L_2=3u$
c) $W_1=0.18u$, $W_2=0.18u$. $L_1=0.18u$, $L_2=0.18u$
d) W1=0.18u, W2=0.54u. L1=0.18u, L2=1.8u



Problem 12 Four different implementations of the 8-input NAND function are shown. If the devices are sized for equal worst-case rise and fall times, compare the input capacitance at each input and the total area for these 4 different implementations



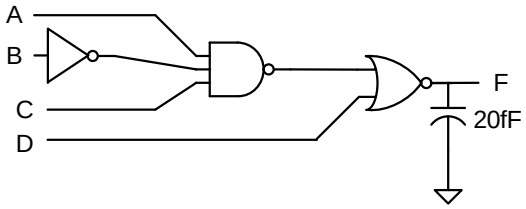
Problem 13 Assume a load capacitance of 40fF is to be driven. Determine t_{HL} and t_{LH} if it is driven by an equal rise/fall inverter (termed the reference inverter) and if it is driven by a minimum-sized inverter.

Problem 14 Assume a 4-input NAND gate, sized for equal worst-case rise and fall times, is driving 10 equal worst-case rise and fall time inverters (termed reference inverters).

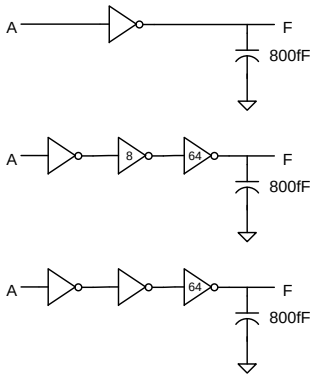
a) Determine t_{HL} and t_{LH} if the switch-level model is used for the MOS transistors.

b) Repeat part a) using the Elmore delay model if there is a parasitic capacitance on each drain and source diffusion of 400Af.

Problem 15 Determine the propagation delay ($t_{HL}+t_{LH}$) from B to F for the following circuit. Assume all devices sized for equal worst-case rise and fall times.



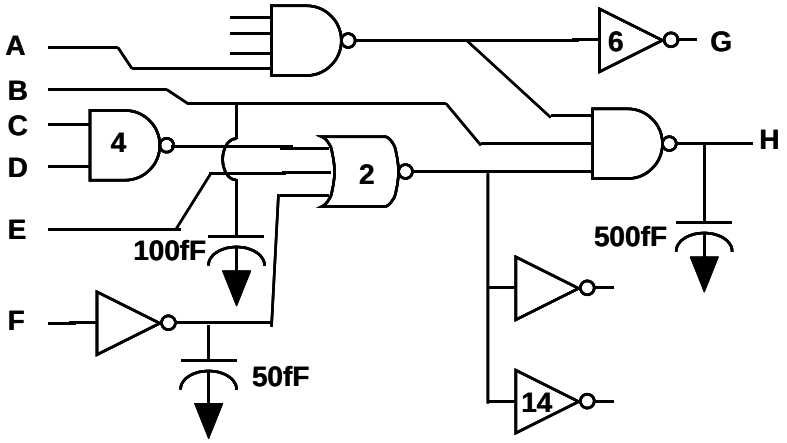
Problem 16 Three different circuits are shown driving the same load. The overdrive factors if different than 1 are indicated. Quantitatively compare the propagation delay of these circuits.



Problem 17 A logic circuit designed in conventional CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 1.5fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the D input to the H output

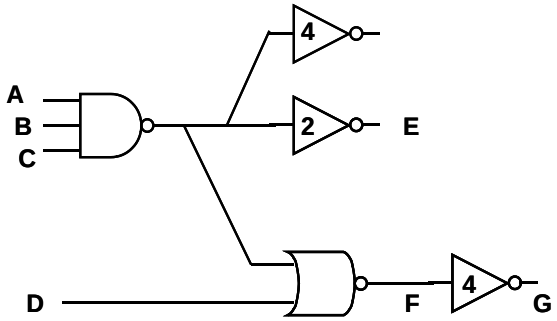
b) Repeat part a) if all devices are minimum sized (the overdrive factor is no longer germane). Assume the input capacitance to the reference inverter is now 0.8fF.



Problem 18 Assume you are working in a 0.18u CMOS process.

a) Size the devices in the 3-input NAND gate for an overdrive of 6 and the 2-input NOR gate for an overdrive of 3 with the equal rise/fall sizing strategy. The overdrive factors for the inverters are indicated.

b) With this sizing, how does the propagation delay from B to G compare to that of a minimum- sized reference inverter driving an identical device?



Problem 19 Assume you have need to drive a 280 pF load as fast as possible. Design an output pad driver that drives this load as fast as possible. Assume the input signal that you are directing to the load drives a minimum-sized reference inverter and that your pad driver is attached to the output of this inverter. Assume you are working in the 0.18u TSMC process and that an equal rise and fall time sizing strategy is to be used.

Problem 20 Assume you are working in a 1u CMOS process (assume Lmin = Wmin = 1u) with V_{DD} = 5V, V_{TN} = 1.5V,V_{TP} = -.5V, C_{OX}=1fF/u^2 and uC_{OX} = 100uA/V^2.

a) Size a CMOS inverter so that V_{TRIP} = 2.5V

b) Size the inverter to that t_{HL} = t_{LH} with t_{HL} as small as possible.

Problem 21 The overdrive factors on each gate are as indicated. The M indicates minimum sizing. If nothing is indicated, assume sizing for equal worst-case rise and fall times. Determine the propagation delay from A to F in terms of t_{REF} for the process.