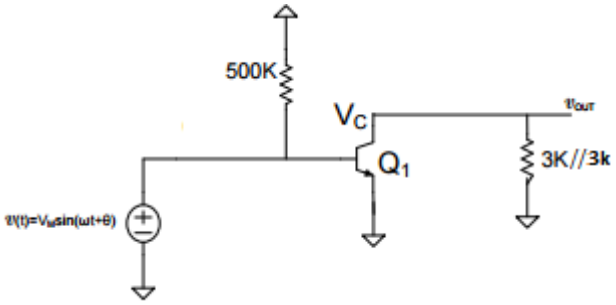
EE330 Fall 2017 HW 9 solutions TA: Joseph Aymond

Problem 1

a)



b) $V_{cq} = 10V - (2k * I_{cq})$

$I_{cq} = \frac{\beta(10 - 0.6)}{500k} = 1.88\ mA$

$V_{cq} = 10V - (2k * 1.88m)$

$V_{cq} = 6.24V$

$V_{outq} = 0$

c) Using the know gain, $A_V = -g_m R_L$

$A_V = -g_m(2k|2k) = -gm(1k)$

$gm = \frac{I_Q}{V_t} = \frac{\beta(10 - 0.6)}{500k * 0.0259} = 0.0726V$

$A_V = -0.0726 * 1000$

$A_V = -72.6$

d) $V_o = -72.6 * 200 * 10^{-6} * \sin(\omega t + \theta)$

$V_o = 14.52 \sin(\omega t + \theta)\ mV$

e) $V_{out} = V_{outq} + V_o$

$V_{out} = 6.24 \pm 14.52 \sin(\omega t + \theta)\ V$

Problem 2

a) $I_D = \mu C_{ox} \left(\frac{W}{2L}\right) (V_{gs} - V_T)^2 = 1.013\ mA$

$V_{ds} \geq V_{gs} - V_T$

$V_{ds} \geq 1.5$

$\rightarrow R_1 = \frac{4 - 1.5}{0.001013} = 2467\Omega$

b) $A_V = -gmR_1 = -(0.00135)(822.3) = -1.11$

c) $\frac{4-V_D}{822.3} = 0.001013$
$V_{DQ} = 3.17V$
$V_D = V_{DQ} + A_V V_{in}(t)$
$V_D = 3.17 + 0.00111\sin(5000t + 75^o)\ V$

Problem 3
Because M_2 is diode connected it can be modeled as $G_L = g_m + g_{02}$, because we can assume $g_{02} \approx 0$ we can say $G_L = g_m$. From this we can create the gain

$$A_V = -\frac{g_{m1}}{g_{m2}}$$
$$V_{out} = A_V V_{in} = -\frac{g_{m1}}{g_{m2}} V_m \cos(\omega t + \theta)$$

Problem 4

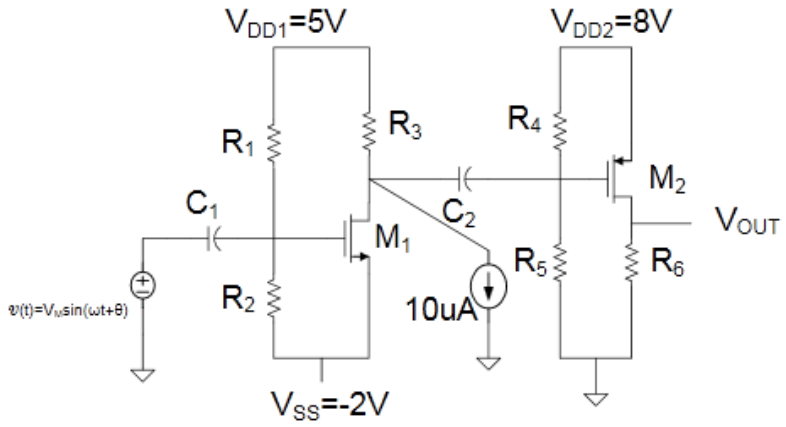
$$A_V = -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{\frac{\mu_n C_{ox} w_1}{l_1}}\sqrt{2I_{DQ}}}{\sqrt{\frac{\mu_p C_{ox} w_2}{l_2}}\sqrt{2I_{DQ}}}$$

This can mostly be cancelled out and gets us the equation

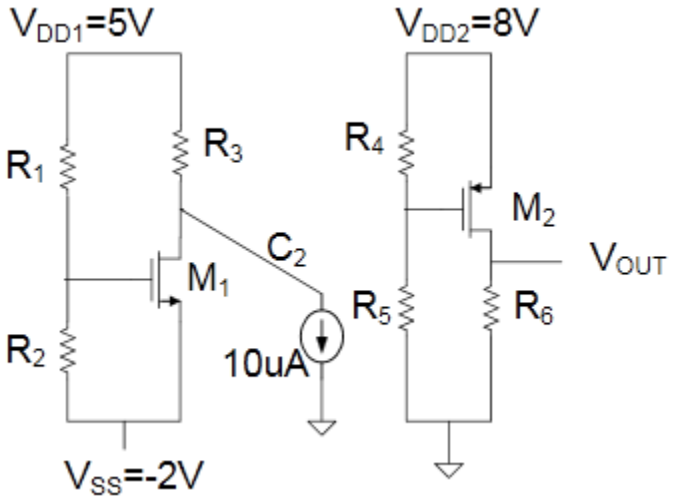
$$A_V = -\sqrt{\frac{\mu_n}{\mu_p}}\sqrt{\frac{W_1 L_2}{W_2 L_1}}$$
$$A_V = \sqrt{\frac{10}{3}}\sqrt{\frac{10 * 1}{6 * 2}}$$
$$A_V = -\frac{5}{3} V_{in}(t)$$

$$V_{outq} = V_{outQ} + A_V V_{in}$$
$$I_{DQ} = \mu_n C_{ox}\left(\frac{W_n}{2L_n}\right)(V_{gs} - V_{TN})^2 = \mu_p C_{ox}\left(\frac{W_p}{2L_p}\right)(V_{out} - V_{DD} - V_{TP})^2$$
$$\rightarrow V_{outQ} = 2V \text{ or } 7V$$
$$V_{out} = V_{outQ} + A_V V_{in}$$
$$V_{out} = 2V - \frac{5}{3} V_M \cos(\omega t + \theta)$$

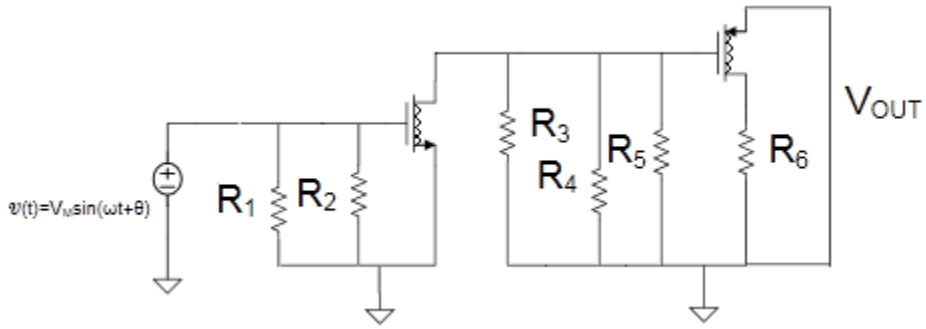
Problem 5



DC circuit

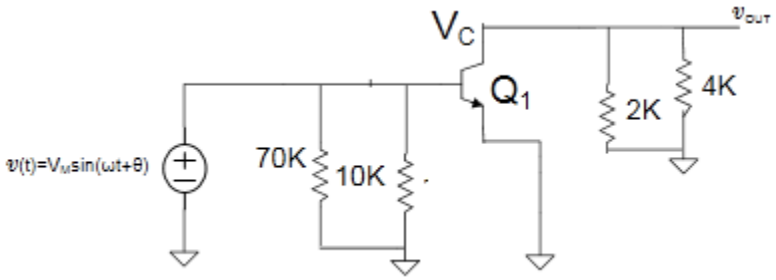


AC circuit



Problem 6

g)



h) $V_B = 32 * \left(\frac{10}{10+70}\right) k = 4V$

$I_{CQ} = \frac{4 - 0.6}{2k} = 1.7\ mA$

$V_{CQ} = 32 - (2k)(I_{CQ})$

$V_{CQ} = 28.6V$

$V_{outq} = 0V$

I) $A_V = -gm(R_L) = -\frac{I_{CQ}}{V_t} * R_L = -\frac{1.7\ mA}{25.9\ mV} * 1.33k$

$A_V = -87.3$

j) $V_{out} = A_V V_{in} = -87.3 * 0.001 \sin(2000\pi t + \theta)$

$V_{out} = -0.0873 \sin(2000\pi t + \theta)$

Problem 7

$I_{DQ} = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{gs} - V_T)^2$

$I_{Dss} = -g_m * V_{in}(t)$

$g_m = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{gs} - V_T) = \frac{0.15\ mA}{V}$

$V_{out} = I_{Dss} * 15k$

$V_{out} = 0.0563 \sin(2\pi * 1000t)$

Problem 8

Right:

$$V * (g_m + g_o) = I \rightarrow R_{eq} = \frac{1}{(g_m + g_o)} \cong \frac{1}{g_m}$$

$$g_m = \sqrt{2 * \mu_n C_{ox} \left(\frac{W}{L}\right) * I_D} \rightarrow assume \left(\frac{W}{L}\right) = 6$$

$R_{eq} = 912.87\ \Omega$

Left:

$$V * (g_m + g_\pi + g_o) = I \rightarrow R_{eq} = \frac{1}{(g_m + g_\pi + g_o)} \cong \frac{1}{g_m}$$

$$g_m = \frac{I_{CQ}}{V_t} = \frac{1\ mA}{26\ mV}$$

$R_{eq} = 26\ \Omega$

Problem 9

a) $y_{11} = \frac{\delta I_1}{\delta V_1} = V_2^2$

$y_{12} = \frac{\delta I_1}{\delta V_2} = 2V_1V_2$

$y_{21} = \frac{\delta I_2}{\delta V_1} = 0.04V_1V_2 \exp(0.2V_1^2V_2)$

$y_{22} = \frac{\delta I_2}{\delta V_2} = 0.02V_1^2 \exp(0.2V_1^2V_2)$

b)

$V_1 = 5V \ \ V_2 = 1V$

$y_{11} = 1$

$y_{12} = 10$

$y_{21} = 29.68$

$y_{22} = 74.21$

c)

$I_{1Q} = (5)(1)^2 = 5A$

$I_{2Q} = 0.1 \exp(0.2(5)^2(1)) = 14.84A$

d)

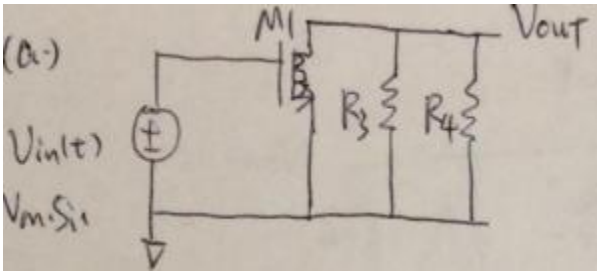
$i_1 = y_{11}V_1 + y_{12}V_2 = 1mV_{RMS} + 10 * 2mV_{RMS}$

$i_1 = 21mV_{RMS}$

$i_2 = y_{21}V_1 + y_{22}V_2 = 29.68 * 1mV_{RMS} + 74.2 * 2mV_{RMS}$

$i_2 = 178.08mV_{RMS}$

Problem 10



b)

Assuming M_1 is working in saturation (W=8, L=12)

$$I_D = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{gs} - V_T)^2 = \frac{V_{DD} - V_D}{R_3}$$

$I_D = 33.3\ \mu A$

$V_D = 1.67V$

c) $A_V = -g_m(R_3||R_4) = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_D} * \frac{R_3 * R_4}{R_3 + R_4}$

$A_V = -2.22$

d) $V_{out} = A_v V_{in}(t)$

$V_{out} = -44.4 \sin(\omega t + \theta)\ mV$

Problem 11

Assume M_1 is in saturation

$$I_D = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{GS} - V_T)^2 = \frac{4V - V_{outQ}}{R_1}$$

$$A_V = -g_{m1}R_1 = -\left(\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)\right)R_1 = -8$$

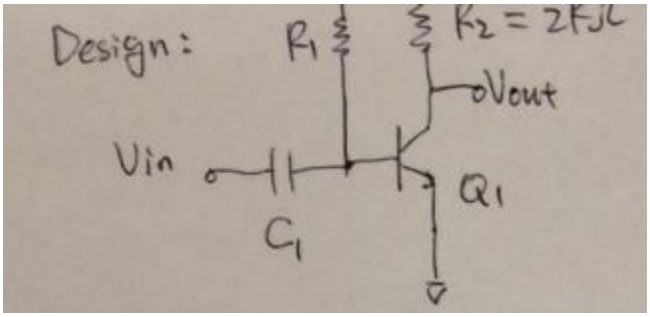
$\rightarrow \frac{W}{L} = 4$

$W = 4\mu \qquad L = 1\mu$

Verify: $V_{DS} = 2V > 1V = V_{GS} - V_T \rightarrow$ it is in saturation

$V_{outQ} = 0$

Problem 12



$$A_V = -\frac{I_{CQ}R_2}{V_t} = -5$$

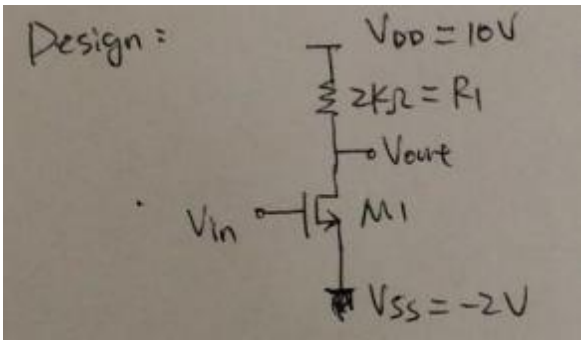
$$I_{CQ} = \frac{5 * 0.026}{2k\Omega} = 65\ uA$$

$$I_{BQ} = \frac{I_{CQ}}{\beta} = 0.65\ \mu A$$

$$\rightarrow R_1 = \frac{(10 - 0.6)V}{0.65 * 10^{-6}A} = 14.46\ M\Omega$$

The emitter area has almost no effect on the gain of this circuit, so choose a convenient value of A_E such as $100\mu^2$

Problem 13



$$A_V = -g_m R_1 = -10,\ \ R1\ is\ 10K, not\ 2K$$

$$g_m = \frac{\mu_n C_{OX} W}{L}(V_{gs} - V_T)$$

$$\frac{W}{L} = \frac{10}{1}, W = 10\mu,\ \ L = 1\mu$$

$$I_D = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{GS} - V_T)^2$$

$$I_D = 0.5\ mA$$

$$V_{outQ} = 10V - 10\ k\Omega * 0.5\ mA = 5V$$

Veriy: $V_{DS} > V_{GS}$

$7V > 1V \rightarrow$ Verified.

Problem 14

Code:

```
Ln#
 1
 2   module reg4b_en(en, clk, in, out);
 3     input en, clk;
 4     input [3:0] in;
 5     output [3:0] out;
 6     reg clk_gate;
 7
 8     always @(posedge clk) begin
 9       if(en)
10         clk_gate = clk;
11       else
12         clk_gate = 0;
13     end
14
15     DFF dff0(.D(in[0]), .Q(out[0]), .clk(clk_gate));
16     DFF dff1(.D(in[1]), .Q(out[1]), .clk(clk_gate));
17     DFF dff2(.D(in[2]), .Q(out[2]), .clk(clk_gate));
18     DFF dff3(.D(in[3]), .Q(out[3]), .clk(clk_gate));
19
20   endmodule
21
```

DFF:

```
Ln#
 1
 2   module DFF(D, Q, notQ, clk);
 3     input D, clk;
 4     output Q, notQ;
 5     reg Q, notQ;
 6
 7     always@(posedge clk) begin
 8         Q <= D;
 9         notQ <= ~D;
10     end
11
12   endmodule
```

Testbench:

```
Ln#
 1  `timescale 1ns/1ps
 2  module reg4_en_tb();
 3
 4    reg enable, clock;
 5    reg [3:0] in;
 6    wire [3:0] out;
 7
 8
 9    reg4b_en test(.en(enable), .clk(clock), .in(in), .out(out));
10
11    initial begin
12      clock = 0;
13      enable = 0;
14      in = 4'b1110;
15      #38
16      in = 4'b1100;
17      #38
18      in = 4'b1000;
19    end
20
21    always #10 clock = ~clock;
22    always #33 enable = ~enable;
23
24
25  endmodule
26
```

Output: