EE 330
Homework Assignment 4
Spring 2018 (Due Friday Feb 2)

Problem 1 3.1 of Weste and Harris (WH)

Problem 2 3.2 of WH

Problem 3 If a transistor of length 10nm and width 15nm has a gate oxide thickness of 25A^o, how many silicon dioxide molecules will be needed for the gate oxide?

Problem 4 What is the resistance in an aluminum interconnect that is 200μm long, 120nm wide, and 80nm thick.

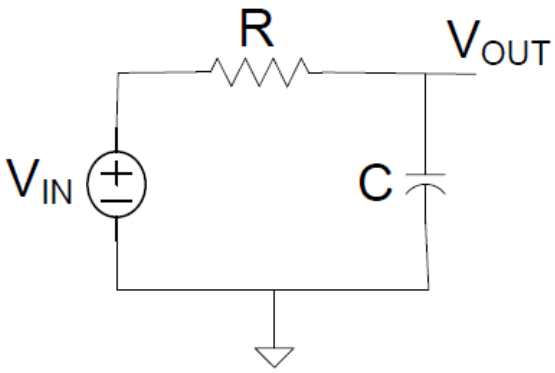
Problem 5 3.5 of WH

Problem 6 How many 12 inch wafers can be obtained from a 2m silicon pull? Assume the kerf width when a wire saw is used is to cut the wafers is 120μm. In solving this problem, state and use a typical value for the wafer thickness.

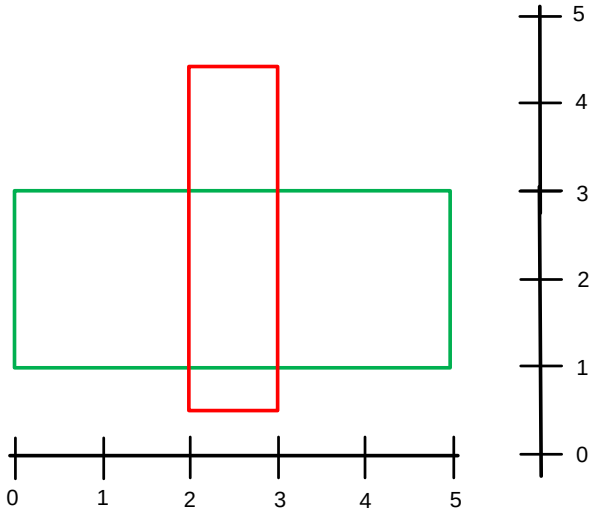
Problem 7 A first-order RC filter is shown. The 3-dB band edge of this filter is given by $\omega_{3dB} = \frac{1}{RC}$. Assume Poly 1 is used to make the resistor and the capacitor is a Poly Insulator Poly (PIP) capacitor. This filter is to be fabricated in the ON 0.5μ CMOS process that is characterized by the parameters attached to this assignment.

a) Design this circuit and estimate the area required to implement this filter in your design if the 3dB band edge is to be located at 500 Hz and the capacitor value is 10 pF.

b) If the resistor is too big or the capacitor is too big, the area required to realize this filter becomes very large. Determine the value of R and C that will minimize the total area and compare the area required for the "minimal area" design with that you required in part a). Use a serpentine layout for the resistor.



Problem 8 Consider the layout of a transistor shown below where red is polysilicon and green is n-active. Rulers with dimensions in µm are shown.



a) What is the drawn length and width of the transistor?
b) Assume positive photoresist is used pattern the polysilicon region to protect it during the polysilicon etch. If the photoresist is under-exposed so that the edges move by 0.1µm from the desired location and the photoresist development is perfect, and the polysilicon is under-etched so that the edges move by 0.1µm, what will be the actual length and width of the transistor?
c) Repeat part b) if negative photoresist is used.

Problem 9 An aluminum interconnect 250µm long and 2µm wide has a measured resistance of 25Ω. Determine the thickness of the aluminum interconnect and the sheet resistance.

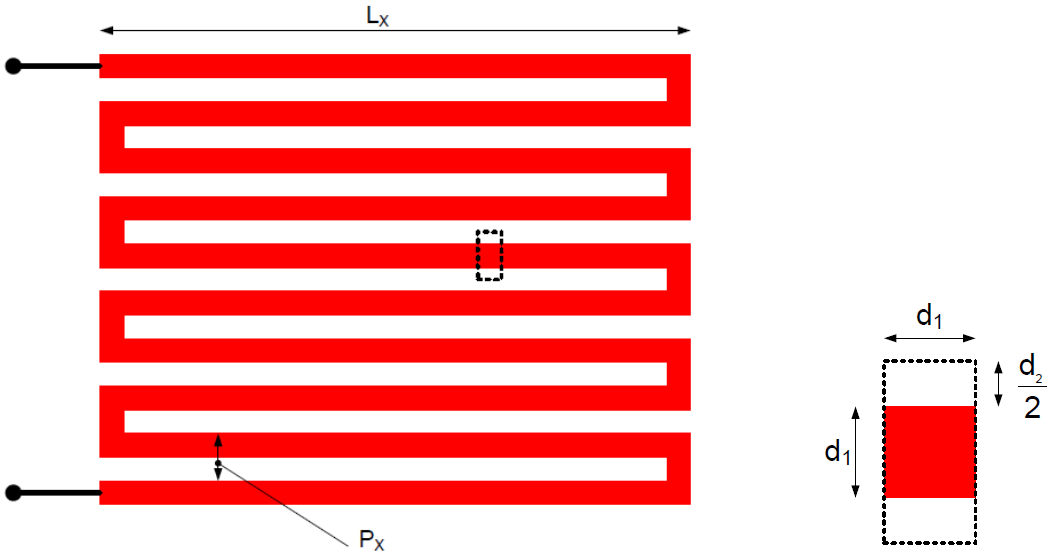
Problem 10 If a copper interconnect has the same thickness and the same width as the aluminum interconnect in Problem 9, how long could it be if it also had the same resistance?

Problem 11 Thermal oxide growth of field oxide causes the wafer surface to become somewhat nonplanar. If 5000Å of field oxide is thermally grown, what is the difference in the thickness of the wafer between regions where field oxide is present and where it is absent. In solving this problem, state and use a typical value for the wafer thickness.

Problem 12 Compare the area required for the layout of a 10K resistor using Poly 1 to that required using p+ diffusion in the ON 0.5µ CMOS process. Use a serpentine layout with minimum width and minimum spacing for the resistive elements and be sure that you meet the design rules of the process. The sheet resistance is characterized in the parameter file located at http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t6au-params.txt (A brief discussion of a serpentine layout appears below).

Serpentine layout:

A serpentine (sometimes termed "meander")layout is shown below. For large valued resistors, the length L_X is generally much larger than the pitch, P_X. The dashed box which includes exactly one square of resistance is expanded below. The dimension d_1 corresponds to the minimum width of the "one-square" resistor and d_2 to the minimum spacing between the serpentine resistor stripes.



Problem 13 and 14 Use Modelsim to create a one-bit half adder. The half adder should have two one-bit inputs, a one-bit output, and a one-bit carry output. Then use the half adder to create a one-bit full adder. The full adder should have two one-bit inputs and a carry in bit. For the outputs use a one-bit output and a carry out bit. Be sure to include screenshots of your Verilog code, and simulation waveforms.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

Extra – Not assigned for fall13

Problem 13 The term **dual damascene** refers to a particular type of interconnect. What does this refer to and what are the benefits of a process that provides dual damascene interconnects?

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Problem 3 Repeat Problem 2 if the low-k dielectric SiLK were used instead of SiO_2. Comment on which of (HfO_2, SiO_2 or SiLK, is the most desirable if used

a) As a dielectric for a gate of a MOS transistor
b) As an insulator between two levels of metal in an interconnect

Problem 13 and 14
Using ModelSim, implement the logic function

$$F = A + B + C$$

using inverters and NAND gates. Include screenshots of your code and simulations.

Problem 13 and 14: Use Modelsim to create a 1-to-4 De-Multiplexer. The De-Multiplexer should have a 4-bit input, two select bits, and four 4-bit outputs. Create a test bench to validate your design. Include screenshots of your Verilog code and simulation results.