EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Exam 1

Spring 2018

Instructions: Students may bring 1 page of notes (front and back) to this exam and a calculator but the use of any device that has wireless communication capability is prohibited. There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$; if reference to a diode is made, assume the process parameter; $J_S=10^{-17}A/\mu^2$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

1. (2pts) There were two major challenges that needed to be overcome for the industry to replace aluminum interconnects with copper interconnects? Give one of these two challenges.

2. (2pts) What is the major reason that contacts from metal to poly are not allowed on top of the gate of a transistor?

3. (2pts) In the late 1940's, the bipolar transistor was invented and it replaced an electronic device that had been used for many years. What electronic device did the bipolar transistor replace?

4. (2pts) SiO_2 is often thermally grown to form a gate oxide. But if SiO_2 is placed on top of metal, a different process is used to form the SiO_2 layer. What process is typically used to form SiO_2 on top of metal?

5. (2pts) How many valence band electrons does Silicon have?

6. (2pts) Static CMOS gates that have pull-up networks comprised of only p-channel devices, pull-down networks comprised of only n-channel devices, and a circuit structure that results in one and only one of these two networks conducting for any Boolean input have 3 very attractive properties. Give two of these three attractive properties.

7. (2pts) What is the distinction between a "contact" and a "via" in a semiconductor process?

8. (2pts) The capacitance between the anode and cathode of a reverse-biased pn junction is quite voltage dependent. Describe what happens in this junction that makes this capacitance voltage dependent.

9. (2pts) The parameter I_S in the standard diode equation is challenging to measure accurately in our laboratory. What is the reason that it is challenging to measure this term accurately in our laboratory

10. (2pts) Why is the capacitance density of Metal 3 to substrate considerably lower than the capacitance density of Metal 1 to substrate in a semiconductor process?

Problem 1 (16 pts) Assume a circuit was designed in a 180nm process with a die area of $5mm^2$. The circuit was fabricated on 8" wafers. The cost of the wafers coming out of the foundry (after processing) was $2500. Though the foundry usually gives the defect density to customers, for some reason the designer was unable to get the defect density from the foundry because the foundry representative argued that the defect density was proprietary. For this reason, the designer was unable to predict the yield or the cost per good die. The circuit was manufactured anyway and after fabrication, 200,000 chips were tested of which 1050 were defective and all defective die failed because of hard faults.

a) What was the defect density in the process?

b) What is the cost per good die for this design?

Problem 2 (16 pts) Consider a Boolean system with three inputs, **A, B**, and **C**, and output **F** defined by the function

$$F = A + \left(\overline{B} \bullet C\right)$$

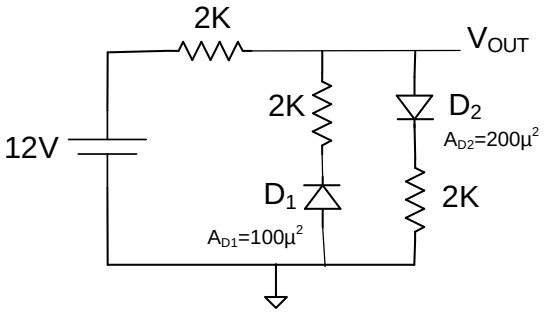
a) Design a CMOS circuit, at the transistor level, that implements the Boolean system described using only NAND and NOR logic gates. Assume the inputs that are available are **A, B**, and **C**.

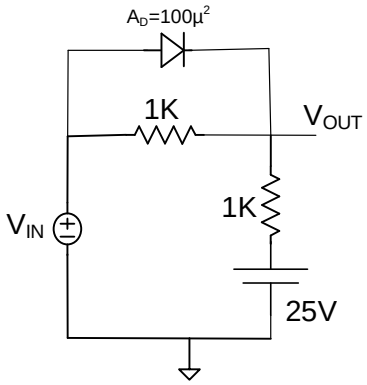
b) Repeat part a) but use compound logic gates instead of NAND and NOR logic.

Problem 3 (16 pts) Consider the following two circuits.

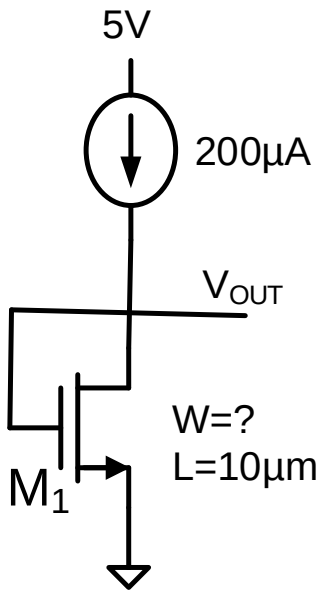
a) For the circuit on the left, determine V_{OUT}

b) For the circuit on the right, assume $V_{IN}=100\sin 1000t$. Obtain an expression for and plot V_{OUT} for one period of the excitation





Problem 4 (16 pts) Consider the following circuit. Determine the width W of transistor M_1 so that V_{OUT}=2.5V.



Problem 5 (16 pts) Assume a resistor R_1 has a resistance of 2KΩ at T=250K and a resistor R_2 has a resistance of 1K at T=250K. Assume the TCR of R_1 is constant of value 1000 ppm/°C and the TCR of R_2 is constant of value -500 ppm/°C.

a) What will be the resistance of R_1 at 300K

b) If R_1 and R_2 are placed in series to form a 3K resistor, what will be the percent change in resistance if the temperature is increased from 250K to 300K?

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um