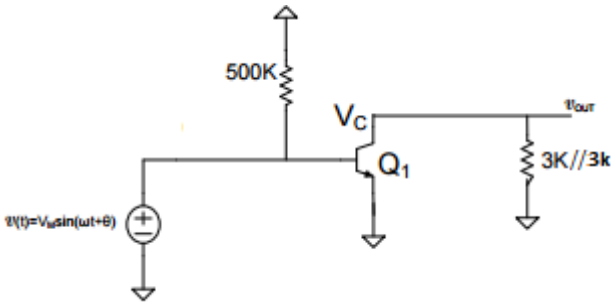
EE330 Spring 2018 HW 9 solutions TA: George Alphonse

Problem 1

a)



b) $V_{cq} = 10V - (2k * I_{cq})$

$I_{cq} = \frac{\beta(10 - 0.6)}{500k} = 1.88\ mA$

$V_{cq} = 10V - (2k * 1.88m)$

$V_{cq} = 6.24V$

$V_{outq} = 0$

c)

$v_{out} = (-g_m v_{IN}) * (\frac{1}{g_o} // R_L)$

$A_v = \frac{v_{OUT}}{v_{in}} = -g_m(\frac{1}{g_o} // R_L)$

Approximate gain, $A_V = -g_m R_L$

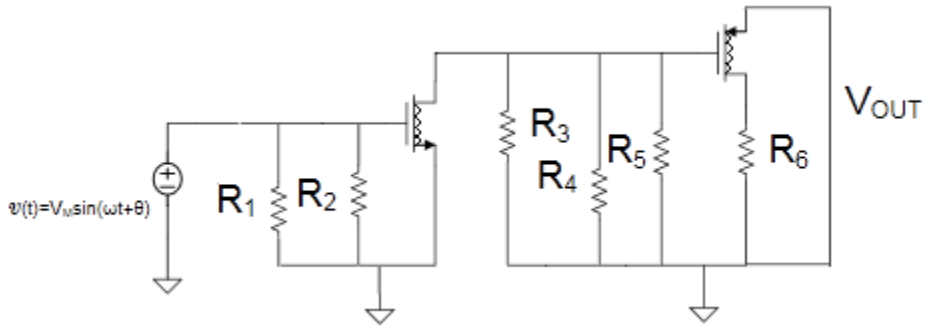
$A_V = -g_m(2k|2k) = -gm(1k)$

$gm = \frac{I_Q}{V_t} = \frac{\beta(10 - 0.6)}{500k * 0.0259} = 0.0726V$

$A_V = -0.0726 * 1000$

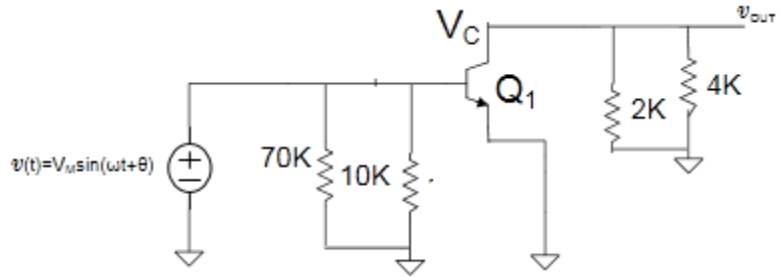
$A_V = -72.6$

Problem 2



Problem 3

a)



b) $V_B = 32 * \left(\frac{10}{10+70}\right) k = 4V$

$I_{CQ} = \frac{4 - 0.6}{2k} = 1.7\ mA$

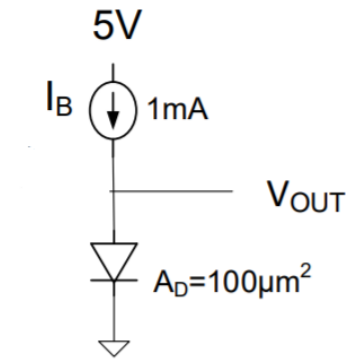
$V_{CQ} = 32 - (2k)(I_{CQ})$

$V_{CQ} = 28.6V$

$V_{outq} = 0V$

Problem 4

a.) DC equivalent circuit

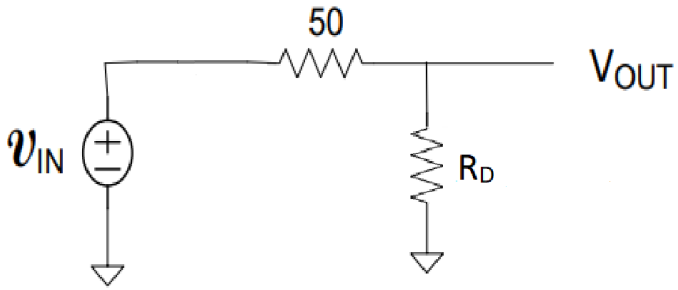


$I_{DQ} = 1mA$

$V_t = (8.615 * 10^{-5}) * (300) = 25.85mV$

$$I_{DQ} = J_S A_D e^{\frac{V_D}{Vt}} \rightarrow V_D = V_{OUT} = V_t * \ln\left(\frac{I_{DQ}}{J_S A_D}\right) = (25.85mV) * \ln\left(\frac{1mA}{\frac{0.5fA}{\mu m^2} * 100\mu m^2}\right) = 0.613\ V$$

b.)



c.)

$$R_D = \frac{V_t}{I_{DQ}} = \frac{25.85mV}{1mA} = 25.85\ \Omega$$

$$v_{out} = \frac{R_D}{R_D + 50\Omega} v_{in}$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{R_D}{R_D + 50\Omega} = \frac{25.85\Omega}{25.85\Omega + 50\Omega} = 0.34\ V/V$$

d.)

$$R_D = \frac{25.85mV}{5mA} = 5.17\ \Omega$$

$$A_v = \frac{5.17\Omega}{5.17\Omega + 50\Omega} = 0.094\ V/V$$

Problem 5

$$I_2 = J_s A_{D2} e^{\frac{V_{OUT}}{Vt}} = \frac{0.5fA}{\mu m^2} * 100\mu m^2 * e^{\frac{V_{out}}{25.85mV}}$$

$$I_{D1} = \frac{0.5fA}{\mu m^2} * 300\mu m^2 * e^{\frac{V_{out}}{25.85mV}}$$

$$I_B = 1mA = I_{D1} + I_2$$

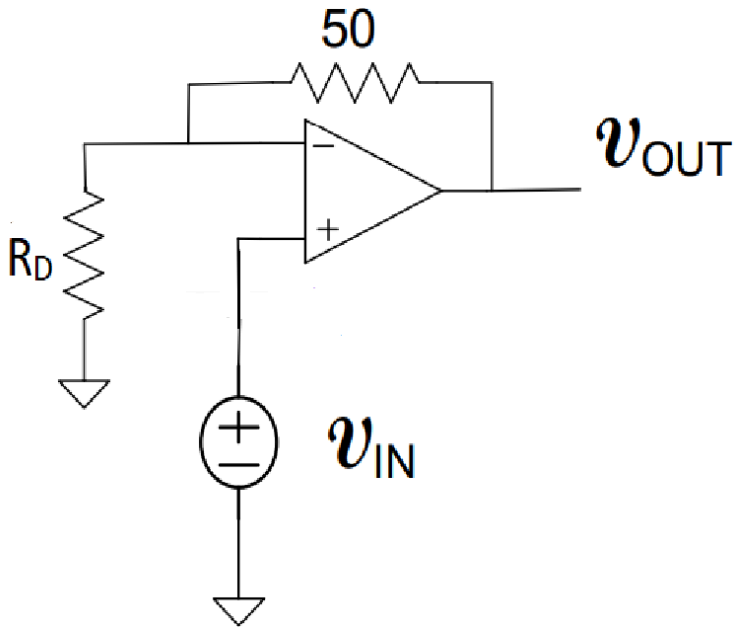
Solve system of equations

$I_2 = 250\ \mu A$

$V_{out} = 0.577\ V$

Problem 6

a.) Small signal equivalent circuit



$$R_D = \frac{V_t}{I_{DQ}} = \frac{25.85mV}{1mA} = 25.85\ \Omega$$

$$A_v = 1 + \frac{50\ \Omega}{R_D} = 1 + \frac{50\ \Omega}{25.85\ \Omega} = 2.93\ V/V$$

b.)

$$R_D = \frac{25.85mV}{10mA} = 2.59\ \Omega$$

$$A_v = 1 + \frac{50\ \Omega}{2.59\ \Omega} = 20.34\ V/V$$

Problem 7

MOSFET:

$$V * (g_m + g_o) = I \rightarrow R_{eq} = \frac{1}{(g_m + g_o)} \cong \frac{1}{g_m}$$

$$g_m = \sqrt{2 * \mu_n C_{ox} \left(\frac{W}{L}\right) * I_D} \rightarrow assume \left(\frac{W}{L}\right) = 6$$

$R_{eq} = 912.87\ \Omega$

BJT:

$$V * (g_m + g_\pi + g_o) = I \rightarrow R_{eq} = \frac{1}{(g_m + g_\pi + g_o)} \cong \frac{1}{g_m}$$

$$g_m = \frac{I_{CQ}}{V_t} = \frac{1\ mA}{26\ mV}$$

$R_{eq} = 26\ \Omega$

Problems 8 and 9

Code:

```
Ln#
 1
 2   module reg4b_en(en, clk, in, out);
 3     input en, clk;
 4     input [3:0] in;
 5     output [3:0] out;
 6     reg clk_gate;
 7
 8     always @(posedge clk) begin
 9       if(en)
10         clk_gate = clk;
11       else
12         clk_gate = 0;
13     end
14
15     DFF dff0(.D(in[0]), .Q(out[0]), .clk(clk_gate));
16     DFF dff1(.D(in[1]), .Q(out[1]), .clk(clk_gate));
17     DFF dff2(.D(in[2]), .Q(out[2]), .clk(clk_gate));
18     DFF dff3(.D(in[3]), .Q(out[3]), .clk(clk_gate));
19
20   endmodule
21
```

DFF:

```
Ln#
 1
 2   module DFF(D, Q, notQ, clk);
 3     input D, clk;
 4     output Q, notQ;
 5     reg Q, notQ;
 6
 7     always@(posedge clk) begin
 8         Q <= D;
 9         notQ <= ~D;
10     end
11
12   endmodule
```

Testbench:

```
Ln#
 1  `timescale 1ns/1ps
 2  module reg4_en_tb();
 3
 4    reg enable, clock;
 5    reg [3:0] in;
 6    wire [3:0] out;
 7
 8
 9    reg4b_en test(.en(enable), .clk(clock), .in(in), .out(out));
10
11    initial begin
12      clock = 0;
13      enable = 0;
14      in = 4'b1110;
15      #38
16      in = 4'b1100;
17      #38
18      in = 4'b1000;
19    end
20
21    always #10 clock = ~clock;
22    always #33 enable = ~enable;
23
24
25  endmodule
26
```

Output: