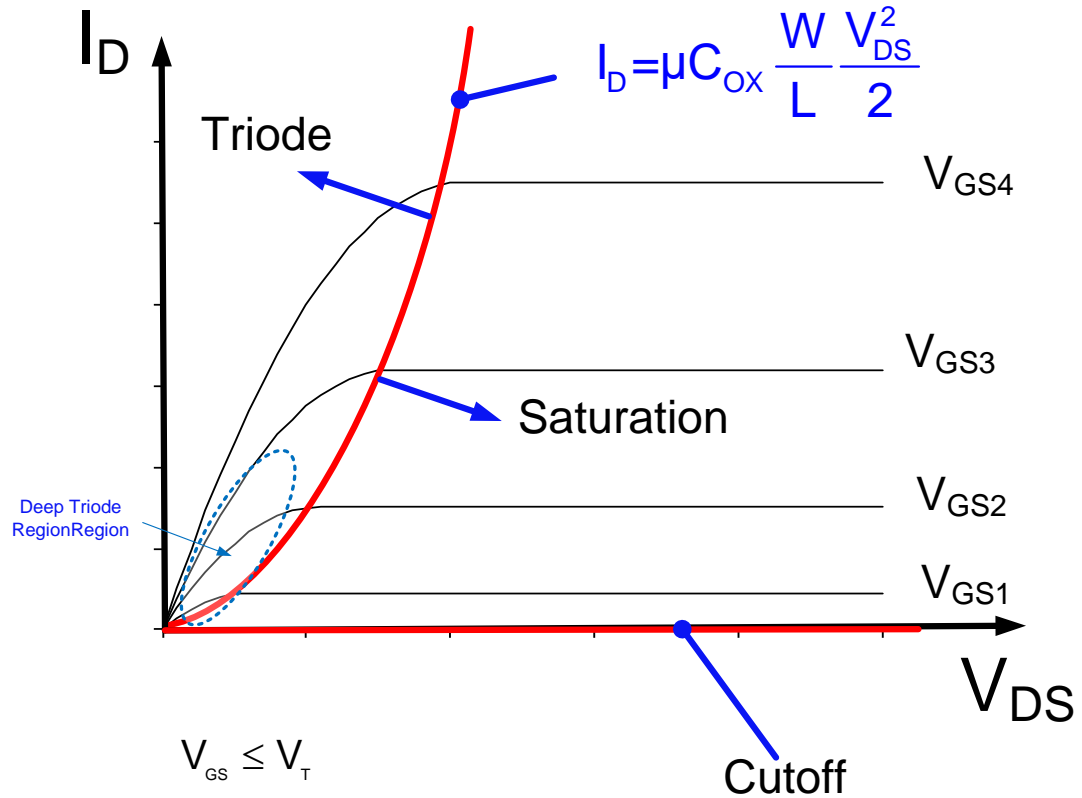
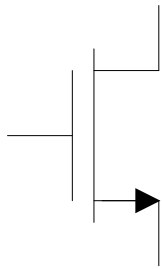


EE 330

Lecture 17

MOSFET Modeling
CMOS Process Flow

Graphical Representation of MOS Model



$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T \end{cases}$$

$$I_G = I_B = 0$$

$$V_{GS} \leq V_T$$

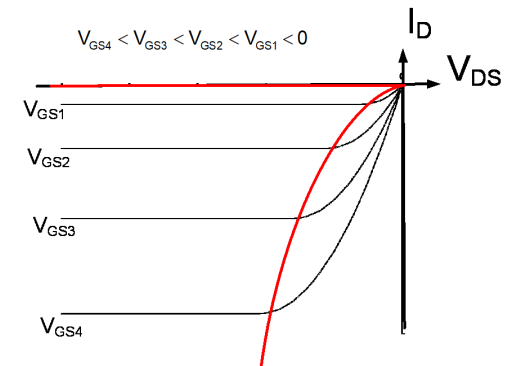
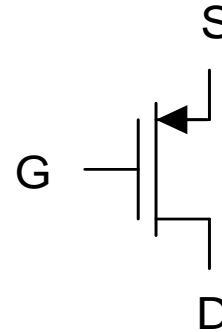
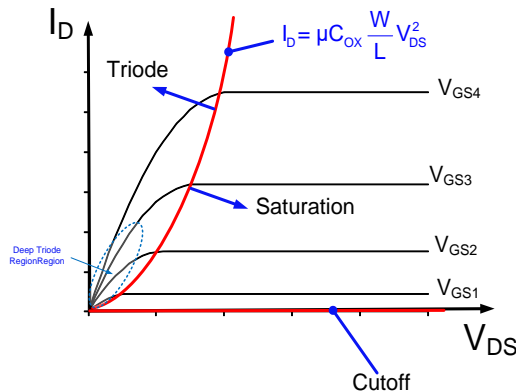
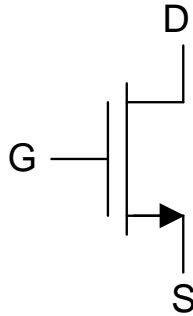
$$V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T$$

$$V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T$$

Parabola separated triode and saturation regions and corresponds to $V_{DS} = V_{GS} - V_T$

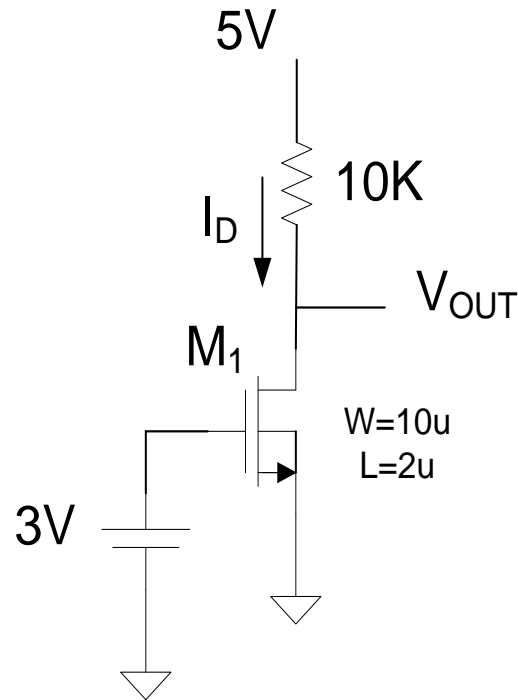
Review from Last Lecture

PMOS and NMOS Models



- Functional form identical, sign changes and parameter values different
- Will give details about p-channel model later

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu A V^{-2}$

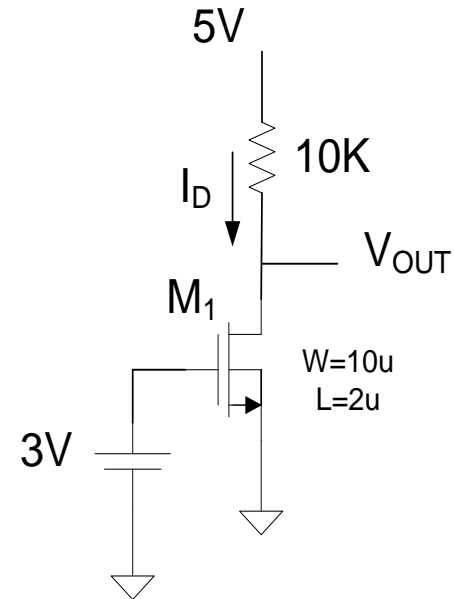


Solution:

Since $V_{GS} > V_T$, M_1 is operating in either saturation or triode region

Strategy will be to guess region of operation, solve, and then verify region

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu A V^{-2}$



Solution:

Guess M_1 in saturation

$$5V = I_D 10K + V_{OUT}$$

$$I_D = \frac{\mu C_{OX} W}{2L} (3 - V_T)^2$$

Required verification: $V_{DS} > V_{GS} - V_T$

Can eliminate I_D between these 2 equations to obtain V_{OUT}

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu AV^{-2}$

Guess M_1 in saturation

Required verification: $V_{DS} > V_{GS} - V_T$

$$\left. \begin{aligned} 5V &= I_D 10K + V_{OUT} \\ I_D &= \frac{\mu C_{OX} W}{2L} (3 - V_T)^2 \end{aligned} \right\}$$

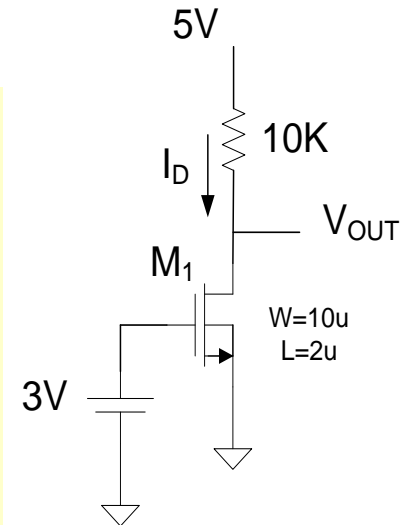
$$V_{OUT} = 5V - 10K \left[\frac{100\mu AV^{-2} 10\mu}{2 \cdot 2\mu} (2V)^2 \right]$$

$$V_{OUT} = 5V - 10K \left[\frac{100\mu AV^{-2} 10\mu}{2 \cdot 2\mu} (2V)^2 \right]$$

$$V_{OUT} = -5V$$

Verification: $V_{DS} = V_{OUT}$

$-5 >? 2V - 0$ No! So verification fails and Guess of region is invalid



Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu A/V^2$

Guess M_1 in triode

Required verification: $V_{DS} < V_{GS} - V_T$

$$5V = I_D 10K + V_{OUT}$$

$$I_D = \frac{\mu C_{OX} W}{L} \left(3 - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

$$V_{OUT} = 5V - 10K \left[\frac{100\mu A/V^2 \cdot 10\mu}{2\mu} \left(2V - \frac{V_{OUT}}{2} \right) V_{OUT} \right]$$

$$V_{OUT} = 5V - \left[5 \left(2V - \frac{V_{OUT}}{2} \right) V_{OUT} \right]$$

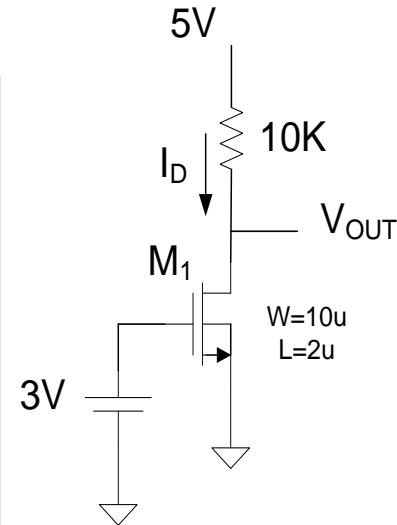
Solving for V_{OUT} , obtain

$$V_{OUT} = 0.515V$$

Verification: $V_{DS} = V_{OUT}$

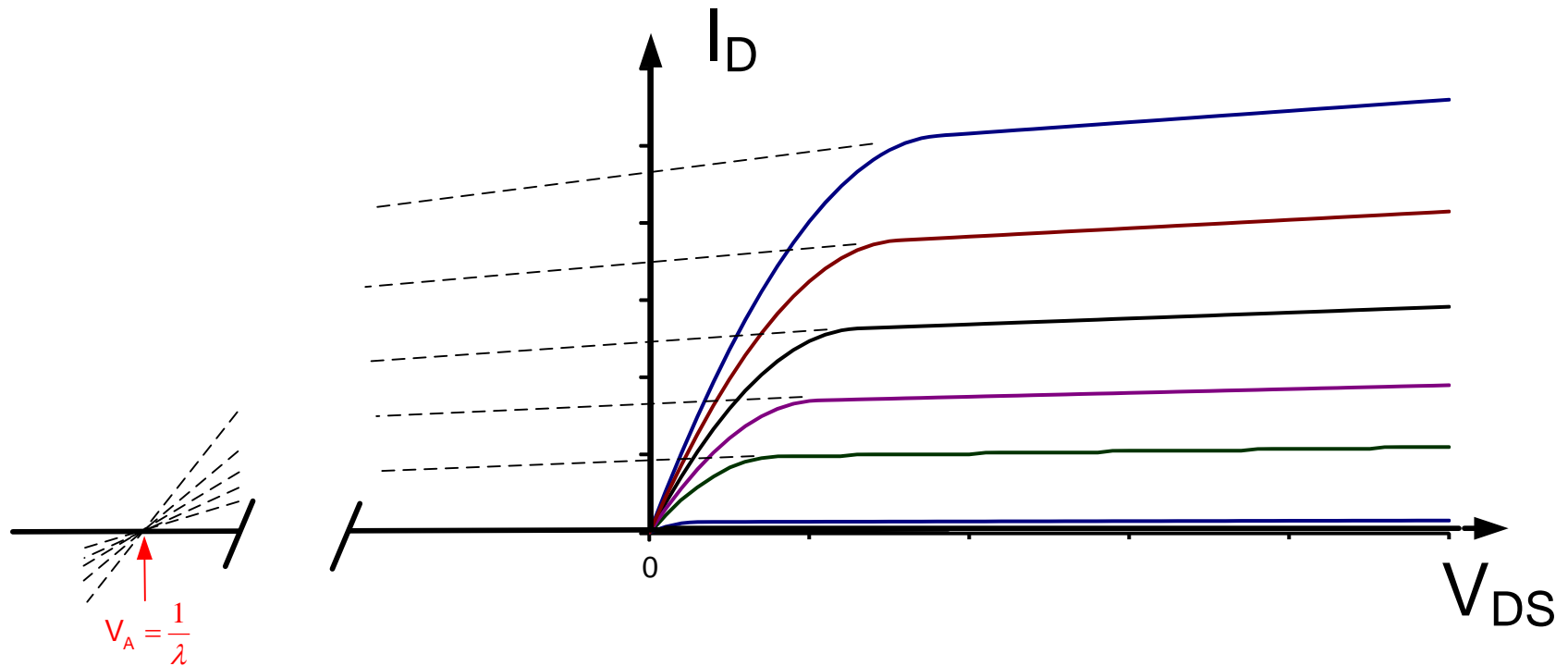
$0.515 < 2V$ Yes!

So verification succeeds and triode region is valid



$$V_{OUT} = 0.515V$$

Model Extensions

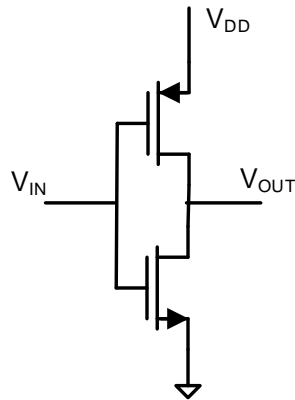


Projections intersect $-V_{DS}$ axis at same point, termed Early Voltage

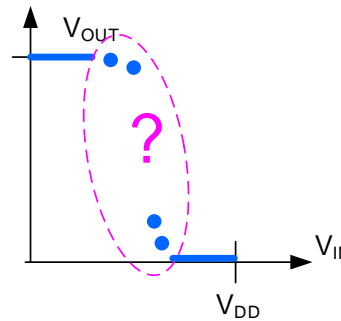
Typical values from -20V to -200V

Usually use parameter λ instead of V_A in MOS model

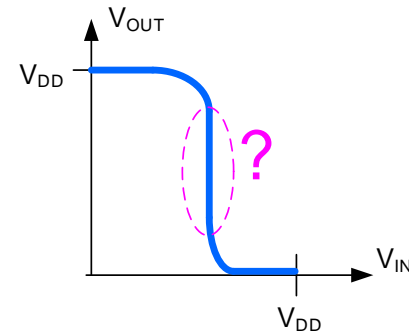
Limitations of Existing Models



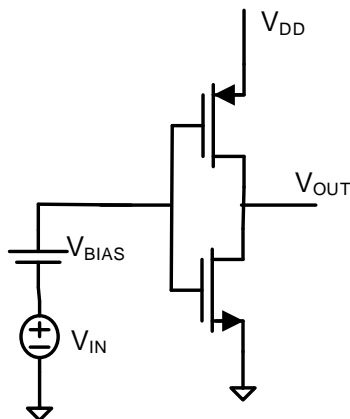
Logic Gate



Switch-Level Models



Simple square-law Model



Voltage Amplifier

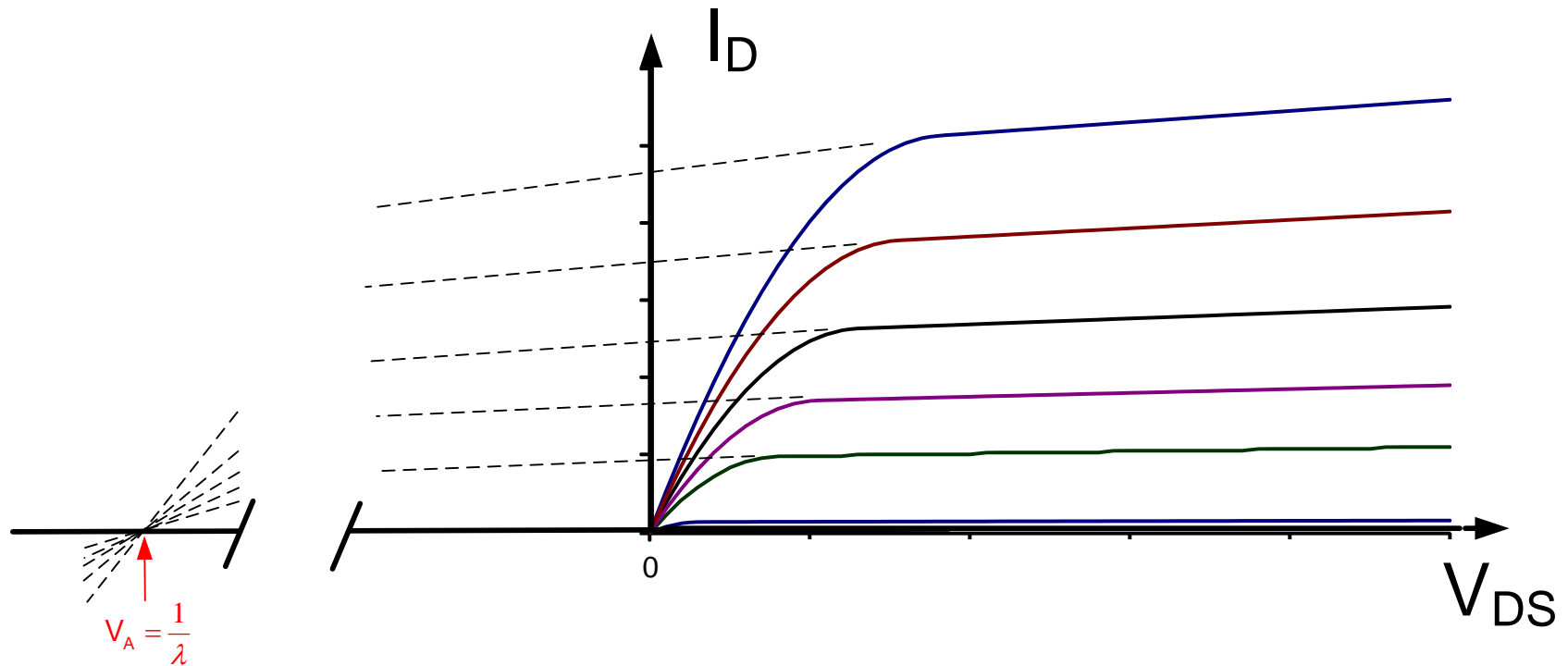
Switch-Level Models

Simple square-law Model



Voltage Gain
Input/Output Relationship ?

Model Extensions

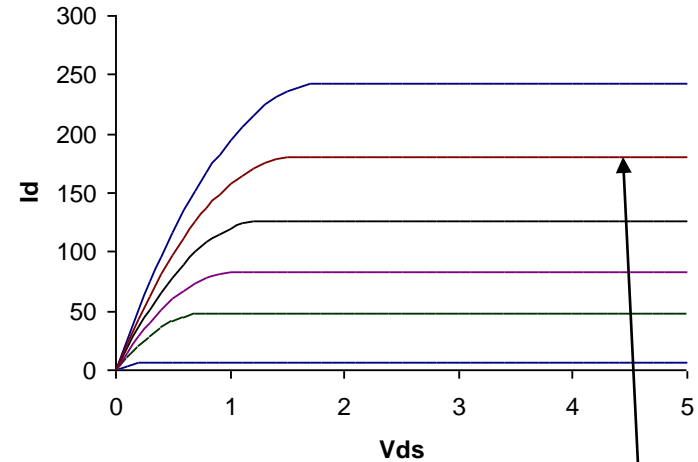


Projections intersect $-V_{DS}$ axis at same point, termed Early Voltage

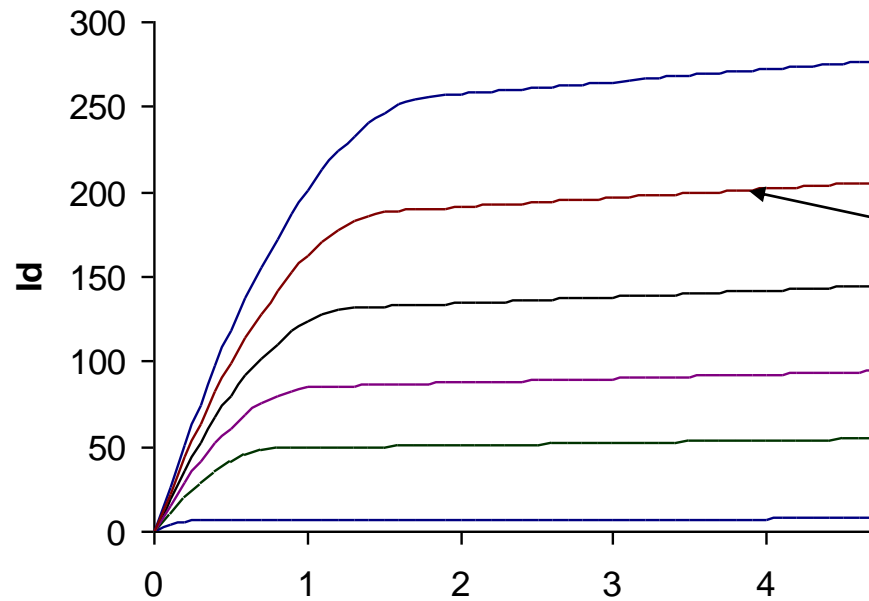
Typical values from -20V to -200V

Usually use parameter λ instead of V_A in MOS model

Model Extensions



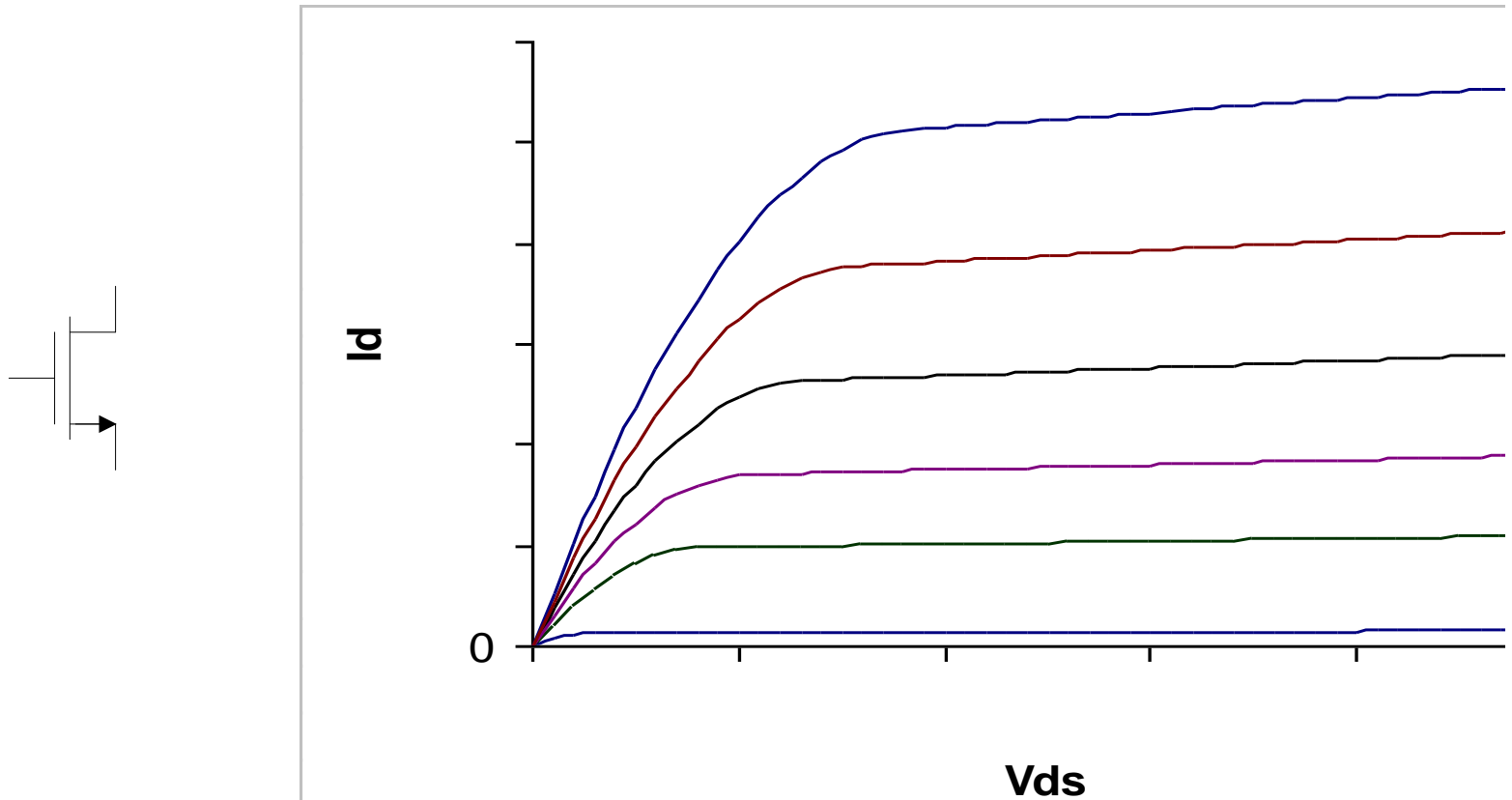
Existing Model



Actual Device

Slope is not 0

Model Extensions



$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

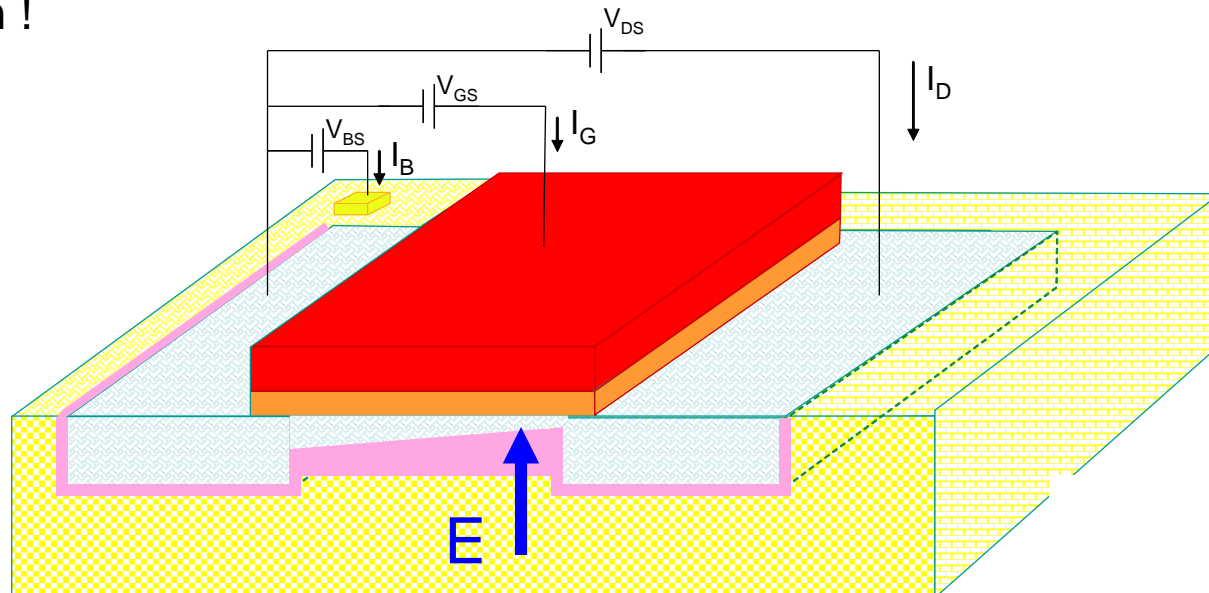
Note: This introduces small discontinuity (not shown) in model at SAT/Triode transition

Further Model Extensions

Existing model does not depend upon the bulk voltage !



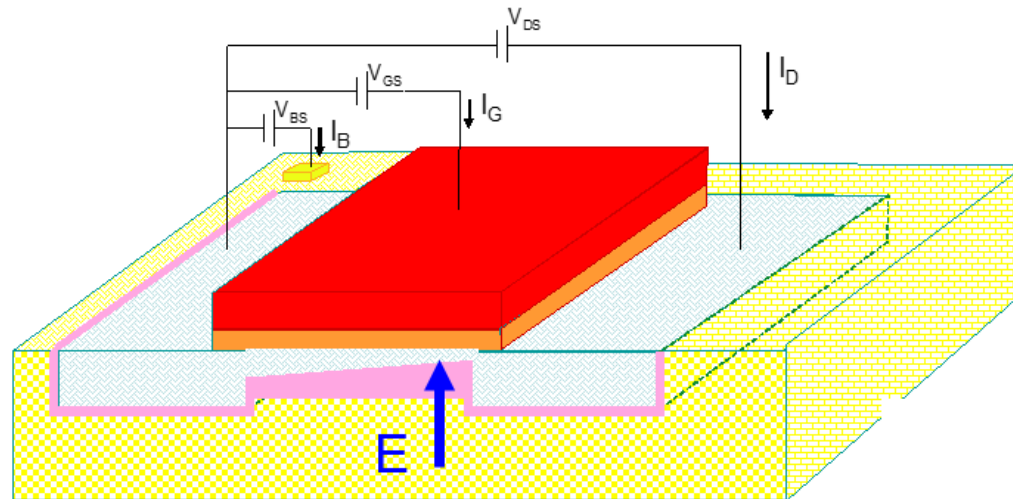
Observe that changing the bulk voltage will change the electric field in the channel region !



Further Model Extensions

Existing model does not depend upon the bulk voltage !

Observe that changing the bulk voltage will change the electric field in the channel region !



Changing the bulk voltage will change the thickness of the inversion layer

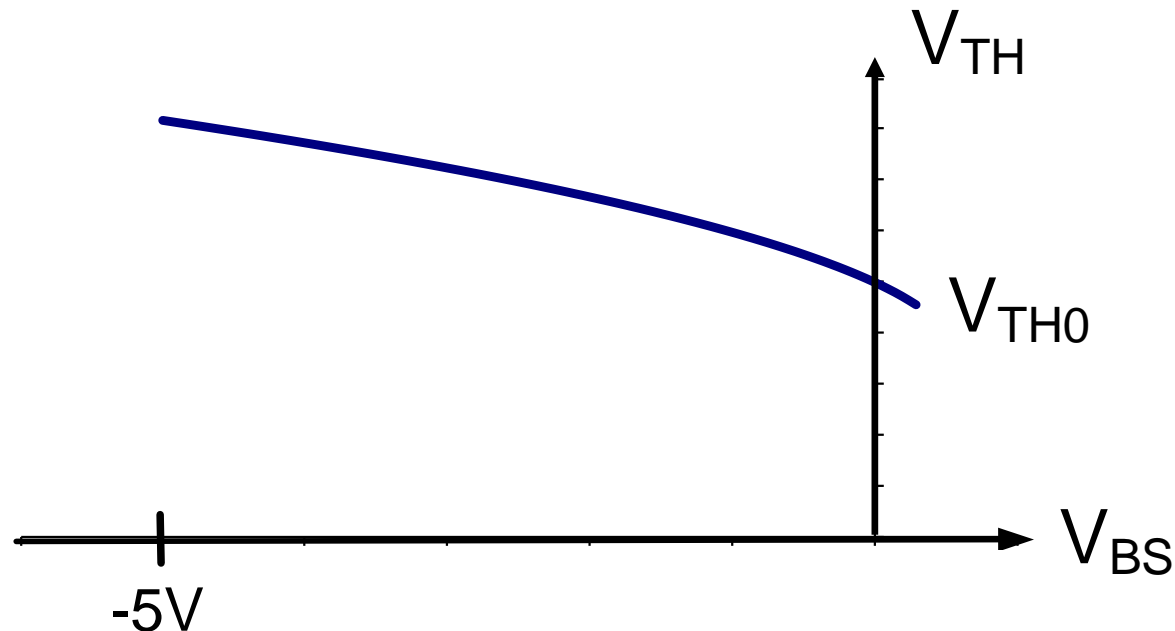
Changing the bulk voltage will change the threshold voltage of the device

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$$

Typical Bulk Effects on Threshold Voltage for n-channel Devices

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

$$\gamma \cong 0.4V^{1/2} \quad \phi \cong 0.6V$$

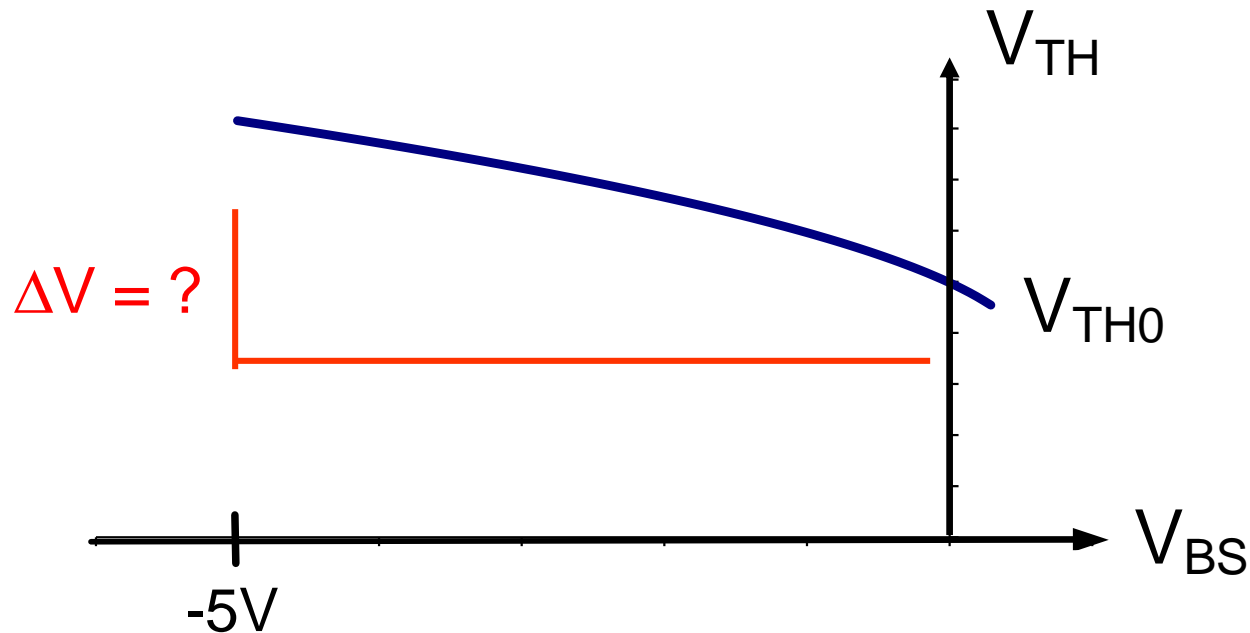


- Bulk-Diffusion Generally Reverse Biased ($V_{BS} < 0$ or at least $V_{BS} < 0.3V$) for n-channel
- Shift in threshold voltage with bulk voltage can be substantial
- Often $V_{BS} = 0$

Typical Bulk Effects on Threshold Voltage for n-channel Devices

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

$$\gamma \cong 0.4V^{1/2} \quad \phi \cong 0.6V$$



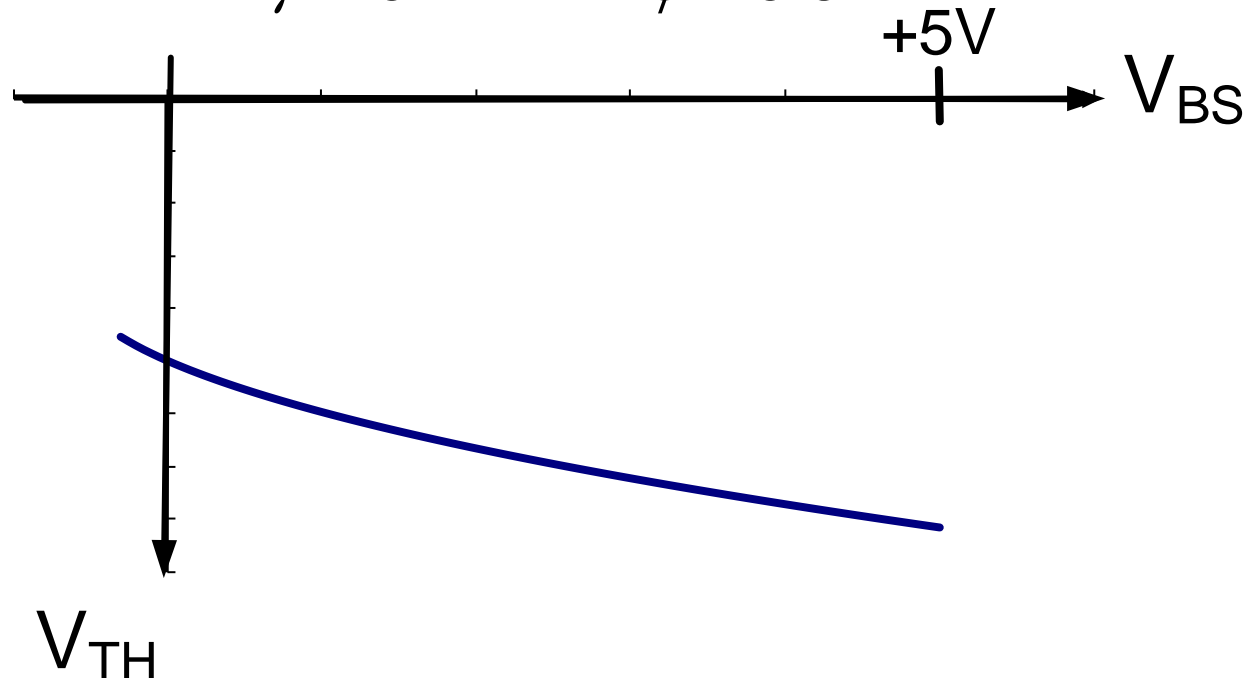
$$\Delta V = V_{TH} - V_{TH0} = \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

$$\Delta V \cong 0.4 \left(\sqrt{0.6V - (-5V)} - \sqrt{0.6} \right) \cong 0.64V$$

Typical Bulk Effects on Threshold Voltage for p-channel Devices

$$V_{TH} = V_{TH0} - \gamma \left(\sqrt{\phi + V_{BS}} - \sqrt{\phi} \right)$$

$$\gamma \cong 0.4V^{1/2} \quad \phi \cong 0.6V$$

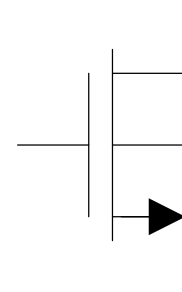


- Bulk-Diffusion Generally Reverse Biased ($V_{BS} > 0$ or at least $V_{BS} > -0.3V$) for p-channel
- Same functional form as for n-channel but $V_{TH0} < 0$
- Magnitude of threshold voltage increases with magnitude of reverse bias

Model Extension Summary

$$I_G = 0$$

$$I_B = 0$$

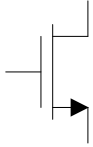


$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \bullet (1 + \lambda V_{DS}) & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

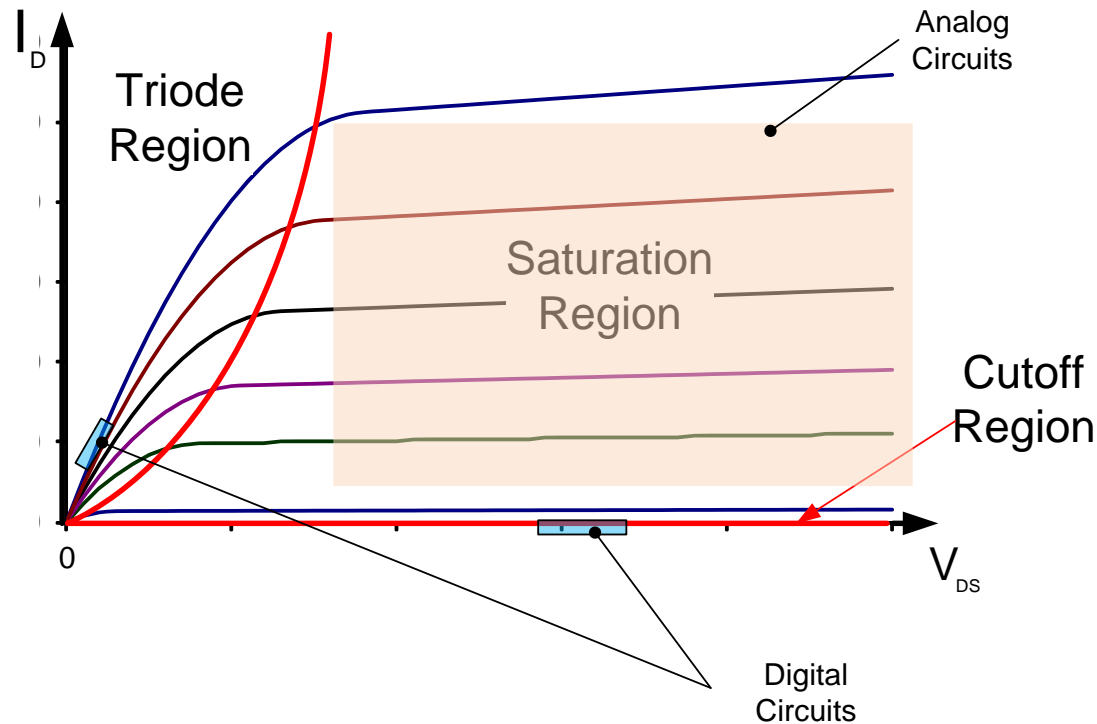
$$V_T = V_{T0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

Model Parameters : $\{\mu, C_{ox}, V_{T0}, \phi, \gamma, \lambda\}$

Design Parameters : $\{W, L\}$ but only one degree of freedom W/L



Operation Regions by Applications



Most analog circuits operate in the saturation region

(basic VVR operates in triode and is an exception)

Most digital circuits operate in triode and cutoff regions and switch between these two with Boolean inputs

Model Extension (short devices)

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

As the channel length becomes very short, velocity saturation will occur in the channel and this will occur with electric fields around $2V/u$. So, if a gate length is around $1u$, then voltages up to $2V$ can be applied without velocity saturation. But, if gate length decreases and voltages are kept high, velocity saturation will occur

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\frac{\alpha}{2}} V_{DS} & V_{GS} \geq V_T \quad V_{DS} < \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \\ \theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} & V_{GS} \geq V_T \quad V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \end{cases}$$

α is the velocity saturation index, $2 \geq \alpha \geq 1$

Model Extension (short devices)

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \frac{\theta_2}{\theta_1} \mu C_{OX} \frac{W}{L} (V_{GS} - V_T)^{\frac{\alpha}{2}} V_{DS} & V_{GS} \geq V_T \quad V_{DS} < \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \\ \theta_2 \mu C_{OX} \frac{W}{L} (V_{GS} - V_T)^\alpha & V_{GS} \geq V_T \quad V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \end{cases}$$

α is the velocity saturation index, $2 \geq \alpha \geq 1$

No longer a square-law model (some term it an α -power model)

For long devices, $\alpha=2$

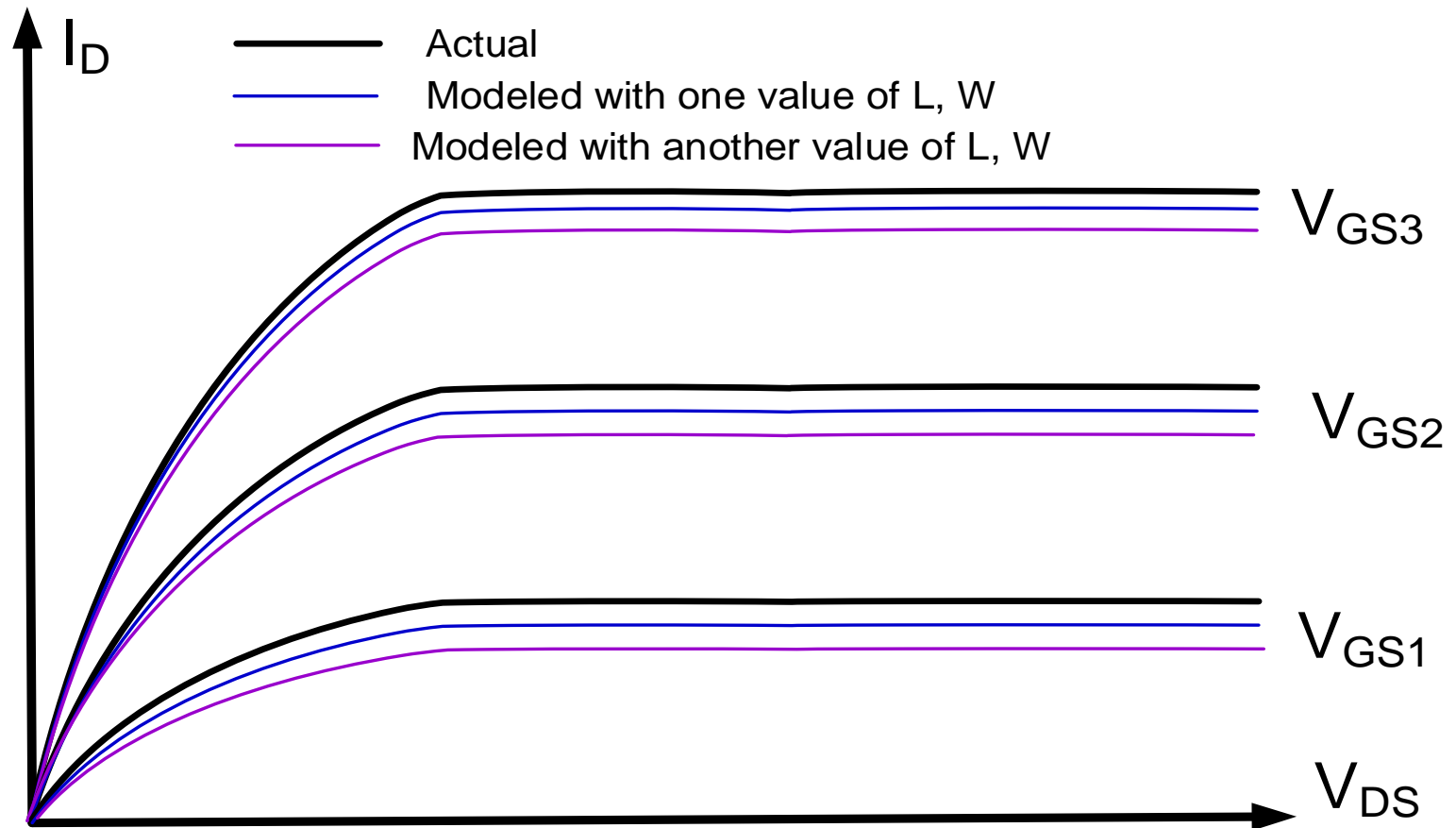
Channel length modulation (λ) and bulk effects can be added to the velocity Saturation as well

Degrading of α is not an attractive limitation of the MOSFET

Model Extension (BSIM model)

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 1.5E-7       NCH     = 1.7E17      TOX       = 1.42E-8
+K1      = 0.8976376    K2      = -0.09255    VTH0      = 0.629035
+K3B     = -8.2369696   W0      = 1.041146E-8   K3        = 24.0984767
+DVT0W   = 0           DVT1W   = 0           NLX       = 1E-9
+DVT0    = 2.7123969   DVT1    = 0.4232931   DVT2W     = 0
+U0      = 451.2322004 UA      = 3.091785E-13   DVT2      = -0.1403765
+UC      = 1.22401E-11 VSAT   = 1.715884E5    UB        = 1.702517E-18
+AGS     = 0.130484    B0     = 2.446405E-6   A0        = 0.6580918
+KETA    = -3.043349E-3 A1     = 8.18159E-7    B1        = 5E-6
+RDSW    = 1.367055E3  PRWG   = 0.0328586    A2        = 0.3363058
+WR      = 1          WINT    = 2.443677E-7   PRWB      = 0.0104806
+XL      = 1E-7       XW      = 0          LINT      = 6.999776E-8
+DWB     = 3.676235E-8 VOFF   = -1.493503E-4  DWG       = -1.256454E-8
+CIT      = 0         CDSC    = 2.4E-4       NFACTOR   = 1.0354201
+CDSCB   = 0         ETA0    = 2.342963E-3   CDSCD     = 0
+DSUB    = 0.0764123 PCLM   = 2.5941582    ETAB      = -1.5324E-4
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505  PDIBLC1   = 0.8187825
+PSCBE1  = 6.611774E8 PSCBE2 = 3.238266E-4  DROUT     = 0.9919348
                                PVAG     = 0
+PRT      = 0         UTE     = -1.5          KT1       = -0.11
+KT1L    = 0         KT2     = 0.022        UA1       = 4.31E-9
+UB1     = -7.61E-18 UC1     = -5.6E-11    AT        = 3.3E4
+WL      = 0         WLN     = 1          WW       = 0
+WWN     = 1         WWL     = 0          LL       = 0
+LLN     = 1         LW      = 0          LWN      = 1
+LWL     = 0         CAPMOD  = 2          XPART    = 0.5
+CGDO    = 2.32E-10  CGSO    = 2.32E-10   CGBO      = 1E-9
+CJ      = 4.282017E-4 PB      = 0.9317787   MJ        = 0.4495867
+CJSW    = 3.034055E-10 PBSW   = 0.8         MJSW     = 0.1713852
+CJSWG   = 1.64E-10  PBSWG  = 0.8         MJSWG    = 0.1713852
+CF      = 0         PVTH0   = 0.0520855   PRDSW     = 112.8875816
+PK2     = -0.0289036 WKETA   = -0.0237483   LKETA     = 1.728324E-3
*)
*
```

Model Errors with Different W/L Values



Binning models can improve model accuracy

BSIM Binning Model

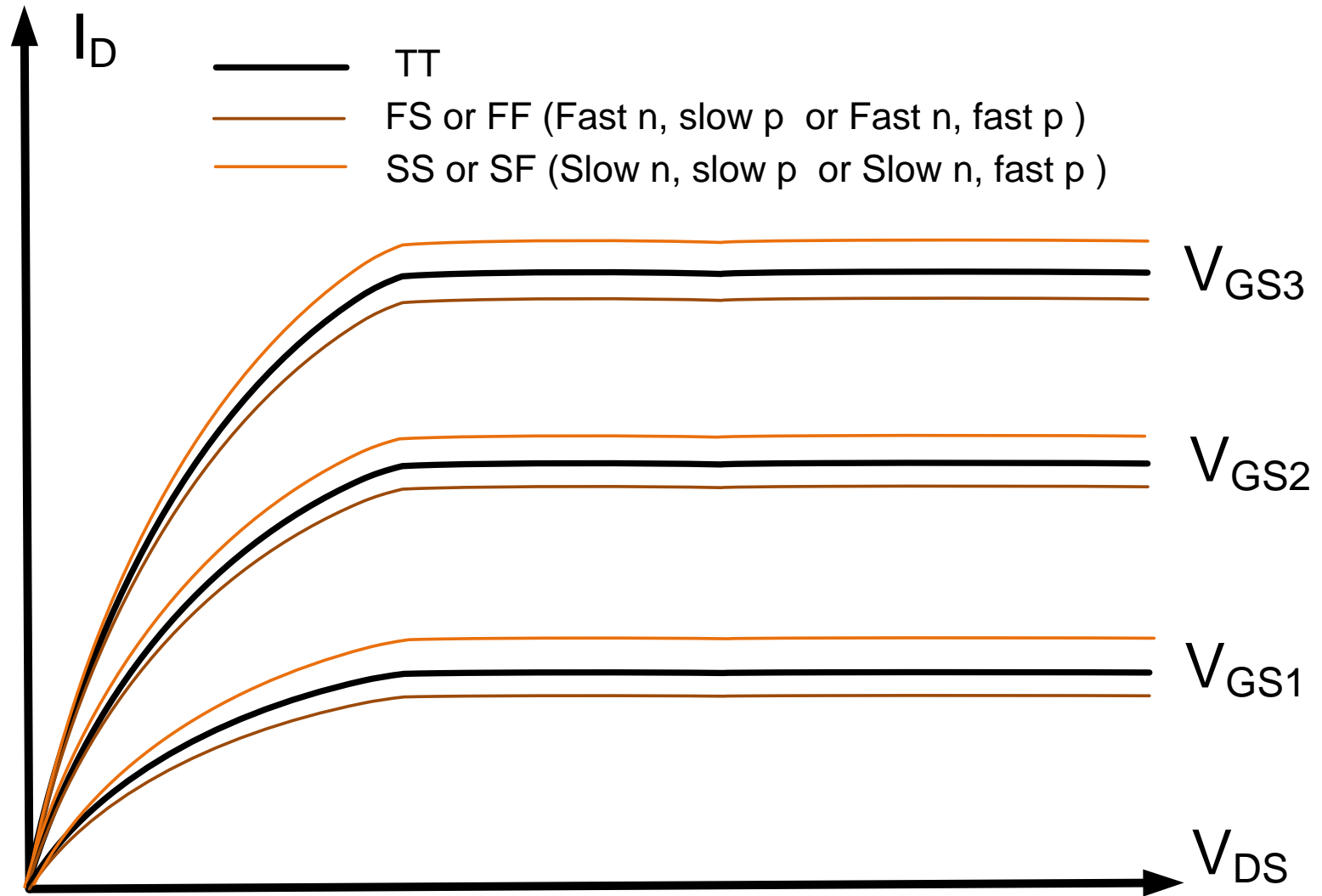
- Bin on device sizes
- multiple BSIM models !

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 1.5E-7       NCH     = 1.7E17      TOX      = 1.42E-8
+K1      = 0.8976376    K2      = -0.09255    VTH0     = 0.629035
+K3B     = -8.2369696   W0      = 1.041146E-8  K3       = 24.0984767
+DVT0W   = 0           DVT1W   = 0          NLX      = 1E-9
+DVT0    = 2.7123969   DVT1    = 0.4232931    DVT2W    = 0
+U0      = 451.2322004  UA      = 3.091785E-13    DVT2     = -0.1403765
+UC      = 1.22401E-11  VSAT   = 1.715884E5    UB       = 1.702517E-18
+AGS     = 0.130484    B0      = 2.446405E-6    A0       = 0.6580918
+KETA    = -3.043349E-3 A1      = 8.18159E-7    B1       = 5E-6
+RDSW    = 1.367055E3  PRWG    = 0.0328586    A2       = 0.3363058
+WR       = 1          WINT    = 2.443677E-7    PRWB     = 0.0104806
+XL       = 1E-7       XW      = 0          LINT     = 6.999776E-8
+DWB     = 3.676235E-8 VOFF    = -1.493503E-4  DWG      = -1.256454E-8
+CIT      = 0          CDSC    = 2.4E-4      NFACTOR  = 1.0354201
+CDSCB   = 0          ETA0    = 2.342963E-3    CDSCD    = 0
+DSUB    = 0.0764123  PCLM    = 2.5941582    ETAB     = -1.5324E-4
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505    PDIBLC1  = 0.8187825
+PSCBE1  = 6.611774E8 PSCBE2  = 3.238266E-4    DROUT    = 0.9919348
                                PVAG    = 0
+PRT      = 0          UTE     = -1.5          KT1      = -0.11
+KT1L    = 0          KT2     = 0.022        UA1      = 4.31E-9
+UB1     = -7.61E-18  UC1     = -5.6E-11    AT       = 3.3E4
+WL       = 0          WLN     = 1          WW      = 0
+WWN     = 1          WWL     = 0          LL      = 0
+LLN     = 1          LW      = 0          LWN     = 1
+LWL     = 0          CAPMOD  = 2        XPART    = 0.5
+CGDO    = 2.32E-10   CGSO    = 2.32E-10    CGBO     = 1E-9
+CJ      = 4.282017E-4 PB      = 0.9317787    MJ       = 0.4495867
+CJSW    = 3.034055E-10 PBSW   = 0.8          MJSW     = 0.1713852
+CJSWG   = 1.64E-10  PBSWG  = 0.8          MJSWG    = 0.1713852
+CF       = 0          PVTH0   = 0.0520855    PRDSW    = 112.8875816
+PK2     = -0.0289036 WKETA   = -0.0237483    LKETA    = 1.728324E-3
*)
*
```

With 32 bins, this model has 3040 model parameters !

Model Changes with Process Variations

(n-ch characteristics shown)



Corner models can improve model accuracy

BSIM Corner Models with Binning

- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS

- bin on device sizes

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          TOX      = 1.42E-8
+XJ      = 1.5E-7       NCH     = 1.7E17      VTH0     = 0.629035
+K1      = 0.8976376    K2      = -0.09255    K3       = 24.0984767
+K3B     = -8.2369696   W0      = 1.041146E-8  NLX      = 1E-9
+DVT0W   = 0           DVT1W   = 0           DVT2W    = 0
+DVT0    = 2.7123969   DVT1    = 0.4232931    DVT2     = -0.1403765
+U0      = 451.2322004  UA      = 3.091785E-13    UB       = 1.702517E-18
+UC      = 1.22401E-11  VSAT   = 1.715884E5    A0       = 0.6580918
+AGS     = 0.130484    B0      = 2.446405E-6    B1       = 5E-6
+KETA    = -3.043349E-3 A1      = 8.18159E-7    A2       = 0.3363058
+RDSW    = 1.367055E3  PRWG   = 0.0328586    PRWB     = 0.0104806
+WR      = 1           WINT    = 2.443677E-7    LINT     = 6.999776E-8
+XL      = 1E-7        XW      = 0           DWG      = -1.256454E-8
+DWB     = 3.676235E-8  VOFF   = -1.493503E-4  NFACTOR  = 1.0354201
+CIT      = 0          CDSC    = 2.4E-4        CDSCD    = 0
+CDSCB   = 0          ETA0    = 2.342963E-3    ETAB     = -1.5324E-4
+DSUB    = 0.0764123  PCLM   = 2.5941582    PDIBLC1  = 0.8187825
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505    DROUT    = 0.9919348
+PSCBE1  = 6.611774E8  PSCBE2 = 3.238266E-4    PVAG     = 0
+DPR1TA  = 0.01       RSH     = 83.5        MORMOD   = 1
+PRT      = 0          UTE     = -1.5          KT1      = -0.11
+KT1L    = 0          KT2     = 0.022         UA1      = 4.31E-9
+UB1     = -7.61E-18  UC1     = -5.6E-11    AT       = 3.3E4
+WL      = 0          WLN     = 1           WW      = 0
+WWN     = 1          WWL     = 0           LL      = 0
+LLN     = 1          LW      = 0           LWN     = 1
+LWL     = 0          CAPMOD  = 2           XPART    = 0.5
+CGDO    = 2.32E-10   CGSO    = 2.32E-10    CGBO     = 1E-9
+CJ      = 4.282017E-4 PB      = 0.9317787    MJ       = 0.4495867
+CJSW    = 3.034055E-10 PBSW   = 0.8          MJSW     = 0.1713852
+CJSWG   = 1.64E-10  PBSWG  = 0.8          MJSWG    = 0.1713852
+CF      = 0          PVTH0   = 0.0520855    PRDSW    = 112.8875816
+PK2     = -0.0289036 WKETA   = -0.0237483    LKETA     = 1.728324E-3
*)
*
```

With 32 size bins and 4 corners, this model has 15,200 model parameters !

How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model

Square-law model (with λ and bulk additions)

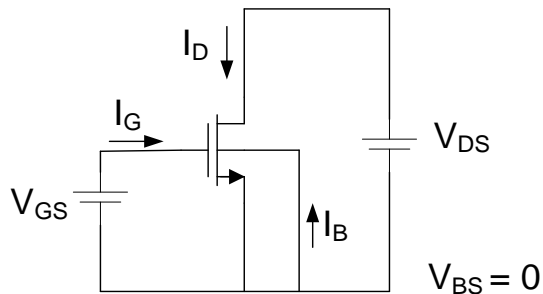
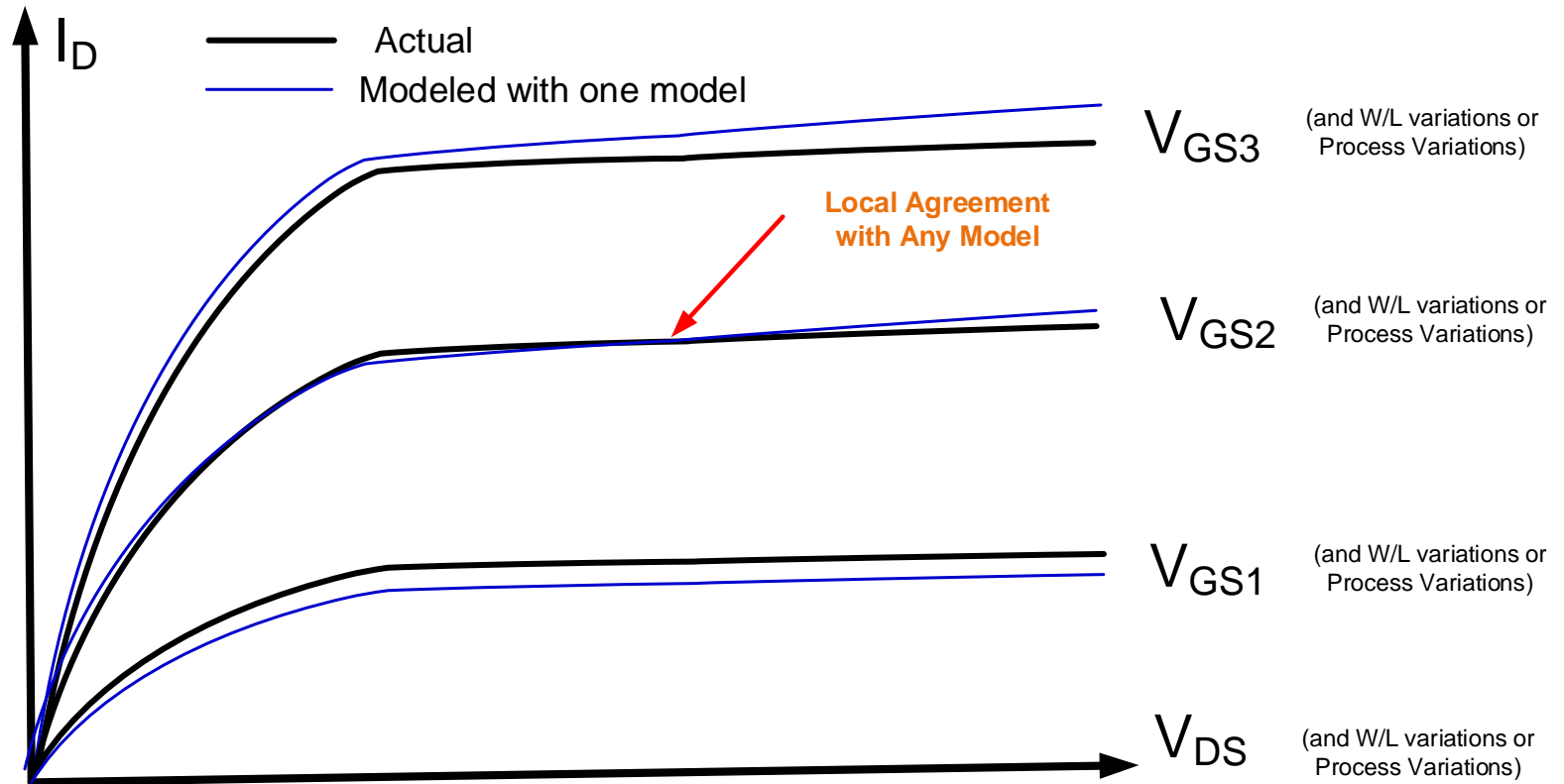
α -law model (with λ and bulk additions)

BSIM model

BSIM model (with binning extensions)

BSIM model (with binning extensions and process corners)

The Modeling Challenge



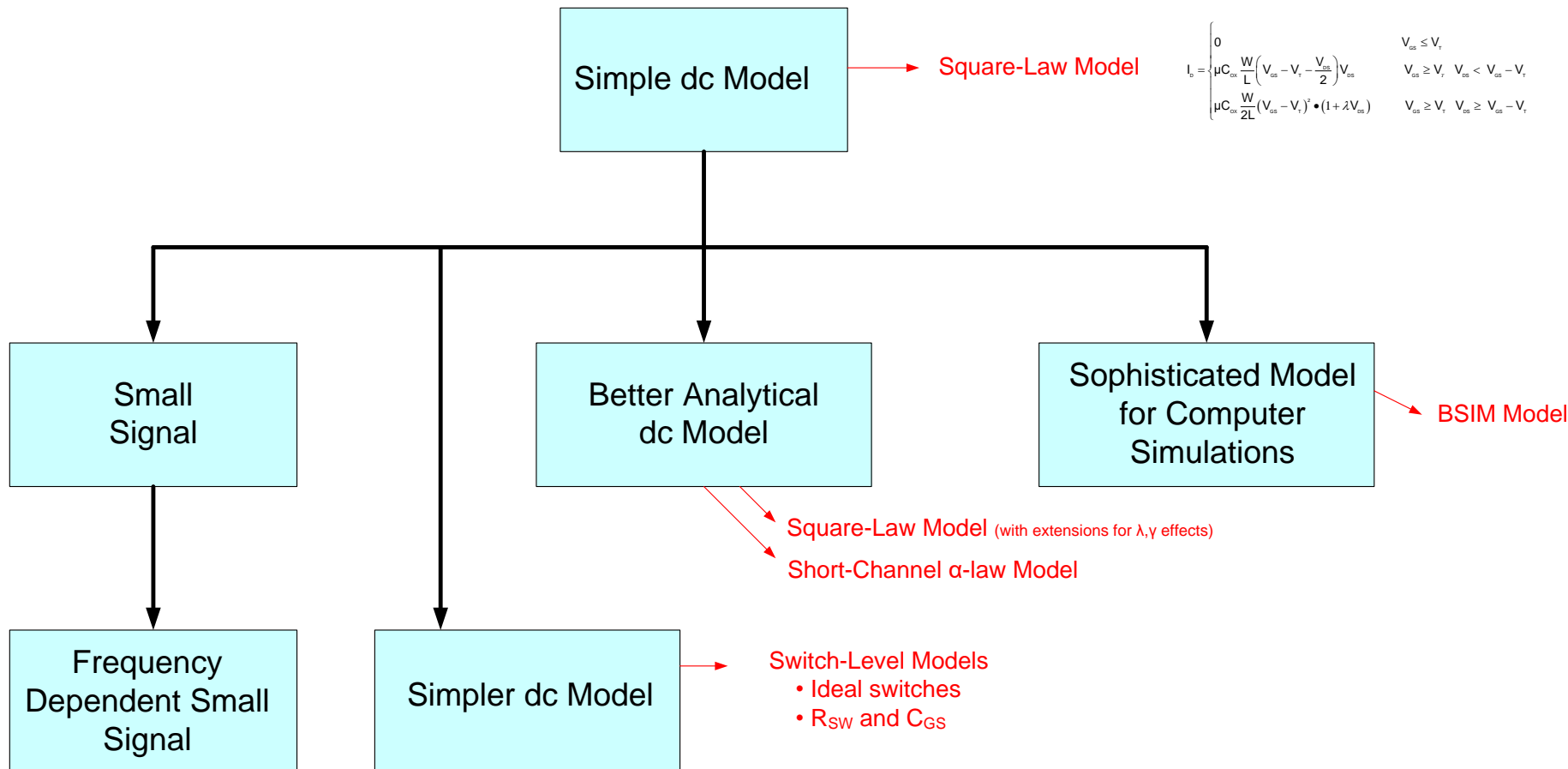
$$I_D = f_1(V_{GS}, V_{DS})$$

$$I_G = f_2(V_{GS}, V_{DS})$$

$$I_B = f_3(V_{GS}, V_{DS})$$

Difficult to obtain analytical functions that accurately fit actual devices over bias, size, and process variations

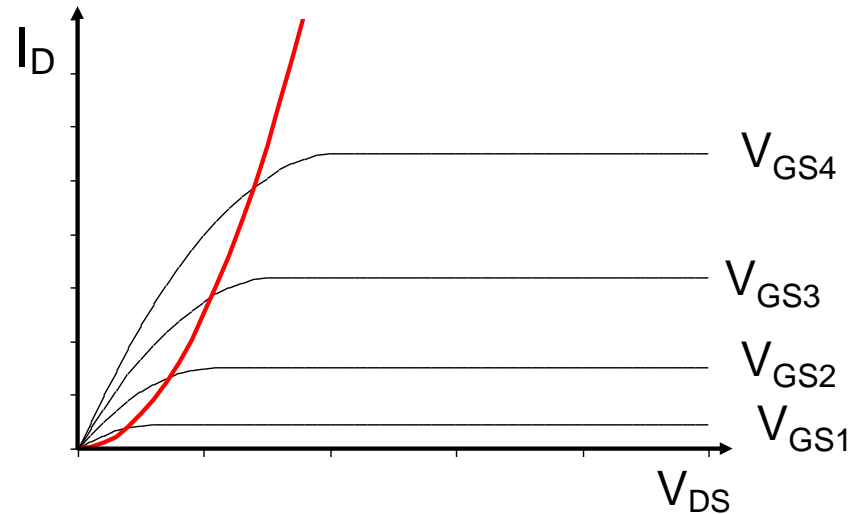
Model Status



In the next few slides, the models we have developed will be listed and reviewed

- Square-law Model
- Switch-level Models
- Extended Square-law model
- Short-channel model
- BSIM Model
- BSIM Binning Model
- Corner Models

Square-Law Model



$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T \end{cases}$$

$$V_{GS} \leq V_T$$

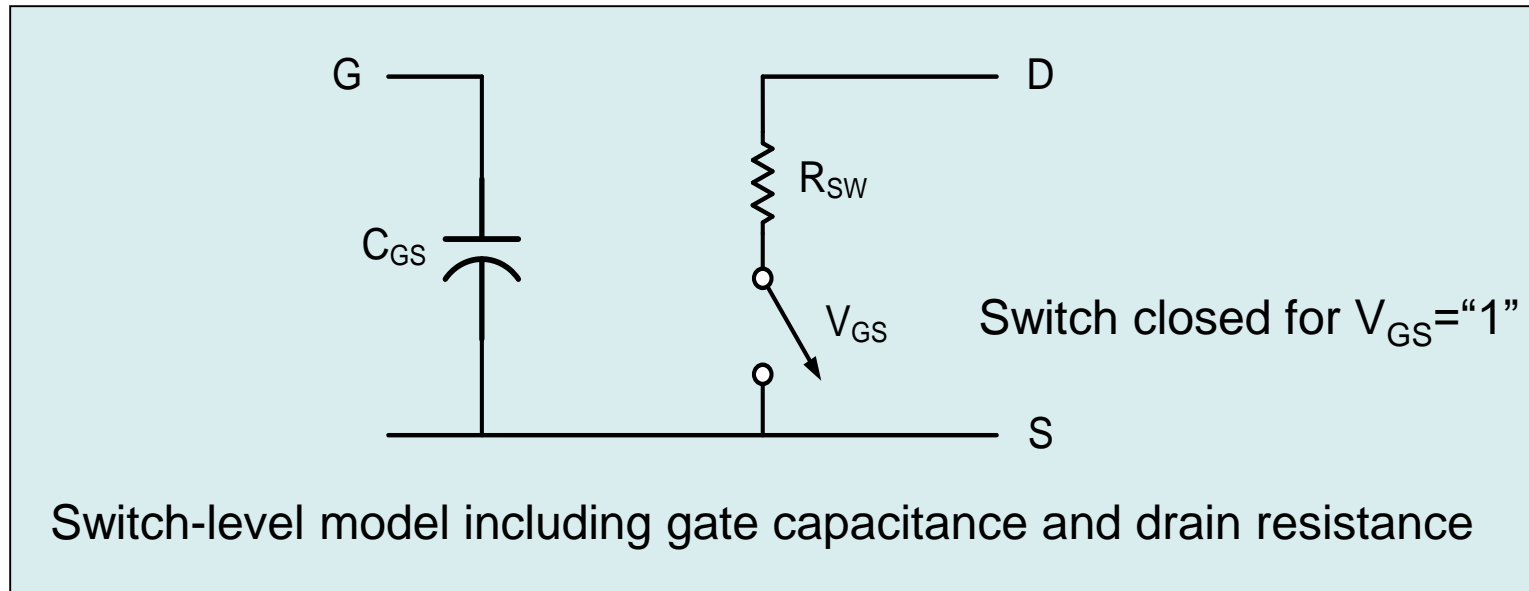
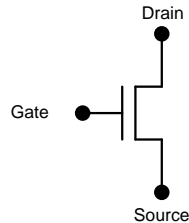
$$V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T$$

$$V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T$$

Model Parameters : $\{\mu, C_{ox}, V_{T0}\}$

Design Parameters : $\{W, L\}$ but only one degree of freedom W/L

Switch-Level Models



C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

$$C_{GS} \cong 1.5\text{fF} \quad R_{sw} \cong \left. \begin{array}{l} 2\text{K}\Omega \text{ n-channel} \\ 6\text{K}\Omega \text{ p-channel} \end{array} \right\}$$

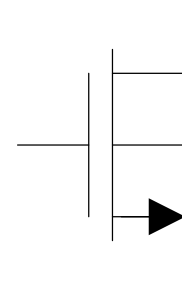
Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Model Parameters : $\{C_{GS}, R_{SW}\}$

Extended Square-Law Model

$$I_G = 0$$

$$I_B = 0$$



$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \bullet (1 + \lambda V_{DS}) & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

$$V_T = V_{T0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

Model Parameters : $\{\mu, C_{ox}, V_{T0}, \phi, \gamma, \lambda\}$

Design Parameters : $\{W, L\}$ but only one degree of freedom W/L

Short-Channel Model

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\frac{\alpha}{2}} V_{DS} & V_{GS} \geq V_T \quad V_{DS} < \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \\ \theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha & V_{GS} \geq V_T \quad V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \end{cases}$$

α is the velocity saturation index, $2 \geq \alpha \geq 1$

Channel length modulation (λ) and bulk effects can be added to the velocity Saturation as well

BSIM model

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 1.5E-7       NCH     = 1.7E17      TOX      = 1.42E-8
+K1      = 0.8976376    K2      = -0.09255     VTH0     = 0.629035
+K3B     = -8.2369696   W0      = 1.041146E-8    K3       = 24.0984767
+DVT0W   = 0           DVT1W   = 0           NLX      = 1E-9
+DVT0    = 2.7123969    DVT1    = 0.4232931    DVT2W    = 0
+U0      = 451.2322004  UA      = 3.091785E-13   DVT2     = -0.1403765
+UC      = 1.22401E-11  VSAT   = 1.715884E5    UB       = 1.702517E-18
+AGS     = 0.130484    B0      = 2.446405E-6    A0       = 0.6580918
+KETA    = -3.043349E-3 A1      = 8.18159E-7    B1       = 5E-6
+RDSW    = 1.367055E3  PRWG   = 0.0328586    A2       = 0.3363058
+WR      = 1           WINT    = 2.443677E-7    PRWB     = 0.0104806
+XL      = 1E-7       XW      = 0           LINT     = 6.999776E-8
+DWB     = 3.676235E-8 VOFF   = -1.493503E-4   DWG      = -1.256454E-8
+CIT      = 0          CDSC    = 2.4E-4       NFACTOR  = 1.0354201
+CDSCB   = 0          ETA0    = 2.342963E-3    CDSCD    = 0
+DSUB    = 0.0764123  PCLM   = 2.5941582    ETAB     = -1.5324E-4
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505   PDIBLC1  = 0.8187825
+PSCBE1  = 6.611774E8 PSCBE2  = 3.238266E-4  DROUT    = 0.9919348
                                     PVAG     = 0

+PRT      = 0          UTE     = -1.5          KT1      = -0.11
+KT1L    = 0          KT2     = 0.022        UA1      = 4.31E-9
+UB1     = -7.61E-18  UC1     = -5.6E-11    AT       = 3.3E4
+WL      = 0          WLN     = 1           WW      = 0
+WWN     = 1          WWL     = 0           LL      = 0
+LLN     = 1          LW      = 0           LWN     = 1
+LWL     = 0          CAPMOD  = 2           XPART    = 0.5
+CGDO    = 2.32E-10   CGSO    = 2.32E-10    CGBO     = 1E-9
+CJ      = 4.282017E-4 PB      = 0.9317787    MJ       = 0.4495867
+CJSW    = 3.034055E-10 PBSW   = 0.8          MJSW     = 0.1713852
+CJSWG   = 1.64E-10  PBSWG  = 0.8          MJSWG    = 0.1713852
+CF      = 0          PVTH0   = 0.0520855    PRDSW    = 112.8875816
+PK2     = -0.0289036 WKETA   = -0.0237483    LKETA    = 1.728324E-3
*)
*
```

Note this model has 95 model parameters !

BSIM Binning Model

- Bin on device sizes
- multiple BSIM models !

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 1.5E-7       NCH     = 1.7E17      TOX      = 1.42E-8
+K1      = 0.8976376    K2      = -0.09255     VTH0     = 0.629035
+K3B     = -8.2369696   W0      = 1.041146E-8   K3       = 24.0984767
+DVT0W   = 0           DVT1W   = 0           NLX      = 1E-9
+DVT0    = 2.7123969   DVT1    = 0.4232931     DVT2W    = 0
+U0      = 451.2322004  UA      = 3.091785E-13    DVT2     = -0.1403765
+UC      = 1.22401E-11  VSAT   = 1.715884E5    UB       = 1.702517E-18
+AGS     = 0.130484    B0      = 2.446405E-6    A0       = 0.6580918
+KETA    = -3.043349E-3 A1      = 8.18159E-7    B1       = 5E-6
+RDSW    = 1.367055E3  PRWG   = 0.0328586    A2       = 0.3363058
+WR       = 1          WINT    = 2.443677E-7   PRWB     = 0.0104806
+XL       = 1E-7       XW      = 0           LINT     = 6.999776E-8
+DWB     = 3.676235E-8 VOFF   = -1.493503E-4  DWG      = -1.256454E-8
+CIT      = 0          CDSC    = 2.4E-4       NFACTOR  = 1.0354201
+CDSCB   = 0          ETA0    = 2.342963E-3    CDSCD    = 0
+DSUB    = 0.0764123  PCLM   = 2.5941582    ETAB     = -1.5324E-4
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505   PDIBLC1  = 0.8187825
+PSCBE1  = 6.611774E8 PSCBE2 = 3.238266E-4  DROUT    = 0.9919348
                                PVAG    = 0
+PRT      = 0          UTE     = -1.5          KT1      = -0.11
+KT1L    = 0          KT2     = 0.022        UA1      = 4.31E-9
+UB1     = -7.61E-18  UC1     = -5.6E-11    AT       = 3.3E4
+WL       = 0          WLN     = 1          WW      = 0
+WWN     = 1          WWL     = 0          LL      = 0
+LLN     = 1          LW      = 0          LWN     = 1
+LWL     = 0          CAPMOD  = 2          XPART    = 0.5
+CGDO    = 2.32E-10   CGSO    = 2.32E-10    CGBO     = 1E-9
+CJ      = 4.282017E-4 PB      = 0.9317787    MJ       = 0.4495867
+CJSW    = 3.034055E-10 PBSW   = 0.8          MJSW     = 0.1713852
+CJSWG   = 1.64E-10  PBSWG  = 0.8          MJSWG    = 0.1713852
+CF       = 0          PVTH0   = 0.0520855    PRDSW    = 112.8875816
+PK2     = -0.0289036 WKETA   = -0.0237483    LKETA    = 1.728324E-3
*)
*
```

With 32 bins, this model has 3040 model parameters !

BSIM Corner Models

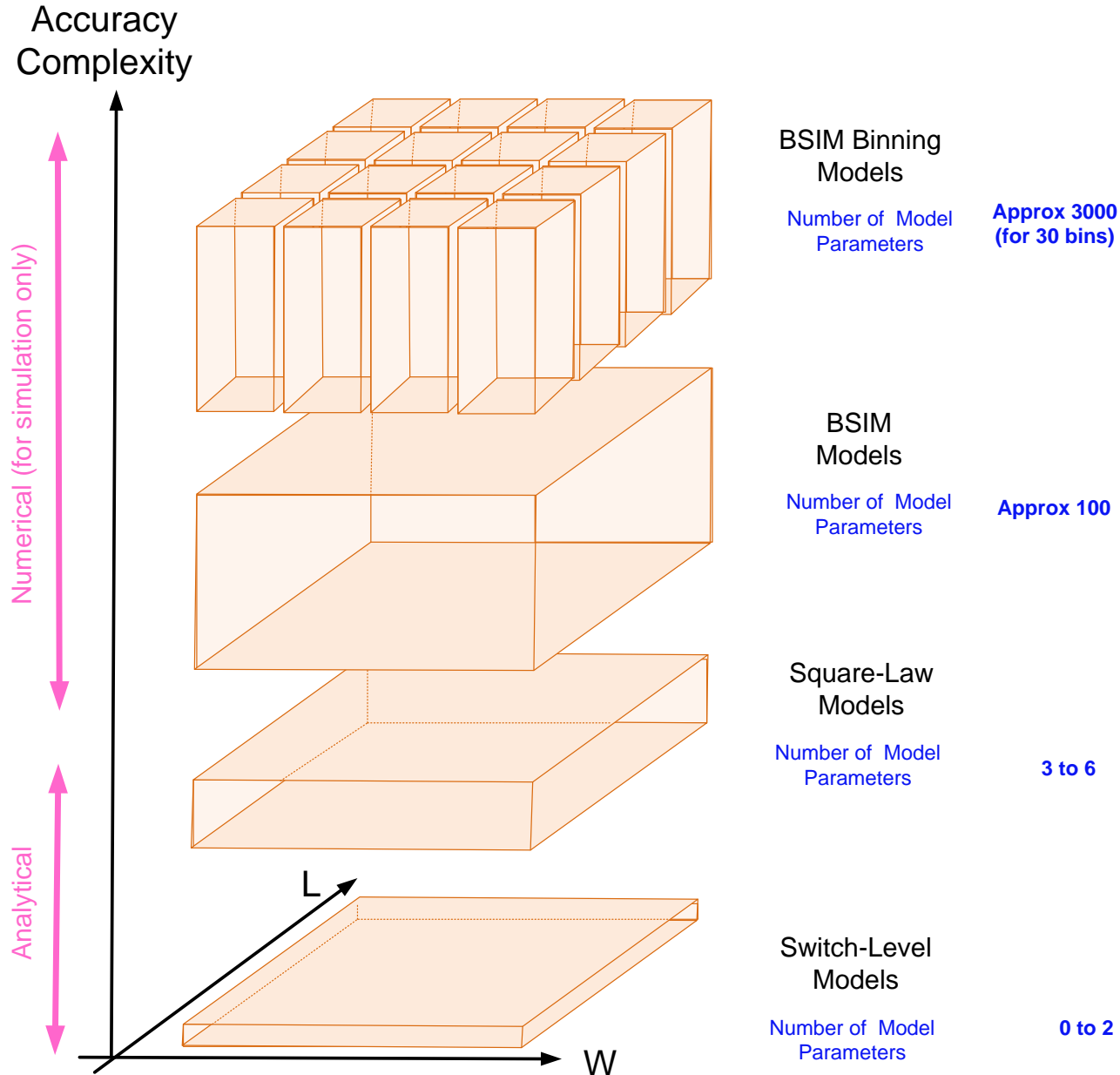
- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS
- five different BSIM models !

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 1.5E-7       NCH     = 1.7E17      TOX       = 1.42E-8
+K1      = 0.8976376    K2      = -0.09255    VTH0      = 0.629035
+K3B     = -8.2369696   W0      = 1.041146E-8    K3        = 24.0984767
+DVT0W   = 0           DVT1W   = 0           NLX       = 1E-9
+DVT0     = 2.7123969   DVT1    = 0.4232931    DVT2W     = 0
+U0      = 451.2322004   UA      = 3.091785E-13    DVT2      = -0.1403765
+UC       = 1.22401E-11  VSAT    = 1.715884E5    UB        = 1.702517E-18
+AGS     = 0.130484     B0      = 2.446405E-6    A0        = 0.6580918
+KETA     = -3.043349E-3 A1      = 8.18159E-7    B1        = 5E-6
+RDSW    = 1.367055E3   PRWG    = 0.0328586    A2        = 0.3363058
+WR       = 1           WINT    = 2.443677E-7    PRWB      = 0.0104806
+XL       = 1E-7        XW      = 0           LINT      = 6.999776E-8
+DWB      = 3.676235E-8 VOFF    = -1.493503E-4  DWG       = -1.256454E-8
+CIT      = 0           CDSC    = 2.4E-4        NFACTOR   = 1.0354201
+CDSCB    = 0           ETA0    = 2.342963E-3    CDSCD     = 0
+DSUB     = 0.0764123   PCLM    = 2.5941582    ETAB      = -1.5324E-4
+PDIBLC2  = 2.366707E-3 PDIBLCB  = -0.0431505   PDIBLC1   = 0.8187825
+PSCBE1   = 6.611774E8  PSCBE2   = 3.238266E-4  DROUT     = 0.9919348
+DELTA    = 0.01       RSH      = 83.5        PVAG      = 0
+PRT      = 0           UTE     = -1.5        MORMOD    = 1
+KT1L     = 0           KT2     = 0.022       KT1       = -0.11
+UB1      = -7.61E-18   UC1     = -5.6E-11    UA1       = 4.31E-9
+WL       = 0           WLN     = 1           AT        = 3.3E4
+WWN      = 1           WWL     = 0           WW        = 0
+LLN      = 1           LW       = 0           LL        = 0
+LWL      = 0           CAPMOD  = 2           LWN       = 1
+CGDO     = 2.32E-10    CGSO    = 2.32E-10    XPART     = 0.5
+CJ       = 4.282017E-4 PB       = 0.9317787   CGBO      = 1E-9
+CJSW     = 3.034055E-10 PBSW    = 0.8          MJ        = 0.4495867
+CJSWG    = 1.64E-10   PBSWG   = 0.8          MJSW      = 0.1713852
+CF       = 0           PVTH0   = 0.0520855   MJSWG     = 0.1713852
+PK2      = -0.0289036 WKETA    = -0.0237483  PRDSW     = 112.8875816
+          LKETA      = 1.728324E-3
*)
*
```

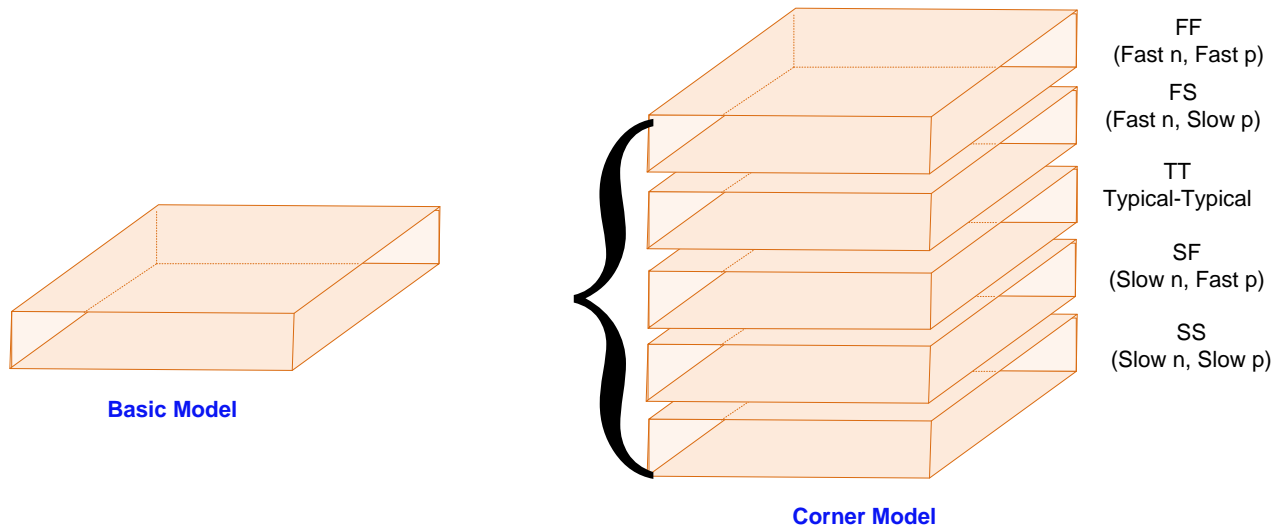
TT: typical-typical
FF: fast n, fast p
FS: fast n, slow p
SF: slow n, fast p
SS: slow n, slow p

With 4 corners, this model has 475 model parameters !

Hierarchical Model Comparisons



Corner Models

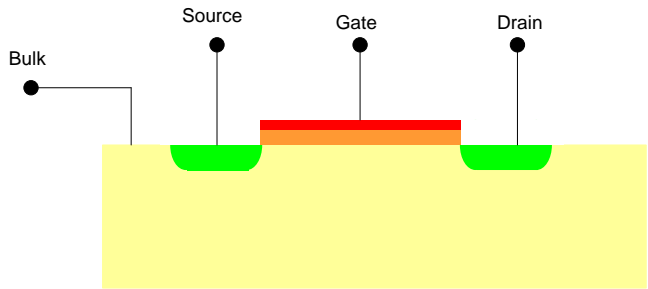


Applicable at any level in model hierarchy (same model, different parameters)

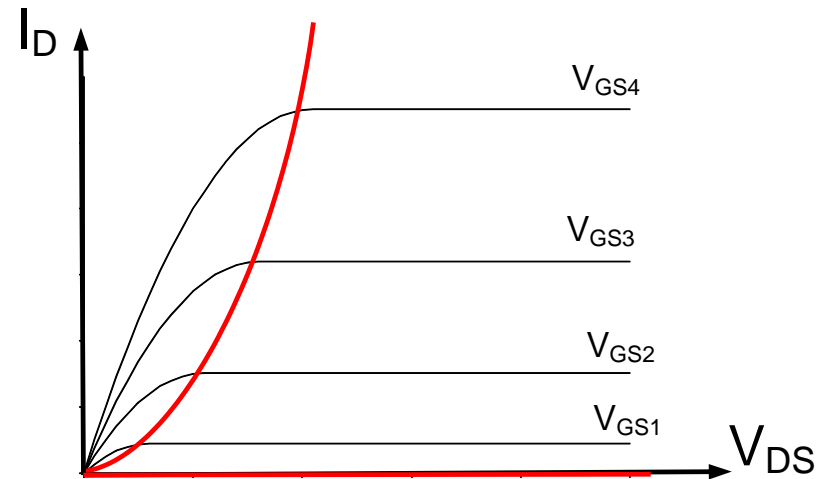
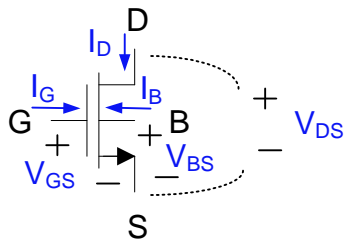
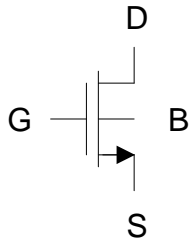
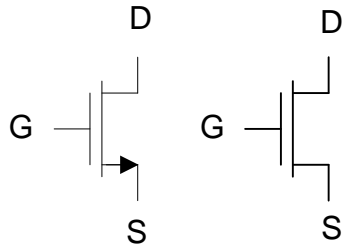
Often 4 corners (FF, FS, SF, SS) used but sometimes many more

Designers must provide enough robustness so good yield at all corners

n-channel p-channel modeling



n-channel MOSFET



$$V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > 0$$

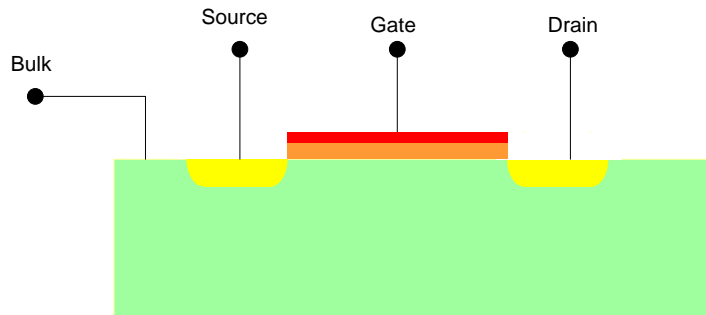
(for enhancement devices)

$$I_D = \begin{cases} 0 & V_{GS} \leq V_{Tn} \\ \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_{Tn} \quad V_{DS} < V_{GS} - V_{Tn} \\ \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{Tn})^2 & V_{GS} \geq V_{Tn} \quad V_{DS} \geq V_{GS} - V_{Tn} \end{cases}$$

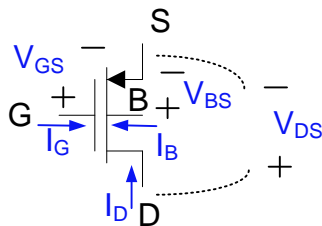
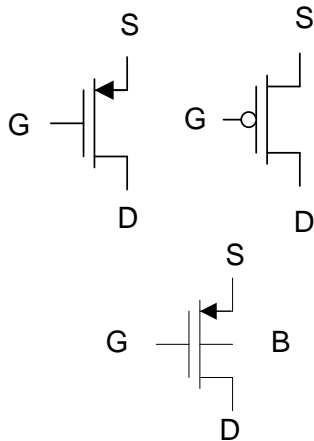
$I_G = I_B = 0$

Positive V_{DS} and V_{GS} cause a positive I_D

n-channel p-channel modeling

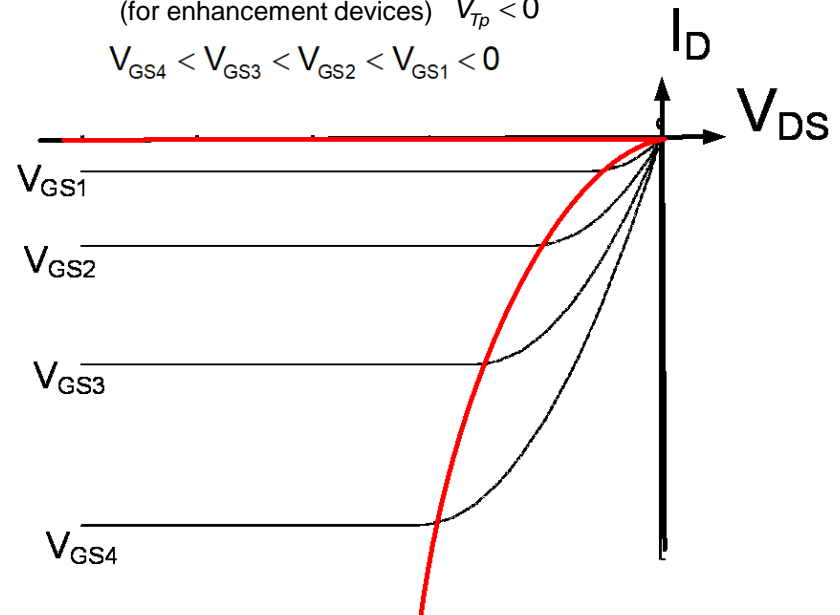


p-channel MOSFET



(for enhancement devices) $V_{Tp} < 0$

$$V_{GS4} < V_{GS3} < V_{GS2} < V_{GS1} < 0$$



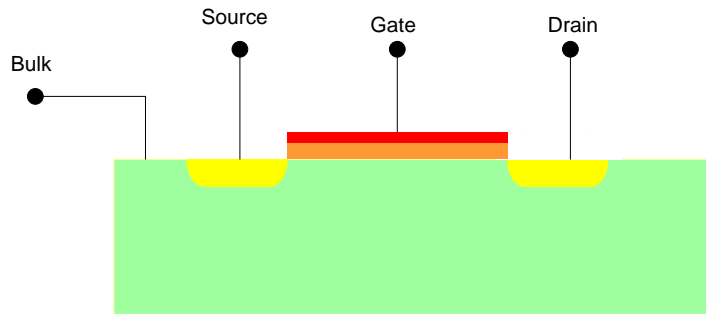
$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{ox} \frac{W}{L} \left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{ox} \frac{W}{2L} (V_{GS} - V_{Tp})^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

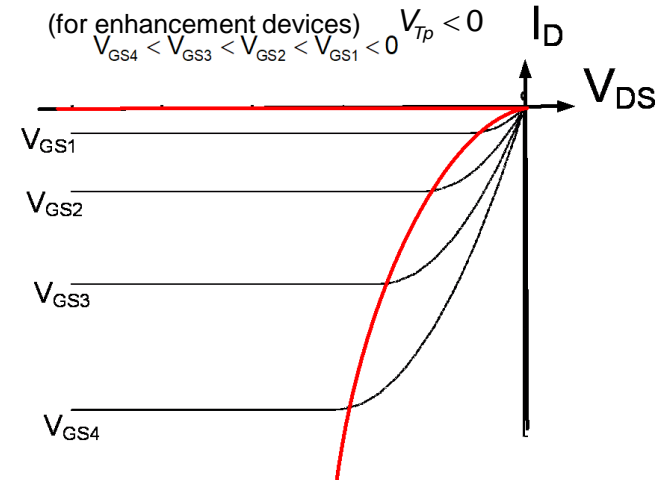
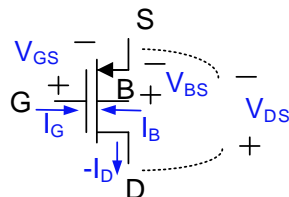
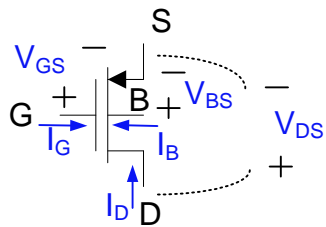
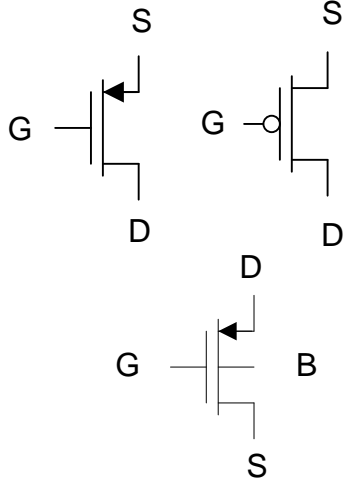
Negative V_{DS} and V_{GS} cause a negative I_D

Functional form of models are the same, just sign differences and some parameter differences (usually mobility is the most important)

n-channel p-channel modeling



p-channel MOSFET

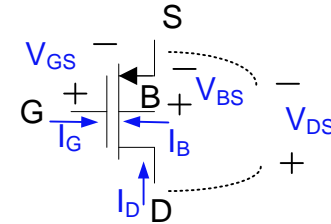
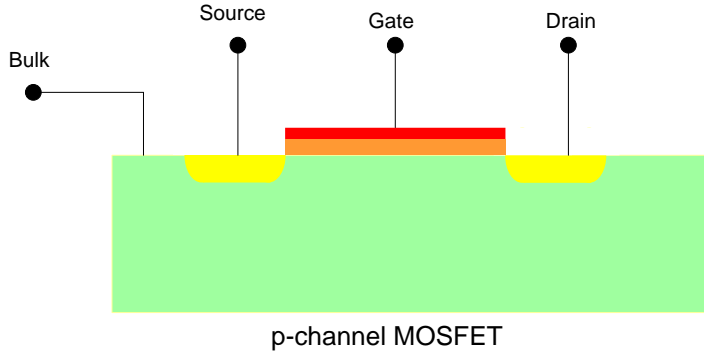


$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{ox} \frac{W}{L} \left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{ox} \frac{W}{2L} (V_{GS} - V_{Tp})^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

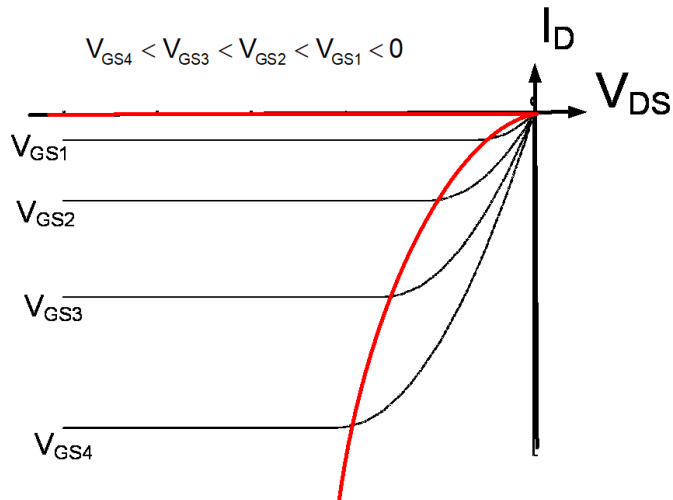
$I_G = I_B = 0$

- Actually should use C_{Oxp} and C_{Oxn} but they are usually almost identical in most processes
- $\mu_n \approx 3\mu_p$
- May choose to model $-I_D$ which will be non-negative

n-channel p-channel modeling



(for enhancement devices)



$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{ox} \frac{W}{L} \left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{ox} \frac{W}{2L} (V_{GS} - V_{Tp})^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

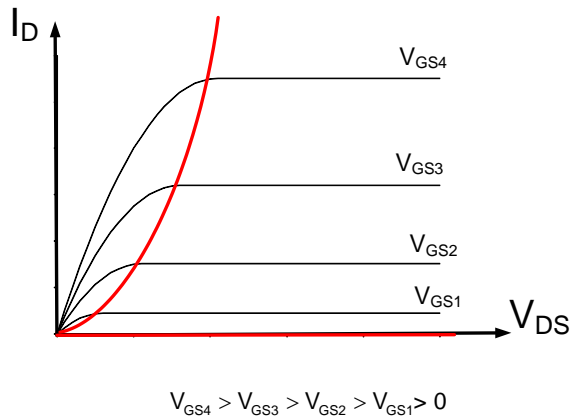
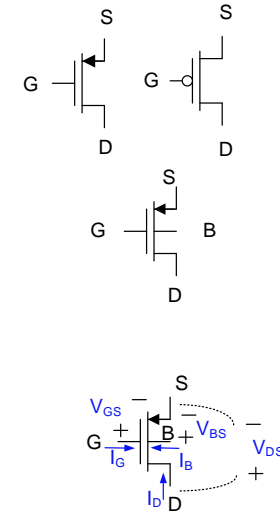
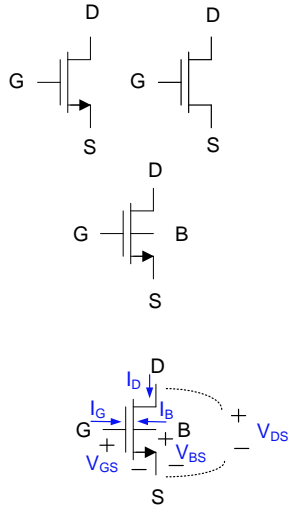
Alternate equivalent representation

$$|I_D| = \begin{cases} 0 & |V_{GS}| \leq |V_{Tp}| \\ \mu_p C_{ox} \frac{W}{L} \left(|V_{GS}| - |V_{Tp}| - \frac{|V_{DS}|}{2} \right) |V_{DS}| & |V_{GS}| \geq |V_{Tp}| \quad |V_{DS}| < |V_{GS}| - |V_{Tp}| \\ \mu_p C_{ox} \frac{W}{2L} (|V_{GS}| - |V_{Tp}|)^2 & |V_{GS}| \geq |V_{Tp}| \quad |V_{DS}| \geq |V_{GS}| - |V_{Tp}| \end{cases}$$

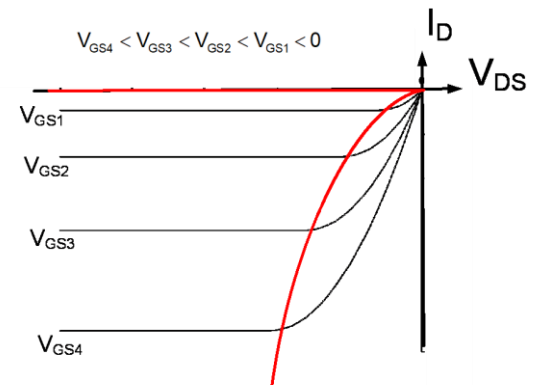
$I_G = I_B = 0$

These look like those for the n-channel device but with ||

n-channel p-channel modeling



Models essentially the same with different signs and model parameters



$$I_D = \begin{cases} 0 & V_{GS} \leq V_{Tn} \\ \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_{Tn}, V_{DS} < V_{GS} - V_{Tn} \\ \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{Tn})^2 & V_{GS} \geq V_{Tn}, V_{DS} \geq V_{GS} - V_{Tn} \end{cases}$$

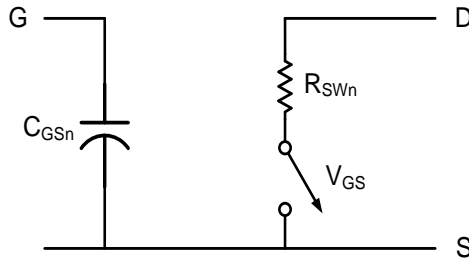
$I_G = I_B = 0$

$$\begin{aligned} V_{GS} &\leq V_{Tn} \\ V_{GS} &\geq V_{Tn} \quad V_{DS} < V_{GS} - V_{Tn} \\ V_{GS} &\geq V_{Tn} \quad V_{DS} \geq V_{GS} - V_{Tn} \end{aligned}$$

$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{ox} \frac{W}{L} \left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \leq V_{Tp}, V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{ox} \frac{W}{2L} (V_{GS} - V_{Tp})^2 & V_{GS} \leq V_{Tp}, V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

Model Relationships



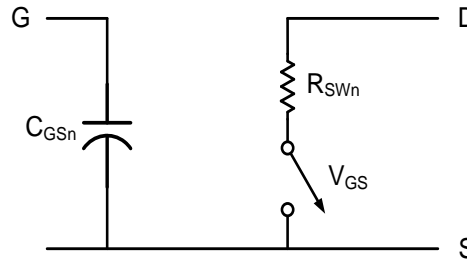
Determine R_{SW} and C_{GS} in the switch-level model for an **n-channel** MOSFET from square-law model in the 0.5u ON CMOS process if $L=1\mu$, $W=1\mu$

(Assume $\mu C_{OX}=100\mu A V^{-2}$, $C_{OX}=2.5fF \mu^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

when SW is on, operation is “deep” triode

Model Relationships



Determine R_{SW} and C_{GS} for an **n-channel** MOSFET from square-law model in the 0.5u ON CMOS process if $L=1\mu$, $W=1\mu$

(Assume $\mu C_{OX}=100\mu A V^{-2}$, $C_{OX}=2.5fF\mu^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

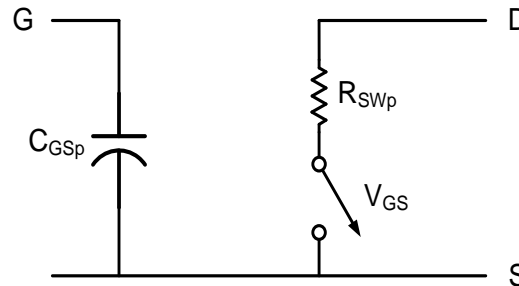
When on operating in deep triode

$$I_D = \mu C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \cong \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$R_{SQ} = \frac{V_{DS}}{I_D} \bigg|_{V_{GS}=V_{DD}} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_T)} \bigg|_{V_{GS}=3.5V} = \frac{1}{(E-4) \left(\frac{1}{1} \right) (3.5-1)} = 4K\Omega$$

$$C_{GS} = C_{OX} WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF$$

Model Relationships



Determine R_{SW} and C_{GS} for an **p-channel** MOSFET from square-law model in the 0.5u ON CMOS process if $L=1\mu$, $W=1\mu$

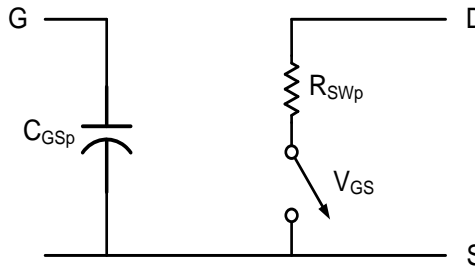
$$(C_{OX}=2.5\text{fFu}^{-2}, V_{T0}=1\text{V}, V_{DD}=3.5\text{V}, V_{SS}=0)$$

Observe $\mu_n \setminus \mu_p \approx 3$

$$-I_D = \begin{cases} 0 & V_{GS} \geq V_T \\ \mu C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \leq V_T, V_{DS} > V_{GS} - V_T \\ \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \leq V_T, V_{DS} \leq V_{GS} - V_T \end{cases}$$

When SW is on, operation is “deep” triode

Model Relationships



Determine R_{SW} and C_{GS} for an p-channel MOSFET from square-law model in the 0.5u ON CMOS process if $L=1\mu$, $W=1\mu$

$$(C_{OX}=2.5fF\mu^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)$$

Observe $\mu_n \setminus \mu_p \approx 3$

$$-I_D = \mu_p C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \cong \mu_p C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$R_{SQ} = \left. \frac{-V_{DS}}{-I_D} \right|_{V_{GS}=V_{DD}} = \left. \frac{1}{\mu_p C_{OX} \frac{W}{L} (V_{GS} - V_T)} \right|_{V_{GS}=3.5V} = \frac{1}{\left(\left(\frac{1}{3} \right) E - 4 \right) \left(\frac{1}{1} \right) |3.5 - 1|} = 12K\Omega$$

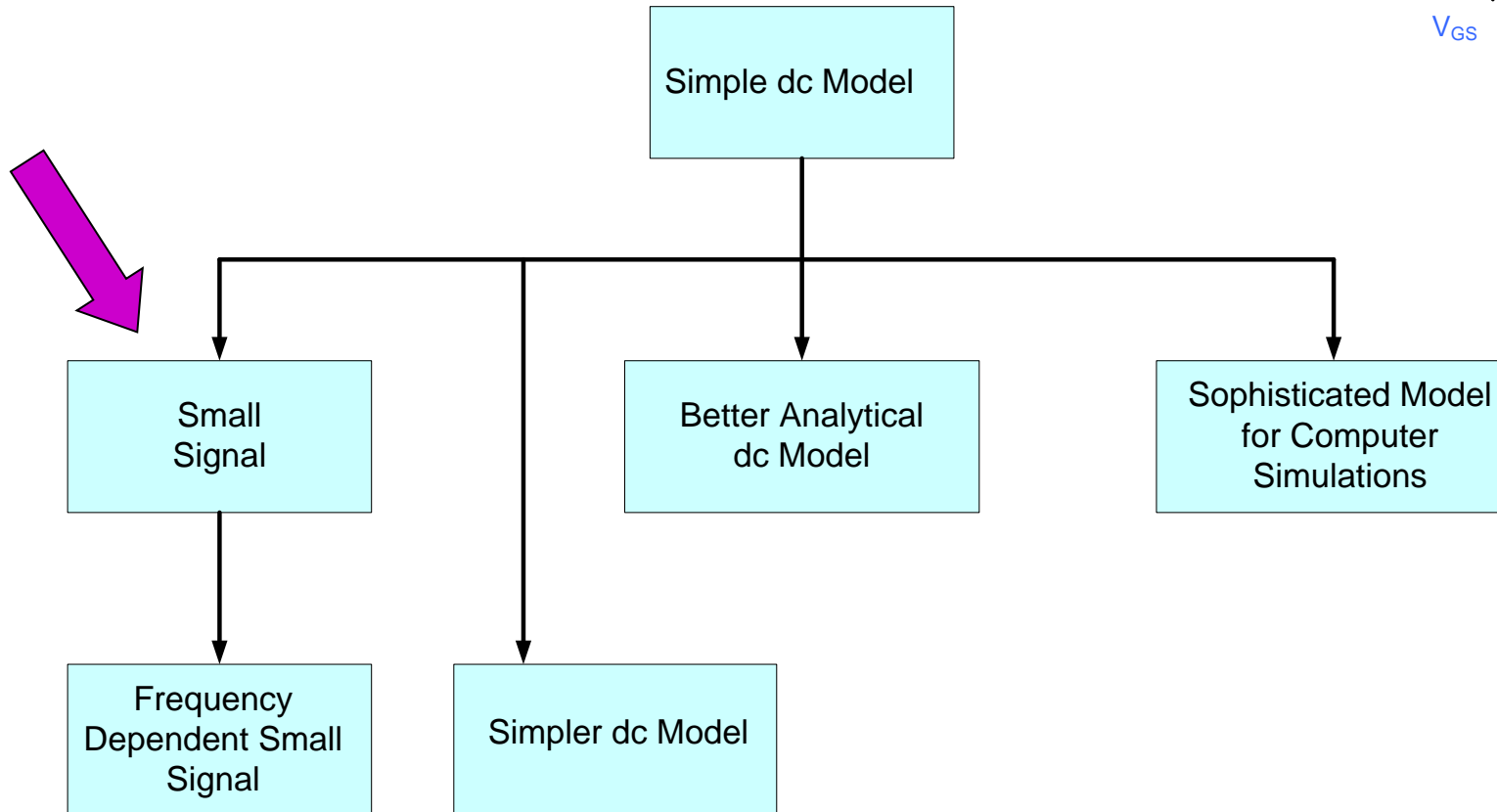
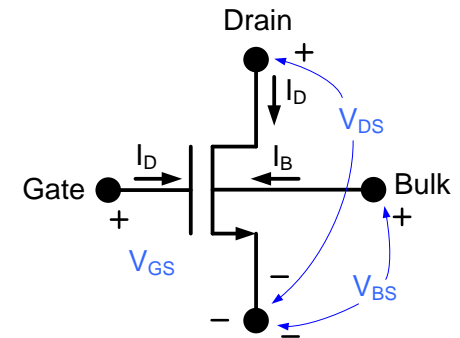
$$C_{GS} = C_{OX} WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF$$

Observe the resistance of the p-channel device is approximately 3 times larger than that of the n-channel device for same bias and dimensions !

Modeling of the MOSFET

Goal: Obtain a mathematical relationship between the port variables of a device.

$$\left. \begin{aligned} I_D &= f_1(V_{GS}, V_{DS}, V_{BS}) \\ I_G &= f_2(V_{GS}, V_{DS}, V_{BS}) \\ I_B &= f_3(V_{GS}, V_{DS}, V_{BS}) \end{aligned} \right\}$$

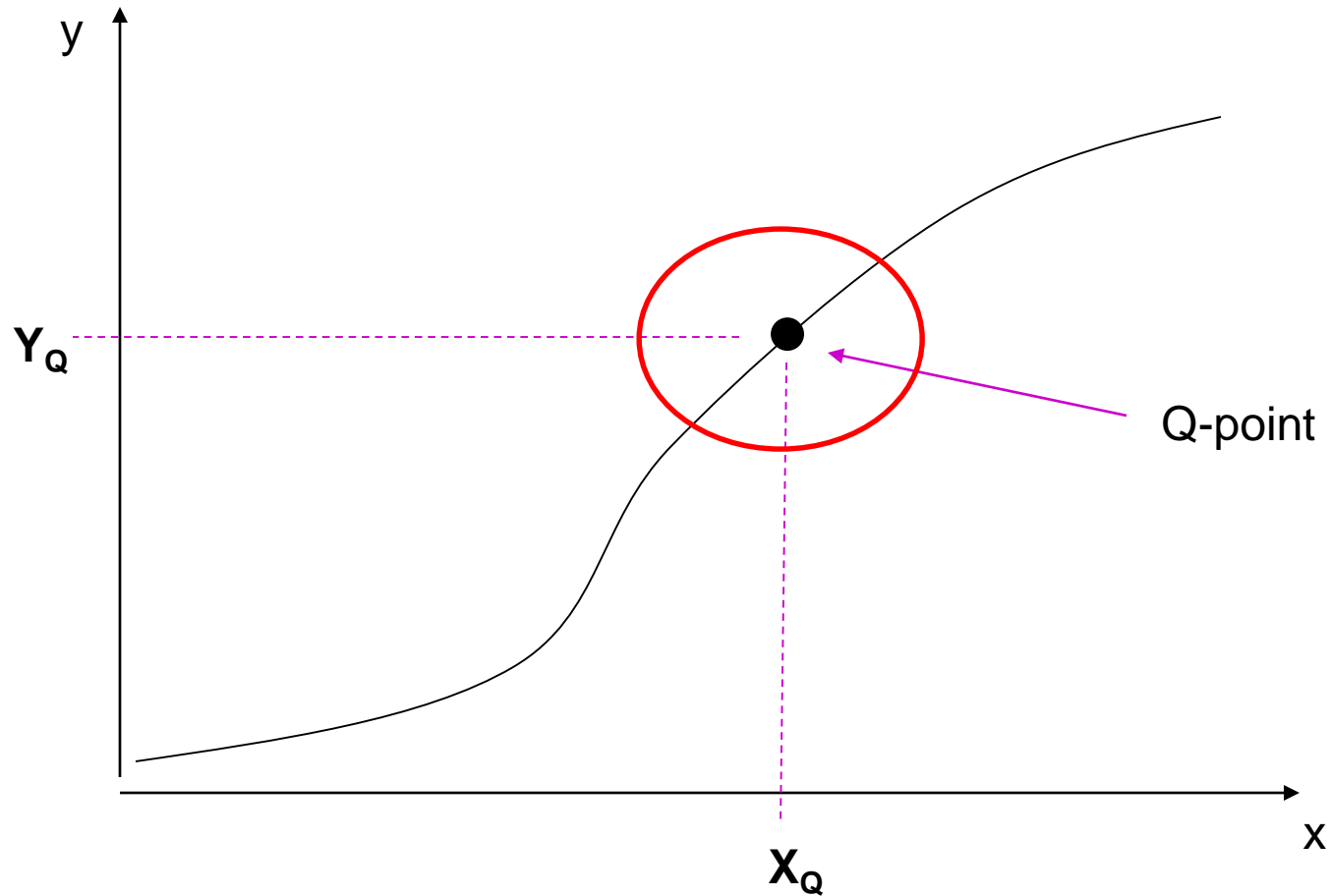


Small-Signal Model

Goal with small signal model is to predict performance of circuit or device in the vicinity of an operating point

Operating point is often termed Q-point

Small-Signal Model



- Behaves linearly in the vicinity of the Q-point
- Analytical expressions for small signal model will be developed later

End of Lecture 17