

# CprE 381, Computer Organization and Assembly-Level Programming, Spring 2019

## Lab 2 Report

Student Name \_\_\_\_\_ Sean Gordon \_\_\_\_\_

Section/Lab Time \_\_\_\_\_ C/10:00 a.m. \_\_\_\_\_

*Refer to the highlighted language in the lab 2 instruction for the context of the following questions.*

- a. [Part 0] At the end of Chapter 3, answer questions 4b), 5a), and 6.

Prelab 2

7/25/2019  
Section C  
Sean Gordon

4b) Entity sys2 is  
port (  
input = w : in std\_logic;  
a\_data : in std\_logic\_vector (7 downto 0);  
b\_data : in std\_logic\_vector (7 downto 0);  
clk : in std\_logic;  
dat\_4 : out std\_logic\_vector (7 downto 0);  
dat\_5 : out std\_logic\_vector (2 downto 0));  
end sys2;

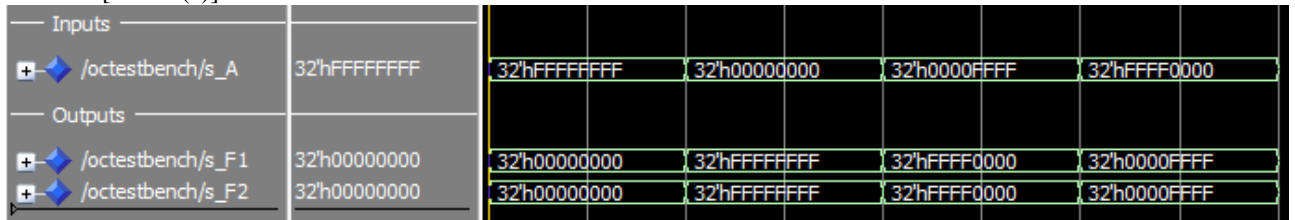
5a)

6)

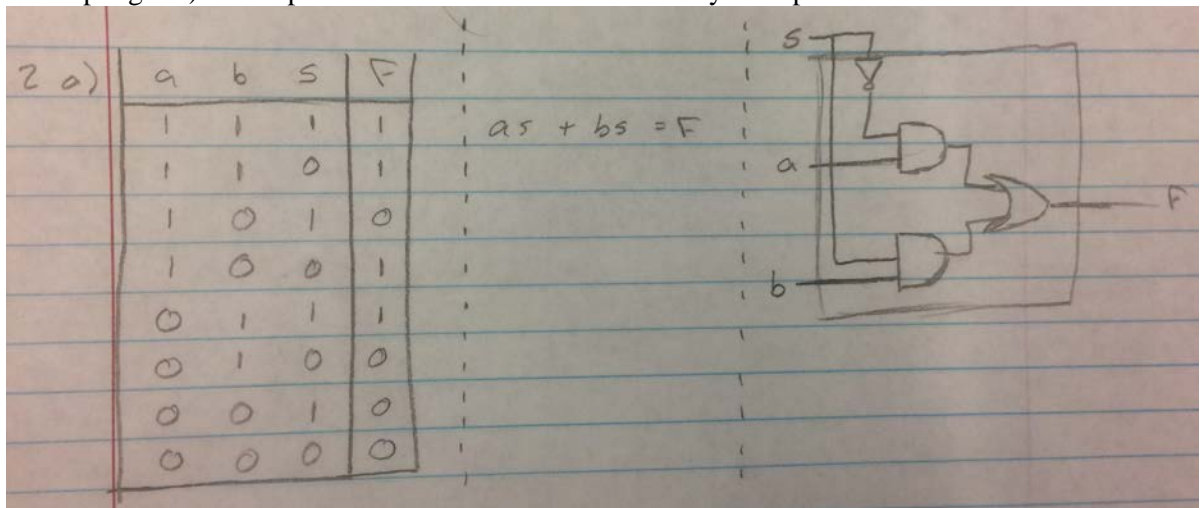
a) semicolon on line 5 misplaced, before closing parentheses rather than after

b) Missing end parenthesis at the end of line 5 before the semicolon

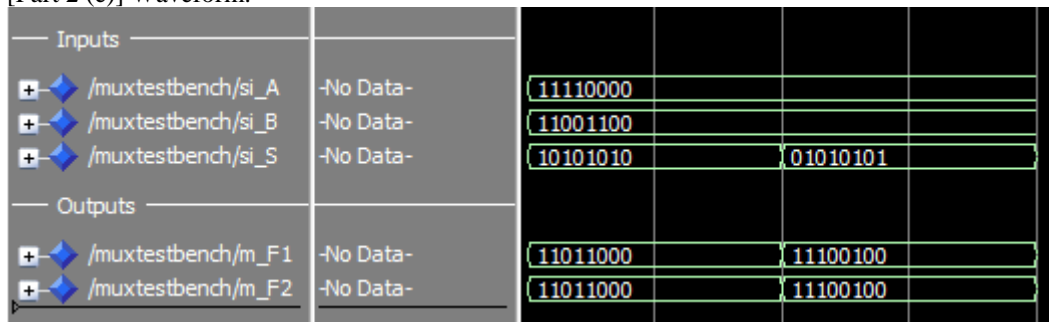
b. [Part 1 (c)] Waveform.



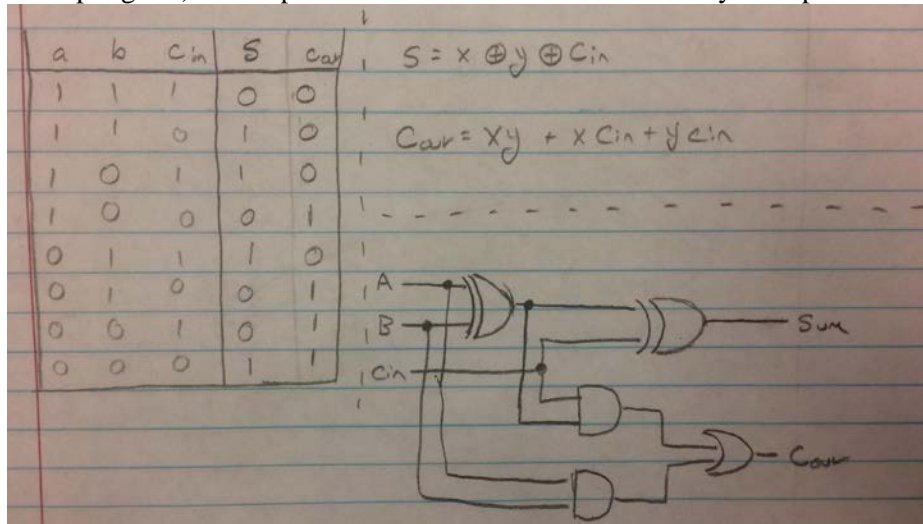
c. [Part 2 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a 2:1 mux. Include this in your report PDF.



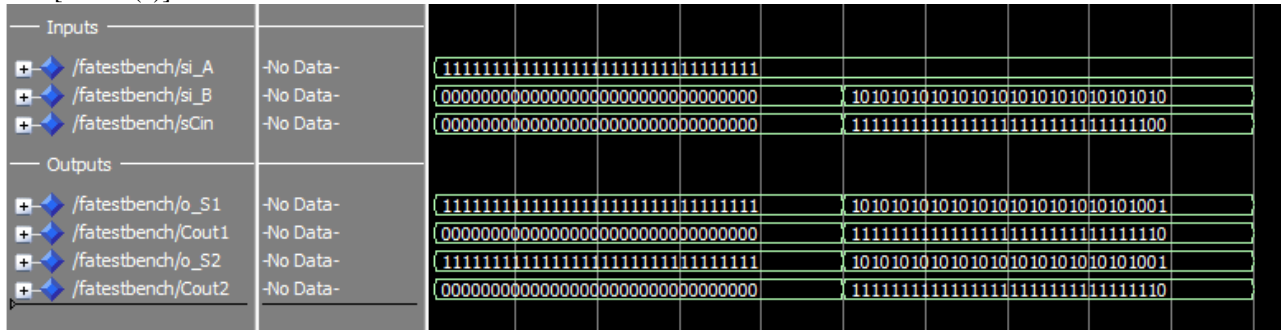
d. [Part 2 (e)] Waveform.



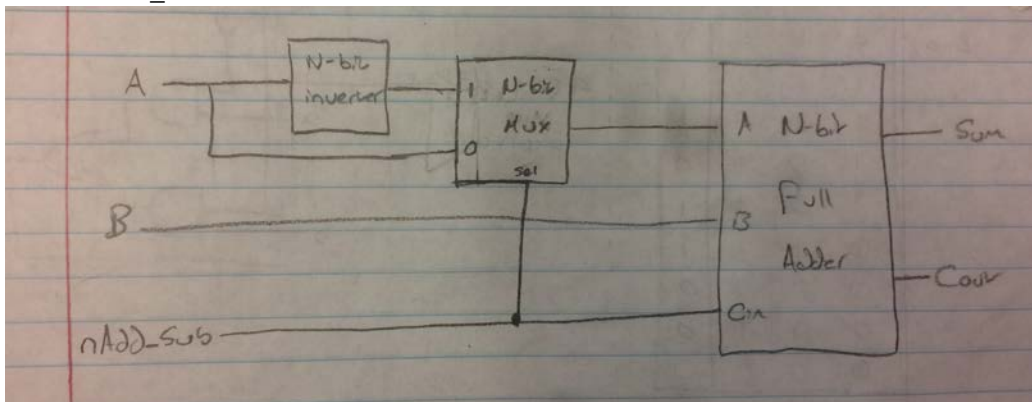
- e. [Part 3 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a full adder. Include this in your report PDF.



- f. [Part 3 (e)] Waveform.

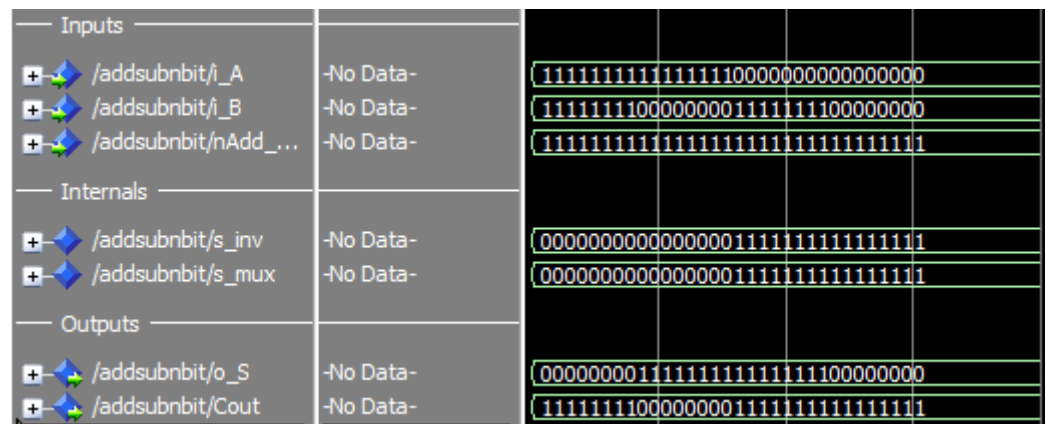
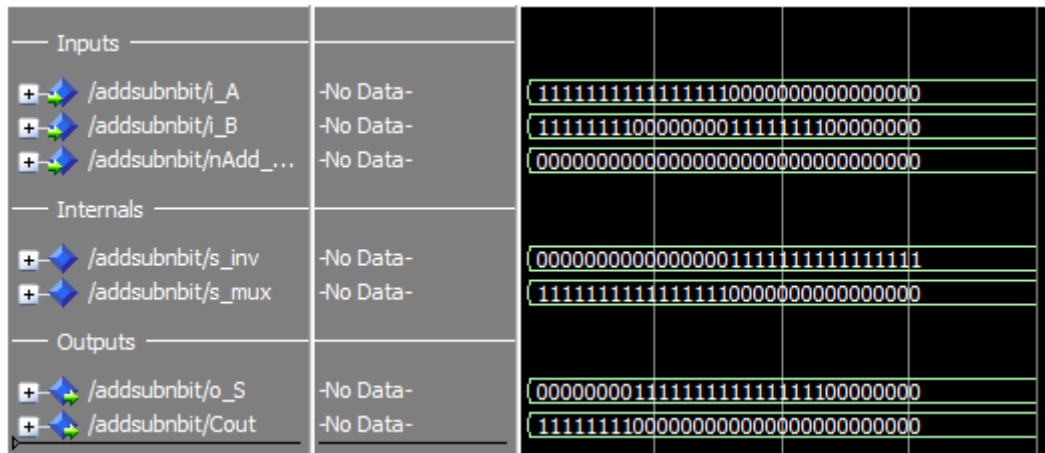


- g. [Part 4 (a)] Draw a schematic (don't use a schematic capture tool) showing how an N-bit adder/subtractor with control can be implemented using only the three main components designed in problems 1), 2), and 3) (the N-bit inverter, N-bit 2:1 mux, and N-bit adder). How is the 'nAdd\_Sub' bit used?



The nAdd\_Sub bit is used to decide between adding and subtracting, using two's complement to achieve the latter. It is fed into the multiplexor as a select bit and into the full adder as a carry in.

- h. [Part 4 (c)] Provide multiple waveform screenshots in your write-up to confirm that this component is working correctly. What test-cases did you include and why?



I included a case alternating the nAdd\_Sub bit, one where the bit is all 0, and one where it is all 1. I felt this was an apt enough test of the performance.

- i. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

- a. How many hours did you spend on this lab?

| Task                | During lab time | Outside of lab time |
|---------------------|-----------------|---------------------|
| Reading lab         | 30 min          | 10 min              |
| Pencil/paper design | 0 min           | 10 min              |
| VHDL design         | 60 min          | 30 min              |
| Assembly coding     | 0 min           | 0 min               |
| Simulation          | 10 min          | 20 min              |
| Debugging           | 20 min          | 70 min              |
| Report writing      | 0 min           | 20 min              |
| Other:              |                 |                     |
| Total               | 120 min         | 160 min             |

- b. If you could change one thing about the lab experience, what would it be? Why?  
That you have to write about your experience at the end. I have much more important things to do, and unless this class is one in a million, the metrics I list here will be disregarded in two or three years' time.
- c. What was the most interesting part of the lab?  
Going home