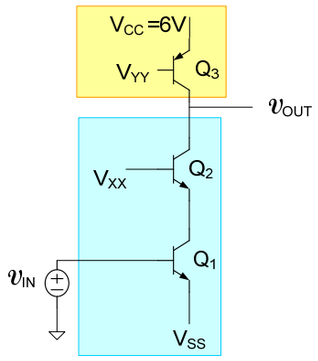
EE 330 Fall 2012
Homework 13

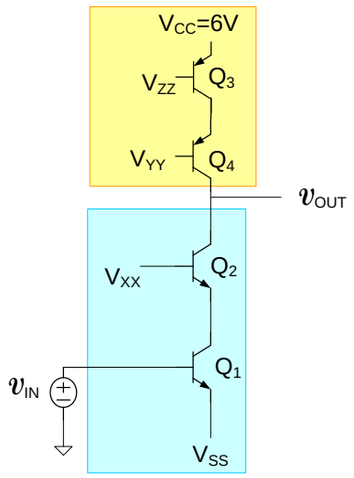
Due Monday November 26 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $L_{MIN}=W_{MIN}=0.5\mu$, and $V_{DD}=3.5V$.

Problem 1 (10 points):
In the circuit below, assume the biasing voltages have been selected so that the quiescent output voltage is 3V and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume $A_{E1}=A_{E2}=A_{E3}=100\mu^2$.

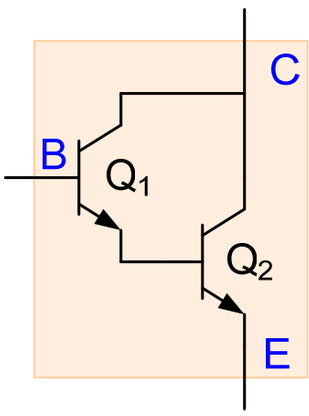


Problem 2 (10 points):
In the circuit below, assume the biasing voltages have been selected so that the quiescent output voltage is 3V and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume $A_{E1}=A_{E2}=A_{E3}=A_{E4}=100\mu^2$.

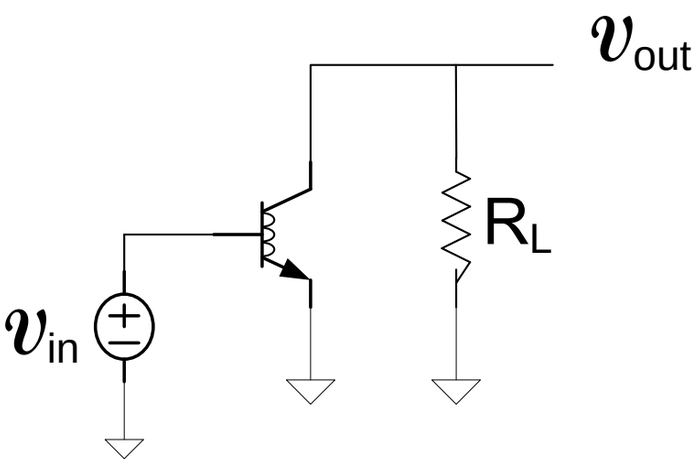


Problem 3 (10 points):
If a DC input voltage of 1uV is placed in series with v_{IN} in the circuit of problem 2, how much change in the output voltage from the quiescent value of 3V can be expected? Comment on the implications of this observation.

Problem 4 (10 points):
The Darlington configuration is shown below. Develop a two-port model for the Darlington configuration in terms of the small-signal parameters y_{11}, y_{12}, y_{21}, and y_{22}. Assume Q_1 and Q_2 are operating in the forward active region.

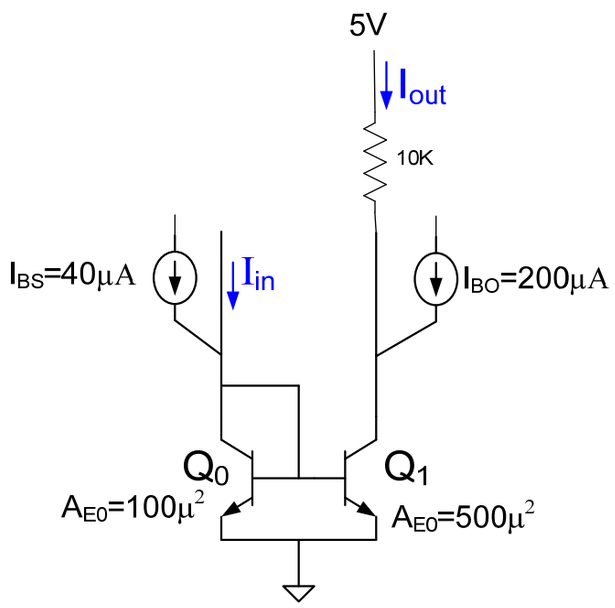


Problem 5 (10 points):
The small-signal equivalent circuit of a common emitter amplifier is shown below. If the emitter area of the BJT is $100\mu^2$ and the load resistor R_L is 2k, bias this circuit so that the quiescent output voltage is 5V and the DC voltage across R_L is also 5V while maintaining the same small-signal gain that this circuit has. You have one dc power supply available of any value you choose and any number of resistors and capacitors.



Problem 6 (10 points):
Consider the following circuit.

a) Determine an analytical expression that relates I_{OUT} to I_{IN}
b) With a computer simulation, plot the relationship between I_{OUT} and I_{IN} as I_{IN} is varied between -40uA and +40uA.

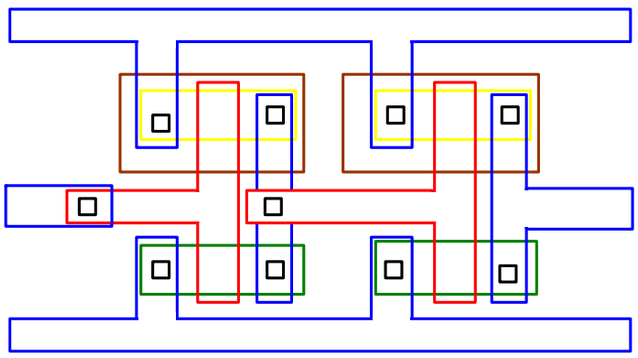


Problem 7 (5 points):
Give all the possible two-input Boolean functions and identify which of them are useful.

Problem 8 (5 points):
Give two gate-level structural implementations of the Behavioral Description: The output "F" is high when both "A" and "B" are high, or when both "C" and "B" are low. Otherwise "F" is low.

Problem 9 (10 points):
A physical layer implementation of a circuit at the layout level is shown below where blue denotes metal, red polysilicon, and green n-active, yellow p-active, brown n-well and black contacts. Assume the upper metal rail is a VDD pin, the lower metal rail is ground, the middle left metal is Boolean input A, and the middle right metal is Boolean output B.

a) Give a physical layer view of this layout at the circuit schematic level. Assume the contact sizes are 2λ x 2λ.
b) Give a structural layer view of this layout at the gate level.



Problem 10 (20 points):
A Boolean System is supposed to have an output “F” that is high when the Boolean inputs “A” and “B” are high, or when the inputs “C” and “D” are high and “E” is low, or when the input “A” is low and the input “E” is high.

a) Give a behavioral description of this system in terms of the input/output variables A, B, C, D, E, and F.
b) Write Verilog code describing this system at the behavioral level.
c) Give a gate-level structural description of this system if the only gates available are NOR gates with any number of inputs.
d) Write Verilog code describing this system at the gate level.
e) Give a transistor-level physical description of this system. You may use any logic style you are familiar with. You need not size the devices.