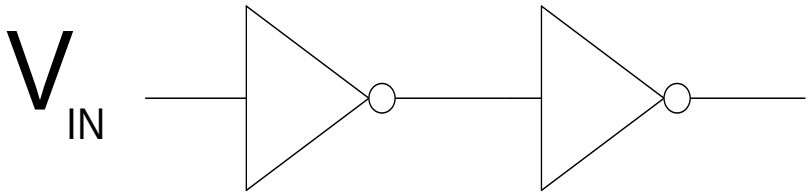
EE 330
Lecture 39

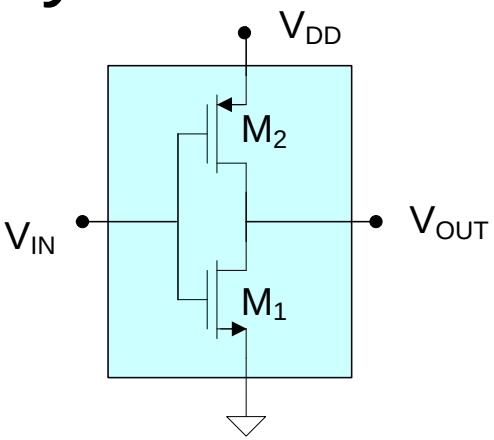
Digital Circuits

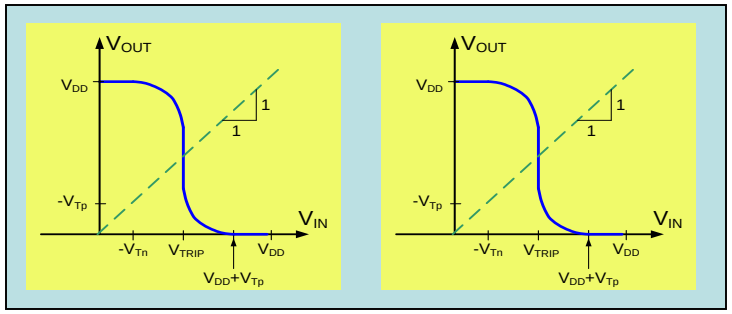
Other MOS Logic Families
Propagation Delay – basic characterization
Device Sizing (Inverter and multiple-input gates)

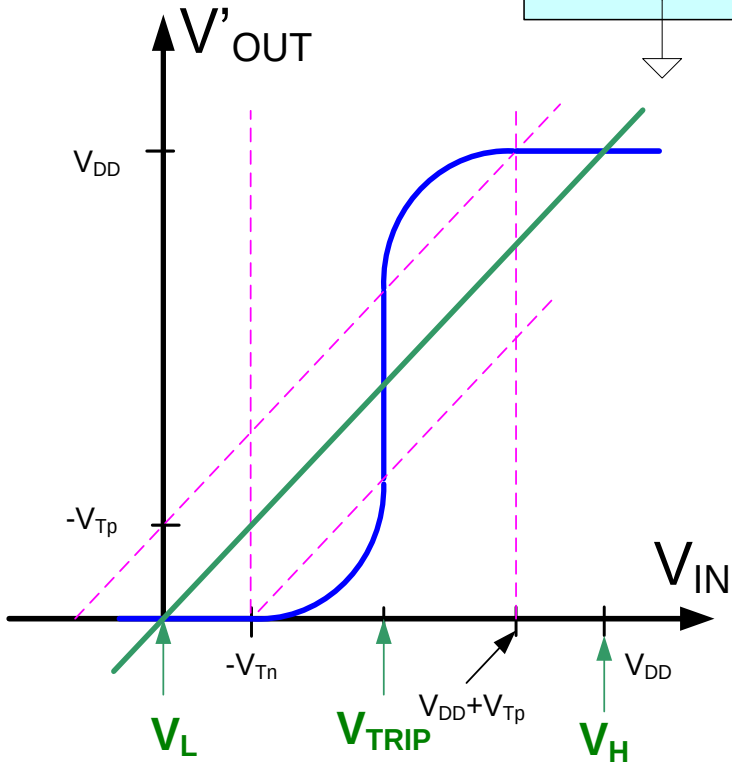
Review from last lecture

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family









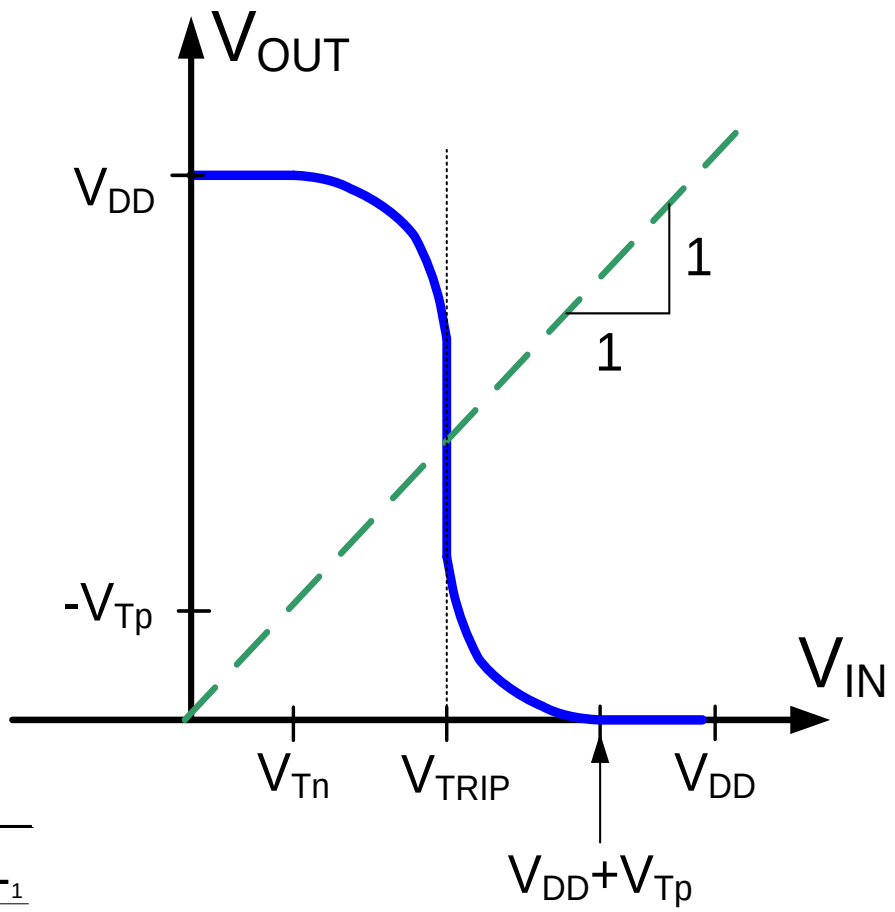
$V_H = V_{DD}$ and $V_L = 0$

Note this is independent of device sizing for THIS logic family !!

Review from last lecture

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

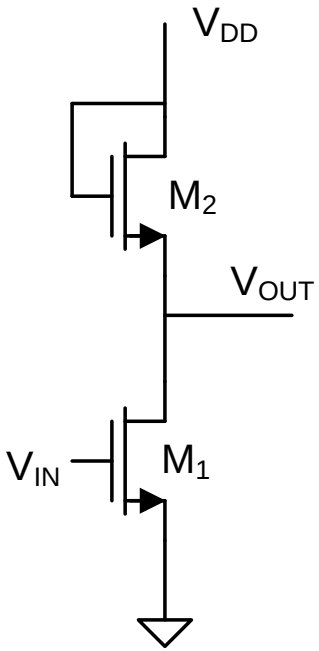


From Case 3 analysis:

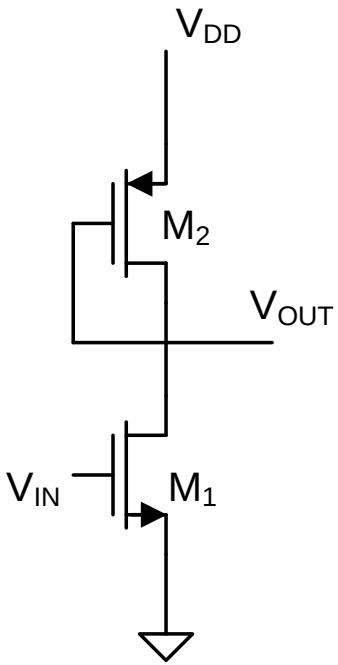
$$V_{IN} = \frac{\left(V_{Tn}\right) + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

Review from last lecture

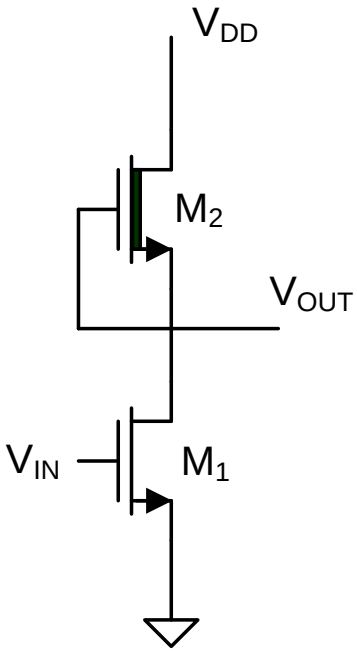
Other MOS Logic Families



Enhancement
Load NMOS



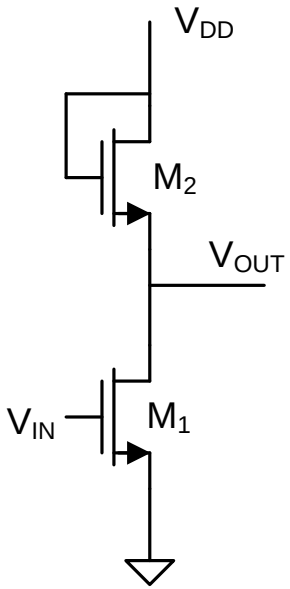
Enhancement Load
Pseudo-NMOS



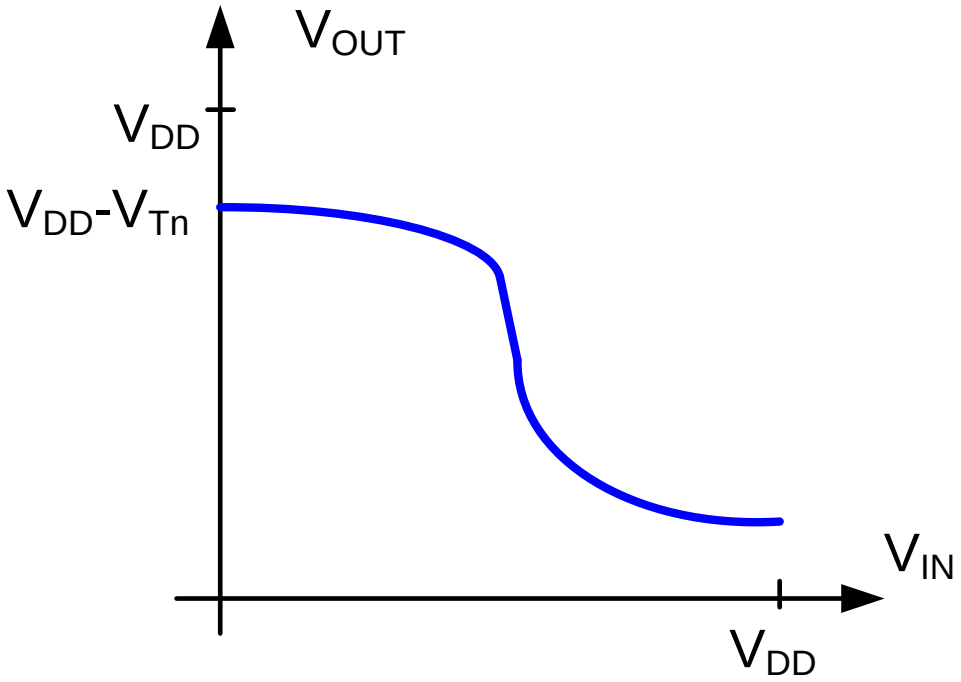
Depletion
Load NMOS

Review from last lecture

Other CMOS/MOS Logic Families

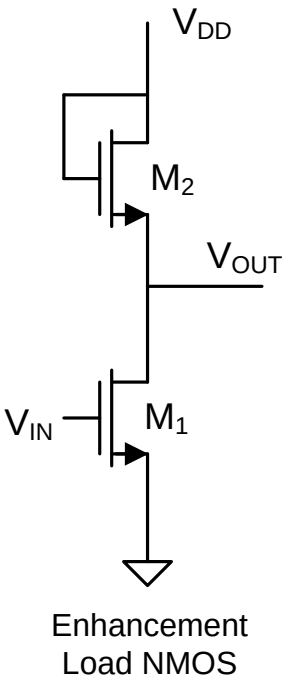


Enhancement
Load NMOS

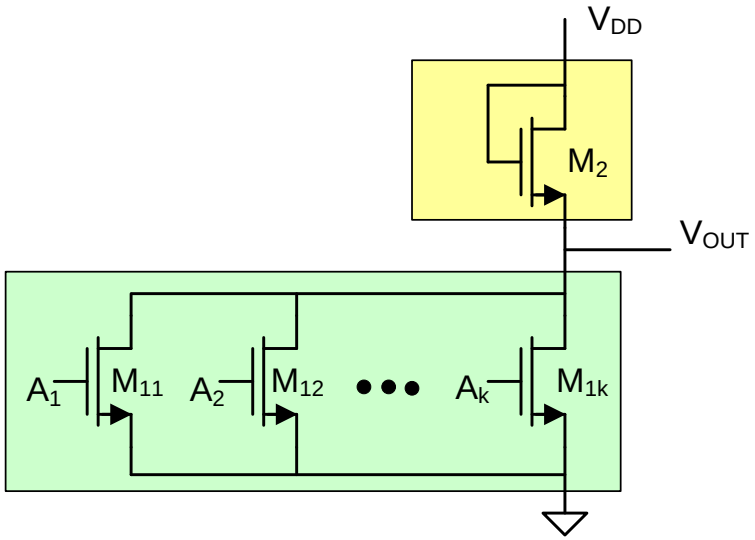


- **High and low swings are reduced**
- **Response time is slow on LH output transitions**
- **Static Power Dissipation Large when V_{OUT} is low (will show)**
- **Very economical process**
- **Termed "ratio logic" (because logic values dependent on device W/L ratios – USE UP DOF!)**
- **May not work for some device sizes**
- **Compact layout (no wells !)**
- **Available to use in standard CMOS process**

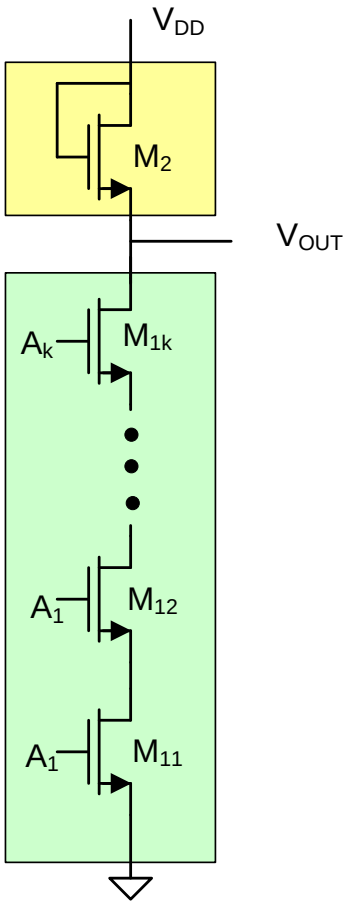
Other CMOS/MOS Logic Families



Enhancement Load NMOS



k-input NOR



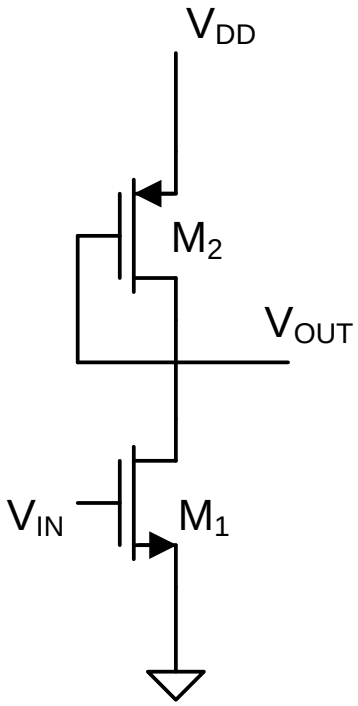
k-input NAND

- **Multiple-input gates require single transistor for each additional input**

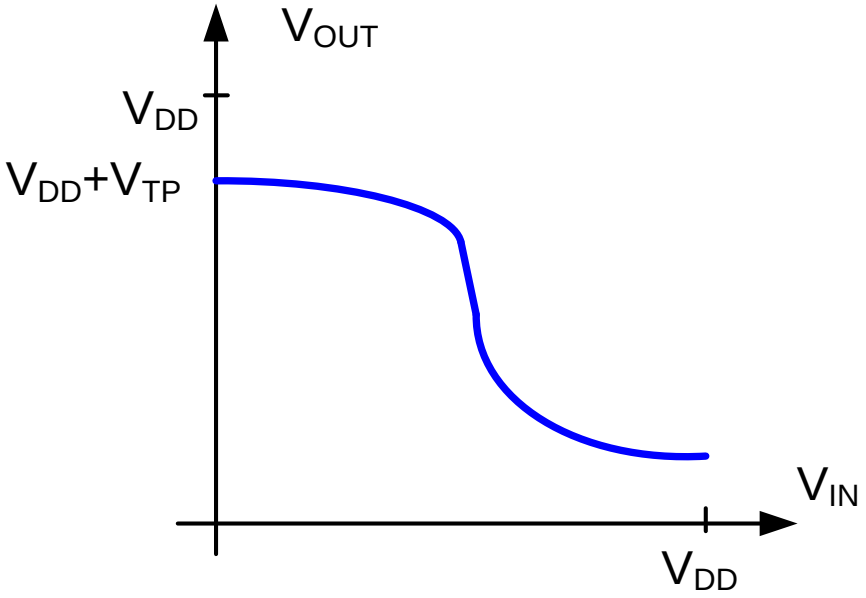
- **Still useful if many inputs are required**

(will be shown that static power does not increase with k)

Other CMOS/MOS Logic Families

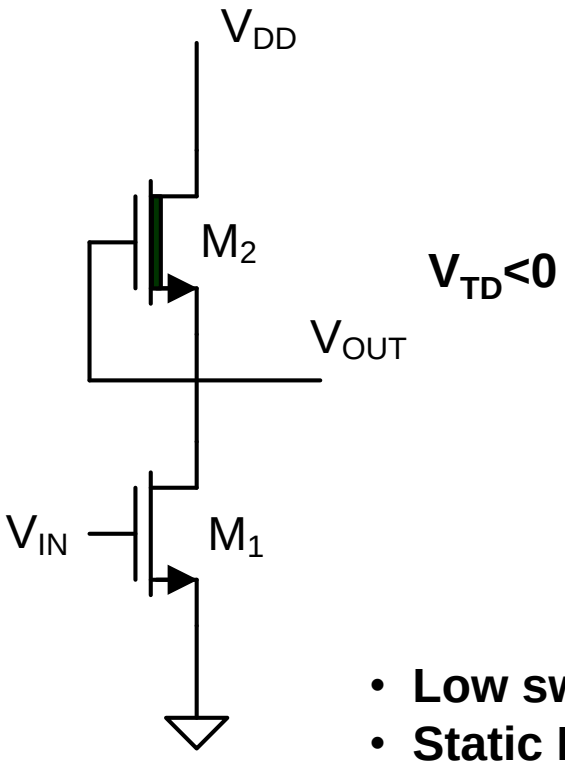


Enhancement Load
Pseudo-NMOS



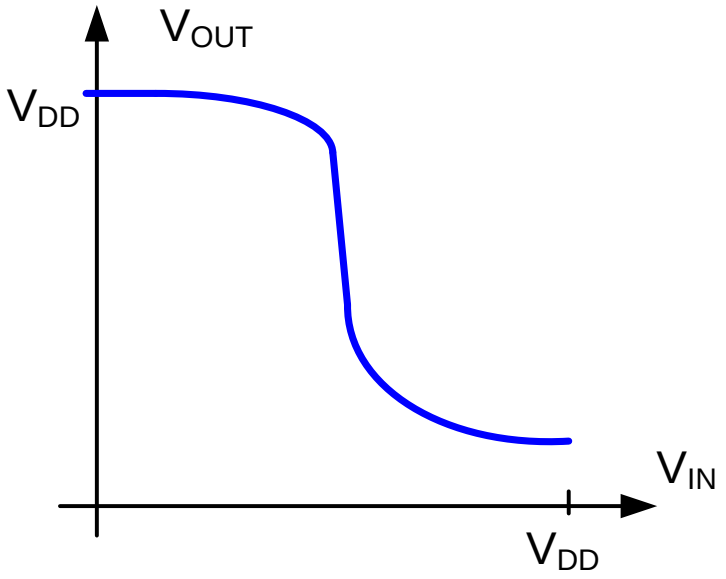
- **High and low swings are reduced**
- **Response time is slow on LH output transitions**
- **Static Power Dissipation Large when V_{OUT} is low**
- **Multiple-input gates require single transistor for each additional input**
- **Termed “ratio” logic**
- **Available to use in standard CMOS process**

Other CMOS/MOS Logic Families



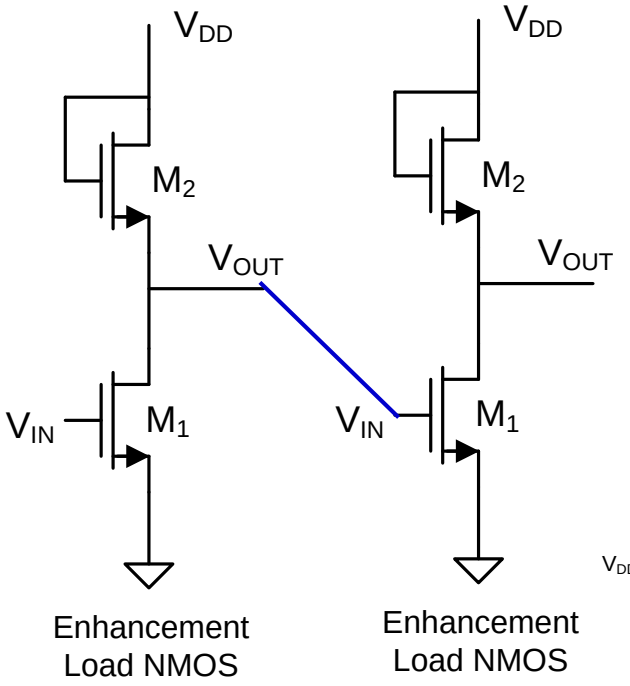
Depletion Load NMOS

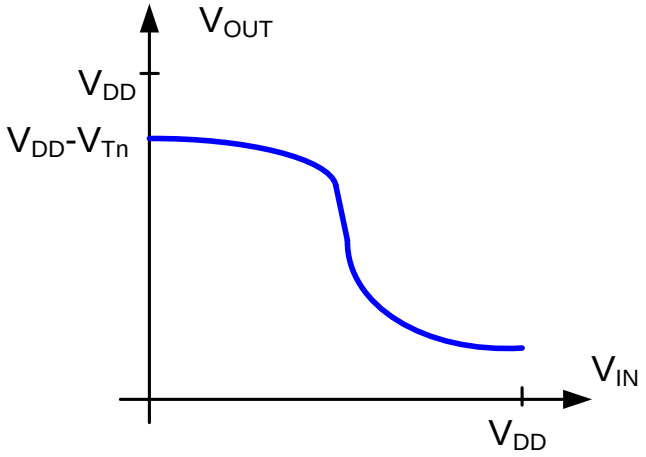
V_{TD}<0

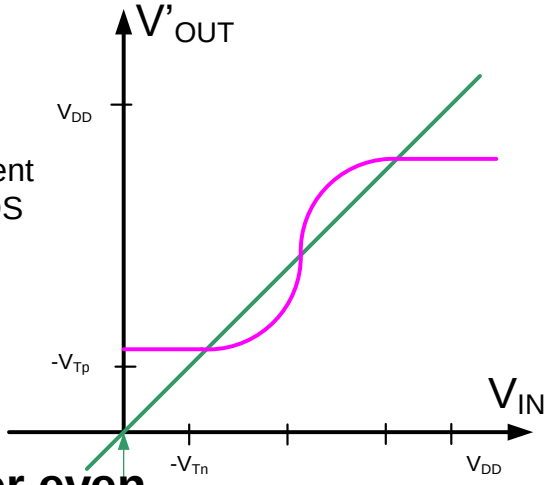


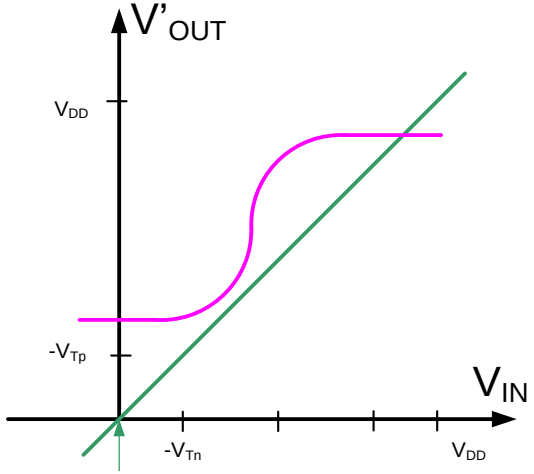
- **Low swing is reduced**
- **Static Power Dissipation Large when V_{OUT} is low**
- **Very economical process**
- **Better than Enhancement Load NMOS**
- **Termed "ratio" logic**
- **Compact layout (no wells !)**
- **Response time slow on L-H output transitions**
- **Dominant MOS logic until about 1985**
- **Depletion device not available in most processes today**

Other CMOS/MOS Logic Families



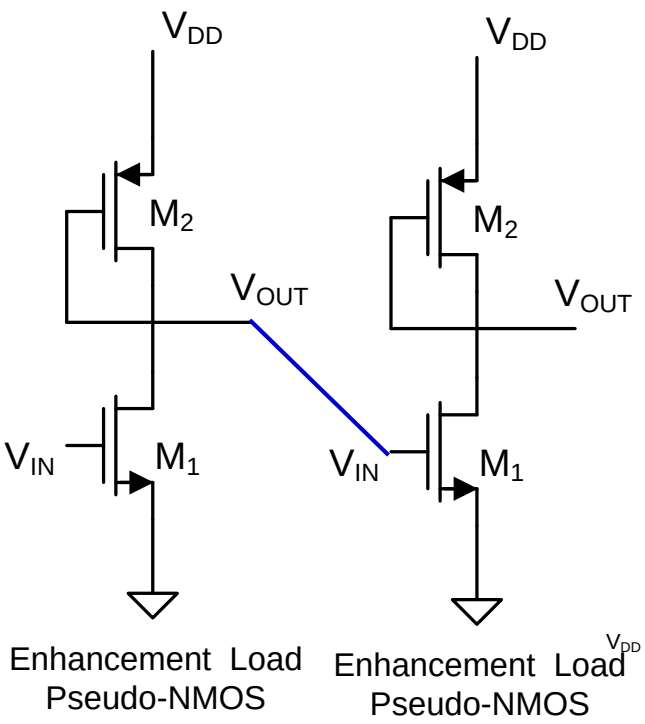


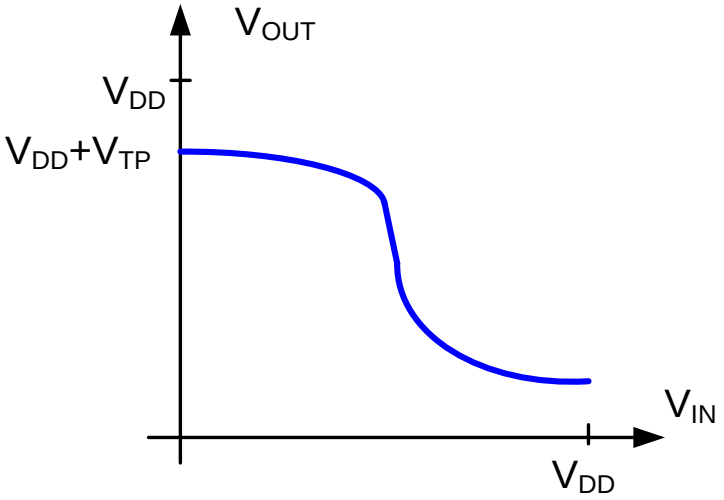


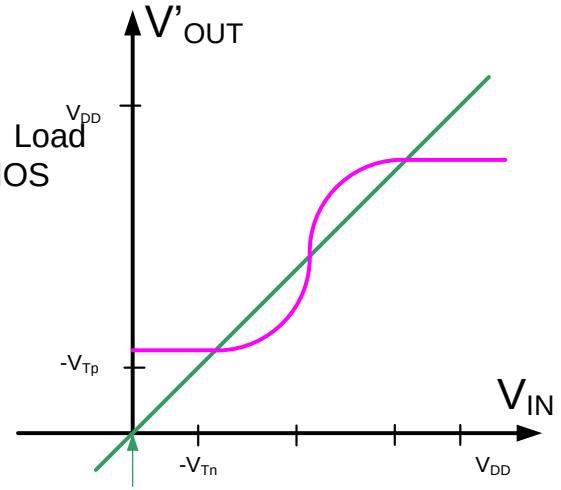


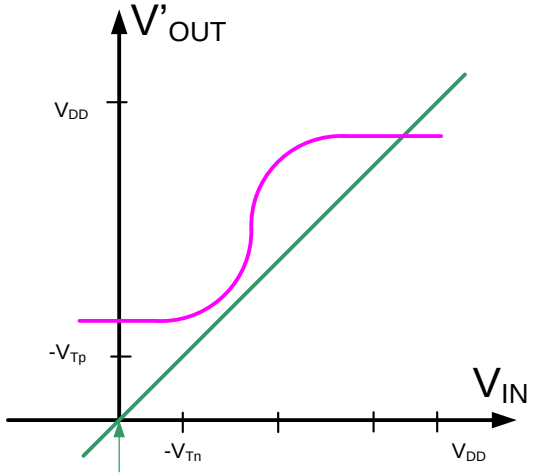
- **Reduced V_H-V_L**
- **Device sizing critical for even basic operation**
- **Shallow slope at V_{TRIP}**

Other CMOS/MOS Logic Families



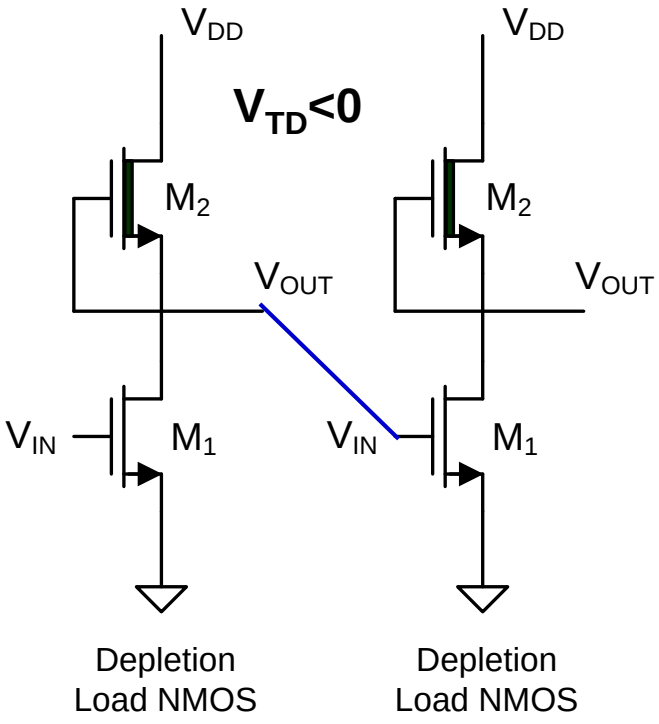


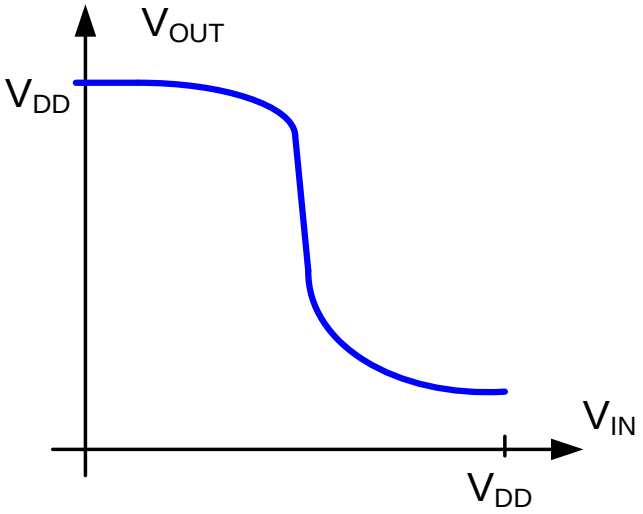


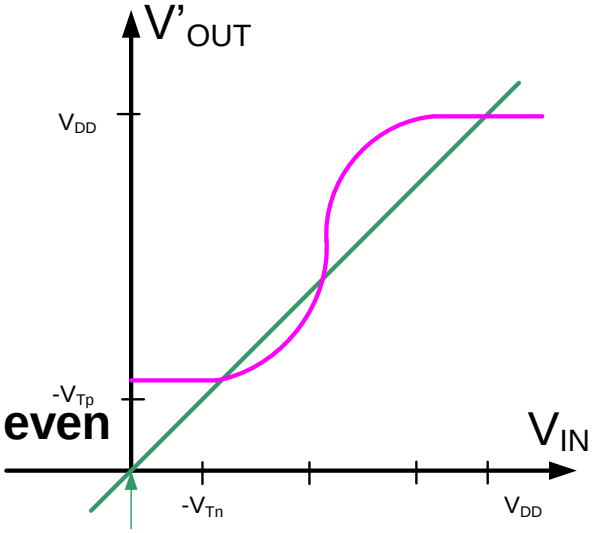


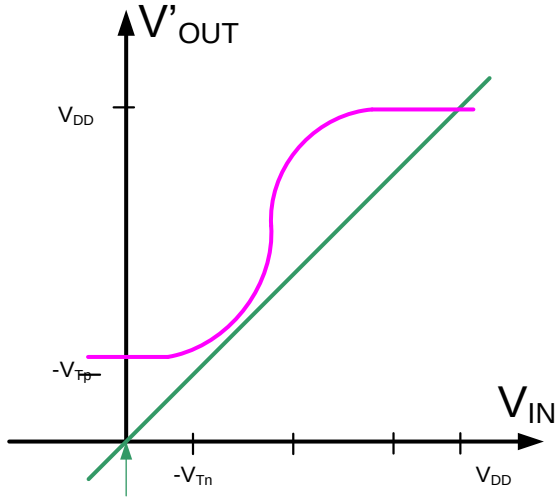
- **Reduced V_H-V_L**
- **Device sizing critical for even basic operation (DOF)**
- **Shallow slope at V_{TRIP}**

Other CMOS/MOS Logic Families









- **Reduced V_H-V_L**
- **Device sizing critical for even basic operation**
- **Shallow slope at V_{TRIP}**

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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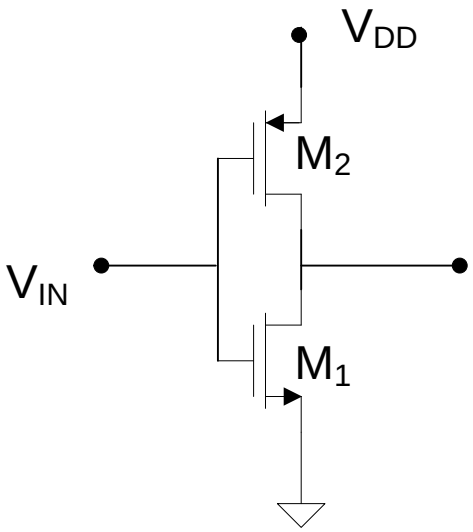
done

partial

Static Power Dissipation in Static CMOS Family

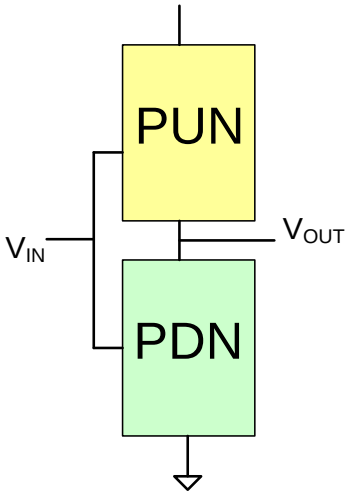


When V_{IN} is Low and V_{OUT} is High, M1 is off and I_{D1}=0

When V_{IN} is High and V_{OUT} is Low, M2 is off and I_{D2}=0

Thus, P_{STATIC}=0

This is a key property of the static CMOS Logic Family ➔the major reason Static CMOS Logic is so dominant

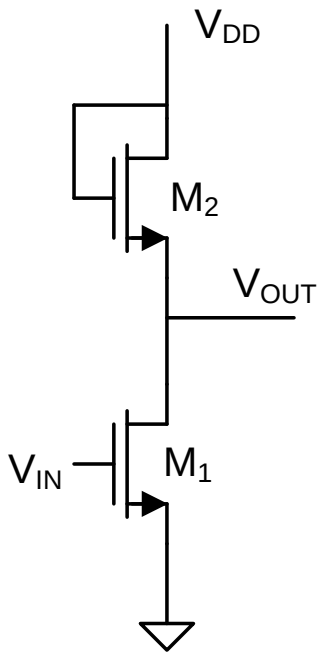


It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Compound Gate in CMOS Process

Static Power Dissipation in Ratio Logic Families

Example:



Enhancement Load NMOS

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L is close to V_{Tn}

Observe:

$V_H=V_{DD}-V_{Tn}$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

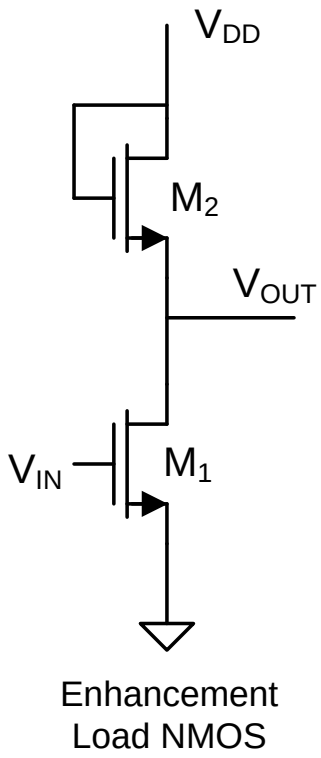
$$I_{D1}=\frac{\mu C_{OX} W_1}{L_1}\left(V_{GS1}-V_T-\frac{V_{DS1}}{2}\right)V_{DS1}$$

$$I_{D1}=10^{-4}\left(5-1-1-\frac{1}{2}\right)\bullet 1=0.25\text{mA}$$

P_L=(5V)(0.25mA)=1.25mW

Static Power Dissipation in Ratio Logic Families

Example:



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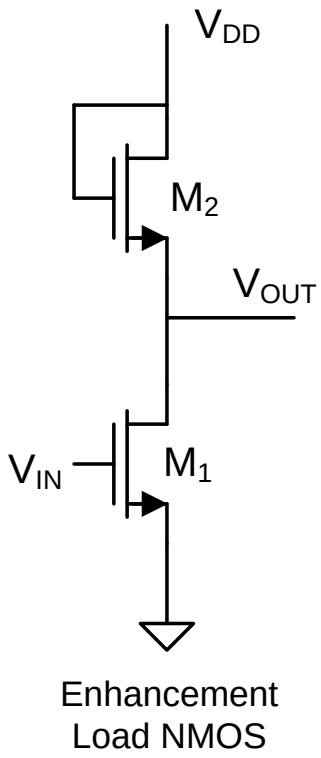
P_L=(5V)(0.25mA)=1.25mW

If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

Static Power Dissipation in Ratio Logic Families

Example:



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P_L=(5V)(0.25mA)=1.25mW

If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2}10^5 \bullet 1.25mW = \mathbf{62.5W}$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today

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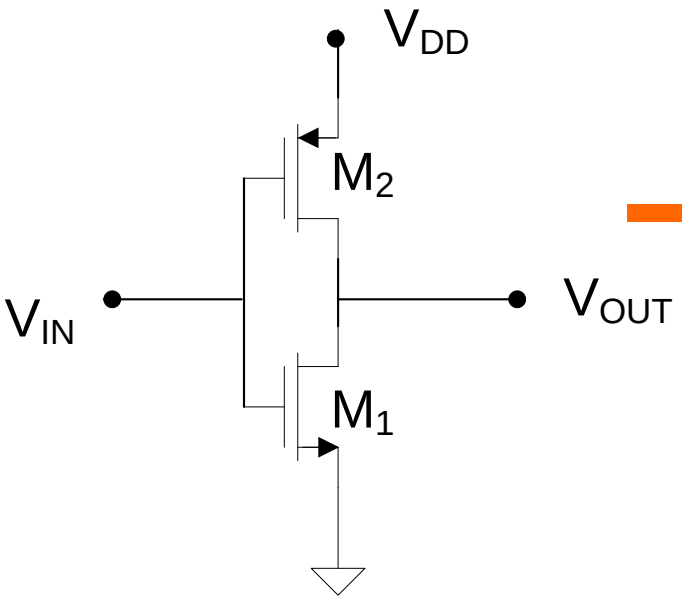
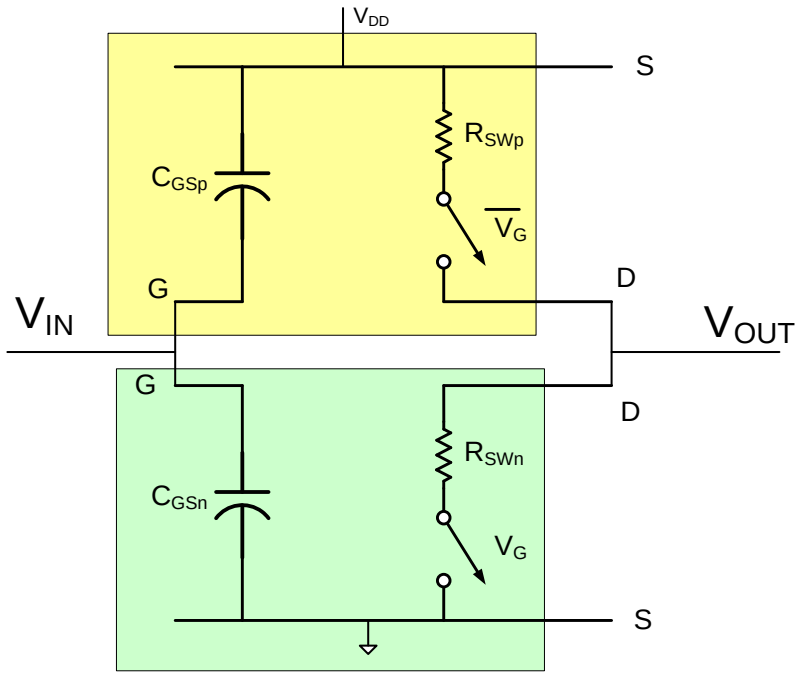
done

partial

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

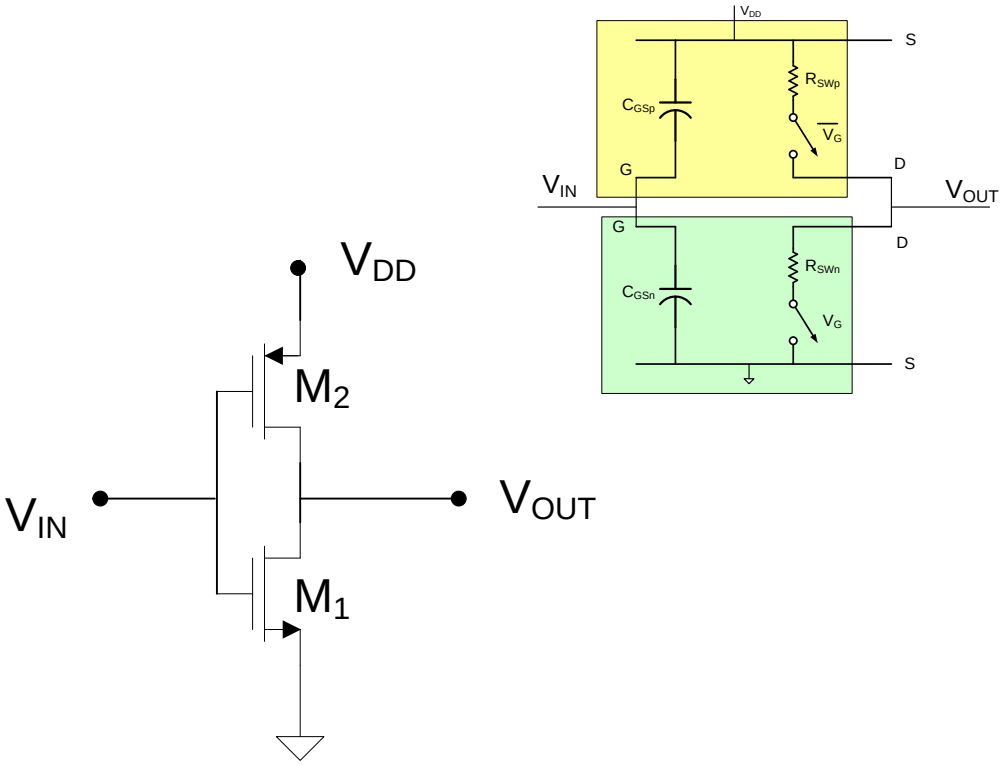


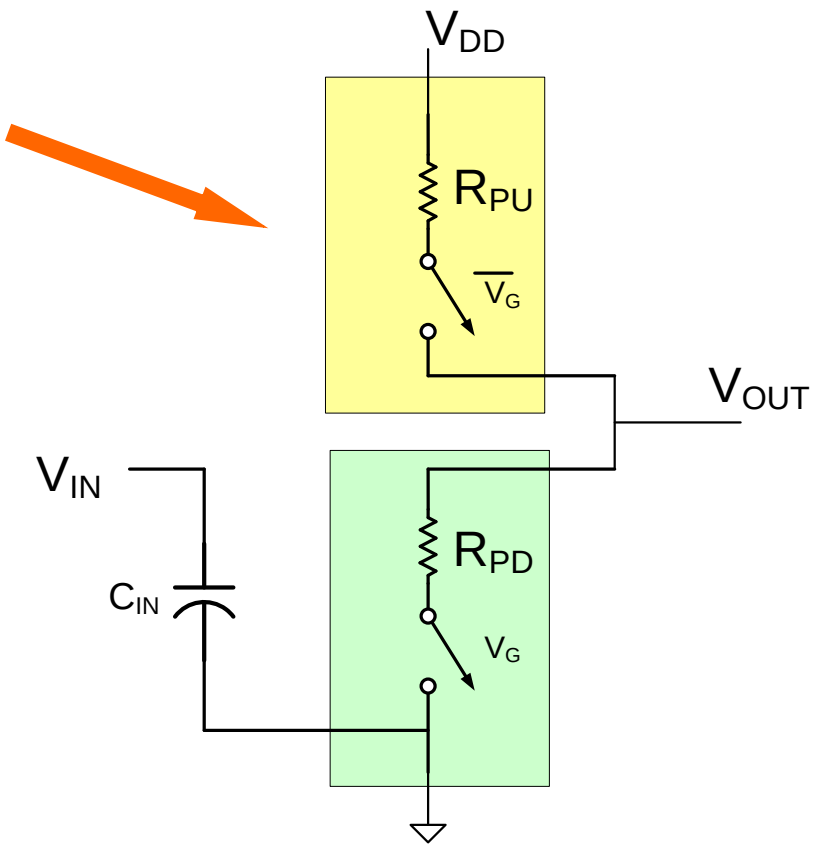


Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

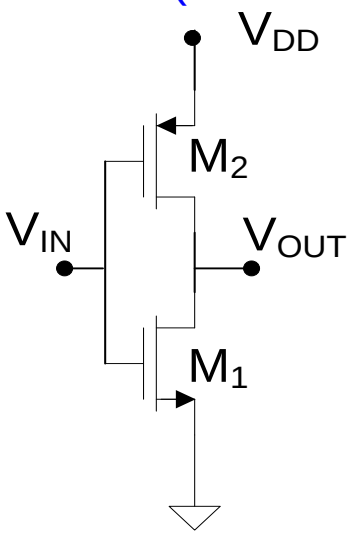


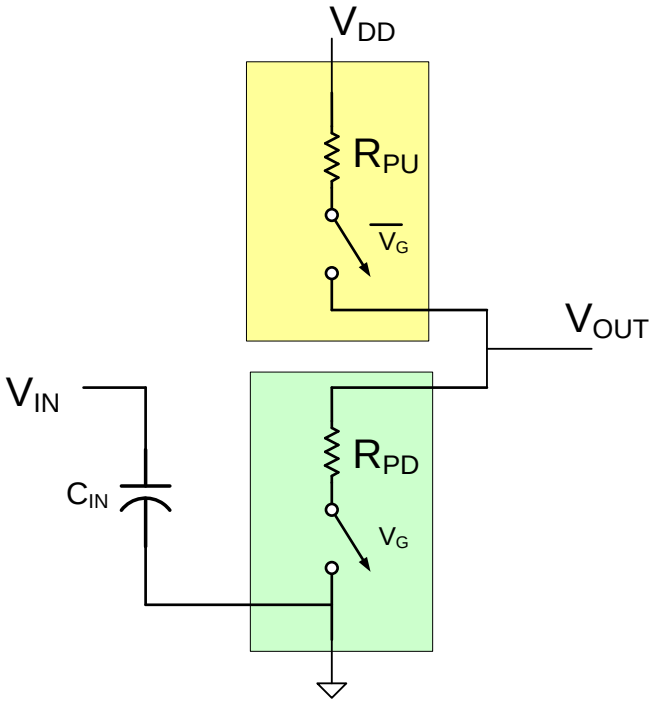


Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

(Review from earlier discussions)





Since operating in triode through most of transition:

$$I_D \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}(V_{GS} - V_T)V_{DS}$$

$$R_{PD} = \frac{V_{DS}}{I_D} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

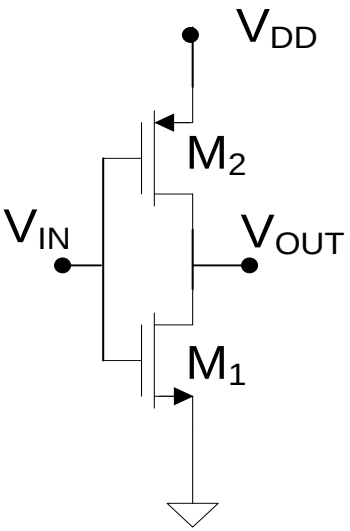
$$I_D = \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}(V_{GS} - V_T)V_{DS}$$

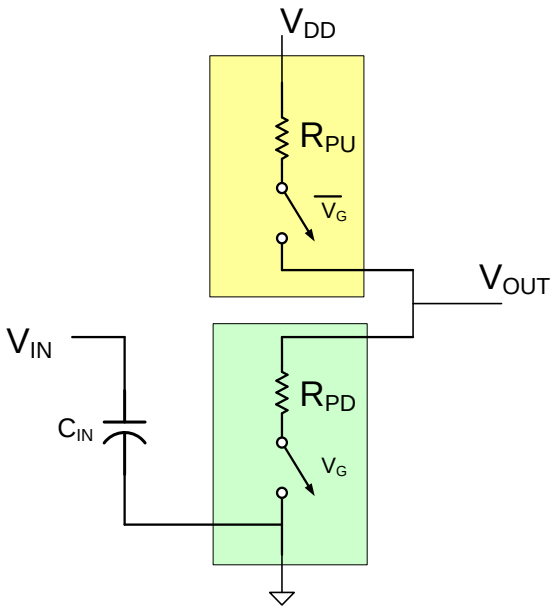
$$R_{PU} = \frac{V_{DS}}{I_D} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)





$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

Example: Minimum-sized M_1 and M_2

If $u_n C_{OX}$=100μAV^{-2}, C_{OX}=4 fFμ^{-2} , $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN}$, L_{MIN}=0.5μ and V_{DD}=5V

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

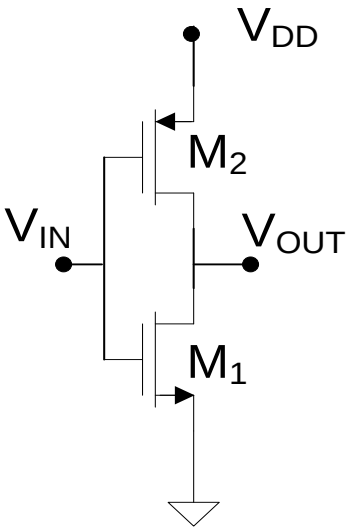
$$R_{PD} = \frac{1}{10^{-4} \bullet 0.8V_{DD}} = 2.5K\Omega$$

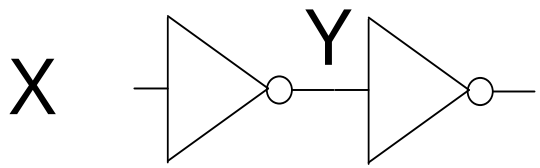
$$R_{PU} = \frac{1}{10^{-4} \bullet \frac{1}{3} \bullet 0.8V_{DD}} = 7.5K\Omega$$

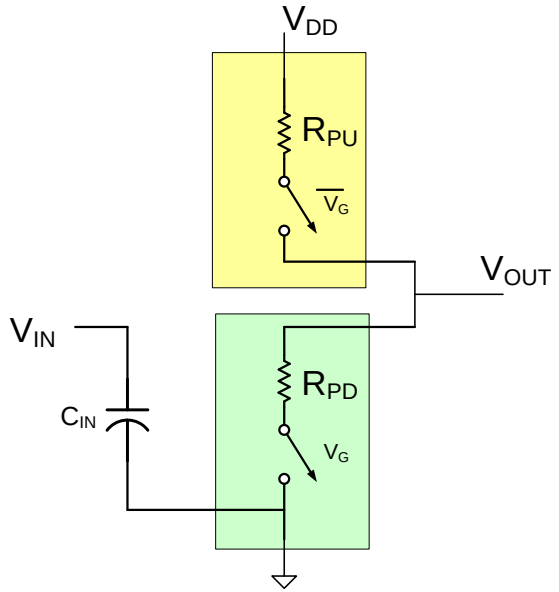
$$C_{IN} = 4 \bullet 10^{-15} \bullet 2L_{MIN}^2 = 2fF$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)







In typical process with Minimum-sized M_1 and M_2 :

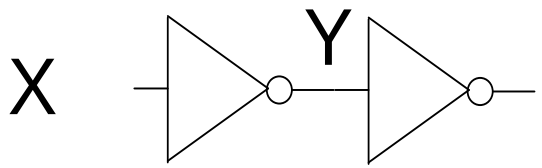
$$R_{PD} \cong 2.5K\Omega$$

$$R_{PU} \cong 3R_{PD} = 7.5K\Omega$$

$$C_{IN} \cong 2fF$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)



In typical process with Minimum-sized M_1 and M_2 :

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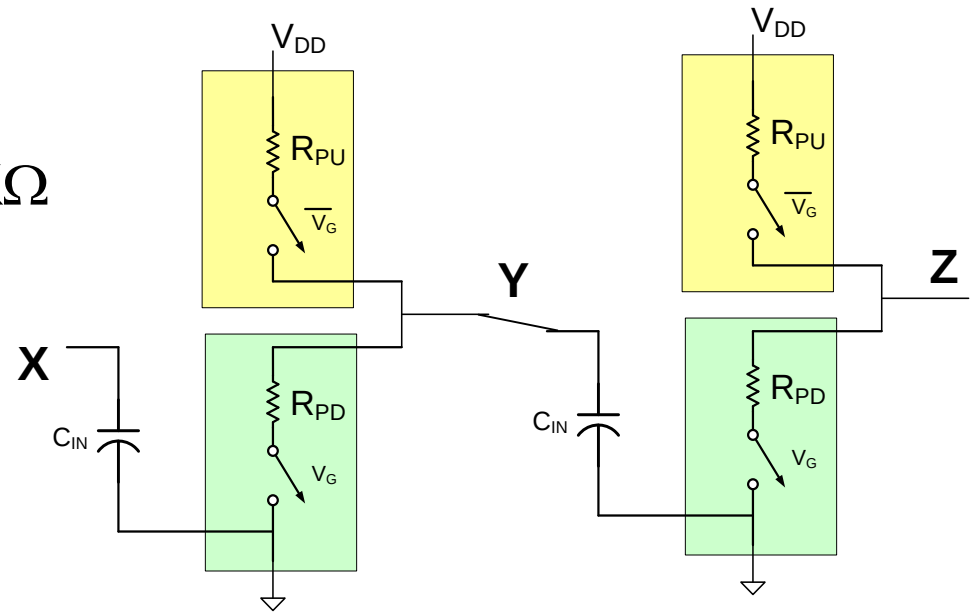
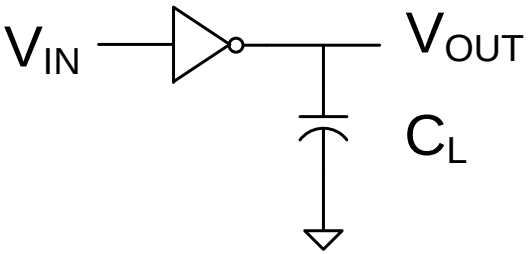


How long does it take for a signal to propagate from x to y?

Propagation Delay in Static CMOS Family

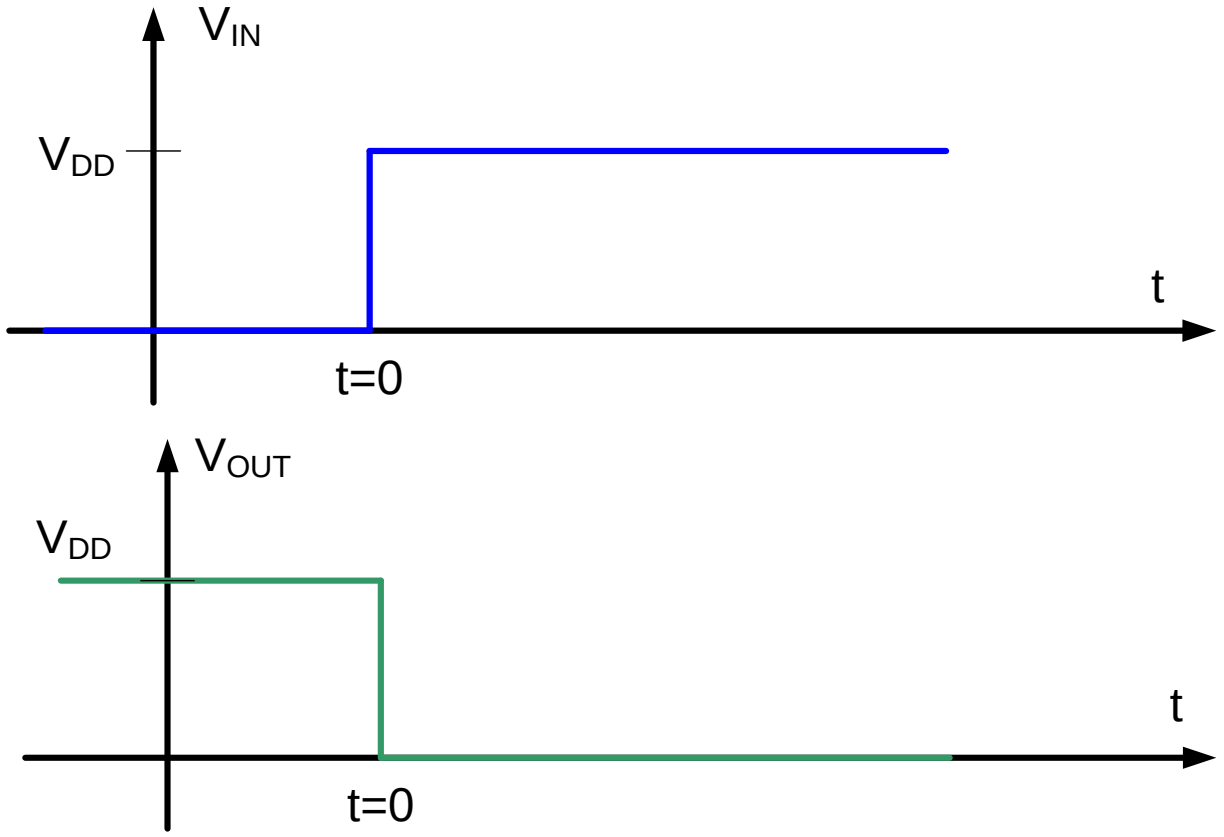
(Review from earlier discussions)

Consider:



For HL output transition, C_L charged to V_{DD}

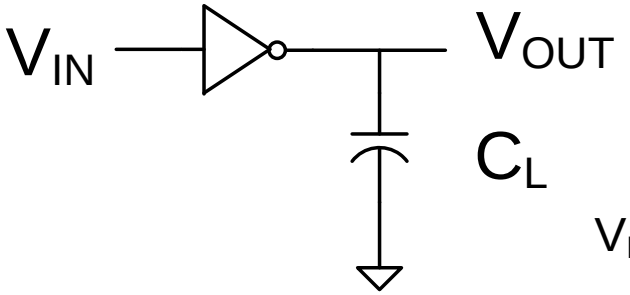
Ideally:



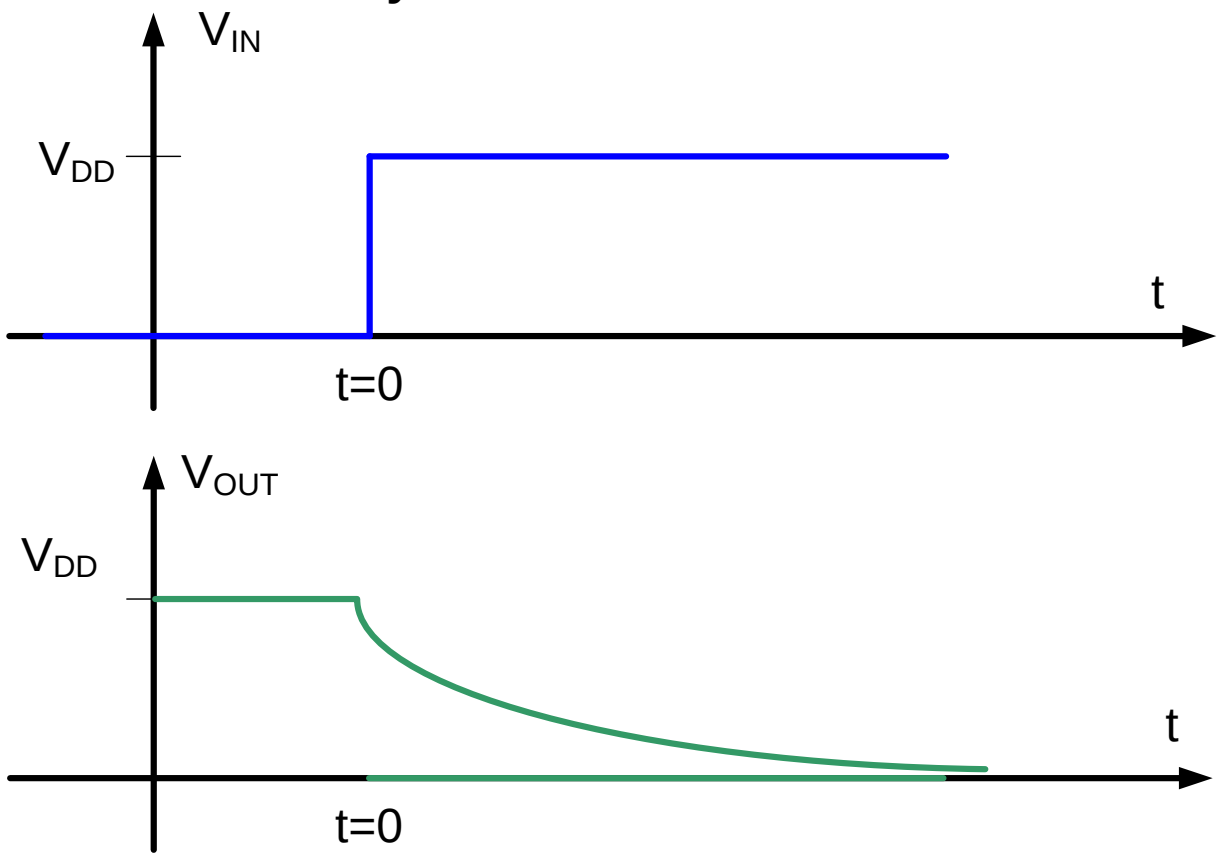
Propagation Delay in Static CMOS Family

(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}



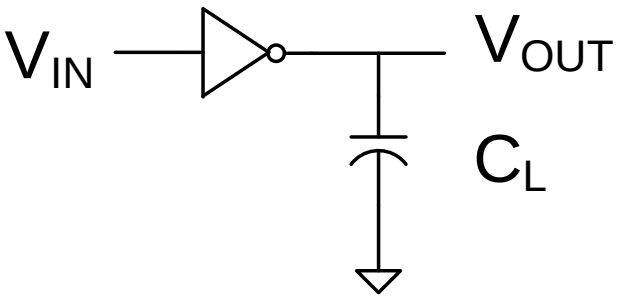
Actually:

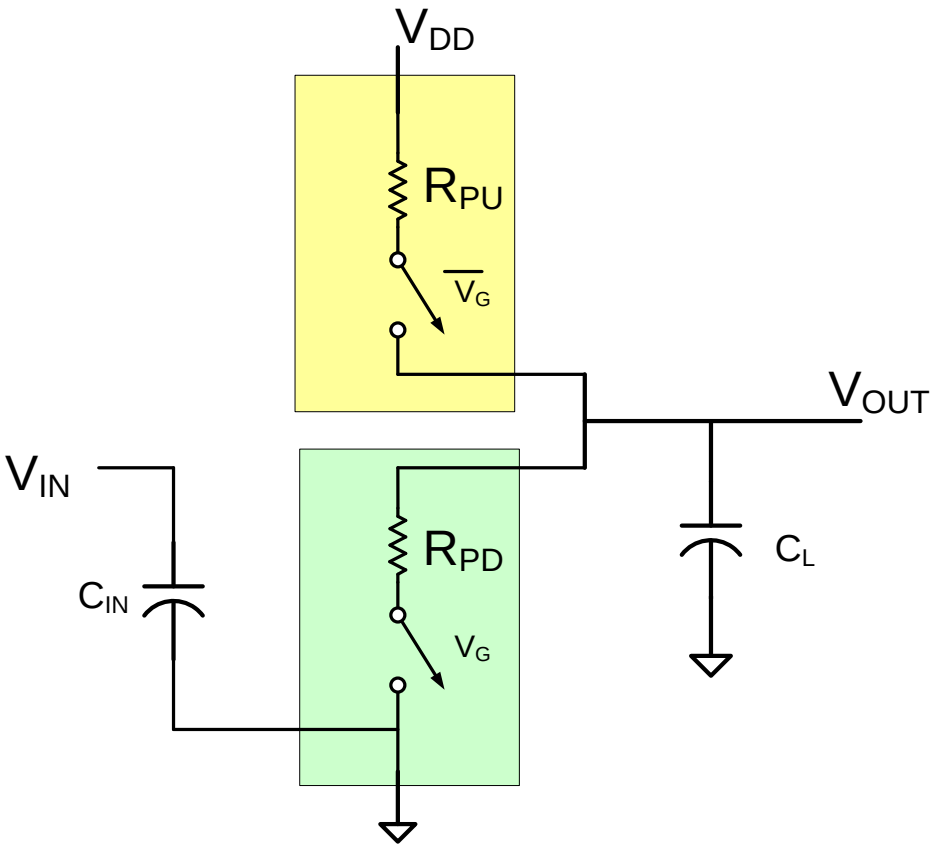


What is the transition time t_{HL} ?

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

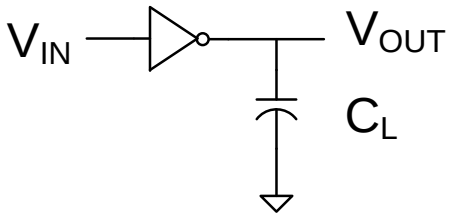


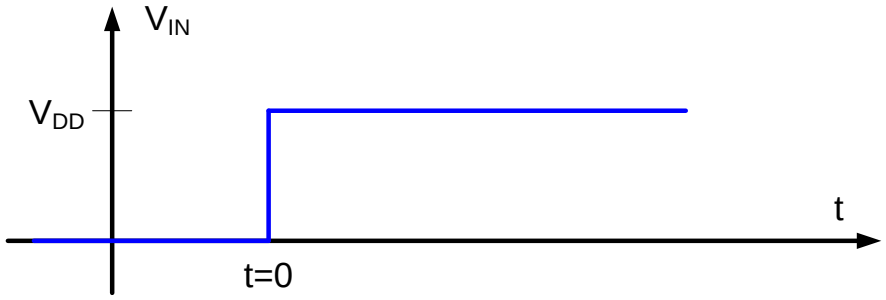


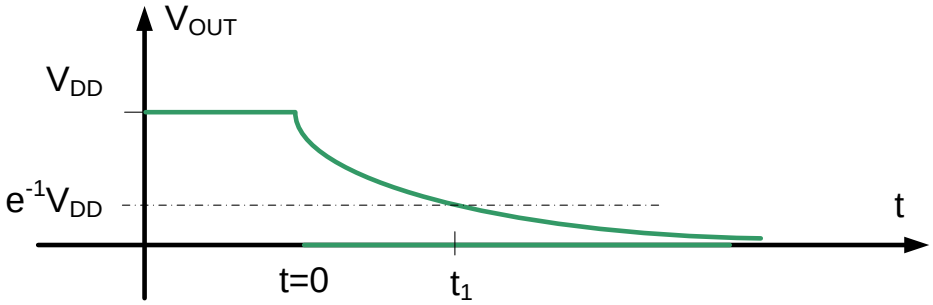
Propagation Delay in Static CMOS Family

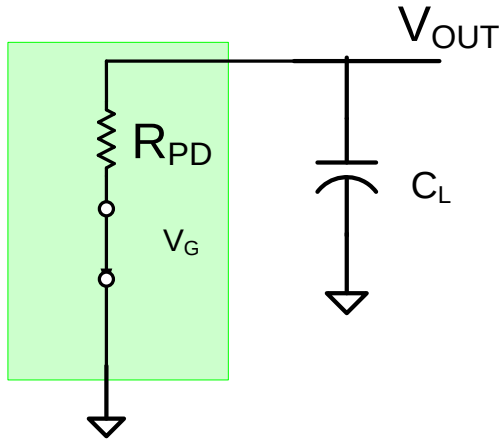
(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}









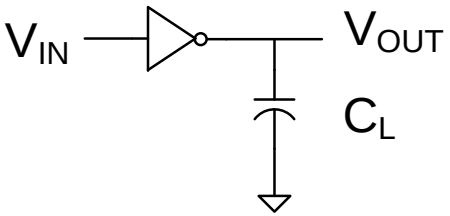
$$V_{OUT}(t) = F + (I - F)e^{\frac{-t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

$$\frac{V_{DD}}{e} = V_{DD}e^{-\frac{t_1}{R_{PD}C_L}} \quad \Rightarrow \quad t_1 = R_{PD}C_L$$

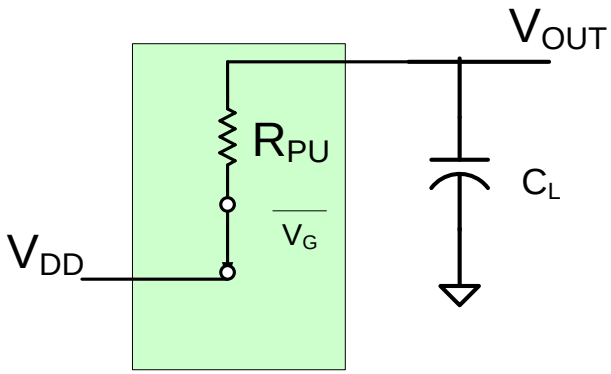
If V_{TRIP} is close to $V_{DD}/2$, t_{HL} is close to t_1

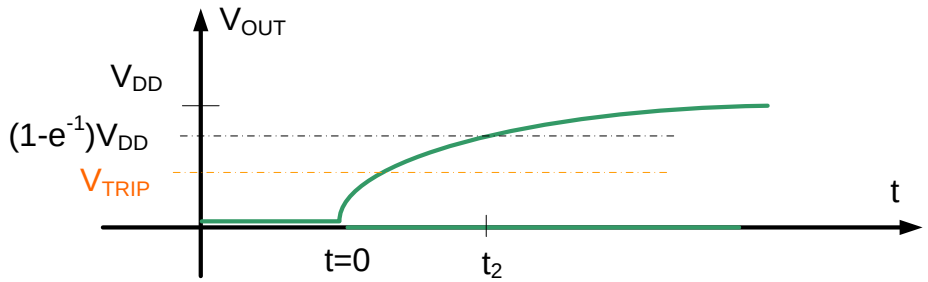
Propagation Delay in Static CMOS Family

(Review from earlier discussions)



For HL output transition, C_L charged to V_{DD}





$$t_{LH} \cong t_2 = R_{PU}C_L$$

Summary:

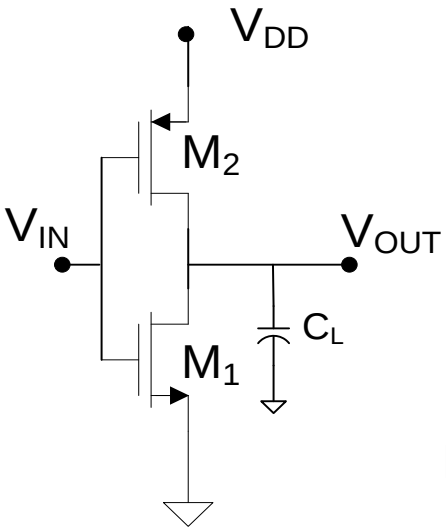
$$t_{LH} \cong R_{PU}C_L$$

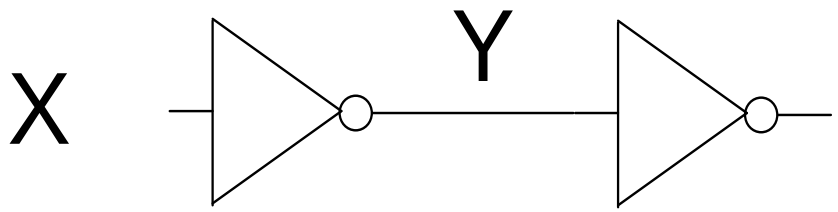
$$t_{HL} \cong R_{PD}C_L$$

For V_{TRIP} close to $V_{DD}/2$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)





In typical process with Minimum-sized M_1 and M_2 :

$$t_{HL} \cong R_{PD}C_L \cong 2.5K \bullet 2fF = 5ps$$

$$t_{LH} \cong R_{PU}C_L \cong 7.5K \bullet 2fF = 15ps$$

(Note: This C_{ox} is somewhat larger than that in the 0.5u ON process)

Note: LH transition is much slower than HL transition

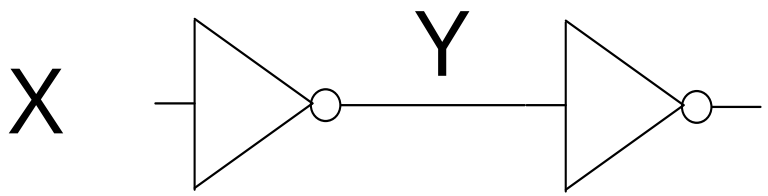
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of t_{HL} and t_{LH}, that is, $t_{PROP}=t_{HL}+t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L \left(R_{PU} + R_{PD} \right)$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked

For basic two-inverter cascade in static 0.5um CMOS logic



$$t_{PROP} = t_{HL} + t_{LH} \cong 20\,p\,\text{sec}$$

Propagation Delay in Static CMOS Family

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L\left(R_{PU} + R_{PD}\right)$$

$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 \left(V_{DD} - V_{Tn}\right)} \qquad R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 \left(V_{DD} + V_{Tp}\right)} \qquad C_{IN} = C_{OX}\left(W_1 L_1 + W_2 L_2\right)$$

If $V_{Tn} = -V_{Tp} = V_T$

$$t_{PROP} = C_{OX}(W_1 L_1 + W_2 L_2)\left(\frac{L_1}{m_n C_{OX} W_1 (V_{DD} - V_T)} + \frac{L_2}{m_p C_{OX} W_2 (V_{DD} - V_T)}\right)$$

If $L_2 = L_1 = L_{\min}$, $m_n = 3m_p$,

$$t_{PROP} = \frac{L_{\min}^2}{m_n (V_{DD} - V_T)}(W_1 + W_2)\left(\frac{1}{W_1} + \frac{3}{W_2}\right) = \frac{L_{\min}^2}{m_n (V_{DD} - V_T)}\left(4 + \frac{W_2}{W_1} + 3\frac{W_1}{W_2}\right)$$

For min size: $W_2 = W_1 = W_{\min}$

$$t_{PROP} = \frac{8L_{\min}^2}{m_n (V_{DD} - V_T)}$$

For equal rise/fall: $W_2 = 3W_1$

$$t_{PROP} = \frac{8L_{\min}^2}{m_n (V_{DD} - V_T)}$$

For min delay: $W_2 = \sqrt{3}W_1$ $\qquad \left(4 + 2\sqrt{3}\right) \cong 7.5$

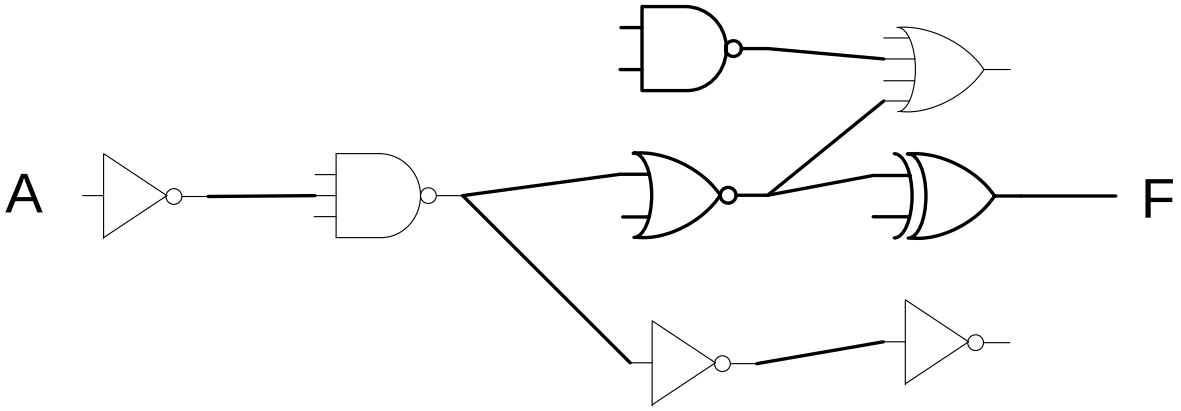
$$t_{PROP} = \frac{(4 + 2\sqrt{3})L_{\min}^2}{m_n (V_{DD} - V_T)}$$

Approximate BSIM values

process	Lmin	u	VT	VDD	Wmin
500	600	34	0.7	5	900
180	180	35	0.4	1.8	180
130	130	59	0.33	1.3	130
90	100	55	0.26	1.1	100
65	65	49	0.22	1	65
45	45	44	0.22	0.9	45

For min L transistors, mobility will saturate as field strength reaches a certain level.

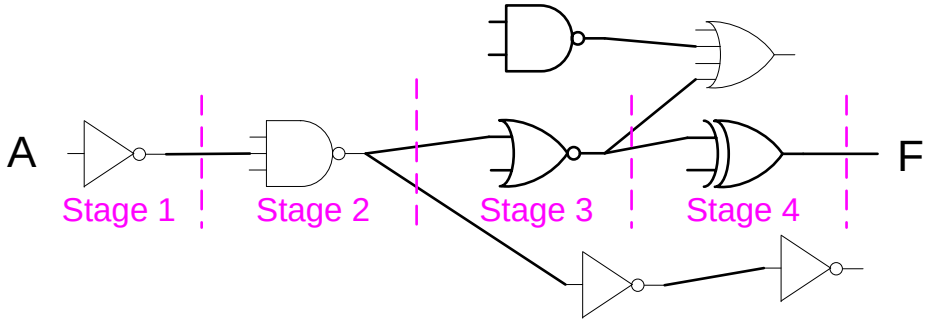
Propagation Delay in Static CMOS Family



The propagation delay through k levels of logic is approximately the sum of the individual delays in the same path

Propagation Delay in Static CMOS Family

Example:



$$t_{HL}=t_{HL4}+t_{LH3}+t_{HL2}+t_{LH1}$$

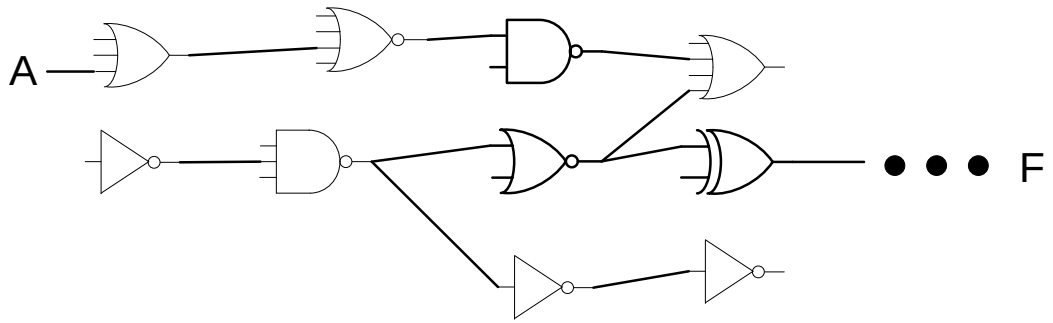
$$t_{LH}=t_{LH4}+t_{HL3}+t_{LH2}+t_{HL1}$$

$$t_{PROP}=t_{LH}+t_{HL}=(t_{LH4}+t_{HL3}+t_{LH2}+t_{HL1})+(t_{HL4}+t_{LH3}+t_{HL2}+t_{LH1})$$

$$t_{PROP}=t_{LH}+t_{HL}=(t_{LH4}+t_{HL4})+(t_{LH3}+t_{HL3})+(t_{LH2}+t_{HL2})+(t_{LH1}+t_{HL1})$$

$$t_{PROP}=t_{PROP4}+t_{PROP3}+t_{PROP2}+t_{PROP1}$$

Propagation Delay in Static CMOS Family



Propagation through k levels of logic

$$t_{HL} \cong t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \bullet\bullet\bullet + t_{XY1}$$

$$t_{LH} \cong t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \bullet\bullet\bullet + t_{YX1}$$

where x=H and Y=L if k odd and X=L and Y=h if k even

$$t_{PROP} = \sum_{i=1}^{k} t_{PROPk}$$

Will return to propagation delay after we discuss device sizing

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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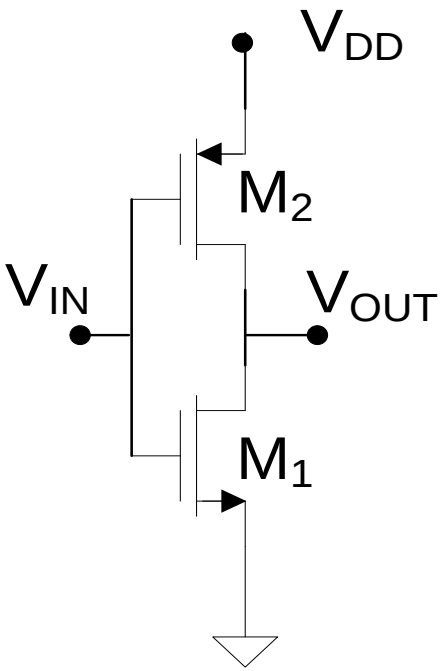
done

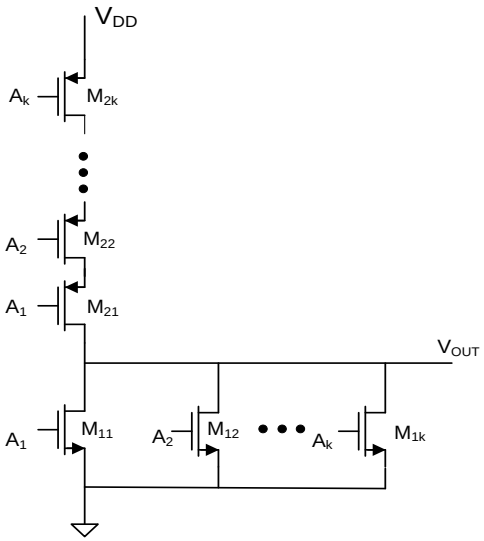
partial

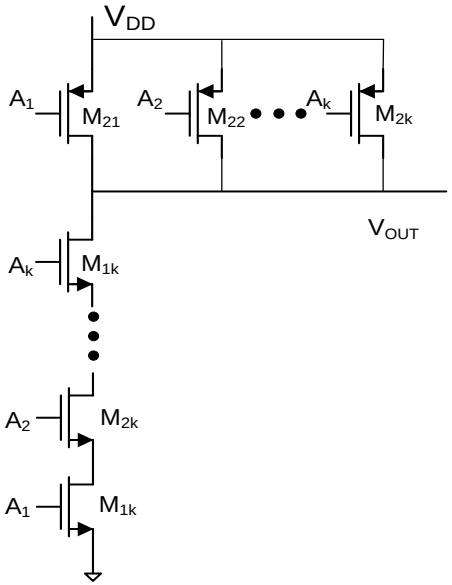
Question:

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes ?

Device Sizing





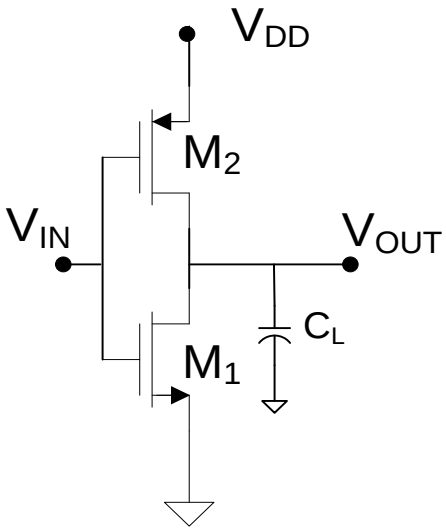


Strategies?

Degrees of Freedom?

Will consider the inverter first

Device Sizing

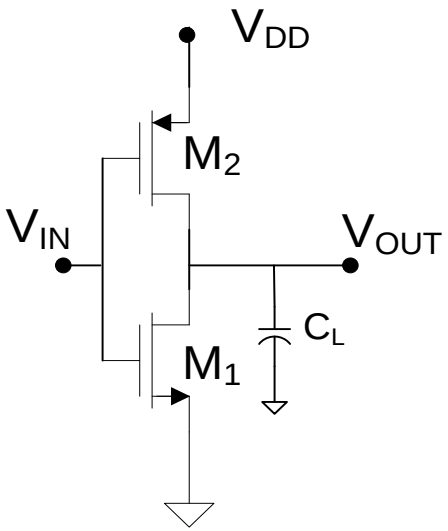


Degrees of Freedom?

Strategies?

Device Sizing

- **Since not ratio logic, V_H and V_L are independent of device sizes for this inverter**
- **With $L_1=L_2=L_{min}$, there are 2 degrees of freedom (W_1 and W_2)**



Sizing Strategies

- **Minimum Size**
- **Fixed V_{TRIP}**
- **Equal rise-fall times (equal worst-case rise and fall times)**
- **Minimum power dissipation**
- **Minimum time required to drive a given load**
- **Minimum input capacitance**

End of Lecture 39