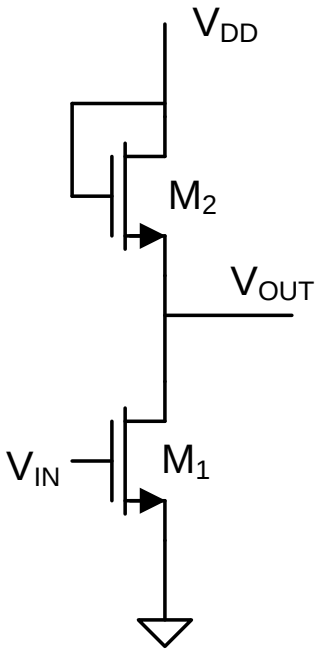
EE 330
Lecture 41

Digital Circuits

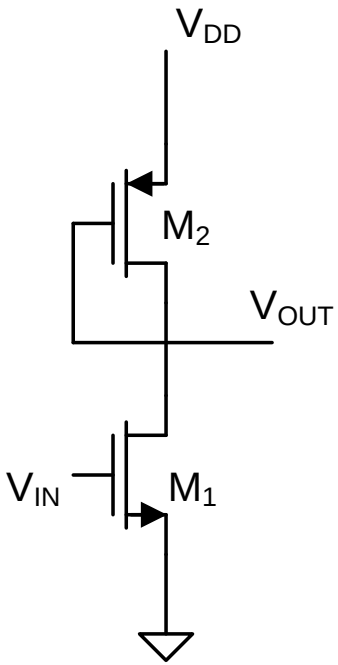
- The Reference Inverter
- Propagation Delay – basic characterization
- Device Sizing (Inverter and multiple-input gates)
- Propagation Delay with Multiple Levels of Logic

Review from last lecture

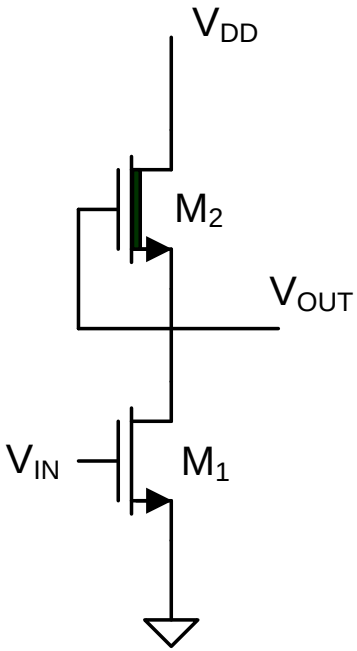
Other MOS Logic Families



Enhancement
Load NMOS



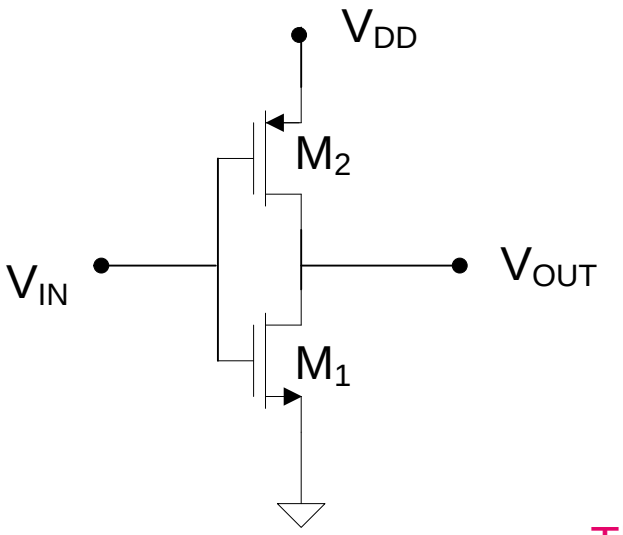
Enhancement Load
Pseudo-NMOS



Depletion
Load NMOS

Review from last lecture

Static Power Dissipation in Static CMOS Family

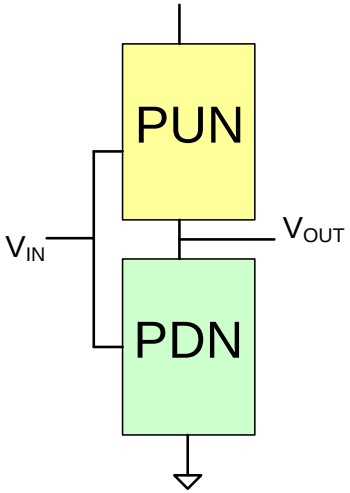


When V_{OUT} is Low, $I_{D1}=0$

When V_{OUT} is High, $I_{D2}=0$

Thus, $P_{STATIC}=0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant



Compound Gate in CMOS Process

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Review from last lecture

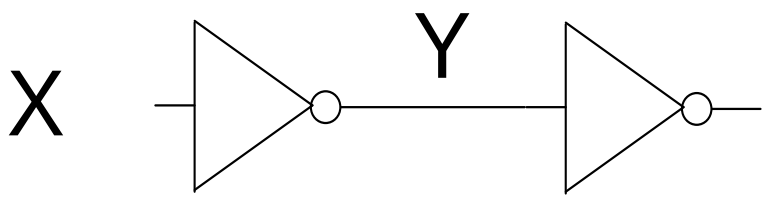
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of t_{HL} and t_{LH}, that is, $t_{PROP}=t_{HL}+t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L \left(R_{PU} + R_{PD} \right)$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked

For basic two-inverter cascade in static CMOS logic

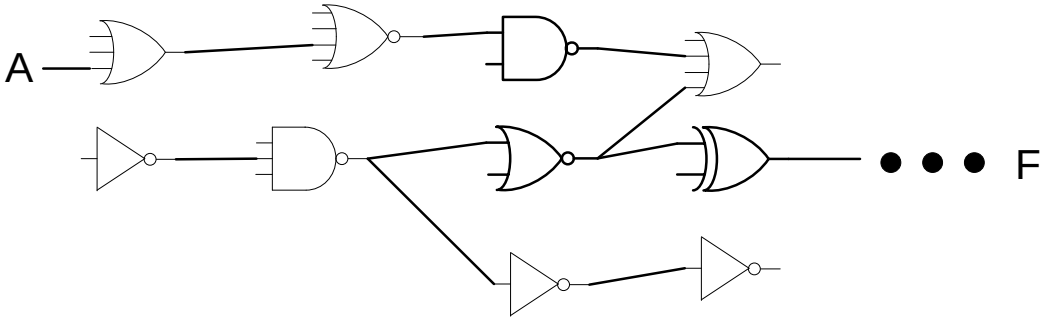


In typical process with minimum-sized M_1 and M_2 :

$$t_{PROP} = t_{HL} + t_{LH} \cong 20\,p\,\text{sec}$$

Review from last lecture

Propagation Delay in Static CMOS Family



Propagation through k levels of logic

$$t_{HL} \cong t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \bullet\bullet\bullet + t_{XY1}$$

$$t_{LH} \cong t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \bullet\bullet\bullet + t_{YX1}$$

where x=H and Y=L if k odd and X=L and Y=h if k even

$$t_{PROP} = \sum_{i=1}^{k} t_{PROPk}$$

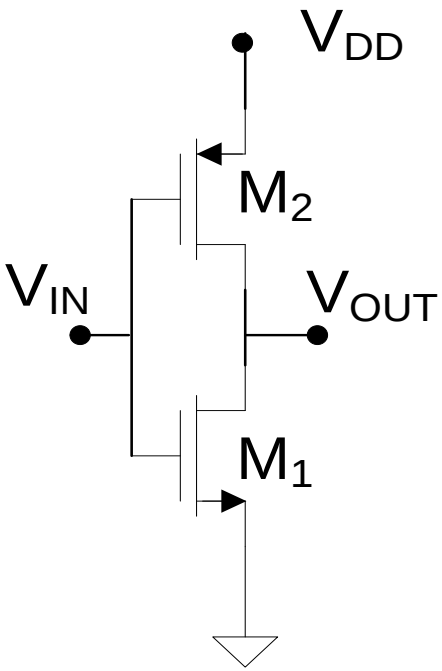
Will return to propagation delay after we discuss device sizing

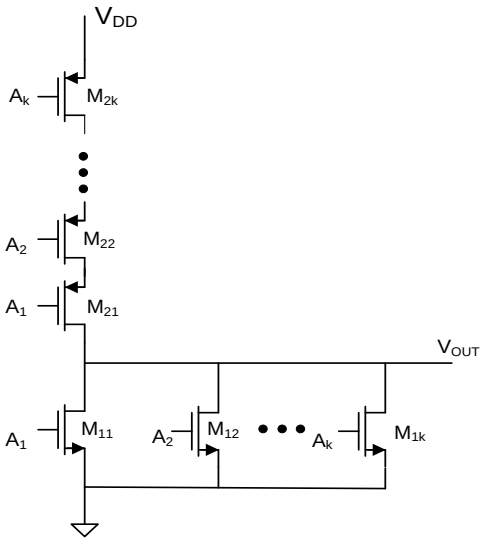
Question:

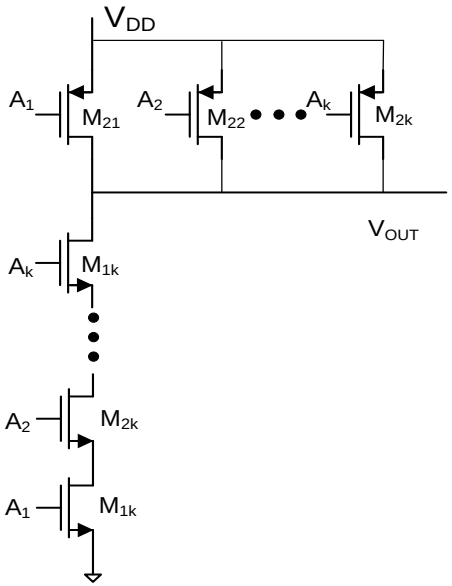
Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes ?

Review from last lecture

Device Sizing







Strategies?

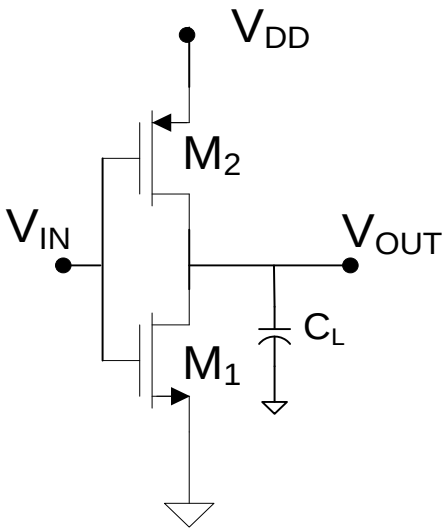
Degrees of Freedom?

Will consider the inverter first

Review from last lecture

Device Sizing

- **Since not ratio logic, V_H and V_L are independent of device sizes for this inverter**
- **With $L_1=L_2=L_{min}$, there are 2 degrees of freedom (W_1 and W_2)**



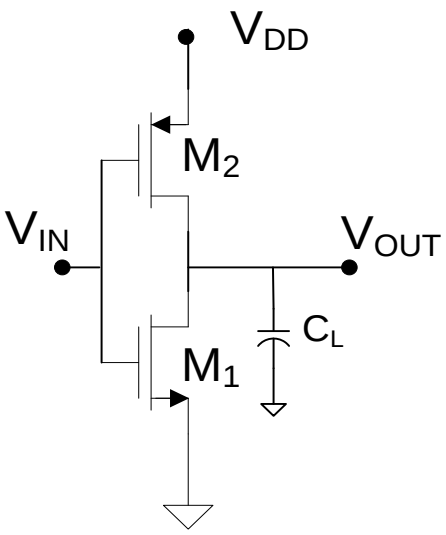
Sizing Strategies

- **Minimum Size**
- **Fixed V_{TRIP}**
- **Equal rise-fall times (equal worst-case rise and fall times)**
- **Minimum power dissipation**
- **Minimum time required to drive a given load**
- **Minimum input capacitance**

Review from last lecture

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$



Sizing Strategy Summary

	Minimum Size	$V_{TRIP}=V_{DD}/2$	Equal Rise/Fall
Size	$W_n=W_p=W_{min}$ $L_p=L_n=L_{min}$	$W_n=W_{min}$ $W_{p=}3W_{min}$ $L_p=L_n=L_{min}$	$W_n=W_{min}$ $W_{p=}3W_{min}$ $L_p=L_n=L_{min}$
t_{HL}	$R_{pd}C_L$	$R_{pd}C_L$	$R_{pd}C_L$
t_{LH}	$3R_{pd}C_L$	$R_{pd}C_L$	$R_{pd}C_L$
t_{PROP}	$4R_{pd}C_L$	$2R_{pd}C_L$	$2R_{pd}C_L$
V_{trip}	$V_{TRIP}=0.42V_{DD}$	$V_{TRIP}=0.5V_{DD}$	$V_{TRIP}=0.5V_{DD}$

- **For a fixed load C_L, the minimum-sized structure has a higher t_{PROP} but if the load is another inverter, C_L will also change so the speed improvements become less apparent**
- **This will be investigated later**

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

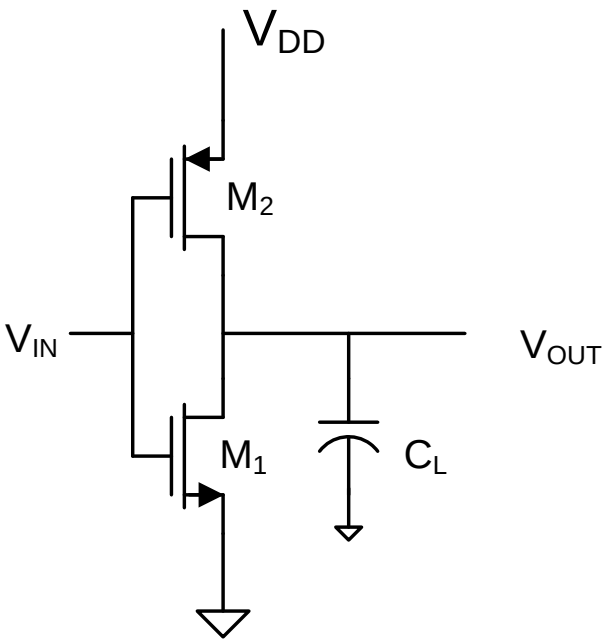
partial

Reference Inverter

The reference inverter

Assume $\mu_n/\mu_p=3$
$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_n$



$$C_{REF} \underset{def}{=} C_{INREF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$R_{PUREF} = \frac{L_{MIN}}{\mu_p C_{OX} 3W_{MIN}\left(V_{DD}+V_{Tp}\right)} \overset{V_{Tp}=-.2V_{DD}}{=} R_{PDREF}$$

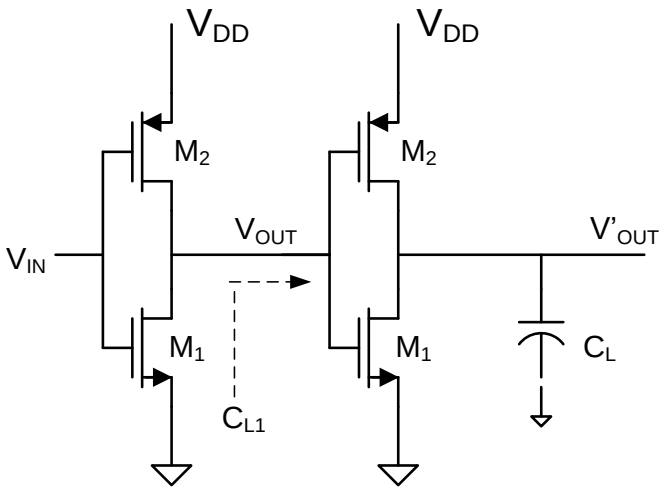
- **Have sized the reference inverter with $W_p/W_n=\mu_n/\mu_p$**
- **In standard processes, provides $V_{TRIP} \approx V_{DD}/2$ and $t_{HL} \approx t_{LH}$**
- **Any other sizing strategy could have been used for the reference inverter but this is most convenient**

Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p=3$
$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_n$



$$C_{L1} = C_{REF} = 4C_{OX} W_{MIN} L_{MIN}$$

$$t_{REF} \underset{def}{=} t_{PROPREF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}$$

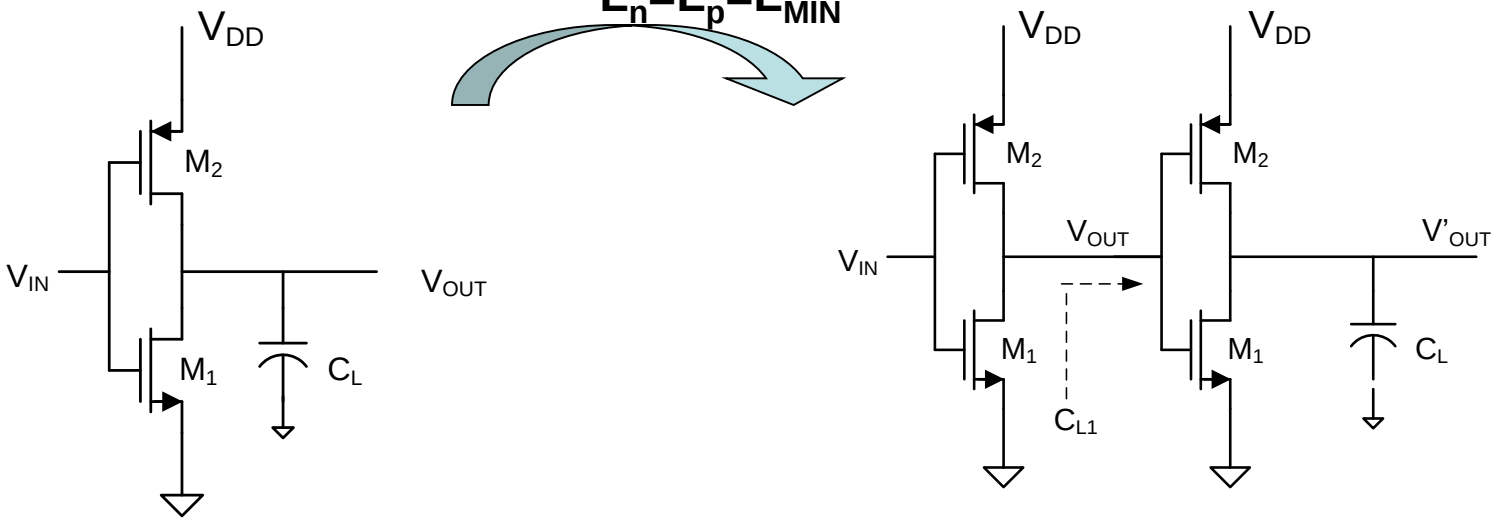
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_n$



Summary: parameters defined from reference inverter:

$$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

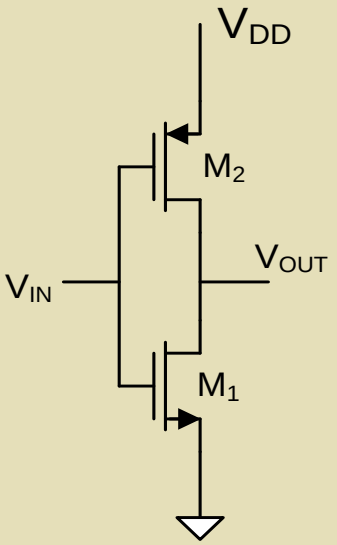
$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)}$$

$$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$t_{PROP} = t_{REF} = 2R_{PDREF}C_{REF}$$

The Reference Inverter

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, $R_{PDREF}=R_{PUREF}$=2.5K

$$R_{PDREF}=R_{PUREF}$$

$$\mathbf{C_{REF}=C_{IN}=4C_{OX}W_{MIN}L_{MIN}}$$

$$R_{PDREF}=\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$\mathbf{t_{HLREF}=t_{LHREF}=R_{PDREF}C_{REF}}$$

$$t_{PROP}=t_{REF}$$

$$\mathbf{t_{REF}=t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}}$$

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

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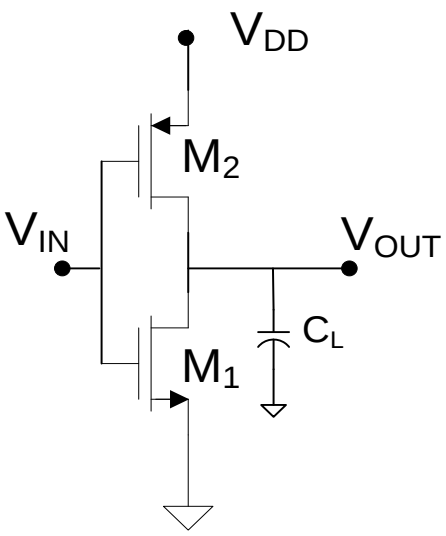
done

partial

Recall: Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$



Sizing Strategy Summary

	Minimum Size	$V_{TRIP}=V_{DD}/2$	Equal Rise/Fall
Size			
t_{HL}			
t_{LH}			
t_{PROP}	$4R_{pd}C_L$	$2R_{pd}C_L$	$2R_{pd}C_L$
V_{trip}	$V_{TRIP}=0.42V_{DD}$	$V_{TRIP}=0.5V_{DD}$	$V_{TRIP}=0.5V_{DD}$

Are the Equal Rise/Fall and the $V_{TRIP}=V_{DD}/2$ Really Twice as Fast as the Minimum Sizing Strategy?

Is this difference significant?

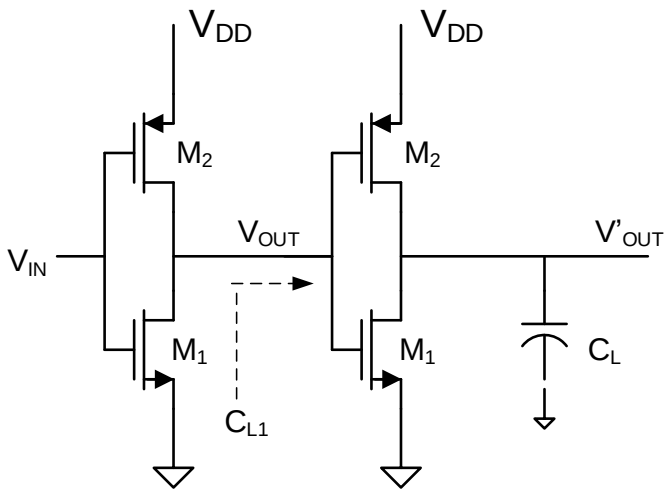
- **For a fixed load C_L, the minimum-sized structure has a higher t_{PROP} but if the load is another inverter, C_L will also change so the speed improvements become less apparent**
- **This will be investigated later**

Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

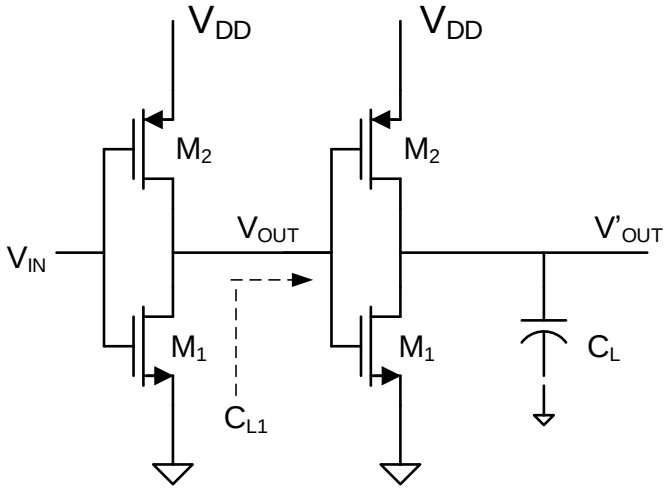
What loading condition should be considered when addressing this question?

- Fixed load C_L?
- Driving identical device?
- Does it make any difference?



Minimum Sized

$W_2=W_1=W_{MIN}$



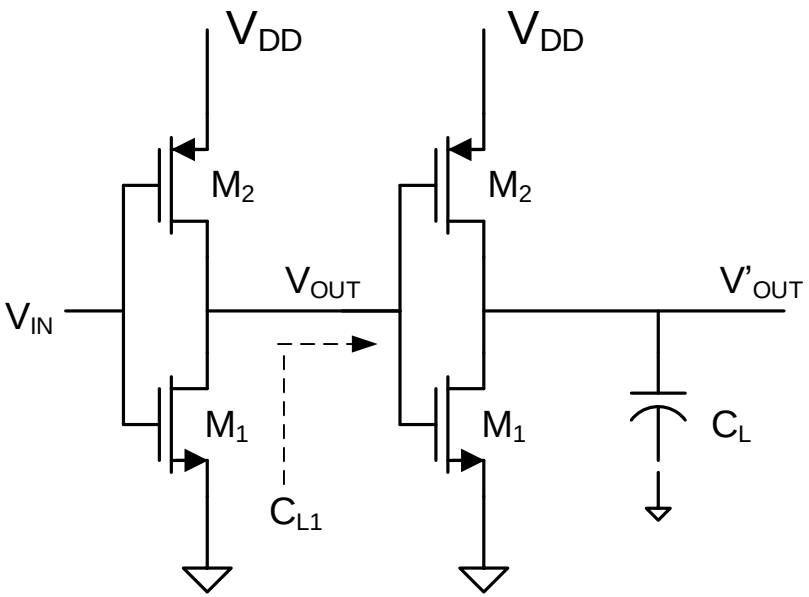
Reference Inverter (equal rise/fall)

$W_2=(\mu_n/\mu_p)W_1$, $W_1=W_{MIN}$

$t_{PROP} = t_{REF}$

Device Sizing

The minimum-sized inverter pair



Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$, $W_n=W_p=W_{MIN}$

Recall:

$$C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

$$R_{PDREF}=\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tm}\right)}$$

$$t_{PROP\_REF}=2R_{PDREF}C_{REF}$$

For minimum-sized inverter pair:

$$C_{L1}=2C_{OX}W_{MIN}L_{MIN}=0.5C_{REF}$$

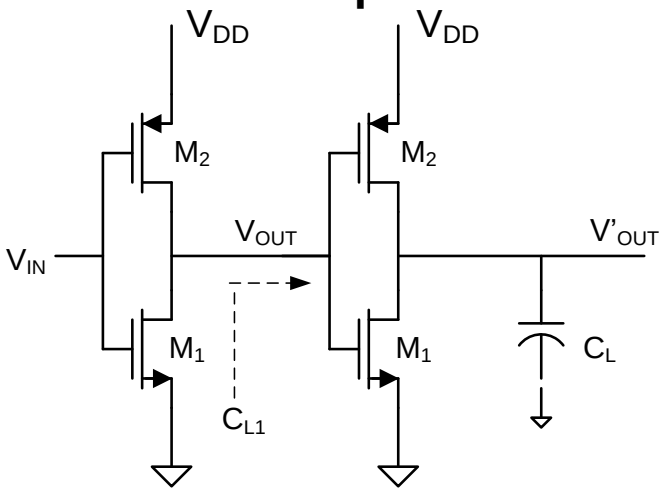
$$R_{PD}=R_{PDREF} \qquad R_{PU}=3R_{PD}=3R_{PDRF}$$

$$t_{PROP}=t_{HL}+t_{LH}=C_{L1}(R_{PDREF}+3R_{PDRF})=.5C_{REF}*4R_{PDREF}=2R_{PDREF}C_{REF}$$

$$t_{PROP}=t_{REF}$$

Propagation Delay

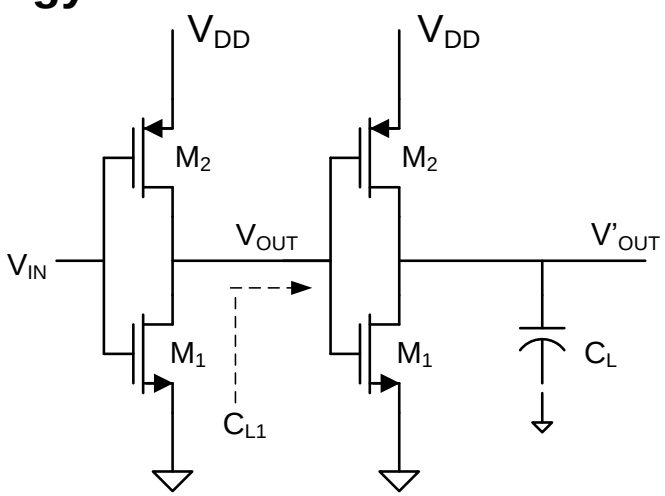
How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?



Minimum Sized

$W_2=W_1=W_{MIN}$

$t_{PROP} = t_{REF}$



Reference Inverter (equal rise/fall)

$W_2=(\mu_n/\mu_p)W_1$, $W_1=W_{MIN}$

$t_{PROP} = t_{REF}$

They are the same!

Even though the t_{LH} rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!

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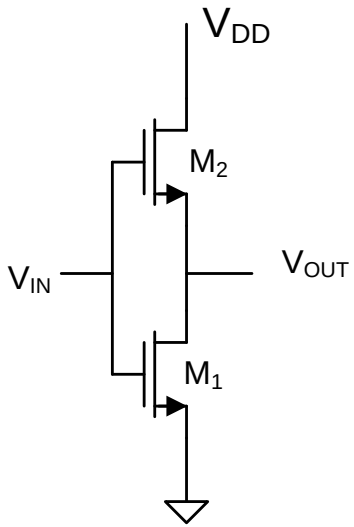
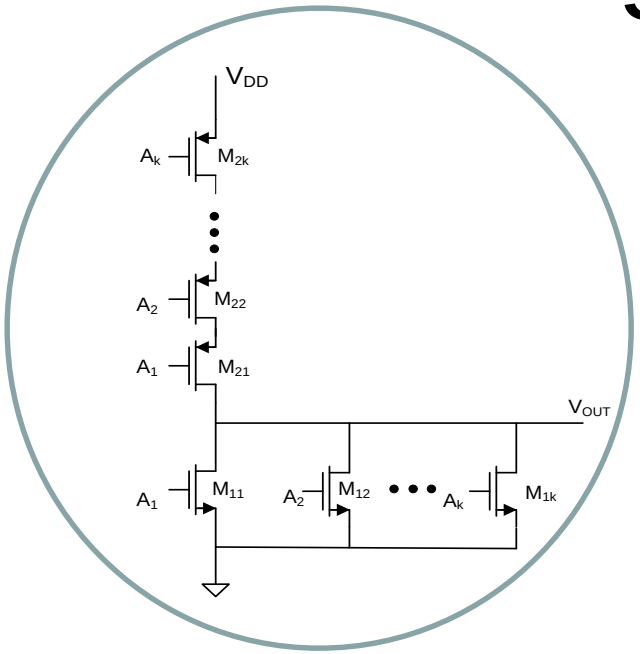
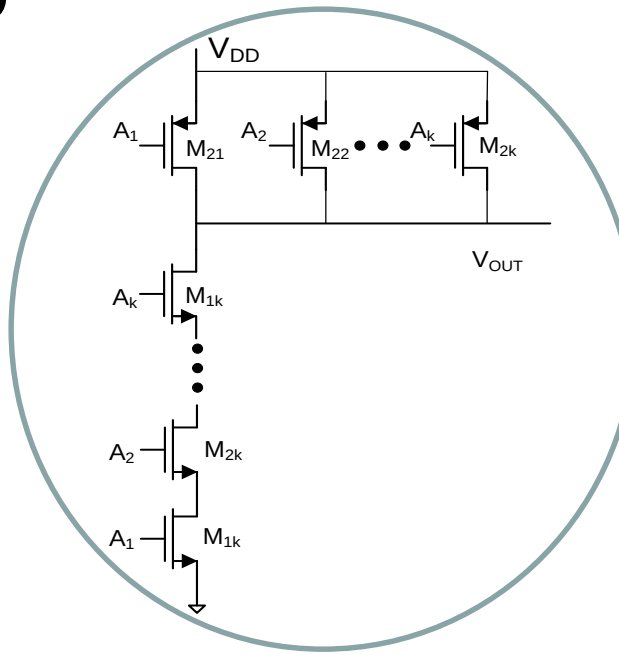
done

partial

Device Sizing







Will consider now the multiple-input gates

Will consider both minimum sizing and equal worst-case rise/fall

Will assume C_L (not shown)=C_{REF}

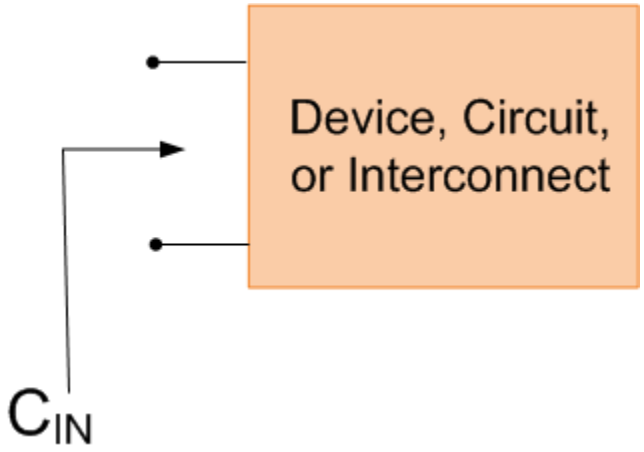
Will initially size so gate drive capability is same as that of ref inverter

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting

Fan In

- **The Fan In (FI) to an input of a gate device, circuit or interconnect that is capacitive is the input capacitance**

- **Often this is normalized to some capacitance (typically C_{REF} of ref inverter).**

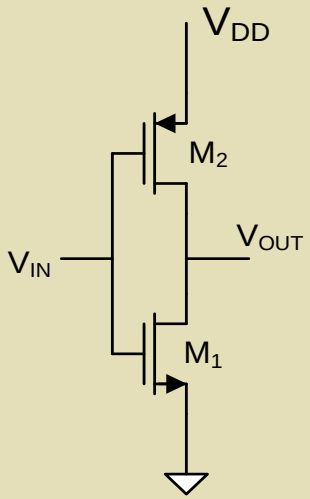


FI $= C_{IN}$ **alternately** **FI** $= \frac{C_{IN}}{C_{REF}}$

Sizing of Multiple-Input Gates

Analysis strategy : Express delays in terms of those of reference inverter

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

$$C_{IN}=C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

$FI_{REF}=C_{REF}$ **alternately** $FI_{REF}=\dfrac{C_{IN}}{C_{REF}}=1$

$$R_{PDREF}=R_{PUREF}=\frac{L_{MIN}}{\mu_n C_{OX}W_{MIN}\left(0.8V_{DD}\right)}$$

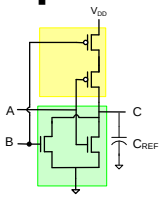
$$t_{HLREF}=t_{LHREF}=R_{PDREF}C_{REF}$$

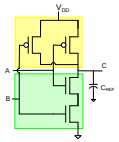
$$t_{REF}=t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}$$

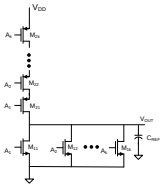
Device Sizing

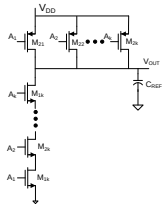
Multiple Input Gates:

2-input NOR **2-input NAND** **k-input NOR** **k-input NAND**









Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

W_n=?

W_p=?

Fastest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized (assume driving a load of C_{REF})

$W_n=W_{min}$

$W_p=W_{min}$

Fastest response (t_{HL} or t_{LH}) = ?

Slowest response (t_{HL} or t_{LH}) = ?

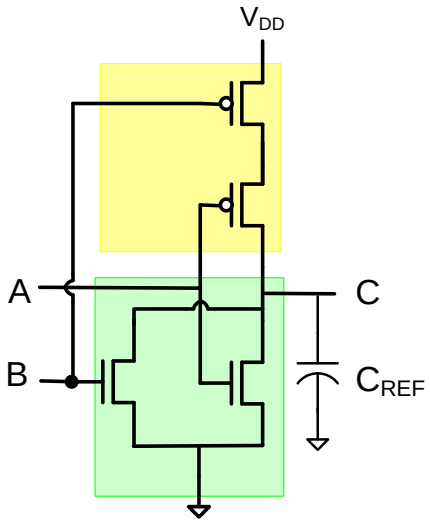
Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: 2-input NOR



(n-channel devices sized same, p-channel devices sized the same)

Assume $L_n=L_p=L_{min}$ and driving a load of C_{REF}

W_n=?

DERIVATIONS

W_p=?

Input capacitance = ?

FI=?

t_{PROP}=? (worst case)

$W_n=W_{MIN}$

$W_p=6W_{MIN}$

$$C_{INA}=C_{INB}=C_{OX}W_{MIN}L_{MIN}+6C_{OX}W_{MIN}L_{MIN}=7C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)4C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)C_{REF}$$

$$FI=\left(\frac{7}{4}\right)C_{REF} \quad or \quad FI=\frac{7}{4}$$

$t_{PROP} = t_{REF}$ (worst case)

Device Sizing

Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)

Assume $L_n=L_p=L_{min}$ and driving a load of C_{REF}

W_n=?

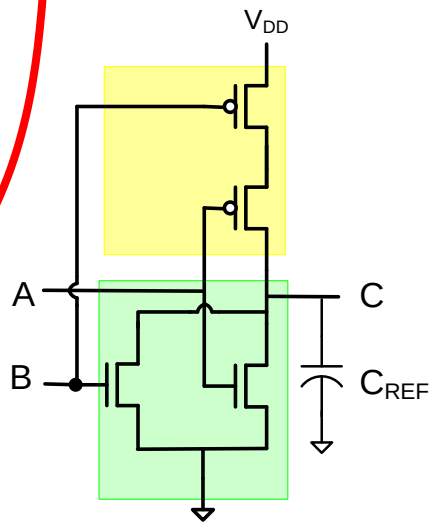
W_p=?

Input capacitance = ?

FI=?

t_{PROP}=? (worst case)

DERIVATIONS



One degree of freedom was used to satisfy the constraint indicated

$W_n=W_{MIN}$

$W_p=6W_{MIN}$

Other degree of freedom was used to achieve equal rise and fall times

$$C_{INA}=C_{INB}=C_{OX}W_{MIN}L_{MIN}+6C_{OX}W_{MIN}L_{MIN}=7C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)4C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)C_{REF}$$

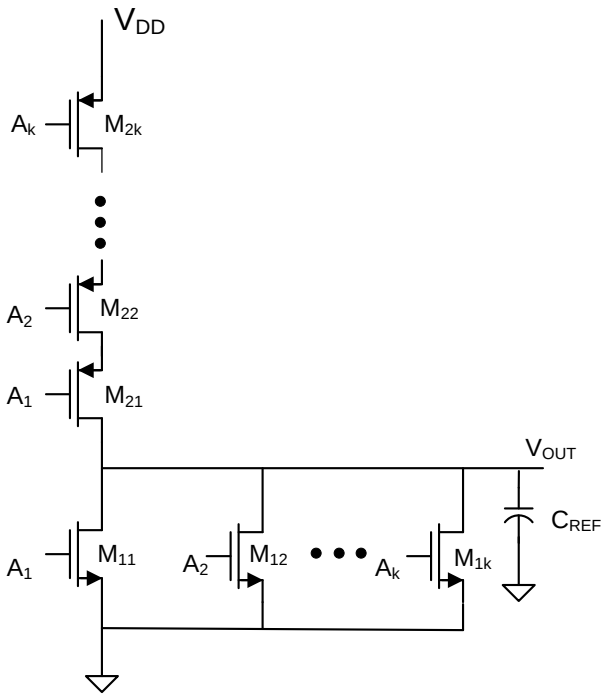
$$FI=\left(\frac{7}{4}\right)C_{REF} \quad or \quad FI=\frac{7}{4}$$

$t_{PROP} = t_{REF}$ (worst case)

Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: k-input NOR



DERIVATIONS

Wn=?

Wp=?

Input capacitance = ?

FI=?

t_{PROP}=?

$W_n = W_{MIN}$

$W_p = 3kW_{MIN}$

$$C_{INx} = C_{OX}W_{MIN}L_{MIN} + 3kC_{OX}W_{MIN}L_{MIN} = (3k+1)C_{OX}W_{MIN}L_{MIN} = \left(\frac{3k+1}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{3k+1}{4}\right)C_{REF}$$

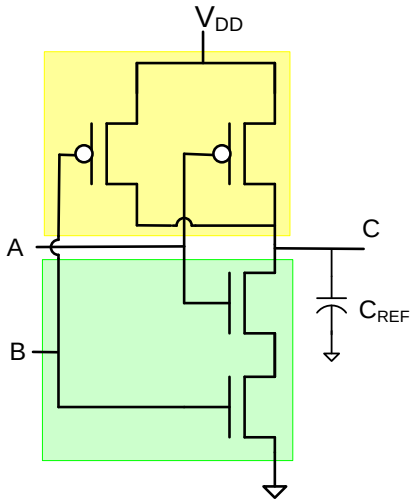
$$FI = \left(\frac{3k+1}{4}\right)C_{REF} \quad or \quad FI = \frac{3k+1}{4}$$

$t_{PROP} = t_{REF}$

Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: 2-input NAND



Wn=?

DERIVATIONS

Wp=?

Input capacitance = ?

FI=?

t_{PROP}=?

$W_n = 2W_{MIN}$

$W_p = 3W_{MIN}$

$$C_{INA} = C_{INB} = 2C_{OX}W_{MIN}L_{MIN} + 3C_{OX}W_{MIN}L_{MIN} = (5)C_{OX}W_{MIN}L_{MIN} = \left(\frac{5}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{5}{4}\right)C_{REF}$$

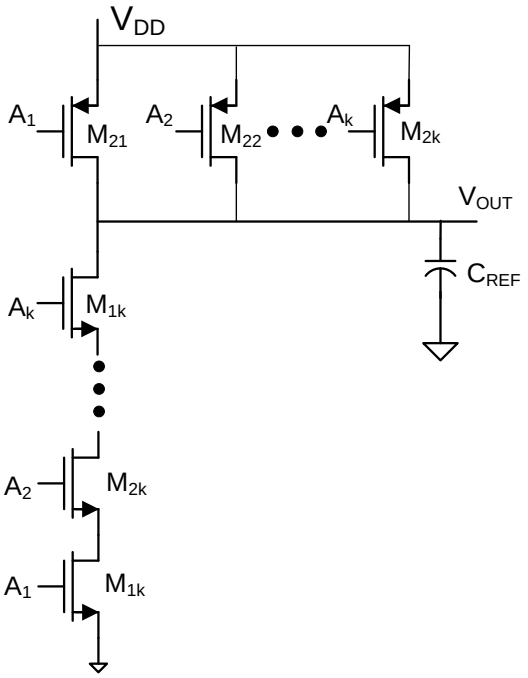
$$FI = \left(\frac{5}{4}\right)C_{REF} \quad or \quad FI = \frac{5}{4}$$

$t_{PROP} = t_{REF}$

Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: **k-input NAND**



DERIVATIONS

Wn=?

Wp=?

Input capacitance = ?

FI=?

t_{PROP}=?

$$W_n = kW_{MIN}$$

$$W_p = 3W_{MIN}$$

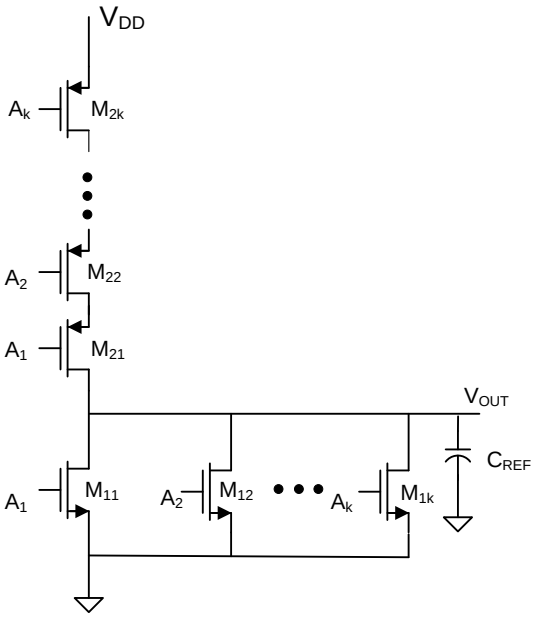
$$C_{INx} = kC_{OX}W_{MIN}L_{MIN} + 3C_{OX}W_{MIN}L_{MIN} = (3+k)C_{OX}W_{MIN}L_{MIN} = \left(\frac{3+k}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{3+k}{4}\right)C_{REF}$$

$$FI = \left(\frac{3+k}{4}\right)C_{REF} \quad or \quad FI = \frac{3+k}{4}$$

$$t_{PROP} = t_{REF}$$

Device Sizing

Comparison of NAND and NOR Gates



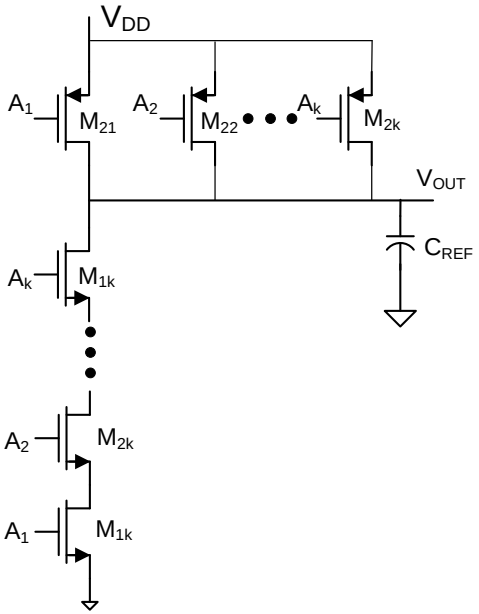
$W_n = W_{MIN}$

$W_p = 3kW_{MIN}$

$C_{INx} = \left(\frac{3k+1}{4}\right) C_{REF}$

$FI = \left(\frac{3k+1}{4}\right) C_{REF}$ *or* $FI = \frac{3k+1}{4}$

$t_{PROP} = t_{REF}$



$W_n = kW_{MIN}$

$W_p = 3W_{MIN}$

$C_{INx} = \left(\frac{3+k}{4}\right) C_{REF}$

$FI = \left(\frac{3+k}{4}\right) C_{REF}$ *or* $FI = \frac{3+k}{4}$

$t_{PROP} = t_{REF}$

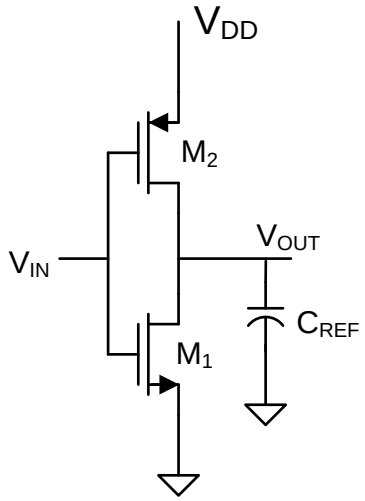
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy

-- (same as $V_{TRIP}=V_{DD}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

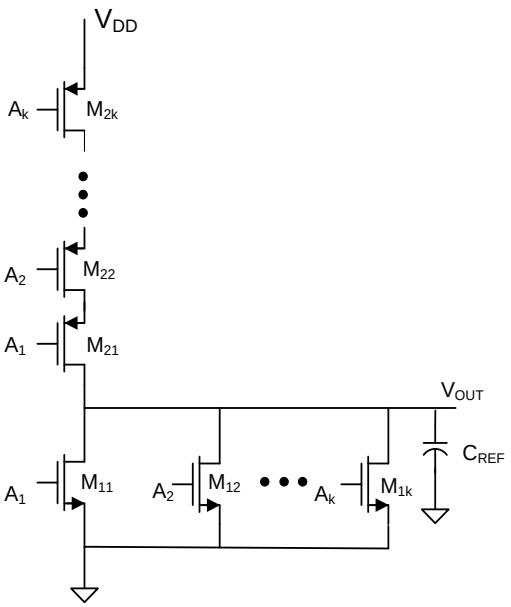


INV

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$C_{IN}=C_{REF}$

FI=1

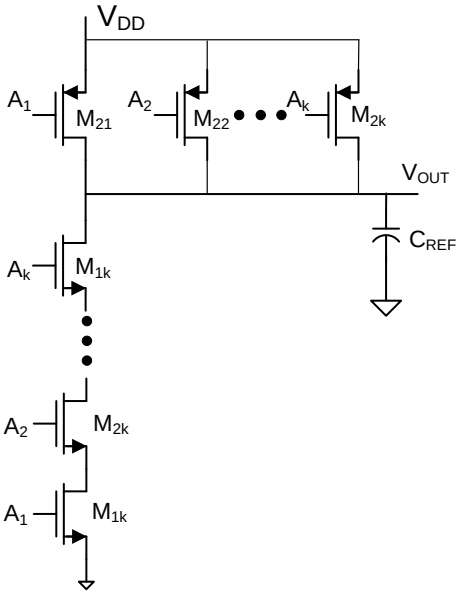


k-input NOR

$W_n=W_{MIN}$, $W_p=3kW_{MIN}$

$$C_{IN}=\left(\frac{3k+1}{4}\right)C_{REF}$$

$$FI=\left(\frac{3k+1}{4}\right)$$



k-input NAND

$W_n=kW_{MIN}$, $W_p=3W_{MIN}$

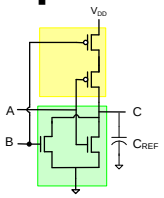
$$C_{IN}=\left(\frac{3+k}{4}\right)C_{REF}$$

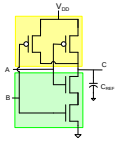
$$FI=\left(\frac{3+k}{4}\right)$$

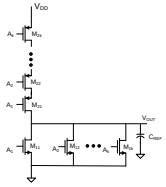
Device Sizing

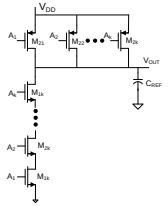
Multiple Input Gates:

2-input NOR **2-input NAND** **k-input NOR** **k-input NAND**









Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Wn=?

Wp=?

Fastest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized (assume driving a load of C_{REF})

Wn=Wmin

Wp=Wmin

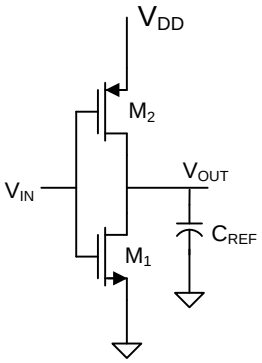
Fastest response (t_{HL} or t_{LH}) = ?

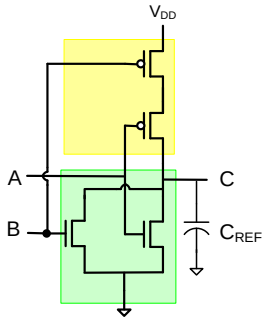
Slowest response (t_{HL} or t_{LH}) = ?

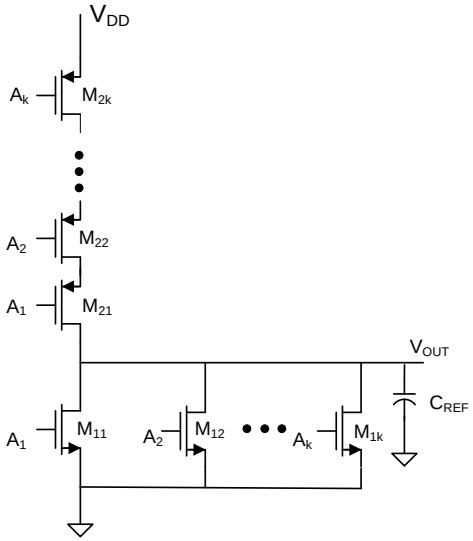
Worst case response (t_{PROP}, usually of most interest)?

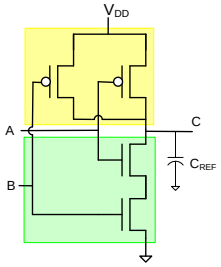
Input capacitance (FI) = ?

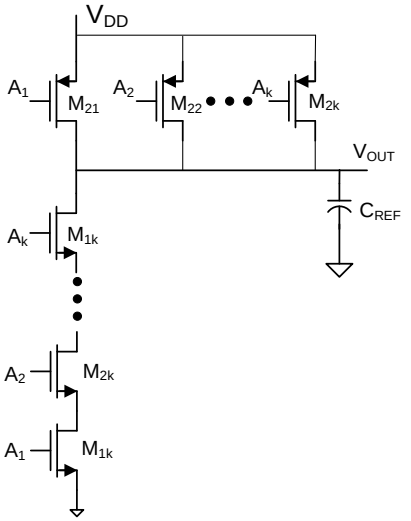
Device Sizing











Minimum Sized **(assume driving a load of C_{REF})** **$W_n=W_{min}$** **$W_p=W_{min}$**

Input capacitance (FI) = ?

$$C_{IN} = C_{OX}W_nL_n + C_{OX}W_pL_p = C_{OX}W_{min}L_{min} + C_{OX}W_{min}L_{min} = 2C_{ox}W_{min}L_{min} = \frac{C_{REF}}{2}$$

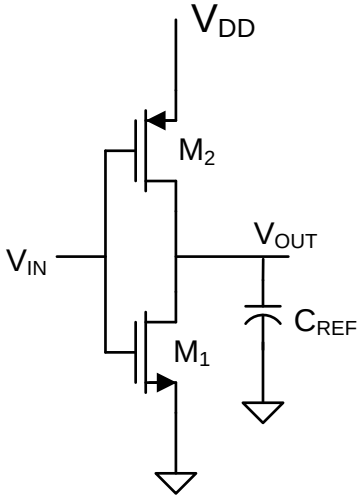
$$FI = \frac{1}{2}$$

Fastest response (t_{HL} or t_{HL}) = ?

Slowest response (t_{HL} or t_{HL}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Device Sizing – minimum size driving C_{REF}



INV

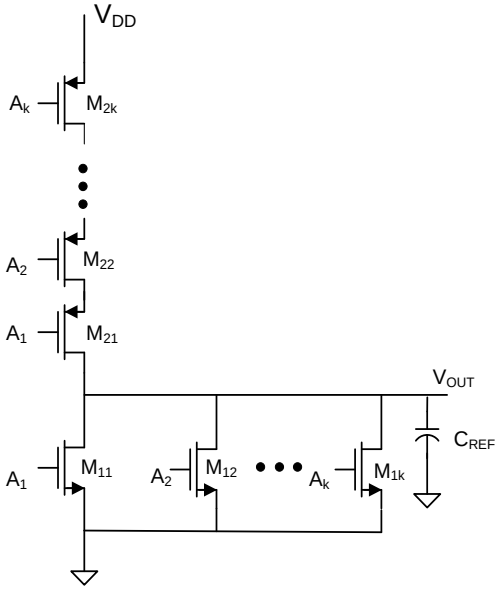
$t_{PROP} = ?$

$$t_{PROP} = 0.5t_{REF} + \frac{3}{2}t_{REF}$$

$$t_{PROP} = 2t_{REF}$$

$$FI = \frac{C_{REF}}{2}$$

$$R_{PU} = R_{PD} = R_{PDREF}$$



k-input NOR

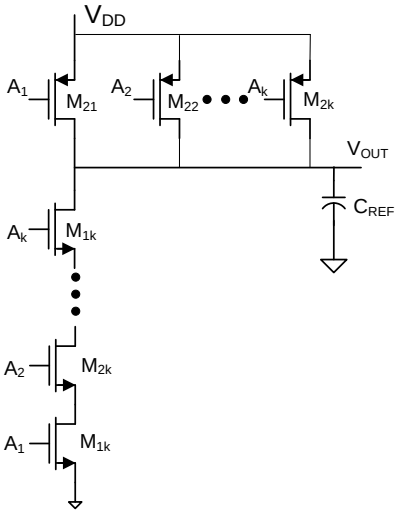
$t_{PROP} = ?$

$$t_{PROP} = 0.5t_{REF} + \frac{3k}{2}t_{REF}$$

$$t_{PROP} = \left(\frac{3k+1}{2}\right)t_{REF}$$

$$FI = \frac{C_{REF}}{2}$$

$$R_{PD} = R_{PDREF} \quad R_{PU} = 3kR_{PDREF}$$



k-input NAND

$t_{PROP} = ?$

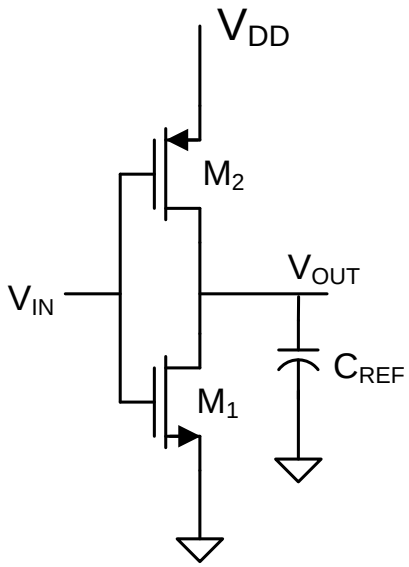
$$t_{PROP} = \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF}$$

$$t_{PROP} = \frac{3+k}{2}t_{REF}$$

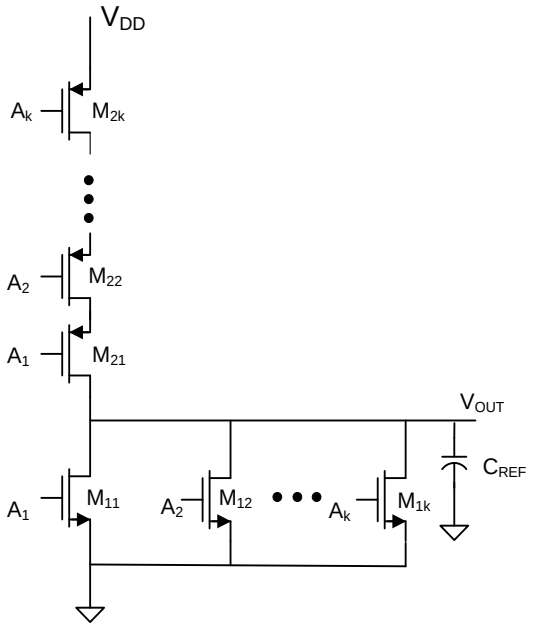
$$FI = \frac{C_{REF}}{2}$$

$$R_{PD} = 3R_{PDREF} \quad R_{PU} = 3R_{PDREF}$$

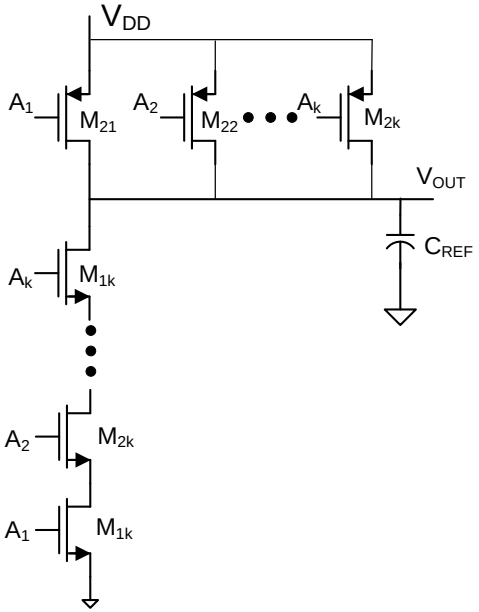
Device Sizing Summary



INV



k-input NOR



k-input NAND

C_{IN} for N_{AND} gates is considerably smaller than for NOR gates for equal worst-case rise and fall times

C_{IN} for minimuim-sized structures is independent of number of inputs and much smaller than C_{IN} for the equal rise/fall time case

R_{PU} gets very large for minimum-sized NOR gate

End of Lecture 41