Homework 4 Fall 2017 TA: Joseph Aymond

Problem 1:

For the 248 nm UV machine, the total amount of wafers that can be made in a year:

$$N_w = 80 * 24 * 365 * \frac{4}{10} = 280{,}320\ wafers$$

Cost per wafer: $C_w = \frac{10M}{N_w} = \$35.67$

Number of chips per wafer: $N_c = \frac{A_w}{A_{chip}} = 1413$

Cost per chip: $C_c = \frac{35.67}{1413} = \$0.025$

For the 193nm UV machine:

Wafers per year: $N_{w2} = 70080$

Cost per wafer: $C_{w2} = \$570.78$

Chips per wafer: $N_{c2} = 4580$

Cost per chip: $C_{c2} = \$0.125$

Cost difference $C_\Delta = 0.125 - 0.025 = \$0.1/chip$

Problem 2:

The dielectric constant of SiO_2 = $K_s = 3.9$

The dielectric constant of HfO_2 = $K_H = 25$

-> Thickness of HfO2: $t_{HfO_2} = \frac{25}{3.9} * t_{SiO_2} = 12.82\ nm$

Problem 3:

The total volume of the oxide $V_{ox} = 7nm * 10\ nm * 2.5\ nm = 175\ nm^3$

The volume of one SiO_2 molecule $V_{SiO_2} = 0.044\ nm^3$

Number of SiO_2 molecules per gate $N_m = \frac{V_{ox}}{V_{SiO_2}} = 3977\ molecules$

Problem 4:

Resistivity of Aluminum $2.8 * 10^{-8}\Omega * m$

Resistance of the interconnect: $R = \frac{2.8*10^{-8}\Omega m}{80\&10^{-9}m} * \frac{500*10^{-6}m}{90*10^{-9}m} = 1944.4\ \Omega$

Problem 5:

The lowest resistance metal for interconnection is silver. It is often not used because silver is very expensive, and because when using silver there is an electro migration issues during fabrication.

Problem 6:

The average thickness of a 12 inch (300 mm) wafer is 750-800 μm With a 120 μm saw the thickness per cut is 870-920 μm.

A 2 meter pull can create $N_w = \frac{2m}{870*10^{-6}m} \sim \frac{2m}{920*10^{-6}m}$=2173 ~ 2298 wafers

Problem 7:

From the last page we find,

Poly 1 sheet resistance = $21.7\frac{\Omega}{\blacksquare}$

$\omega_{3dB} = \frac{1}{RC} = 2\pi f \rightarrow R = \frac{1}{2\pi f * c} = 39.79 * 10^6 \Omega$

a. The minimum area of a poly1 resistor is

$A_{Resistor} = \frac{39.79*10^6}{21.7} * 0.6^2 \mu m^2 = 660.11 * 10^3 \mu m"$

The minimum area of a Poly1-Poly2 ($864\frac{aF}{\mu m\text{^}2}$) capacitor is

$A_{Capacitor} = \frac{20pF}{864\frac{aF}{\mu m\text{^}2}} = 23.15 * 10^3\ \mu m^2$

Total Area $A = A_{Res} + A_{Cap} = 660.11 * 10^3 + 23.15 *\ 10^3 = 683.26 * 10^3\ \mu m^2$

b) We will start with the minimized size resistor has a sheet of x ■ and the capacitor has an area of $y\ \mu m^2$.

Total area $A = (0.6 * 0.6) * x + y = 0.36x + y$

$\frac{1}{RC} = \omega_{3dB} = 2\pi f \rightarrow RC = \frac{1}{2\pi f} = 0.000796\ Hz$

$(x * 21.7)(864 * 10^{-18} * y) = 0.000796 \rightarrow y = \frac{42.46 * 10^9}{x}$

$A = 0.36x + \left(\frac{42.46 * 10^9}{x}\right) \rightarrow A_{min}\ when\ 0.36x = \frac{42.46 * 10^9}{x}$

$x = 343430\ \blacksquare's \rightarrow y = \frac{42.46 * 10^9}{343430} = 123635\ \mu m\text{^}2$

$R = 343430 * 21.7 = 7.45 * 10^6 = 7.45M\Omega$

$C = 123635 * 864 * 10^{-18} = 106.8 * 10^{-12} = 106.8\ pF$

Problem 8:

a. Length = $1\mu m$, width = $2\mu m$
b. Positive photoresist overexposed increases the size.
   Length = $1 + 0.1 + -0.1 = 1\ \mu m$
   Width is unchanged.
c. Overexposing negative photoresist decreases the size
   Length = $1 - 0.1 + 0.1 = 1.0\ \mu m$

Problem 9

Resistivity of Aluminum $2.8 * 10^{-8}\Omega * m$

Resistance of the interconnect $R_{Al} = \frac{\rho l}{wt} \rightarrow t = \frac{\rho l}{wR} = \frac{2.8*10^{-8}*500*10^{-6}}{1*10^{-6}*50} = 280 * 10^{-9}m = 280nm$

Sheet resistance $= \frac{\rho}{t} = \frac{2.8*10^{-8}}{280*10^{-9}} =\ 0.1\ \Omega/\blacksquare$

Problem 10

Resistivity of Copper $1.68 * 10^{-8} \Omega * m$

$$R_{Al} = \frac{\rho l}{wt} \rightarrow l = \frac{Rwt}{\rho} = \frac{1 * 10^{-6} * 50 * 280 * 10^{-9}}{1.68 * 10^{-8}} = 833.33 * 10^{-6} = 833.33\ \mu m$$

Problem 11

Approximately 53% of the oxide grows above the wafer, and 47% grows into the wafer.
The increased wafer height $W_{height} = 0.53 * 5000 = 2650Å$

Problem 12

Poly 1: $21.7\Omega/\blacksquare$
N+: $82.7\Omega/\blacksquare$

For 10k Ohms
Poly1: $\frac{10{,}000}{21.7} = 460.8\ \blacksquare's$

N+: $\frac{10{,}000}{82.7} = 120.9\ \blacksquare's$

There are a lot of different ways to create the serpentine layout, depending on how many rows you want to make. The diagram used 10 so with 10 as our bases,

Poly 1 has 47 squares per row, 10 rows, 9 connections. This means there are 18 corners.
$(47 * 10) + 9 - (18 * 0.45) = 470.9\ \blacksquare's$. We want 460.9, so we will remove 10 from the bottom row. The area taken up by the polysilicon is $(((47 * 10) + 9 - 10) * 0.6 * 0.6) = 168.84\ \mu m^2$ but the entire serpentine design, including the space between rows, takes up $(47 * 0.6) * (19 * 0.6) = 321.48 \mu m^2$.

N+ has 12 squares per row, 10 rows, 9 connections, and 18 corners.
$(12 * 10) + 9 - (18 * 0.45) = 120.9\ \blacksquare's$ which is the number we want. The area taken up by the N+ is $(((12 * 10) + 9) * 0.6 * 0.6) = 46.44\ \mu m^2$ but the entire serpentine design with the space between rows takes up $(12 * 0.6) * (19 * 0.6) = 82.08 \mu m^2$.

So the polysilicon alone takes up $\frac{168.8}{46.44} = 3.63$ times the space as the N+ and the entire serpentine design of the polysilicon takes up $\frac{321.48}{82.08} = 3.92$ times the space of the N+ serpentine design.

Problem 13-14

Code

/home/jaaymond/ee330/verilog/EE330Homework/1to4MUX.v (/MUX1to4_tb

```
Ln#
 1  `timescale 1ns/1ps
 2  module MUX1to4(in, outA, outB, outC, outD, s1, s2);
 3    input [3:0] in;
 4    input  s1, s2;
 5    output [3:0] outA, outB, outC, outD;
 6    reg [3:0] oA, oB, oC, oD;
 7
 8    assign outA = oA;
 9    assign outB = oB;
10    assign outC = oC;
11    assign outD = oD;
12
13    always @(*) begin
14      if(s1 == 0) begin
15        if(s2 == 0) begin
16          oA <= in;
17          oB <= 4'd0;
18          oC <= 4'd0;
19          oD <= 4'd0;
20        end
21        else begin
22          oA <= 4'd0;
23          oB <= 4'd0;
24          oC <= in;
25          oD <= 4'd0;
26        end
27       end
28       else begin
29        if(s2 == 0) begin
30          oA <= 4'd0;
31          oB <= in;
32          oC <= 4'd0;
33          oD <= 4'd0;
34        end
35        else begin
36          oA <= 4'd0;
37          oB <= 4'd0;
38          oC <= 4'd0;
39          oD <= in;
40        end
41      end
42    end
43  endmodule
```

Test bench

/home/jaaymond/ee330/verilog/EE330Homework/1to4MUX_tb.v (/MUX1to4_tb) - De

```
Ln#
 1  `timescale 1ns/1ps
 2
 3  module MUX1to4_tb();
 4
 5    reg [3:0] in;
 6    reg s1, s2;
 7    wire [3:0] outA, outB, outC, outD;
 8
 9    MUX1to4 mux(.in(in), .outA(outA), .outB(outB), .outC(outC),
10      .outD(outD), .s1(s1), .s2(s2));
11
12    initial begin
13     in = 4'b0001;
14     s1 = 0;
15     s2 = 0;
16    end
17
18    always #20 s1 <= ~s1;
19    always #40 s2 <= ~s2;
20
21  endmodule
```

Output