EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 3
Spring 2017

Instructions: This is a 50 minute exam. Students may bring 3 page of notes (front and back) to this exam. There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF} = \infty$. Specify clearly what process parameters you are using in any solution requiring process parameters. Also attached to this exam is a table discussed in class that relates to the basic amplifier configurations.

1. (2pts) Which of the basic MOS amplifiers is characterized by a high noninverting voltage gain?

2. (2pts) How much voltage gain is possible in a single-stage CE amplifier if current source biasing is used?

3. (2pts) The cascode amplifier is actually a cascade of two stages. What basic bipolar amplifier configuration is used as the first stage of a cascode amplifier?

4. (2pts) In class we were interested in the basic amplifier structures created with both bipolar and MOS devices but derived the two-port amplifier models for the bipolar amplifiers first. What was the major reason we derived the bipolar amplifier models before the MOS amplifier models?

5. (2pts) Though an NMOS process is less expensive than a CMOS process and though the area required for basic gates is physically smaller in the NMOS process, the CMOS process has been the dominant process for over two decades. What is the major reason that the CMOS process has become more dominant?

6. (2pts) What is one important reason that the designer would like the trip point of the basic CMOS inverter near $V_{DD}/2$?

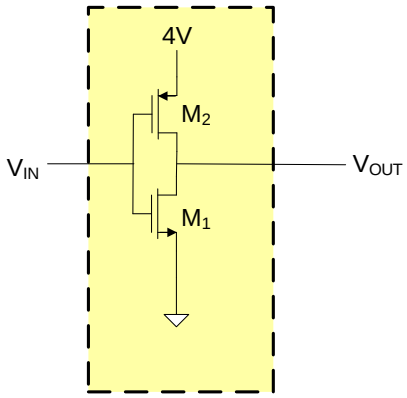
7. (2pts) The polygons in a layout are a part of the Geometric Description File (GDF) for a design. Which of the 3 major hierarchical levels of a digital design corresponds to data in the GDF?

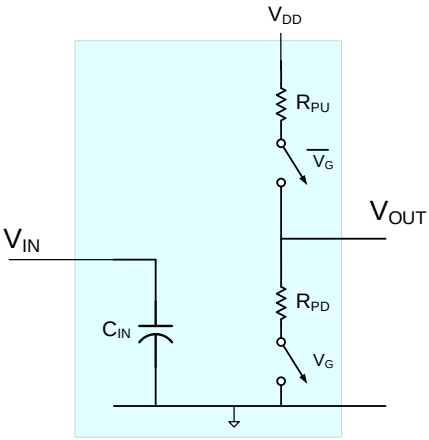
8. (2pts) When using the V_{TEST}-I_{TEST} method to derive the two-port amplifier models, what termination is placed on the input port when calculating the output impedance?

9. (2pts) What is the major reason current sources are preferred over resistors, capacitors, and dc voltage sources when biasing integrated amplifiers?

10. (2 pts) When discussing the SCR, it was observed that there is a really undesirable problem associated with the parasitic SCR that can be formed in a standard CMOS process. What is this problem and why is it bad?

Problem 1 (16 Pts.) Consider a CMOS inverter shown in the dashed box below. Assume the inverter was designed with $L_1=L_2=1\mu$,$W_1= 30\mu$, and $W_2=50\mu$ in a CMOS process with parameters given at the top of this exam. Derive the switch-level model shown in the right below for this CMOS inverter.

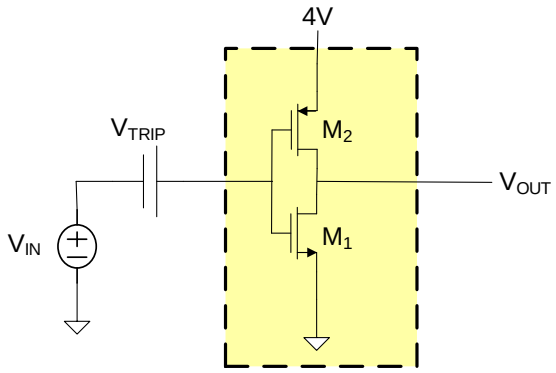




Problem 2 (16 Pts.) Consider a CMOS inverter shown in the dashed box below. This circuit can also be used as an analog amplifier. In this application, the dc voltage source V_{TRIP} has the same value as the trip voltage of the circuit when used as a digital inverter.

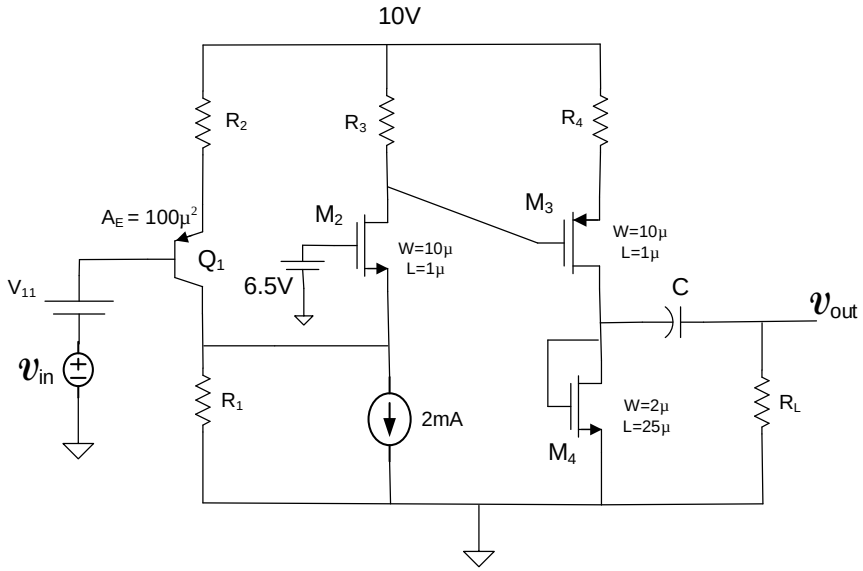
a) Draw the small-signal equivalent circuit in terms of the small-signal model parameters of the transistors (Since biased with V_{TRIP}, M_1 and M_2 are operating in the saturation region).

b) Derive the voltage gain in terms of the small-signal model parameters of the MOS transistors.



Problem 3 (16 Pts.) Consider the following circuit. Assume the MOS transistors are operating in the saturation region, the BJT is operating in the forward active region, and the capacitors are large.

a) Draw the small signal equivalent circuit
b) Determine the small-signal voltage gain in terms of the small-signal model parameters.

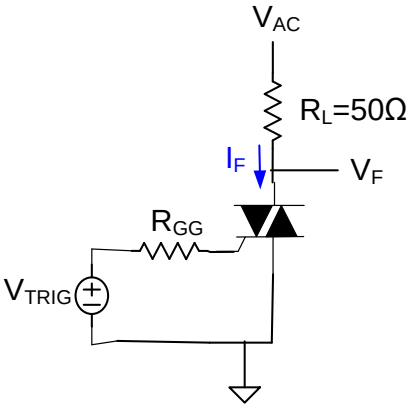


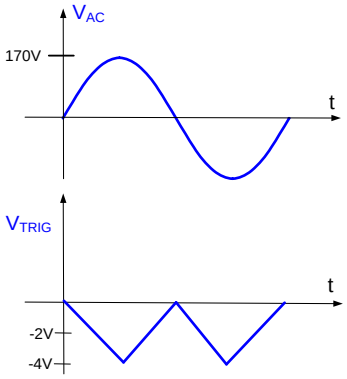
Problem 4 (16 Pts.) Design a current generator circuit that has output sinking currents of 5uA and 100uA. You have available MOS transistors, one resistor of value 100K, and a 5V dc voltage source.

Problem 5 (16 Pts) Consider the following circuit. One period of the periodic voltage V_{AC} and V_{TRIG} are shown below. Assume $V_{AC}=120\sin(120\pi t)$ and the magnitude of the gate trigger voltage of the Triac is 2V. Assume the gate trigger current is small.

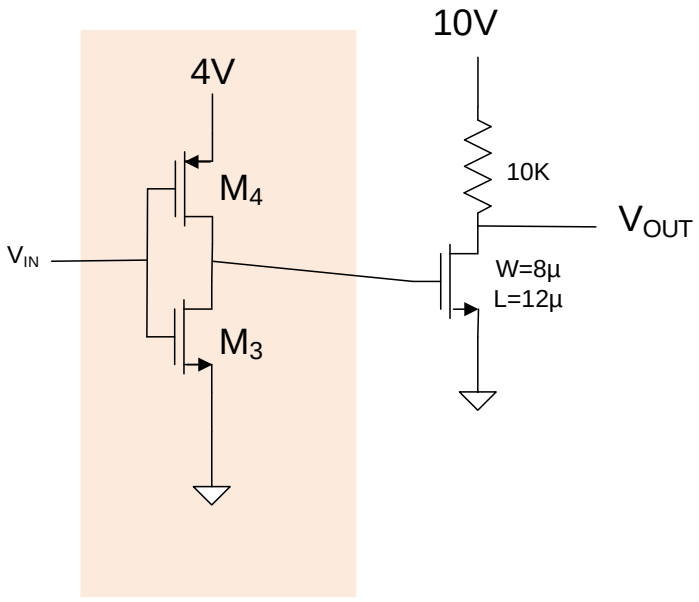
a) (12pts) Obtain an expression for and plot $V_F(t)$ for one period of the controlling signal.

b) (4 pts) Determine the quadrants of operation of the Triac





Problem 6 Extra Credit (10 Pts) Assume M3 and M4 are sized with W=1µ and L=1µ. Determine V_{OUT} for one period of the excitation if $V_{IN}=2+2\sin(100t)$.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

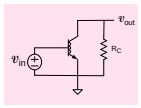
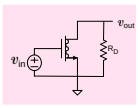
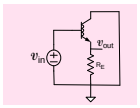
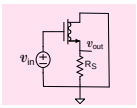
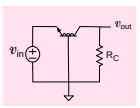
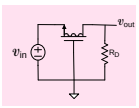
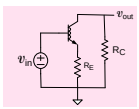
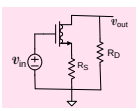
PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

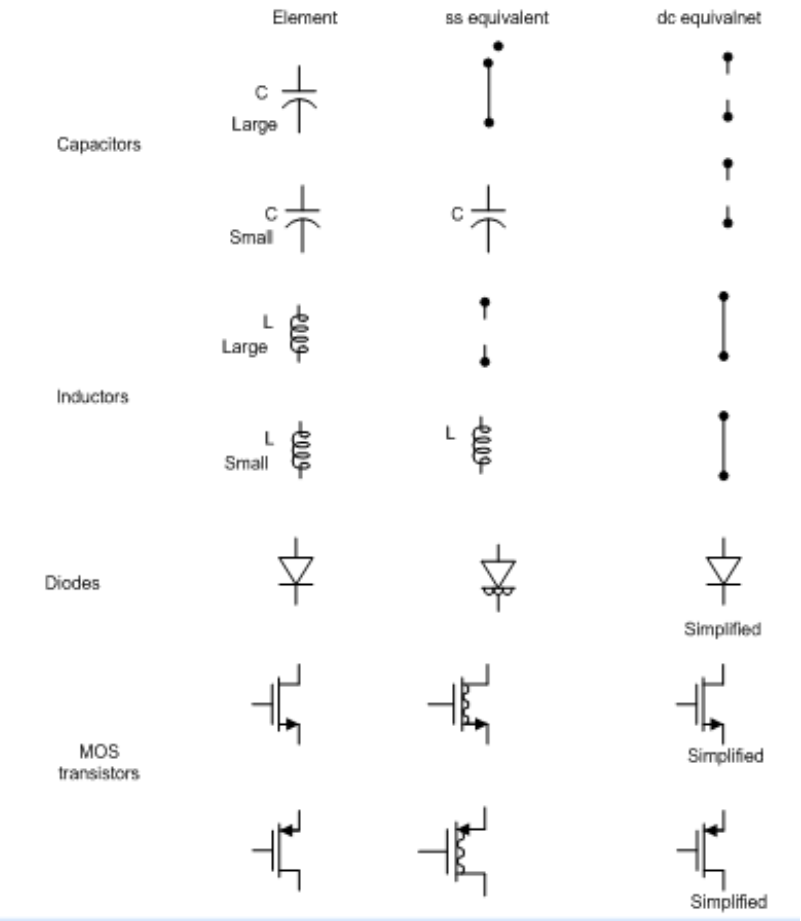
CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

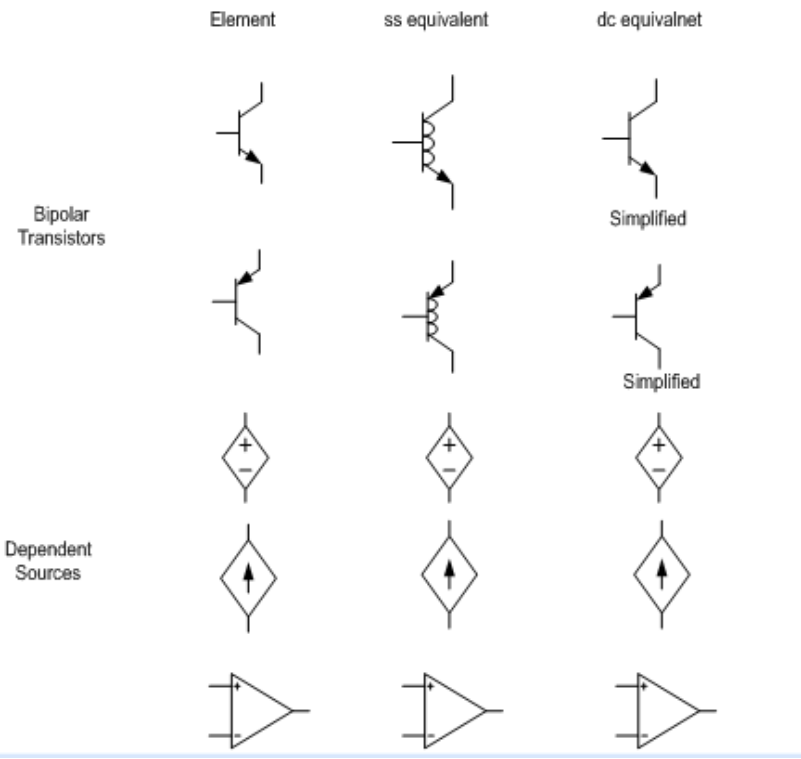
Basic Amplifier Gain Table

	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
								
A_V	$-g_mR_C$		$\frac{g_m}{g_m+g_E} \approx 1$		g_mR_C		$-\frac{R_C}{R_E}$	
	$-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$	$\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	$\frac{I_{CQ}R_C}{V_t}$	$\frac{2I_{DQ}R_C}{V_{EB}}$		
R_{in}	r_π		$r_\pi+\beta R_E$		g_m^{-1}		$r_\pi+\beta R_E$	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞
R_{out}	R_C		g_m^{-1}		R_C		R_C	
			$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$				

Dc and small-signal equivalent elements

	Element	ss equivalent	dc equivalnet
dc Voltage Source	V_{DC}		V_{DC}
ac Voltage Source	V_{AC}	V_{AC}	
dc Current Source	I_{DC}		I_{DC}
ac Current Source	I_{AC}	I_{AC}	
Resistor	R	R	R


Element
ss equivalent
dc equivalnet
Capacitors
C
Large
C
Small
C
Inductors
L
Large
L
Small
L
Diodes
Simplified
MOS
transistors
Simplified
Simplified


Element
ss equivalent
dc equivalnet
Bipolar
Transistors
Simplified
Simplified
Dependent
Sources