CprE 381, Computer Organization and Assembly-Level Programming, Spring 2019

Lab 4 Report

Student Name _____Sean Gordon_____

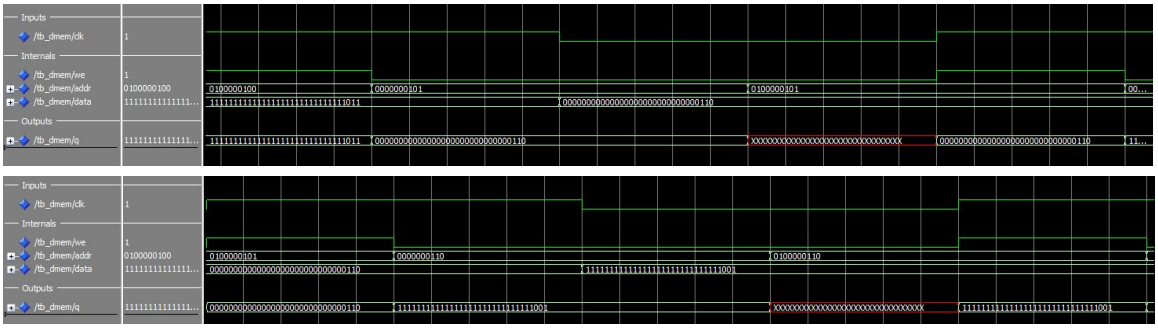
Section/Lab Time _____C/10:00 am_____

Refer to the highlighted language in the lab 4 instruction for the context of the following questions.

a. [Part 0] based on your understanding of the VHDL implementation, provide a 2-3 sentence description of each of the individual ports (both generic and regular)

clk: Conventional clock input, used to synchronize component and as a reliable timing medium. addr: Provides next memory address in ram. Thanks to the code, Quartus will create an initialization for ram at this location. data: Data to store at the given location in ram. Inserted into the 2D array 'ram'. we: Write enable. Allows data to be written to ram. q: Output for device. The data held in ram after all processes has run is put here.

b. [Part 1 (b)] Waveforms.



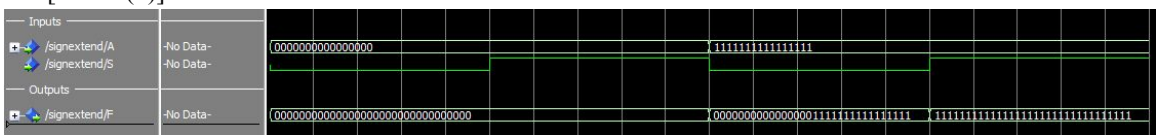
c. [Part 2 (a)] What are the MIPS instructions that require some value to be sign extended? What are the MIPS instructions that require some value to be zero extended?

Sign extended	Zero Extended
• Add Immediate • Add Immediate Unsigned • Load Byte Unsigned • Load Halfword Unsigned • Load Linked • Load Word • Set Less Than Imm. • Set Less Than Imm. • Store Byte • Store Conditional • Store Halfword • Store Word • Load FP Single • Load FP	• And Immediate • Or immediate

d. [Part 2 (b)] what are the different 16-bit to 32-bit "extender" components that would be required by a MIPS processor implementation?

An and gate and some wires? Used with a control signal to sign or unsign extend using 0 or the most significant bit.

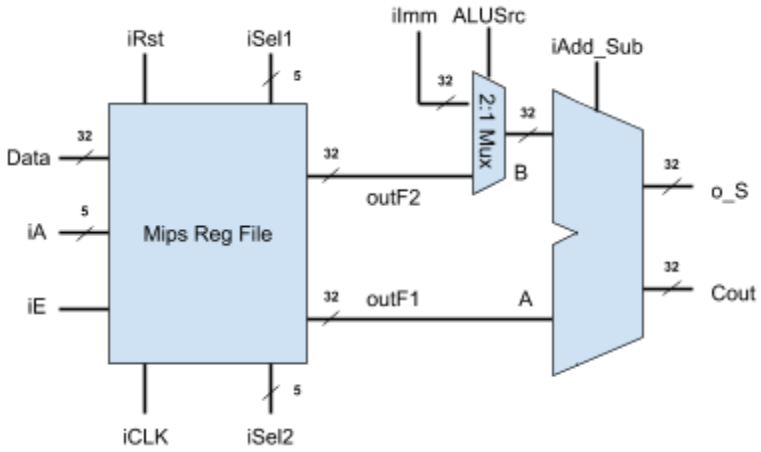
e. [Part 2 (d)] Waveform.



f. [Part 3 (a)] what control signals will need to be added to the simple processor from Lab #3? How do these control signals correspond to the ports on the mem.vhd component analyzed in problem 2)?

A write enable and a sign extend control switch. The we signal would port directly into the mem.vhd component, while the sign extend control signal would help put the correct data into memory

g. [Part 3 (b)] Draw a schematic of a simplified MIPS processor consisting only of the base components used in Lab #3, the extender component described in problem (1), and the data memory from problem (2).



h. [Part 3 (c)] Waveform.

Yeah no time

i. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

1. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	30 min	40 min
Pencil/paper design	10 min	10 min
VHDL design	50 min	4:00
Assembly coding		
Simulation	10 min	45 min
Debugging	20 min	3:00
Report writing		
Other:		

Total	2:00	9:35

2. If you could change one thing about the lab experience, what would it be? Why?
   Just scrap these labs and teach VHDL this is ridiculous.

3. What was the most interesting part of the lab?
   Contemplating how heinously inefficient these labs are.