EE 330

Homework Assignment 6
Fall 2019 (Due Friday Oct 4)

Unless specified to the contrary assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=300\mu A/V^2$,$\mu_p C_{OX}=\mu_n C_{OX}/4$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$. Correspondingly, assume all npn BJT transistors have model parameters $J_S= 10^{-14}A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S= 10^{-14}A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. If parameters are needed for process characterization beyond what is given, use the measured parameters from the TSMC 0.18µ process given below as model parameters.

Problem 1

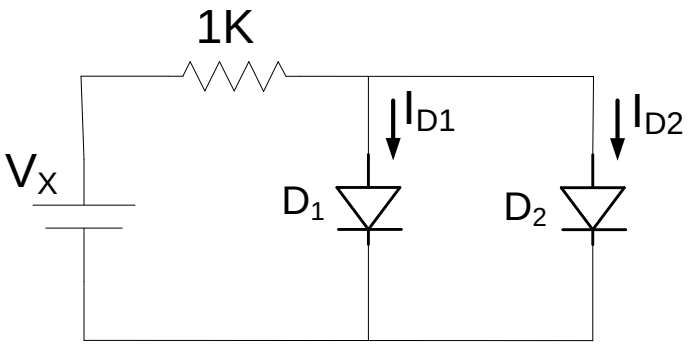
Size an n-channel transistor in the TSMC 0.18µ CMOS process so that the impedance in the switch-level model is 6000Ω when operating with a 1.8V power supply.
Repeat for an n-channel transistor in the ON 0.5µ process when operating with a supply voltage of 3.5V and the IBM 0.13µ CMOS process when operating with a 1.5V supply.
Characteristics of the ON and IBM processes are also attached.

Problem 2

If a minimum-sized inverter designed in the ON 0.5µ CMOS process could directly drive a minimum-sized inverter designed in the IBM 0.13µ CMOS process, what would be t_{HL} and t_{LH}? Assume a supply voltage of 1.5V. Neglect any interconnect parasitics.

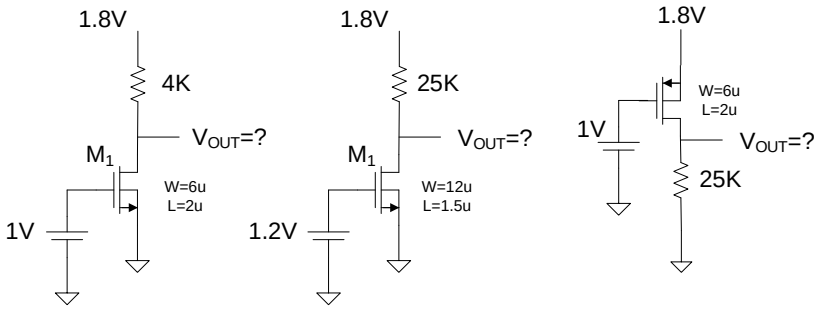
Problem 3

Assume the junction area of D_1 is $150\mu^2$ and that of D_2 is 5 times as large. Determine the current I_{D1} if $V_X=1.5V$. Assume J_S for the process where the diodes are fabricated is $5fA/\mu^2$.



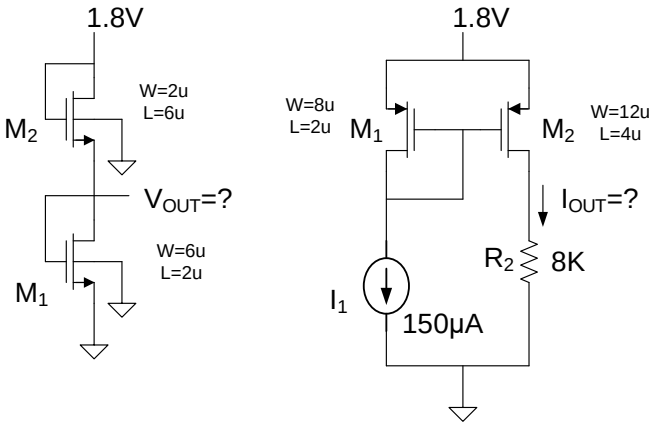
Problem 4

Analytically determine the variable indicated by a ? in the following circuits. Assume the devices are in a process with $\mu_n C_{OX}=300\mu A/V^2$,$\mu_p C_{OX}=\mu_n C_{OX}/4$,$V_{TNO}=0.5V$, $V_{TPO}=-0.5V$, and $C_{OX}=8fF/\mu^2$.



Problem 5

Analytically determine the variable indicated by a ? in the following circuits. Assume a process with $\mu_n C_{OX}=300\mu A/V^2$,$\mu_p C_{OX}=\mu_n C_{OX}/4$,$V_{TNO}=0.5V$, $V_{TPO}=-0.5V$, and $C_{OX}=8fF/\mu^2$

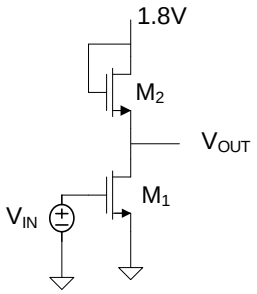


Problem 6

Consider the following circuit.

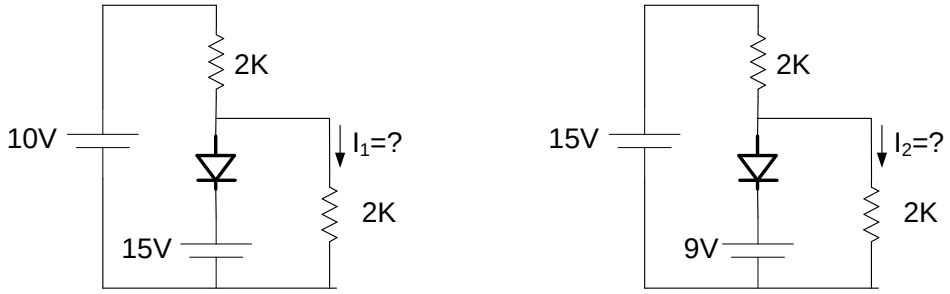
a) If $V_{IN}=1V$, determine the dimensions of M_1 that will result in an output voltage of 1V. Assume that the dimensions of M_2 are $W_2=8\mu$ and $L_2=2\mu$. The relevant model parameters of the devices are $V_{TN}=0.5V$, $V_{TP}=-0.5V$, $\mu_n C_{OX}=300\mu AV^{-2}$ and $\mu_p C_{OX}=75\mu AV^{-2}$.

b) Repeat part a) if the goal is to have an output voltage of 0.2V.



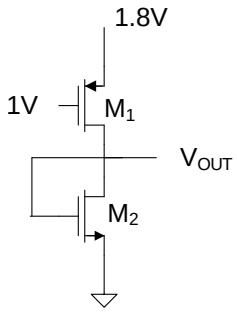
Problem 7

Determine the currents indicated with a ? in the following circuits. Assume the diodes are ideal.



Problem 8

c) Determine V_{OUT} for the following circuit. Assume the devices M_1 and M_2 are identically sizes with W=5µ and L=2µ. The relevant model parameters of the devices are V_{TN}=0.5V, V_{TP}=-0.5V, $\mu_n C_{OX}$=300µAV^{-2} and $\mu_p C_{OX}$=75µAV^{-2}.



Problem 9

Design a circuit using only MOS transistors that has an output voltage of 1.1V in the TSMC 0.18u CMOS process. In addition to the transistors, you have a single dc power supply of 2V available. You may use as many MOS transistors as you want and can specify any size for the devices.

Problem 10

Assume a junction capacitor has a capacitance of 500fF with zero volts bias. What will be the value of this capacitor with a reverse bias of 2V? With a forward bias of 250mV?

Problem 11

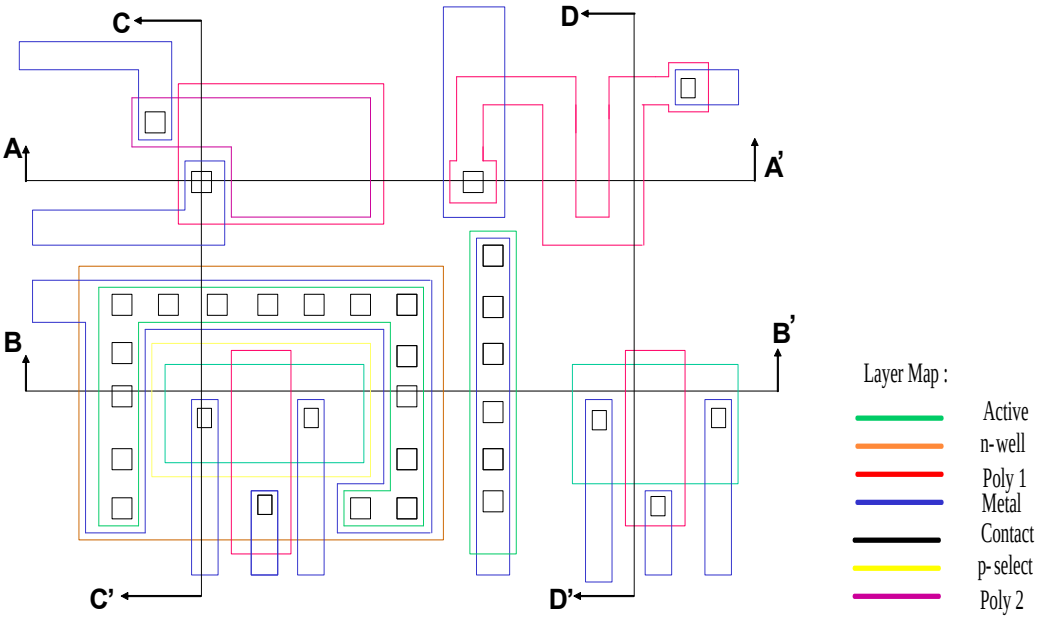
Design a voltage programmable capacitor that varies between 2pF at 0V bias and 2.5pf at a bias of 4V.

Problem 12

Sketch a cross-sectional view along the AA' cross-section for the CMOS layout shown below. Assume a basic CMOS process in which the n-select mask is generated from the compliment of the p-select mask.

Problem 13

Repeat Problem 12 along the CC’ cross-section



Problem 14 (weighted as two problems)

Using Modelsim, create a 1 bit half adder. The inputs should be A and B while the outputs should be HS (the sum) and Cb (the carry bit.) Using this 1 bit half adder program, create a full adder as well. The full adder will have A, B, and Cin as inputs. FS (the sum) and Cout (the carry bit) will be the outputs. Use the truth tables below as a guide. Create a test bench to verify your half adder and full adder functionality separately. Include screenshots of your Verilog code and simulation waveforms.

Input		Output	
A	B	HS	Cb
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder Truth Table

Input			Output	
A	B	Cin	FS	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Truth Table

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON

MOSIS WAFER ACCEPTANCE TESTS

RUN: T86S VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		463	-248	uA/um
Vth		0.67	-0.91	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.8	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.49	0.57	V^0.5
K' (Uo*Cox/2)		57.8	-19.1	uA/V^2
Low-field Mobility		475.38	157.09	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

AMI 0.5u Process Description Continued

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	84.4	109.2	22.9	1102	41.9	0.09	0.09	ohms/sq
Contact Resistance	60.9	150.6	15.8		26.8		0.81	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	818	808	ohms/sq
Contact Resistance	0.81			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	426	724	85		30	15	9	37	aF/um^2
Area (N+active)			2434		34	17	12		aF/um^2
Area (P+active)			2351						aF/um^2
Area (poly)				899	56	16	9		aF/um^2
Area (poly2)					46				aF/um^2
Area (metal1)						33	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	361	241			71	49	33		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						46	34		aF/um
Fringe (metal2)							54		aF/um
Overlap (N+active)			292						aF/um
Overlap (P+active)			387						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.04	volts
Vinv	1.5	2.29	volts
Vol (100 uA)	2.0	0.12	volts
Voh (100 uA)	2.0	4.86	volts
Vinv	2.0	2.47	volts
Gain	2.0	-18.26	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		98.75	MHz
D256_WIDE (31-stg,5.0V)		153.47	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.00	uW/MHz/gate

COMMENTS: SUBMICRON

MOSIS WAFER ACCEPTANCE TESTS

RUN: T85X (8WL_8LM_OL) VENDOR: IBM-BURLINGTON
TECHNOLOGY: SIGE013 FEATURE SIZE: 0.13 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SIGE8WL_IBM-BU

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.16/0.12			
Vth		0.41	-0.42	volts
SHORT	20.0/0.12			
Idss		406	-178	uA/um
Vth		0.43	-0.42	volts
Vpt		3.6	-3.6	volts
WIDE	20.0/0.12			
Ids0		155.2	-127.9	pA/um
LARGE	20.0/20.0			
Vth		0.12	-0.23	volts
Vjbkd		2.7	-3.2	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.28	0.23	V^0.5
K' (Uo*Cox/2)		308.0	-48.8	uA/V^2
Low-field Mobility		553.02	87.62	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	UNITS
Sheet Resistance	6.7	6.3	6.6					ohms/sq
Sheet Resistance				78	51	50	50	mohms/sq
Contact Resistance	9.4	9.2	8.3		0.68	1.37	2.00	ohms
Gate Oxide Thickness	31							angstrom

PROCESS PARAMETERS	M5	M6	M7	M8	N_W	PPLY+BLK	N+BLK	POLY_NON	POLY_NON TaN	UNITS
Sheet Resistance	41	44	7	7.4						mohms/sq
Sheet Resistance					327	321.2	73.4	231.6	1547.4 58.9	ohms/sq
Contact Resistance	2.19	2.51	2.51	2.53						ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	M7	M8	TaN	MiM	UNITS
Area (substrate)	973	1203	109	57	41	32	27	23	20	17	14	24		aF/um^2
Area (N+active)		11176												aF/um^2
Area (P+active)		10496												aF/um^2
Area (r well)	605													aF/um^2
Area (N+ HA varactor)		2390												aF/um^2
Area (M1)			128											aF/um^2
Area (M2)				171										aF/um^2
Area (M3)					182									aF/um^2
Area (M4)						176								aF/um^2
Area (M5)							82							aF/um^2
Area (M6)								81						aF/um^2
Area (M7)									45					aF/um^2
Area (M8)										85				aF/um^2
Area (MiM)													4100	aF/um^2
Fringe (substrate)	60	68												aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.50	volts
Vinv	1.5	0.52	volts
Vol (100 uA)	2.0	0.01	volts
Voh (100 uA)	2.0	1.18	volts
Vinv	2.0	0.53	volts
Gain	2.0	-18.48	
Ring Oscillator Freq.			
DIV1024 (31-stg,1.2V)		376.81	MHz
D1024_THK (31-stg,2.5V)		279.93	MHz
Ring Oscillator Power			
DIV1024 (31-stg,1.2V)		5.13	nW/MHz/gate
D1024_THK (31-stg,2.5V)		26.50	nW/MHz/gate
Operational Amplifier			
Gain		10	

COMMENTS: DEEP_SUBMICRON