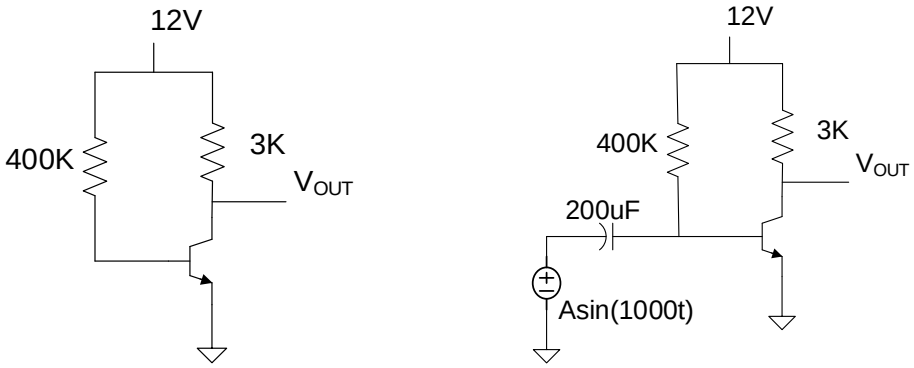
EE 330
Homework 8
Spring 2018
Due Friday March 2

Each problem is worth 10 points except Problem 11-12 which is worth 20 points. The first 12 problems are followed by practice problems. The practice problems will not be collected or graded but solutions will be posted. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$ and $V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$ and $V_{Tp} = -0.5V$. Correspondingly, assume all npn BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta = 100$ and all pnp BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. If parameters are needed for CMOS process characterization beyond what is given, use the measured parameters from the TSMC 0.18µ process given below as model parameters. Assume all diodes are characterized by the model parameters $J_{SX} = 0.5A/\mu m^2$, $V_{G0} = 1.17V$, and $m = 2.3$.

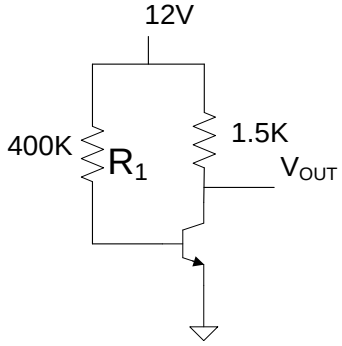
Problem 1

Assume the emitter area for the BJT is $400\mu^2$, the base area is $800\ \mu^2$, $\beta = 100$, and $J_S = 50fA/\mu^2$. Determine the output voltage V_{OUT} for the two circuits shown if A=0V.



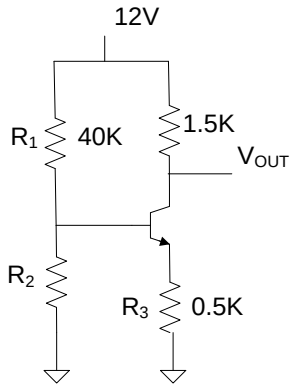
Problem 2

The process parameter β for a BJT is quite variable from one process run to another. If the β in a process varies between 90 and 120, what is the corresponding variation in the output voltage V_{OUT} for the circuit shown?



Problem 3

The 400K resistor in the previous problem is often termed a biasing resistor since it is used to establish the desired value of the quiescent output voltage and the biasing scheme whereby this single resistor is used to establish the base current is termed a self-bias. An alternative biasing scheme is shown below. In this circuit, the resistor R_1 has been reduced to 40K and a second resistor R_2 has been added to the circuit. This scheme is often termed a fixed-bias scheme. In this circuit, determine R_2 so that the quiescent output voltage is the same as that for the circuit of the previous problem when the value of β is the nominal value of 100.



Problem 4

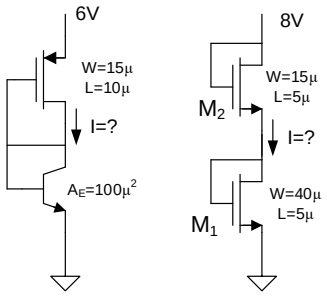
Using the value of R_2 determined in the previous problem, compare the variation of the output voltage of the self-bias circuit to that of the fixed-bias circuit if β varies between 90 and 120.

Problem 5

In the previous homework assignment you were asked to design a circuit using only MOS transistors (no resistors or other components) that has an output voltage of 1Vwhen biased with a single dc power supply of 2.5V. Comment on solving this problem if you have only BJTs available.

Problem 6

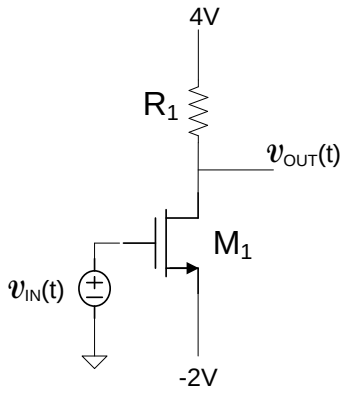
Determine the currents labeled with a ?



Problem 7

Determine the maximum value of R_1 that will keep M_1 in saturation. M_1 has dimensions W=6μ and L=3μ and is in a process with $\mu_n C_{OX} = 350\mu A/V^2$, $\mu_p C_{OX}$ =

$70\mu A/V^2$, $V_{Tn} = 0.5V$, $V_{Tp} = -0.5V$, $C_{OX} = 8fF/\mu^2$, $\lambda = 0$, and $\gamma = 0$. Assume $v_{IN}(t)$ is very small.

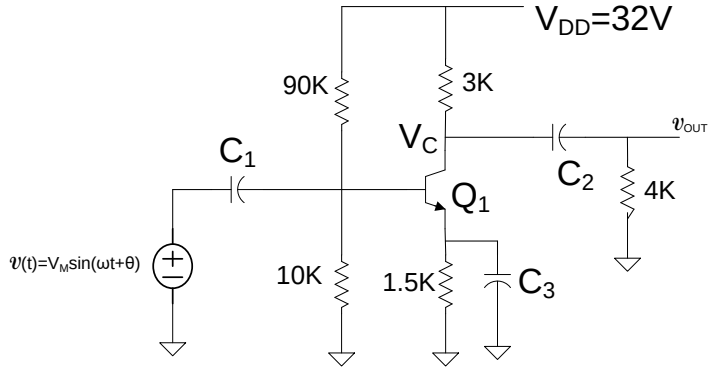


Problem 8

Determine the small-signal voltage gain of the circuit in the previous problem if the value of R_1 is ½ the value needed to keep M_1 in saturation

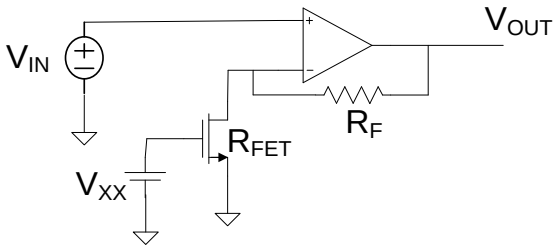
Problem 9

Assume the capacitors are all very large. Determine the quiescent value of V_C and V_{OUT}.



Problem 10

Assume V_{IN} is a low frequency sinusoidal waveform given by the expression V_{IN}=.025sin1000t and assume that W=4μm, L=1μm for the MOSFET. The output voltage of this circuit should be a sinusoidal waveform of the same frequency as the input. Define the voltage gain to be the ratio of the p-p value of the output sinusoidal signal to the p-p value of the sinusoidal input signal. With this definition of gain, determine the voltage gain of this circuit if V_{XX}=2V.



Problem 11 and 12

(counts as 2 problems) Use Modelsim to implement an 8-bit Gray counter. The counter should only count up on a positive clock edge. The counter should also have an enable bit to start and stop the counter. Include screenshots of your Verilog code, and simulation waveforms.

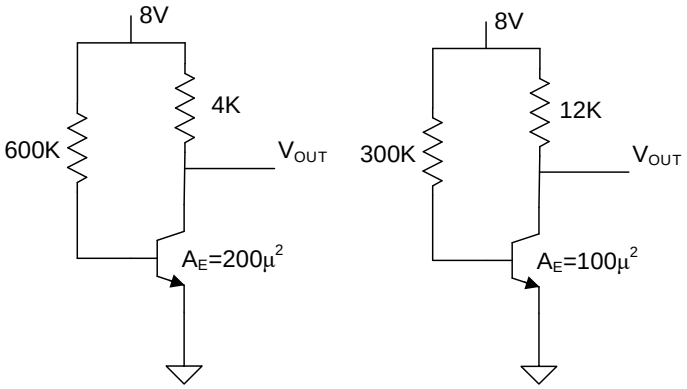
Extra Practice Problems (not collected or graded)

Problem P1

In the circuit shown the dimensions of the transistor are W=10u and L=1u. Assume C_1 and C_2 are very large. Determine the quiescent value of V_D and V_{OUT}

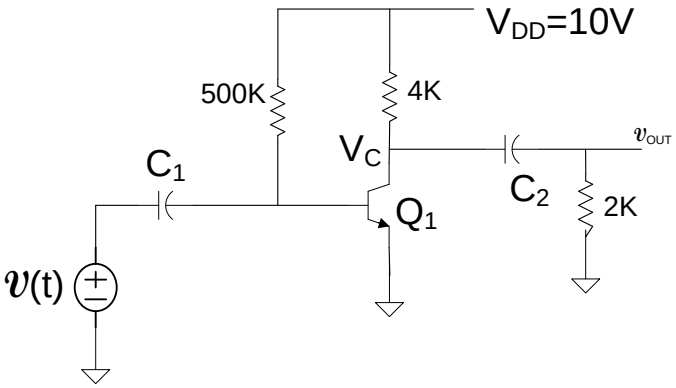
Problem P2

Determine the output voltage for the following circuits



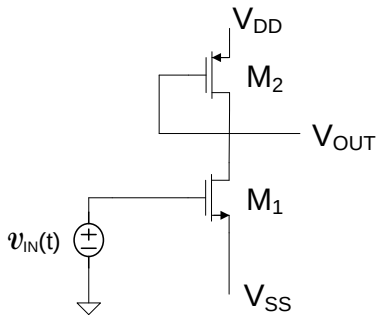
Problem P3

Assume the capacitors are very large. Determine the quiescent value of V_C and V_{OUT},



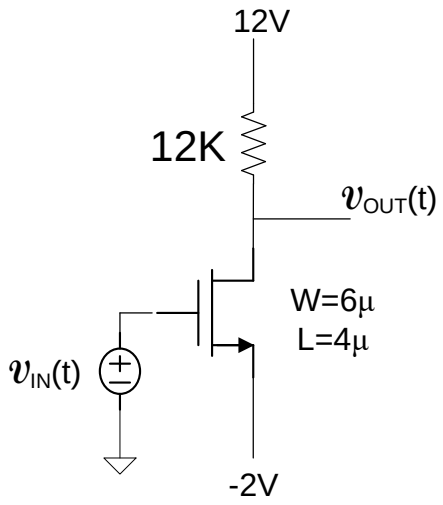
Problem P4

Consider the following circuit. Determine the output voltage if V_{DD}=5V, V_{SS}=-2V, W_1=10u, L_1=2u, W_2=3u and L_2=1u. Assume $\mu_n C_{OX}$ = 350μA/V^2, $\mu_p C_{OX}$ = 70μA/V^2, V_{Tn} = 0.5V, V_{Tp}= -0.5V, C_{OX}=8fF/μ^2, λ = 0, and γ = 0. Assume v_{IN} (t) is very small.



Problem P5

Obtain the quiescent output voltage

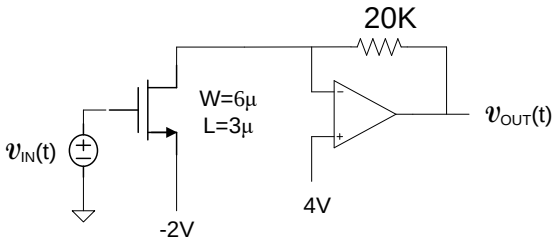


Problem P6

Consider the following circuit where the op amp is assumed to be ideal.

a) Determine the quiescent output voltage.

b) If the input is a 1KHz square wave with high and low values of 0V and 25mV, determine the output voltage

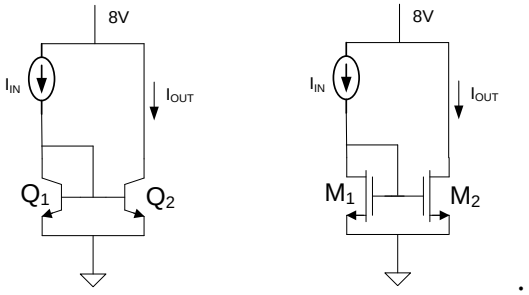


Problem P7

Consider the two circuits shown.

a) Determine the output current for the bipolar circuit if $A_{E1}=300u^2$ and $A_{E2}=1200u^2$ and $I_{IN}=1mA$. Assume β is very large.

b) Determine the output current for the MOS circuit if $W_1/L_1=10$ and $W_2/L_2=20$ and $I_{IN}=1mA$.



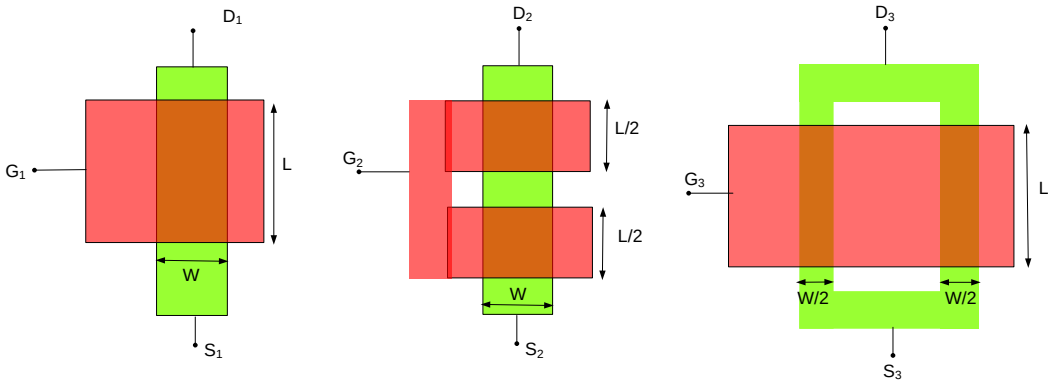
Problem P8

Express the output current for the bipolar circuit in terms of the input current and the emitter areas for the circuit of Problem P7. Assume β is very large. Also

express the output current for the MOS circuit in terms of the input current and the "W/L" ratios for the circuit of Problem P7. What conclusion can be drawn about the relative performance between these two circuits?

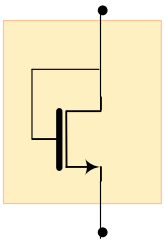
Problem P9

Three devices are shown. The color green is used to denote n-active and the red denotes polysilicon. Relative device dimensions are as indicated. Make a comparison of the performance of these structures.



Problem P10

The circuit shown has been proposed as a rectifier. Compare the dc performance of this circuit to that of the pn junction. Does is behave as a rectifier?



MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.51	volts
SHORT	20.0/0.18			
Idss		547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE	20.0/0.18			
Ids0		14.4	-4.7	pA/um
LARGE	50/50			
Vth		0.43	-0.42	volts
Vjbkd		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.7	7.8	8.0	59.7	313.6	0.08	0.08	ohms/sq

Contact Resistance	10.6	11.0	10.0									4.79	ohms
Gate Oxide Thickness	41												angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08		0.08	0.08	0.03	930	ohms/sq
Contact Resistance	9.24		14.05	18.39	20.69		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34			984		aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235	41	35	29	21	14							aF/um
Fringe (poly)			70	39	29	23	20	17						aF/um
Fringe (metal1)				52	34		22	19						aF/um
Fringe (metal2)					48	35	27	22						aF/um
Fringe (metal3)						53	34	27						aF/um
Fringe (metal4)							58	35						aF/um
Fringe (metal5)								55						aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.72	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		300.36	MHz
DIV1024 (31-stg,1.8V)		363.77	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate