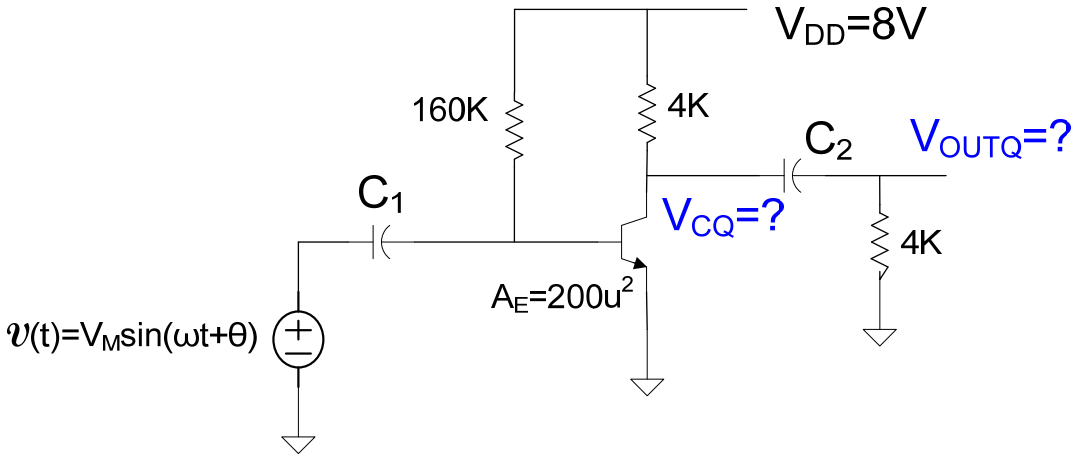
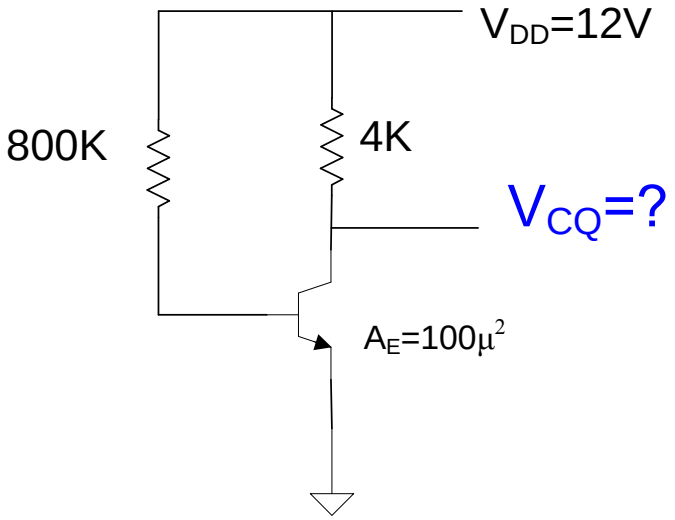
EE 330 Fall 2012
Homework 10

Due Friday October 26 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

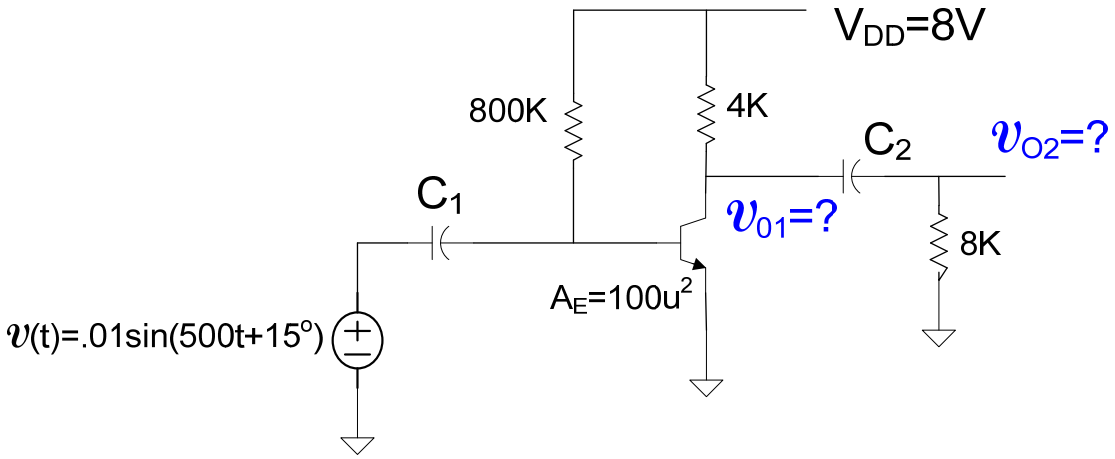
Unless specified to the contrary, assume in the following problems that bipolar devices are from processes with J_S at 300°K of $0.25fA/\mu^2$, β_n=100, βp=25,V_{AF}=100V and all MOS devices are from a process with $\mu_n C_{OX}$=100 μ A/V^2, V_{Tn}=0.75V, V_{TP}= -0.75V, λ=.01V^{-1}, γ= 0.4$V^{-1/2}$, and μ_n/μ_p=3.

Problem 1 (10 points):
Determine the voltages indicated with a "?" Assume C_1 and C_2 are large.

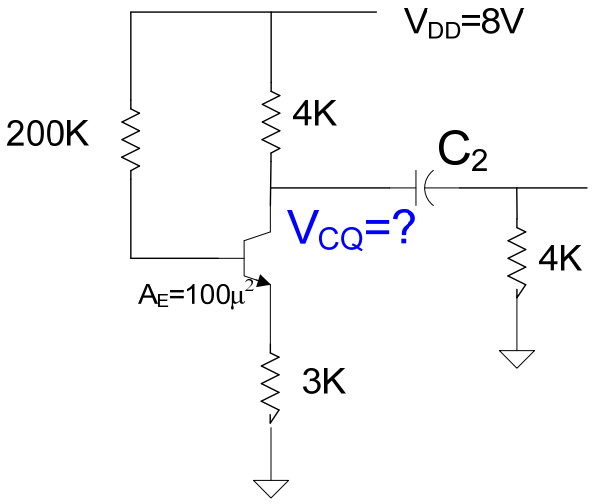


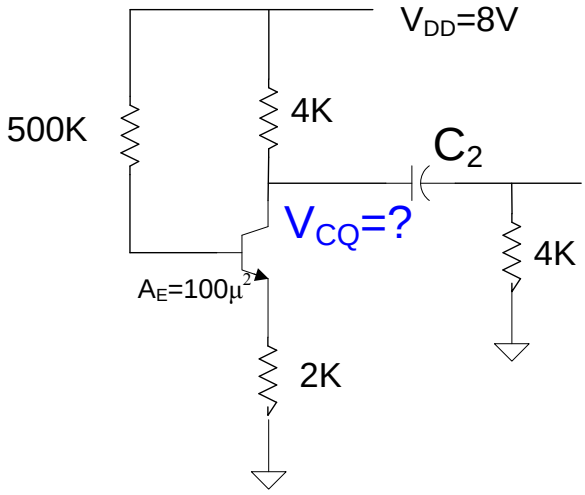


Problem 2 (10 points):
Determine the small signal output voltages indicated with a "?". Assume C_1 and C_2 are large.

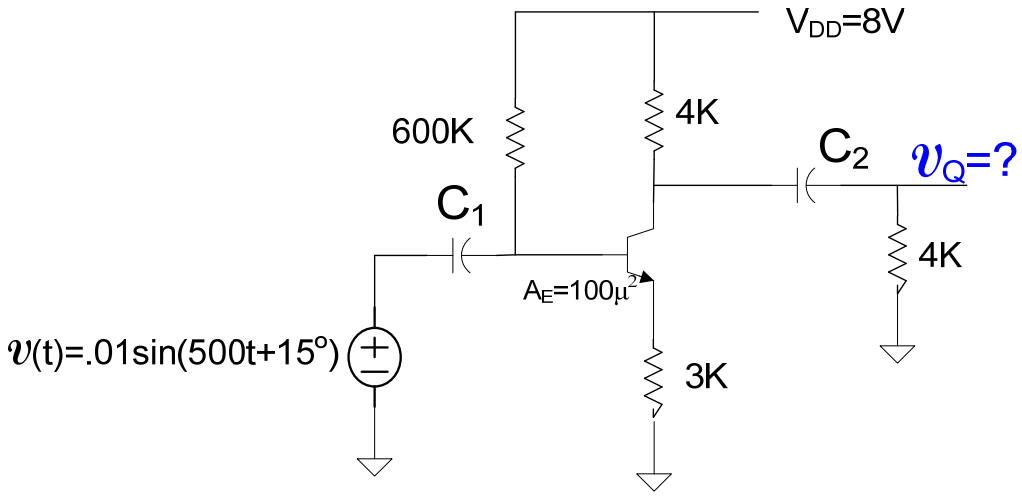


Problem 3 (10 points):
Determine V_{CQ}. Assume C_2 is large.

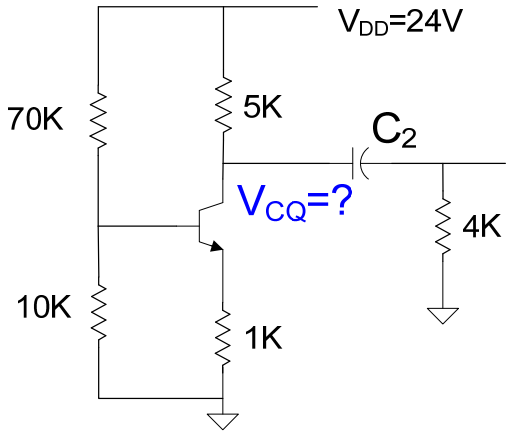


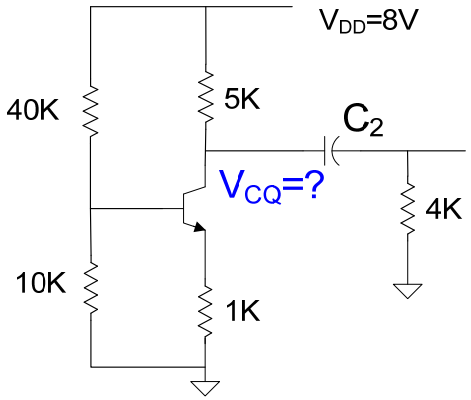


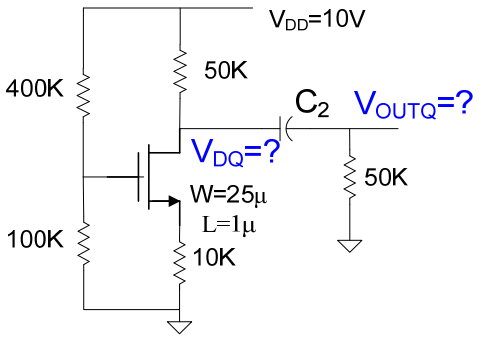
Problem 4 (10 points):
Determine the small signal output voltage. Assume C_1 and C_2 are large.

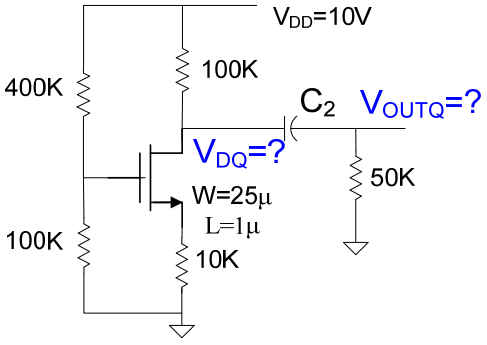


Problem 5 (10 points):
Determine V_{CQ} and V_{OUTQ} where indicated.

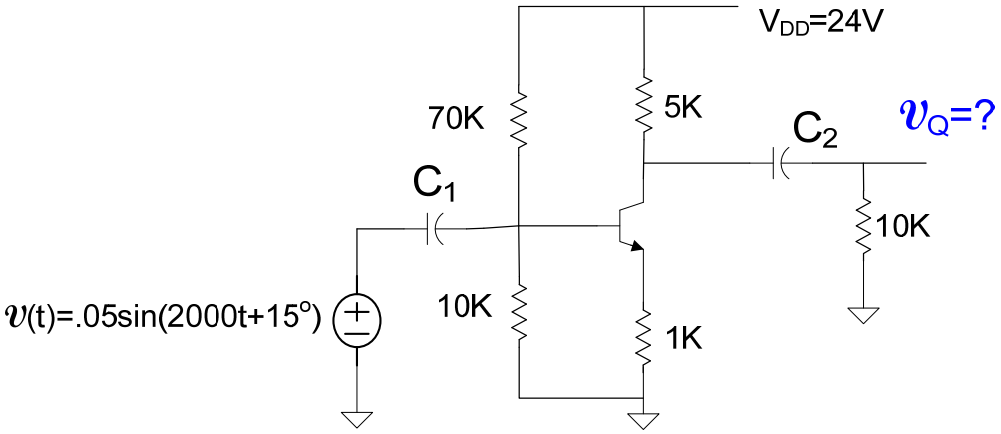


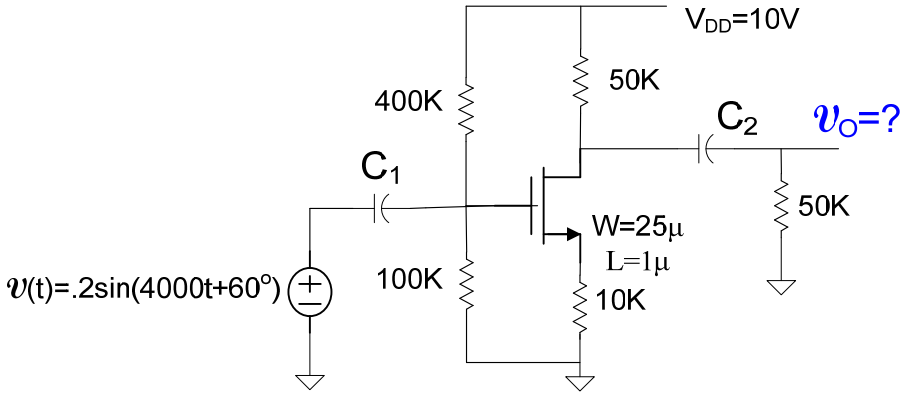






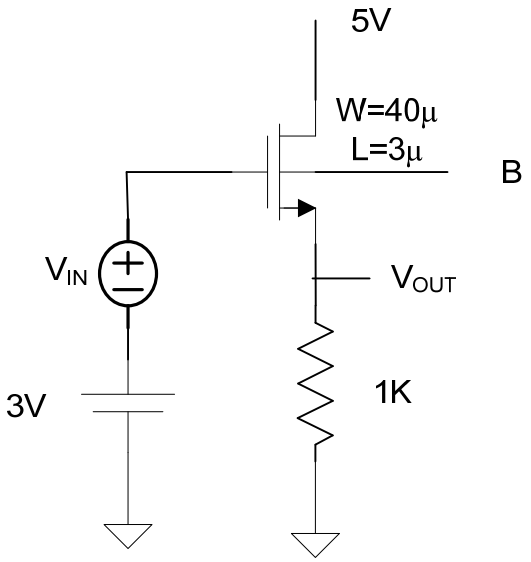
Problem 6 (10 points):
Determine the small signal output voltages. Assume C_1 and C_2 large.



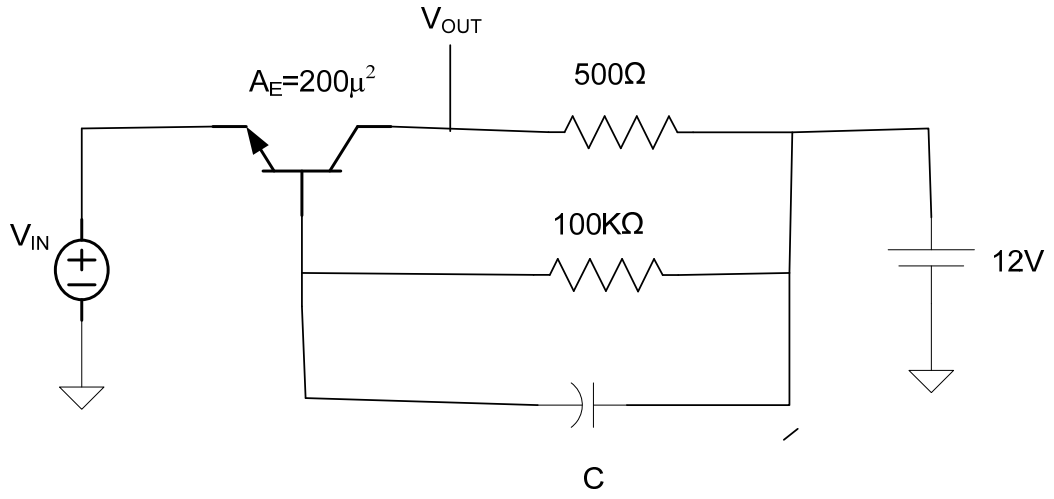


Problem 7 (10 points):
For the following circuit:

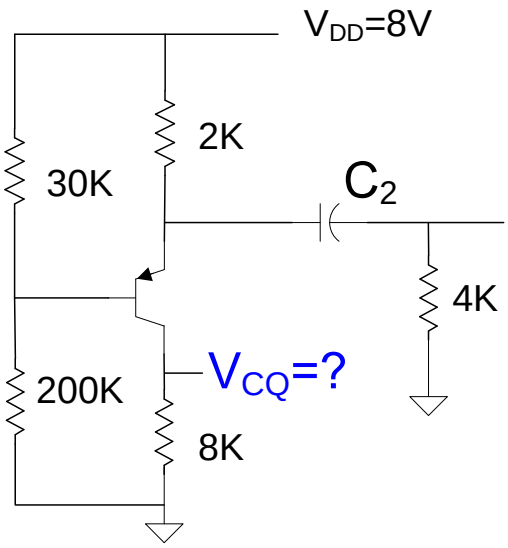
a) Obtain the Quiescent output voltage if the bulk denoted as B is connected to ground
b) Repeat part a) if the bulk is connected to the source
c) Obtain the small signal voltage gain if the bulk is connected to ground
d) Repeat part c) if the bulk is connected to the source

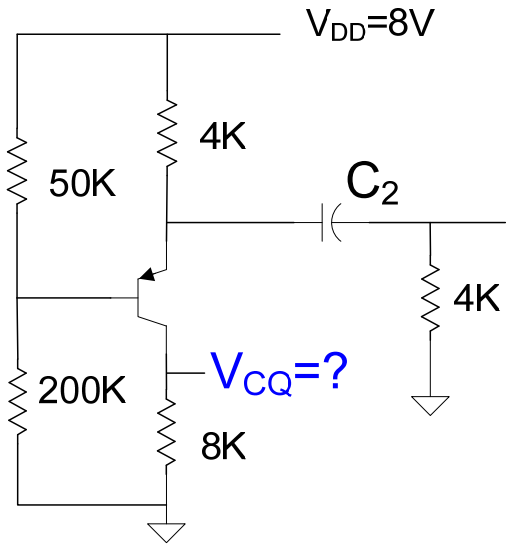


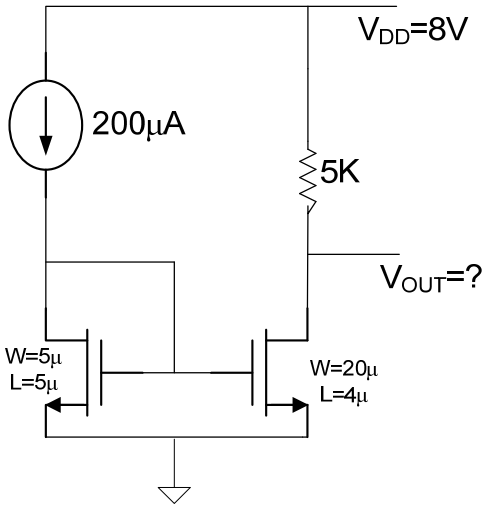
Problem 8 (10 points):
Determine the quiescent output voltage and the small signal voltage gain for the following circuit. Assume the capacitor C is very large.

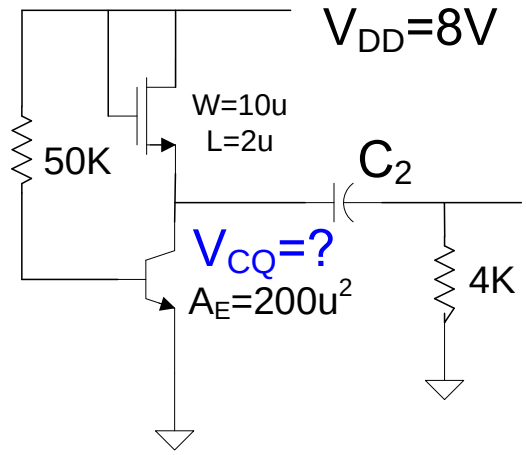


Problem 9 (10 points):
Determine the variables indicated with a "?"

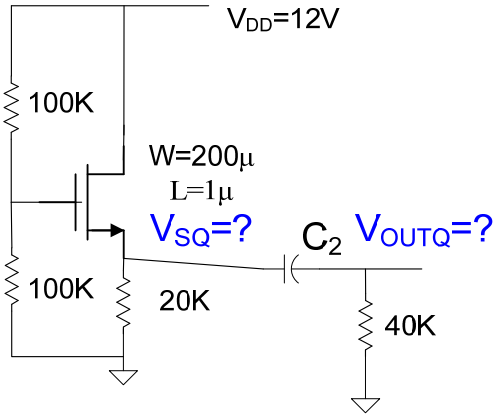


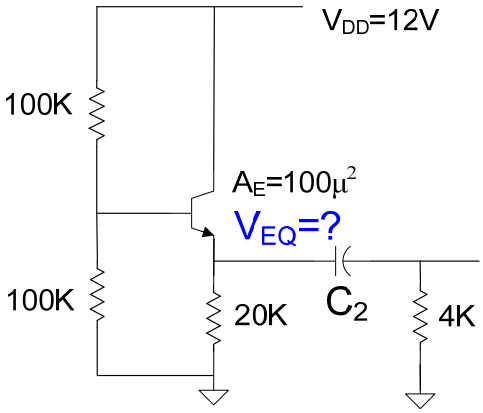


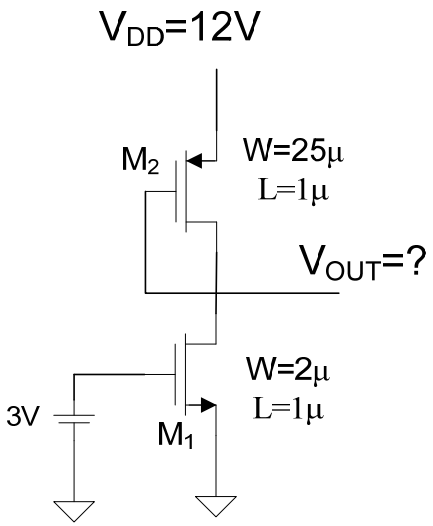


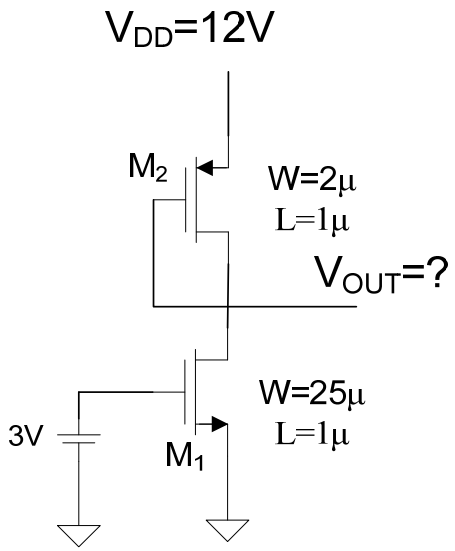


Problem 10 (10 points):
Determine the variables indicated with a "?"

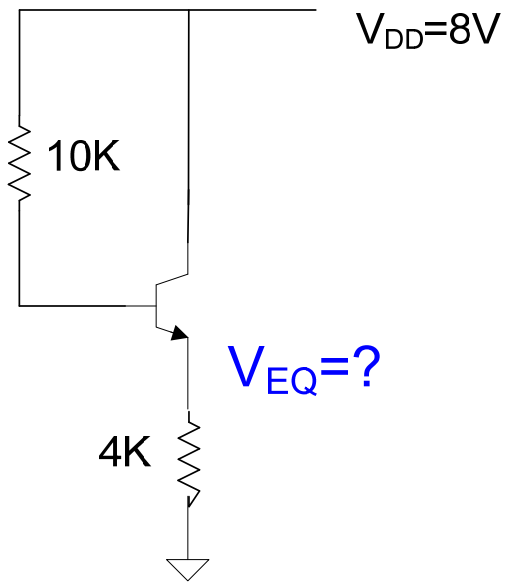


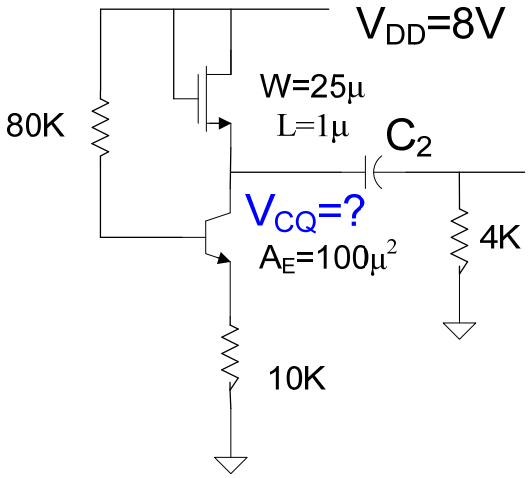


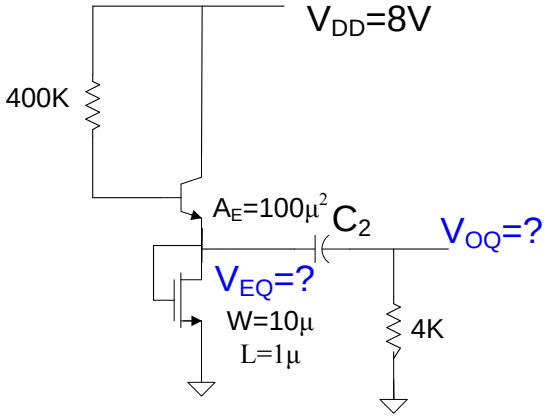


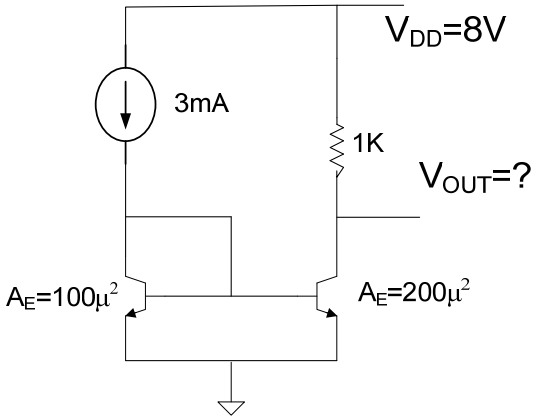


Problem 11 (10 points extra credit):
Determine the variables indicated with a "?"









Problem 12 (10 points extra credit):
For two single-bit inputs A and B, in Verilog, provide the following two-input gates: AND, OR, NAND, NOR, XOR. They may all be outputs of the same module. Demonstrate your code with proper simulation.