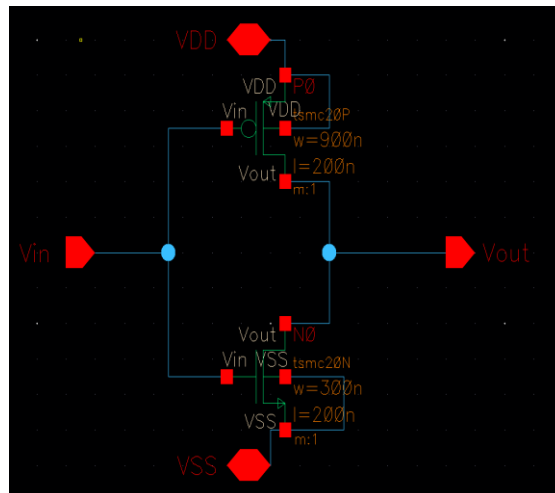
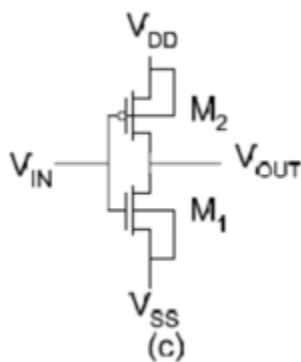


Introduction:

In this lab I refreshed my mind on Boolean algebra and built a CMOS circuit. I also built the layout of a PMOS transistor. The CMOS inverter and the n used I to create a cascaded inverter circuit to observe the time domain behavior of the circuit.

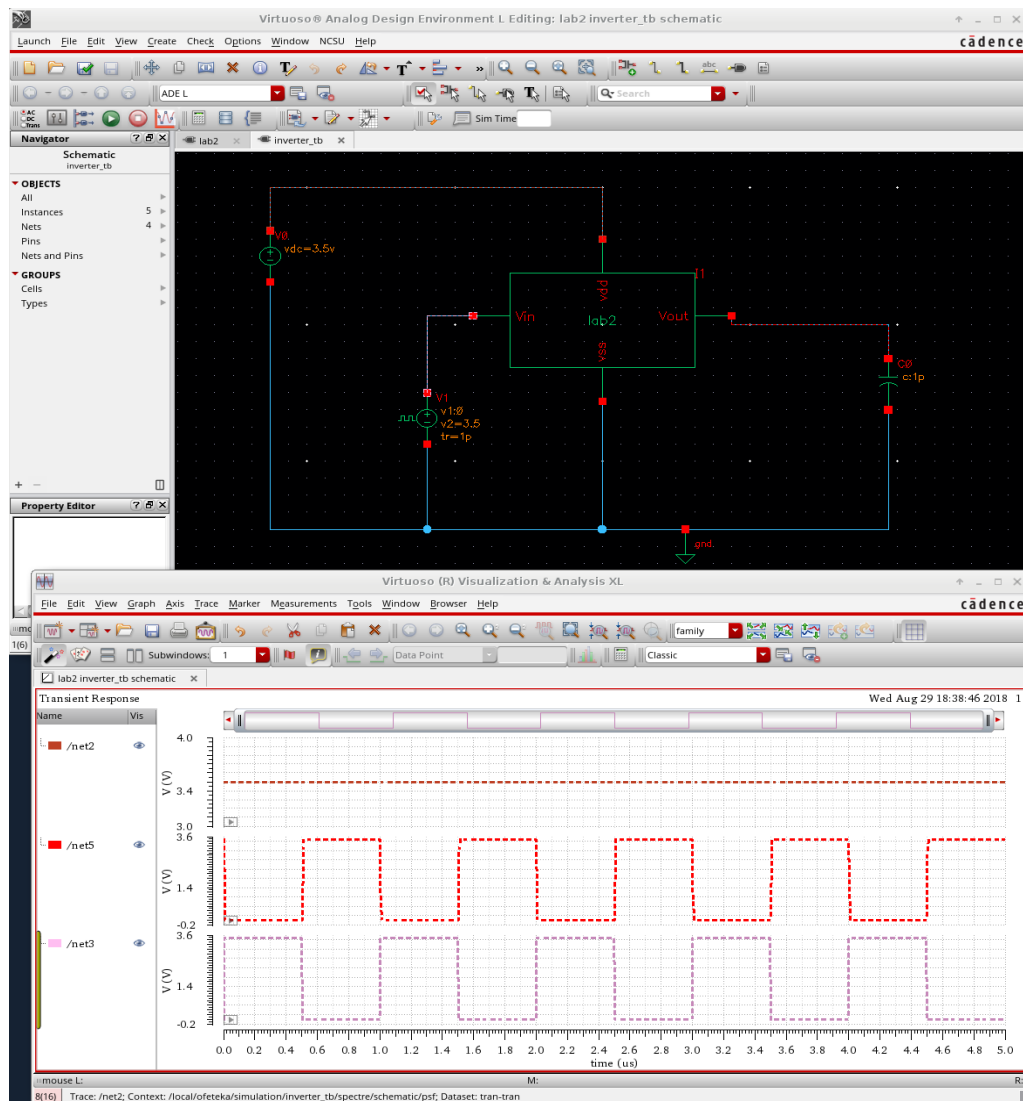
Part 2: Simulation of a CMOS Inverter

Schematic design



The schematic design was based on the design in figure 1 with the NMOS as nmos4 and PMOS as pmos4 in the analoglib. The values of width and length of the MOSFETS were set according to the data given.

2.3_4 symbol creation and inverter transient stimulation



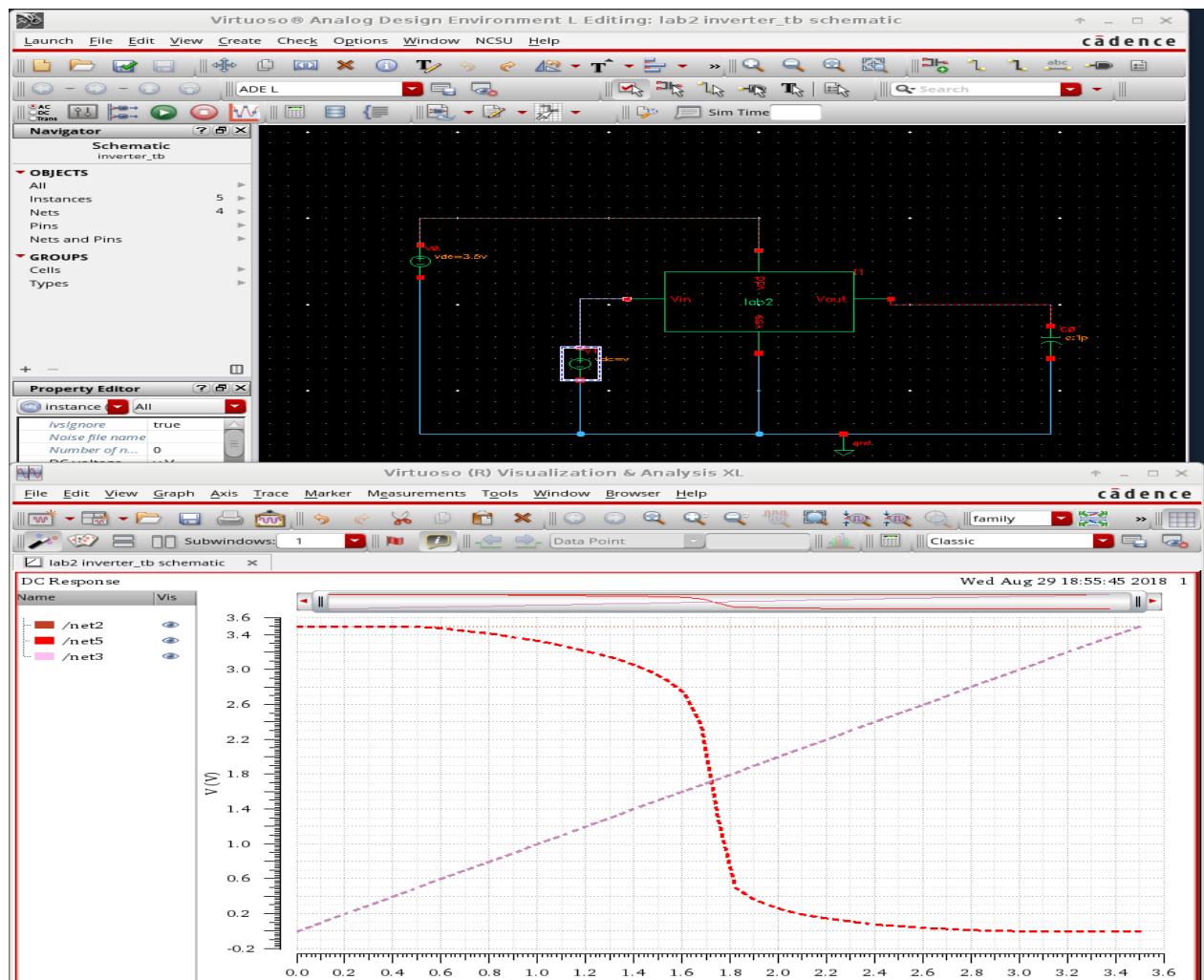
By using vsources from analogLib, I set the DC voltage to 3.5 V, zero value of 0 V, one value of 3.5 V, waveform period of 1u s, rise & fall time of 1p s, and linear type of rising & falling edge.

For powering the inverter (VDD and VSS), I used a Vdc of 3.5 V and Vss to 0v.

In the Analog Design Environment (ADE L), I set the transient analysis to run about 10u s

Part 2.5 Inverter transfer characteristic simulation

In this part I used the Dc sweep configuration where the voltage was just set as V but will range from 0V to 3.5V. when the voltage reaches around 1.7 V, input and output is equal. The maximum value of VIN that can be applied and still keep the output near VDD is about 0.5 V. The minimum value of VIN that will keep the output near 0V is about 2.7 to 2.8 V.



Part2.6 Inverter driving a load

From the transient analyses of the Figures below, we can see that with input signals remain the same, there are different changes in output when the capacitance load of the circuit is being changed. This is because when we increase the capacitance load, it takes longer time for the capacitor to charge or discharge. Therefore, it produces the following changes for the output in the transient response.

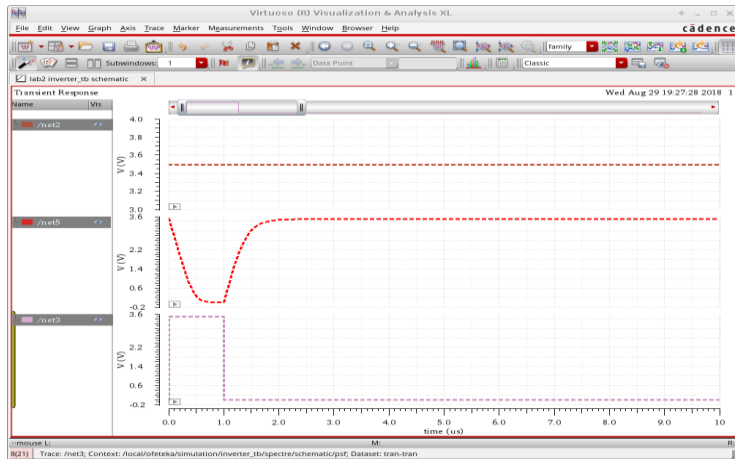


Figure 1 100pF

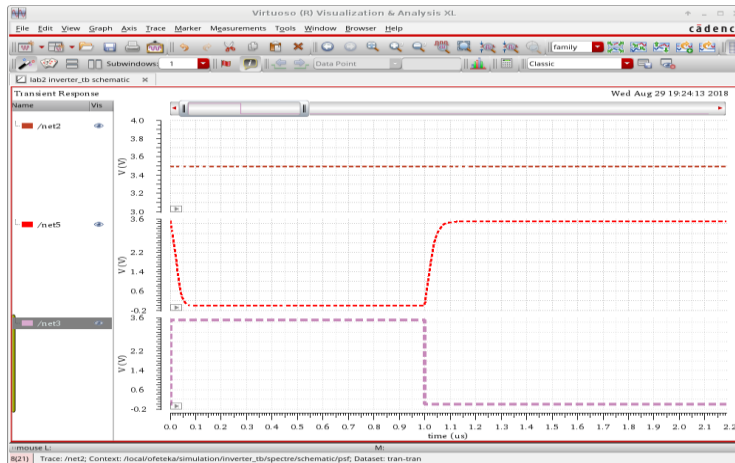


Figure 2 10pF

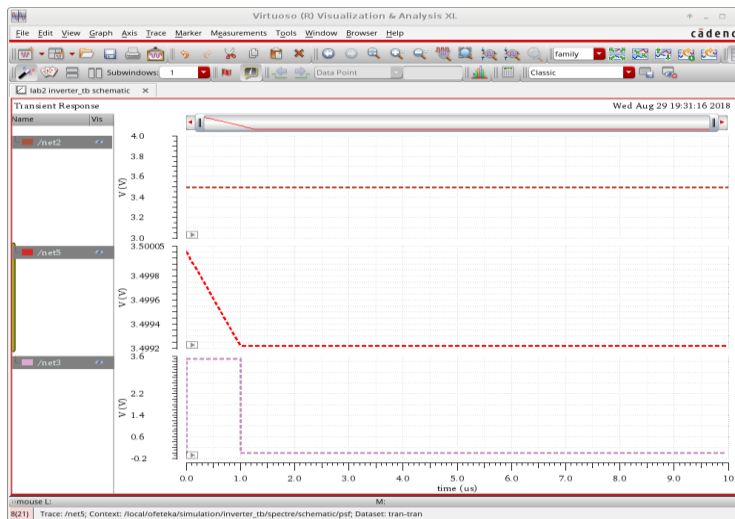
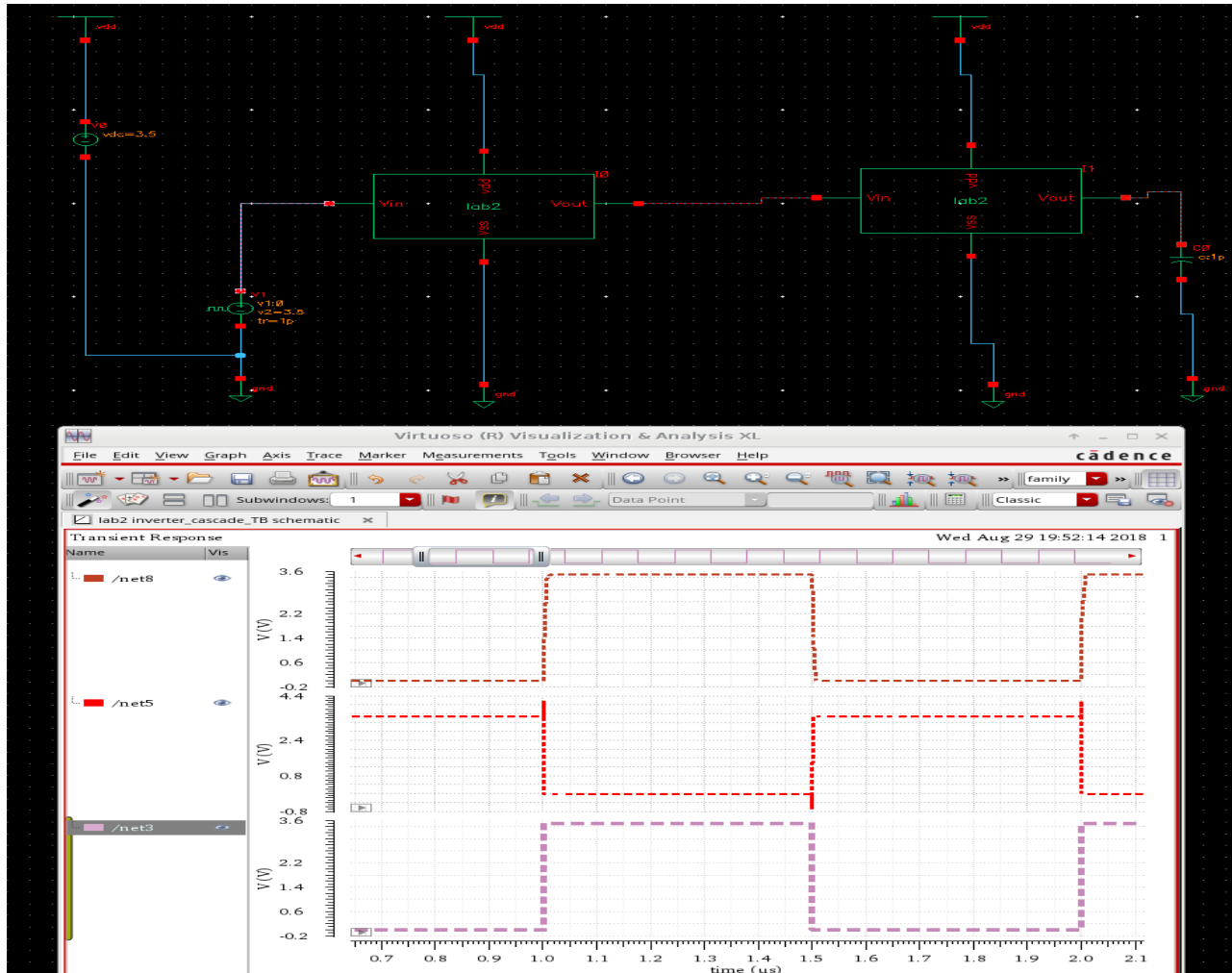


Figure 3 1uF

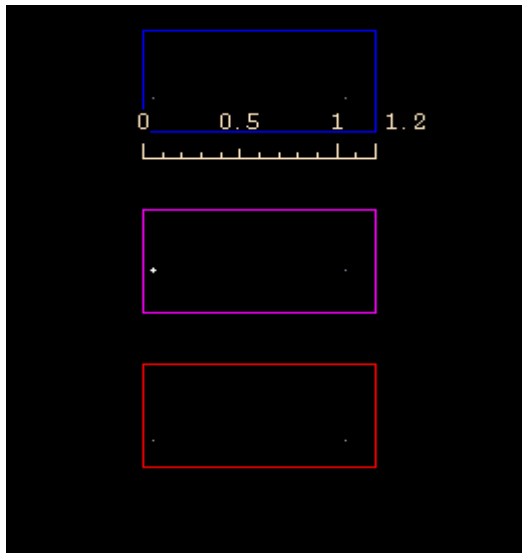
Part 3 Cascaded Inverters



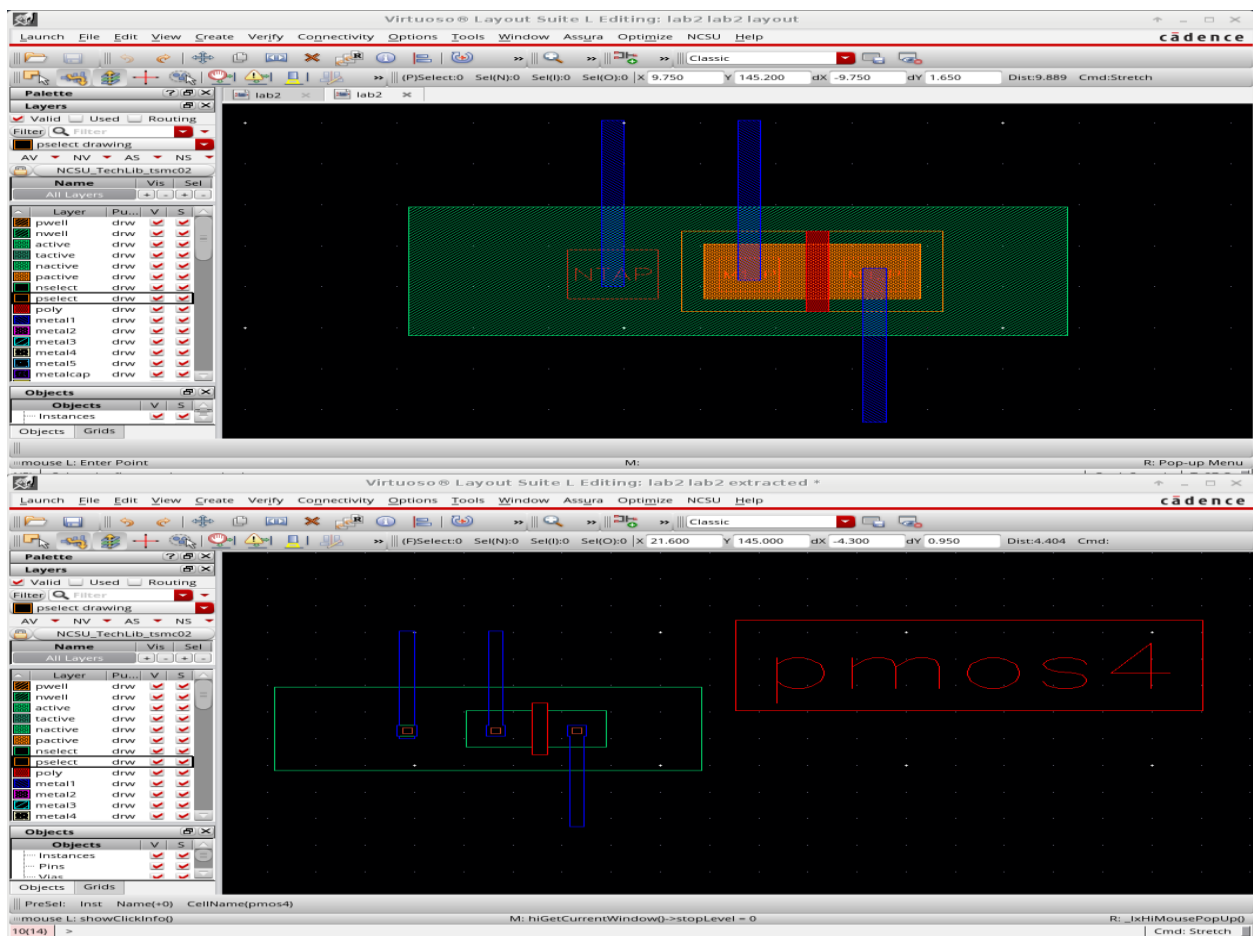
In the schematic design, I labeled input of inverter 1 as net8, output of inverter 1 as net5, and output of inverter 2 as net3. From the transient analysis, we can see that input of inverter 1 is almost exactly the same as output of inverter 2. But from the DC response, we do see that they have a little loss of signal integrity but there is a small delay that can be neglected.

Part4 Introduction to Layout

In this part I was to familiarize myself with the layout XL tool. This is the tree rectangles (metal1, metal2, and poly) of dimensions 0.6 microns by 0.2 microns with the ruler.



Layout of a PMOS transistor



As shown in the layout below, the layout of a PMOS transistor is made out of 6 parts, the M1_P, NTAP, M1_POLY, Nwell, meatal1, and Pselect labeled as follow.

M1_P, the connection between the drain and the source

NTAP, used to connect the bulk of the PMOS device

M1_POLY, the active part of the transistor

Nwell, the highly doped area of the transistor

meatal1, serve for connection to the source, drain and gate to an external device

Conclusion:

From this lab, I've learned more on how to draw a schematics circuit especially on creating a symbol cell for the schematic design. I also learn how to draw the layout of transistor. Also the size of the transistor models will also affect the results that we are getting.