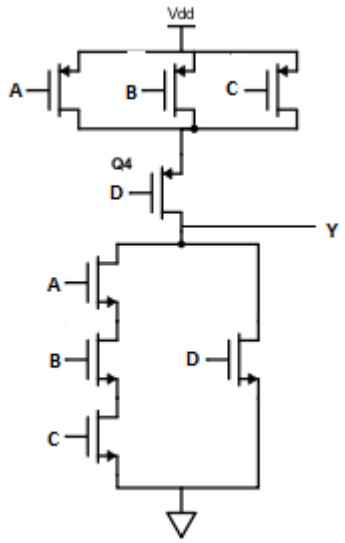
Homework 3 Spring 2018 TA: George Alphonse

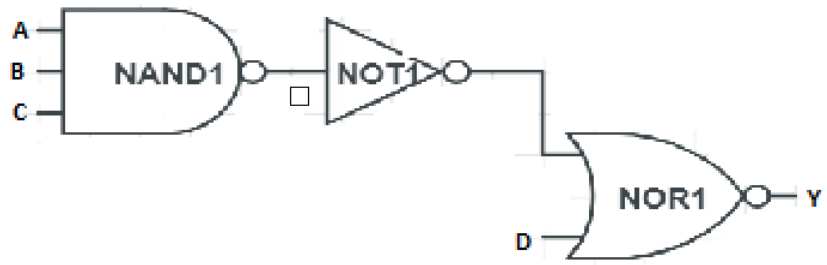
Problem 1.)

$Y = \overline{ABC + D}$

Example of compound gate using 8 Transistors

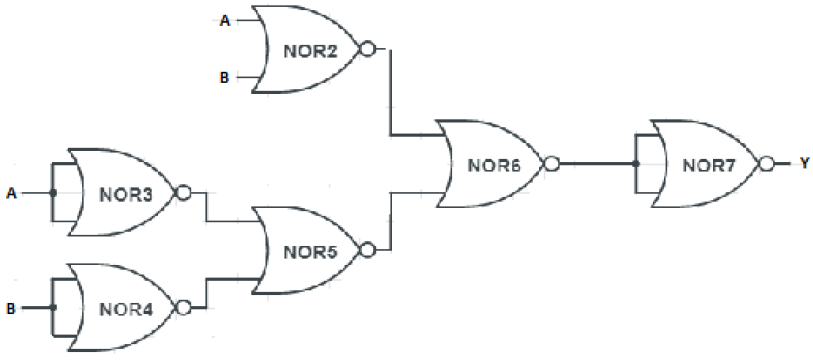


Example using static CMOS gates using 12 Transistors



Problem 2.)

$Y = \bar{A}\bar{B} + AB = \overline{A + B} + \overline{\bar{A} + \bar{B}}$

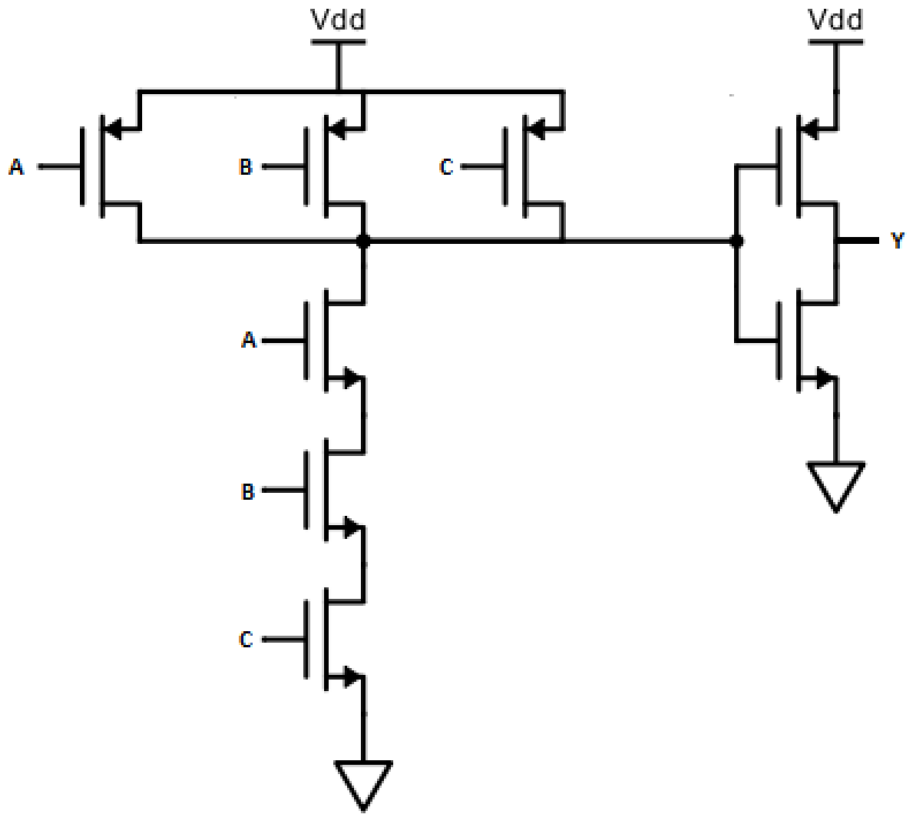


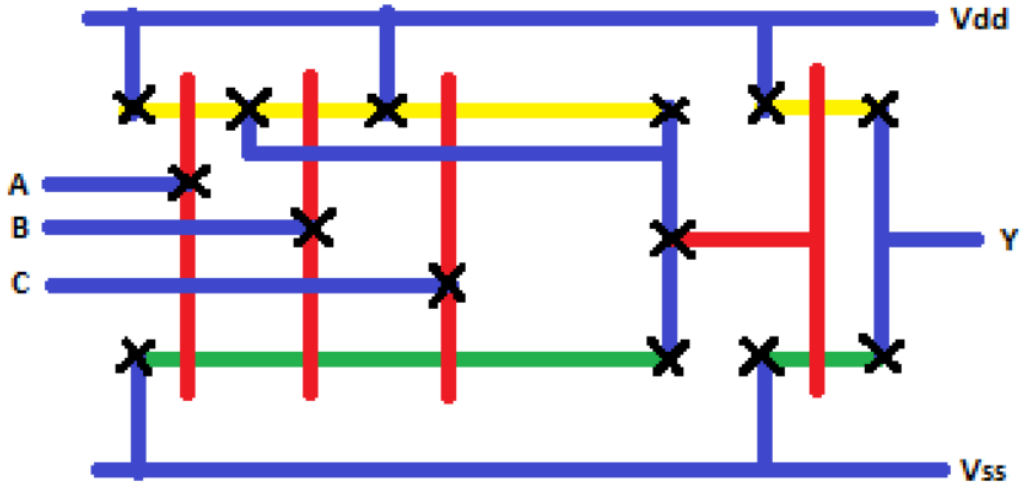
Problem 3.)

For minimum sized CMOS NAND gate, R_{SWN} = 4kΩ

$t_{HL} = R_{SWN} * C_L$ = 4kΩ * 60fF = 240 ps

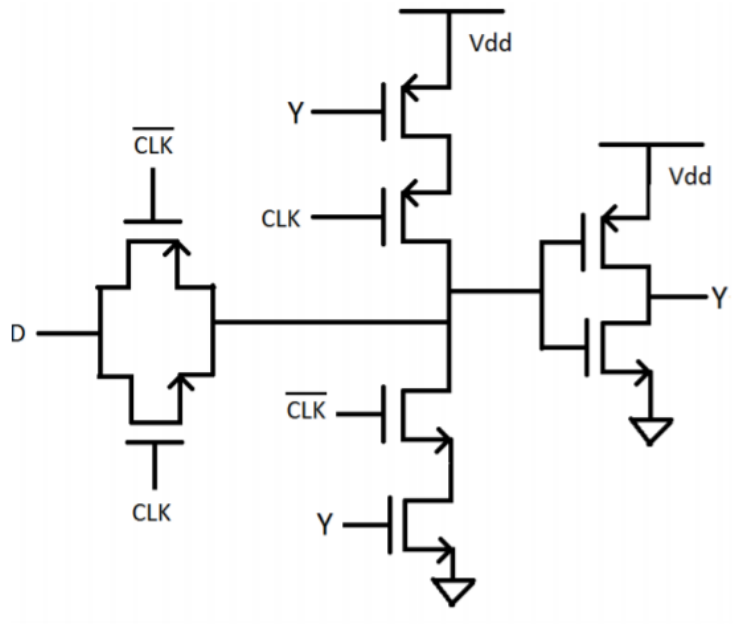
Problem 4.)



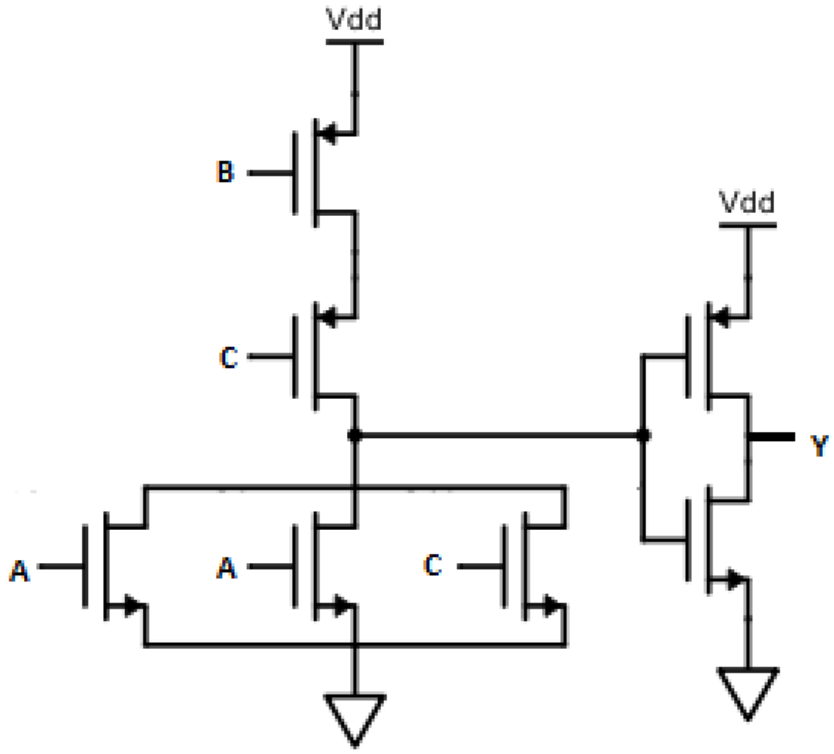


Problem 5.)

The second inverter is combined with the transmission gate, rather than two separate components.

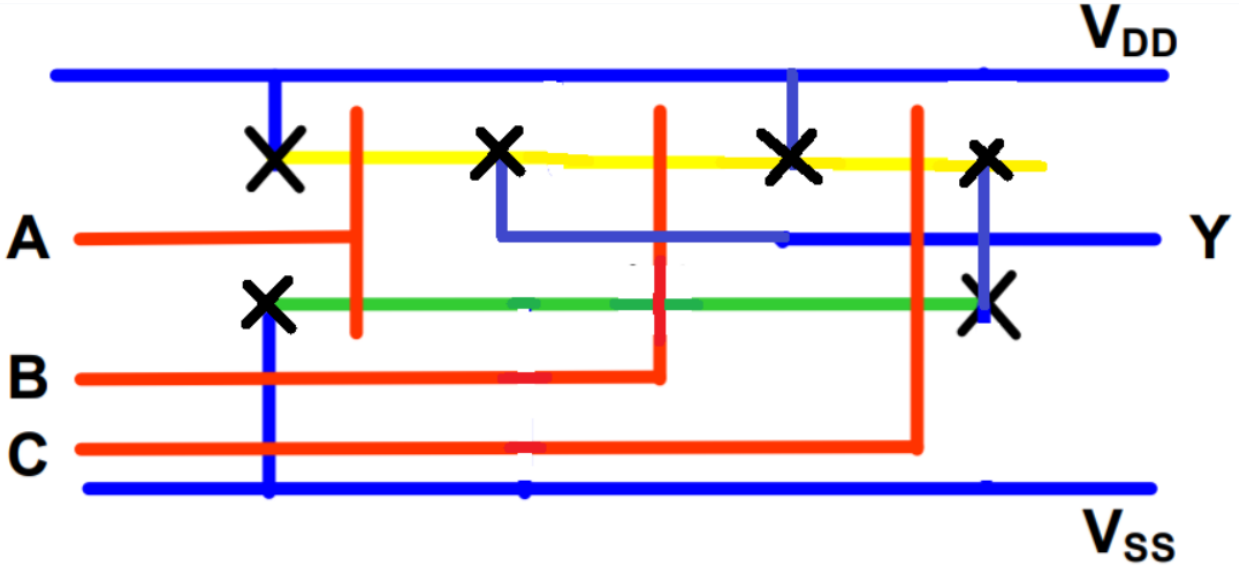


Problem 6.)



Problem 7.)

Reorder the metal1 connections to the pactive as shown below
Remove the metal1 between the A and B inputs over the nactive
Connect Y to the end of the nactive
Remove the contact over the poly and the nactive



Problem 8.)

a.) $R_W = \frac{2.82\times10^{-8}}{0.2um} * \frac{180um+20um+20um-5um}{5um} = 6.02\ \Omega$

$V_{Resistor} = \frac{50\Omega}{50\Omega+6.02\Omega} * 5V = 4.46\ V$

b.) $R_W = \frac{1.68\times10^{-8}}{0.2um} * \frac{180um+20um+20um-5um}{5um} = 3.66\ \Omega$

$V_{Resistor} = \frac{50\Omega}{50\Omega+3.66\Omega} * 5V = 4.66\ V$

c.) $5 - 5 \times .05 = 4.75\ V$

$4.75\ V = 5V * \frac{50}{50+R_W} \rightarrow R_W = 2.63\ \Omega$

$2.63\ \Omega = \frac{2.82\times10^{-8}}{0.2\ um} * \frac{180um+20um+20um-5um}{W} \rightarrow W \geq 11.5\ um$

Problem 9.)

Each inverter has $C_L = 1.5\ fF + 1.5\ fF = 3fF$
total load capacitance $C = 3\ pF * 12 = 36\ fF$
$R_{SWp} = 6k\Omega \rightarrow T_{LH} = 6\ k * 36\ f = 216 * 10^{-12}s = 216\ ps$

Problem 10.)

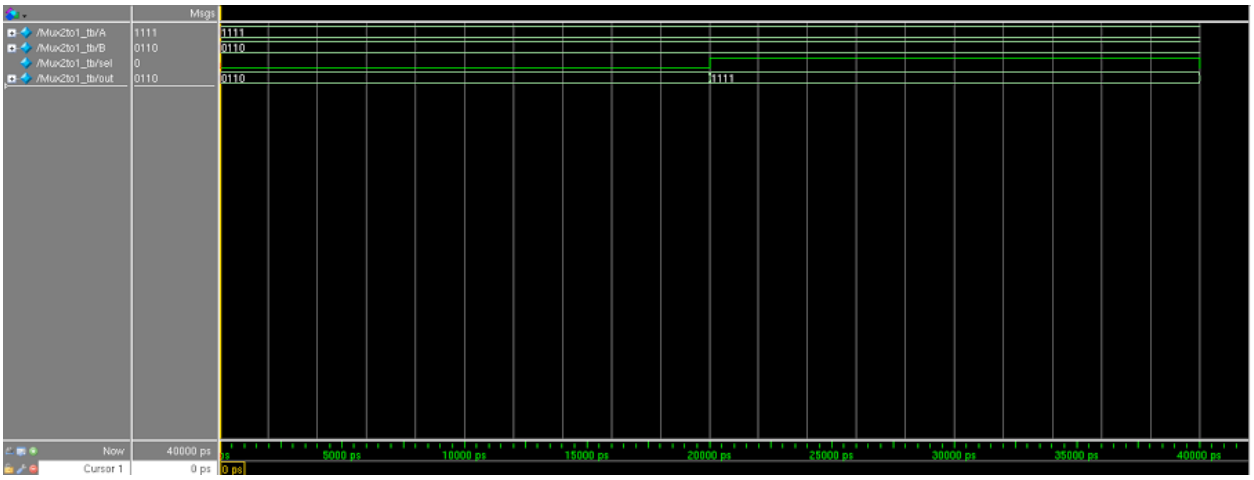
2to1Mux

/home/alphonse/ee330/verilog/Mux2to1.v (/Mux2to1

```
Ln#
 1  `timescale 1ns/1ps
 2  module Mux2to1(In1, In2, sel, out);
 3      input [3:0] In1, In2;
 4      input sel;
 5      output [3:0] out;
 6      wire [3:0] out;
 7
 8      assign out = sel ? In1 : In2;
 9  endmodule
```

/home/alphonse/ee330/verilog/Mux2to1_tb.v (/Mux2to1_tb) - Default

```
Ln#
 1  `timescale 1ns/1ps
 2  module Mux2to1_tb();
 3    reg[3:0] A, B;
 4    reg sel;
 5    wire [3:0] out;
 6
 7    Mux2to1 mux1(.In1(A), .In2(B), .sel(sel), .out(out));
 8
 9    initial begin
10      A = 4'b1111;
11      B = 4'b0110;
12      sel = 0;
13    end
14
15    always
16      #20 sel <= ~sel;
17  endmodule
```



4to1Mux

/home/alphonse/ee330/verilog/Mux4to1.v (/Mux4to1_tb/gate1) - Default

```
Ln#
 1
 2  `timescale 1ns/1ps
 3  module Mux4to1(In1, In2, In3, In4, sel, out);
 4      input [3:0] In1, In2, In3, In4;
 5      input [1:0] sel;
 6      output [3:0] out;
 7      wire [3:0] out, mux1, mux2;
 8
 9      Mux2to1 gate1(.In1(In1), .In2(In2), .sel(sel[0]), .out(mux1));
10      Mux2to1 gate2(.In1(In3), .In2(In4), .sel(sel[0]), .out(mux2));
11      Mux2to1 gate3(.In1(mux1), .In2(mux2), .sel(sel[1]), .out(out));
12  endmodule
```

/home/alphonse/ee330/verilog/Mux4to1_tb.v (/Mux4to1_tb) - Default

```
Ln#
 1  `timescale 1ns/1ps
 2  module Mux4to1_tb();
 3    reg[3:0] A, B, C, D;
 4    reg [1:0] sel;
 5    wire [3:0] out;
 6
 7    Mux4to1 gate1(.In1(A), .In2(B), .In3(C), .In4(D), .sel(sel), .out(out));
 8
 9    initial begin
10      A = 4'b1111;
11      B = 4'b0110;
12      C = 4'b1001;
13      D = 4'b0000;
14      sel = 2'b00;
15    end
16
17    always
18      #20 sel <= sel+1;
19  endmodule
```