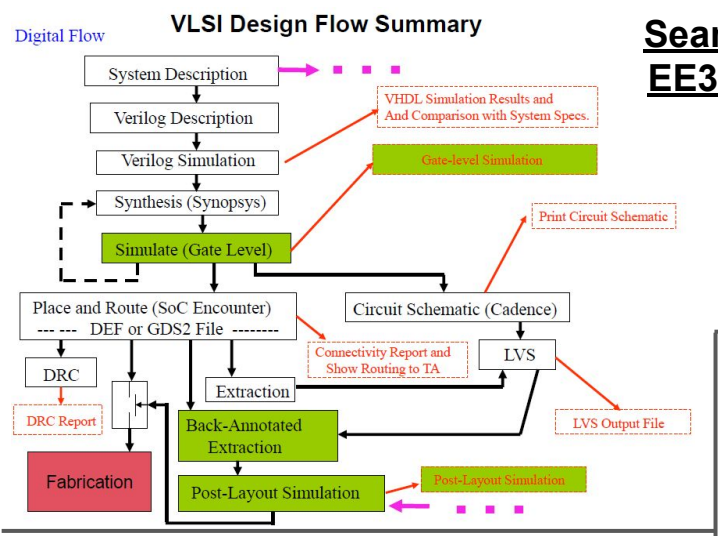
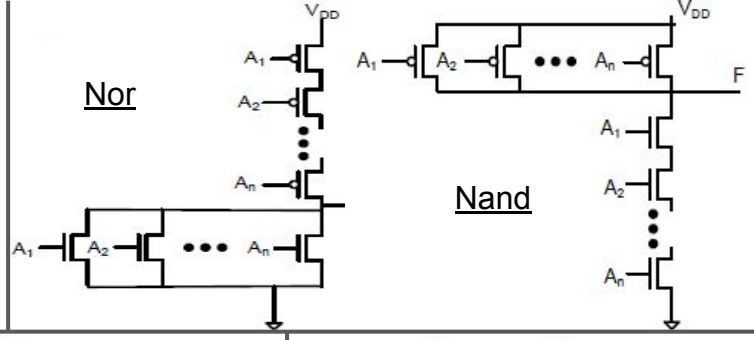
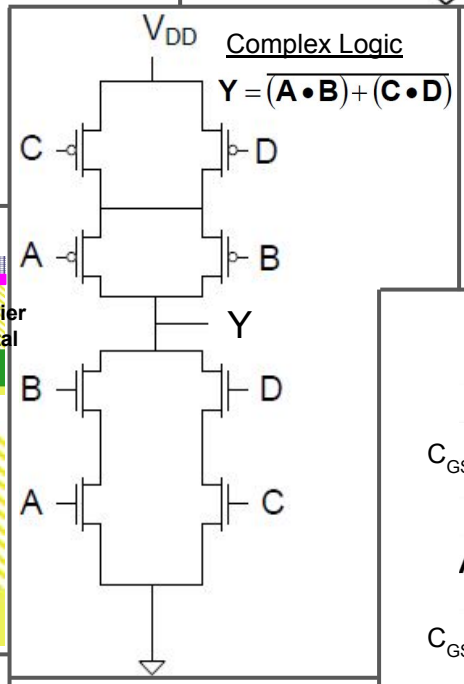
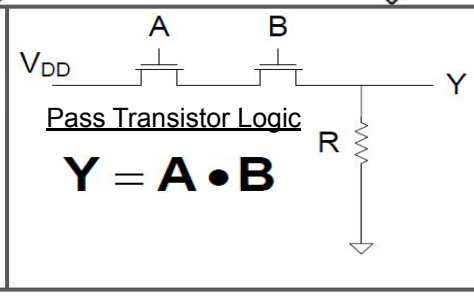
Sean Gordon EE330 Notes

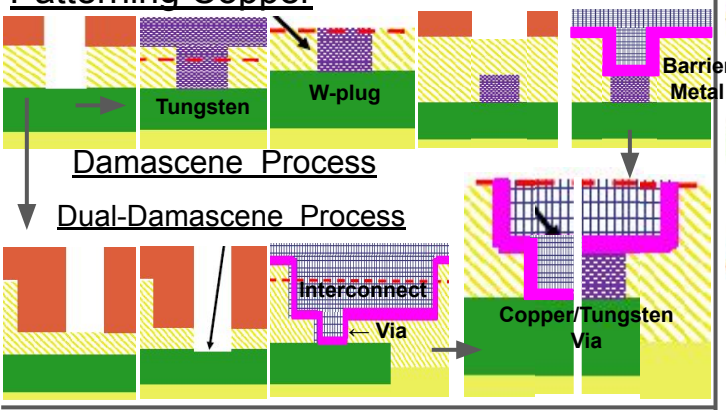




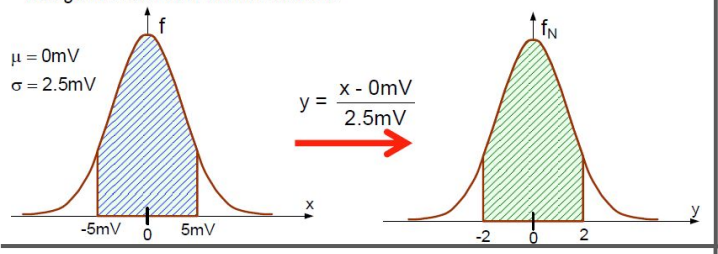




Patterning Copper



Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the standard deviation of the offset voltage is 2.5mV and the mean is 0V.

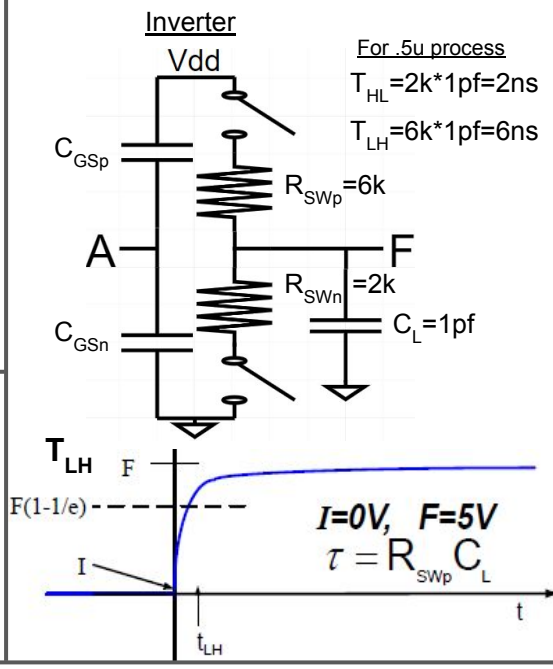


Diode Stuff

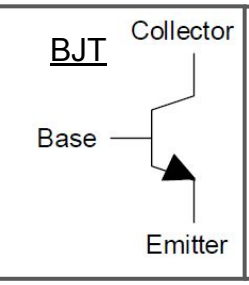
$I_d = I_S(e^{(Vd/Vt)}-1)$ Approx Vd = .7v

Common Dopants:

Boron: Used for P-type
Phosphorus: N-type, bulk dope, diffuses fast
Arsenic: N-type, Active region dope, diffuses slower



Julius E. Lilenfeld invented Field Effect Transistor.
Oskar Heil improved the MOSFET



William Shockley fathered transistor, discovered junction transistor, used it to create silicon valley. Company spawned Fairchild semiconductors

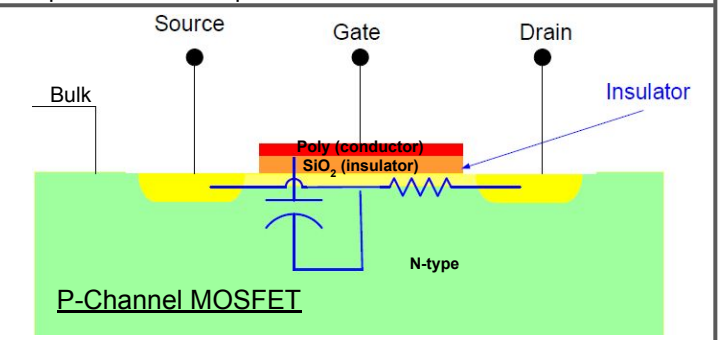
Hard Faults: $Y_H = e^{-Ad}$,

A=area, d=defect dens. (e.g. $2cm^{-2}$)

$C_{Good} = C_{fab}/(Y_H Y_S)$

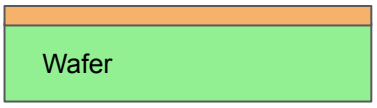
Jack Kilby built first electronic circuit. All components were on chip ½ size of paperclip.

Robert Noyce founded Fairchild and Intel. Invented integrated chip. Oversaw microprocessor invention.



Use masks or reticles to define features on a wafer

- Masks same size as wafer
- Reticles used for projection
- Reticle much smaller (but often termed mask)
- Reticles often of quartz with chrome
- Quality of reticle throughout life of use is critical
- Single IC may require 20 or more reticles
- Cost of "mask set" now exceeds $1million for state of the art processes
- Average usage 500 to 1500 times
- Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
- Serve same purpose as a negative (or positive) in a photographic process
- Usually use 4X optical reduction - exposure area approx. 860mm²
  (now through 2022 ITRS 2007 litho, Table LITH3a)



Photolithography: Process of transferring geometric shapes from a mask onto the surface of a wafer.
Involves cleaning, barrier layer formation, photoresist application, soft baking, mask alignment, exposure and development, and finally soft baking.
After cleaning, silicon dioxide (barrier layer) deposited. Then photoresist applied, usually with a centrifuge. Layer usually 1u thick.

Positive - When resist is exposed to UV, becomes more soluble. Mask therefore holds exact pattern of what will remain.
Negative - When exposed, polymerizes and developer solution removes only unexposed portions. Leaves 'negative' of pattern to be transferred.

Deposition

Application of something to the surface of the silicon wafer or substrate
- Layers 15A to 20u thick

Methods
- Physical Vapor Deposition (nonselective)
  - Evaporation/Condensation
  - Sputtering (better host integrity)
- Chemical Vapor Deposition (nonselective)
  - Reaction of 2 or more gases with solid precipitate
  - Reduction by heating creates solid precipitate (pyrolytic)
- Screening (selective)
  - For thick films
  - Low Tech, not widely used today

Implantation

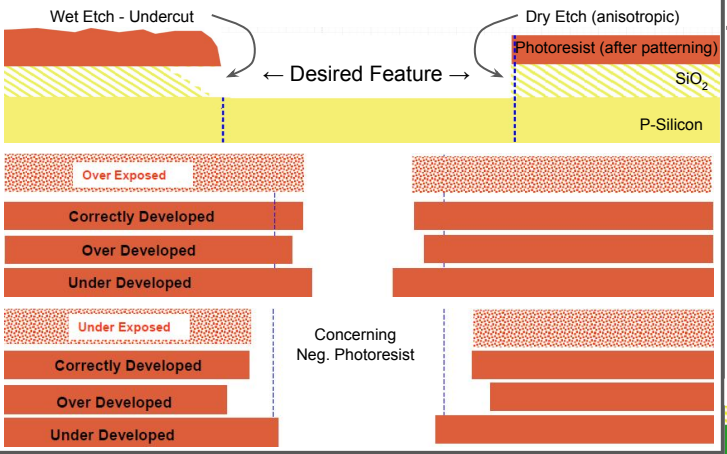
Application of impurities into the surface of the silicon wafer or substrate
- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security

Etching

Selective Removal of Unwanted Materials

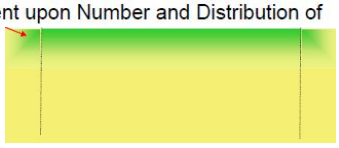
> Wet Etch
- Inexpensive but under cutting a problem

> Dry Etch
- Often termed ion etch or plasma etch



Diffusion

Controlled Migration of Impurities
- Time and Temperature Dependent
- Both vertical and lateral diffusion occurs
- Crystal orientation affects diffusion rates in lateral and vertical dimensions
- Materials Dependent
- Subsequent Movement
- Electrical Properties Highly Dependent upon Number and Distribution of Impurities
- Diffusion at 800°C to 1200°C



Source of Impurities
- Deposition
- Ion Implantation
  - Depth depending on ion speed/enery
  - More accurate control of doping levels
  - Fractures silicon crystaline structure during implant
  - Annealing occurs during diffusion

Types of Impurities
- n-type Arsenic, Antimony, Phosphorous
- p-type Gallium, Aluminum, Boron

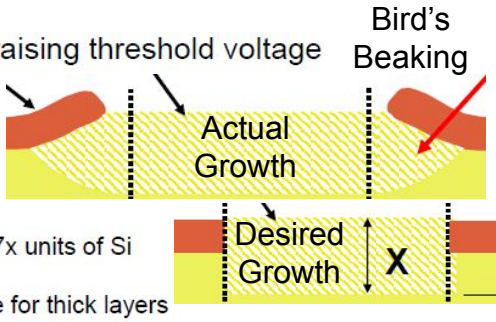
Oxidation

SiO_2 is widely used as an insulator
- Excellent insulator properties

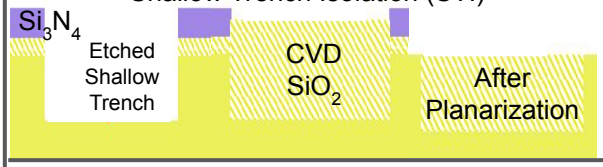
Used for gate dielectric
- Gate oxide layers very thin

Used to separate devices by raising threshold voltage
- termed field oxide
- field oxide layers very thick

Methods of Oxidation
- Thermal Growth (LOCOS)
  - Consumes host silicon
  - x units of SiO_2 consumes .47x units of Si
  - Undercutting of photoresist
  - Compromises planar surface for thick layers
  - Excellent quality
- Chemical Vapor Deposition
  - Needed to put SiO_2 on materials other than Si

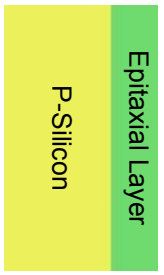


Shallow Trench Isolation (STI)



Epitaxy

Single Crystaline Extension of Substrate Crystal
- Commonly used in bipolar processes
- CVD techniques
- Impurities often added during growth
- Grows slowly to allow alignmnt with substrate



Polysilicon

Elemental contents identical to that of single crystaline silicon
- Electrical properties much different
- If doped heavily makes good conductor
- If doped moderately makes good resistor
- Widely used for gates of MOS devices
- Widely used to form resistors
- Grows fast over non-crystaline surface
- Patterned with Photoresist/Etch process
- Silicide often used in regions where resistance must be small
  - Refractory metal used to form silicide
  - Designer must indicate where silicide is applied (or blocked)

Metalization

Aluminum widely used for interconnect

Copper often replacing aluminum in recent processes

Must not exceed maximum current density
- around 1ma/u for aluminum and copper

Ohmic Drop must be managed

Parasitic Capacitances must be managed

Interconnects from high to low level metals require connections to each level of metal

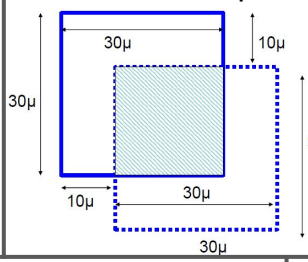
Stacked vias permissible in some processes

- Aluminum usually deposited uniformly over entire surface and etched to remove unwanted
- Mask is used to define area in photoresist where aluminum is to be removed

Copper:
- Plasma etches not effective at removing copper bc of absence of volatile compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms

Damascene or Dual Damascene processes used to pattern copper

Interconnect Capacitance



Cap. Densities:
M1-Sub: .05fF/u²
M1-M2: .07fF/u²
M2-Sub:.025fF/u²

$A_{C1C2}=(20u)^2=400u^2$

$C_{12}=A_{C1C2}*C_{D12}=$
$400u^2*.07fF/u^2=28fF$

Interconnect Resistance

$R = (L/(H*W))*\rho$ | ρ/H=Sheet Res.=R_{SH}

$R = (L/W)*R_{SH}$

Only part of sqr → .7 | .55 | 1

#Sqrs Method: #Sqr*R_{SH}

Determine the resistance and capacitance of a Poly interconnect that's 0.6u wide and 800u long and compare that with the same interconnect if M1 were used.

R_{SH}=23.5, $C_{P\text{-}Sub}$=84

$n_{sq}=\frac{800\mu}{0.6\mu}=1333$

$A=(0.6\mu)(800\mu)=480\mu^2$

$R_{POLY}=n_{SQ}R_{SH}=7.7\cdot1333=10.3K\Omega$

$C_{P\text{-}SUB}=A\cdot C_{DPS}=480\mu^2\cdot103aF\mu^{-2}=49.4fF$

Temp. Coefficients 4 Res. & Cap.

TCR=(1/R*dR/dT) * 10^6 ppm/°C

$R(T_2)\approx R(T_1)[1+(T_2-T_1)(TCR/10^6)]$

TCR= ? ppm/°C

TCR can be substituted w/ VCR, then substitute all Ts with Vs