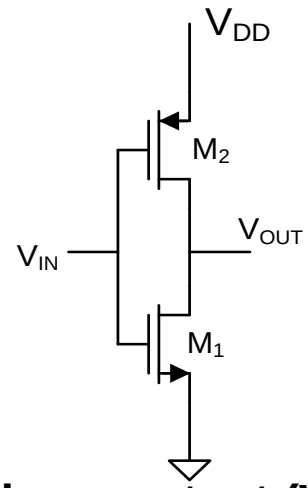
EE 330
Lecture 43

Digital Circuits

- Optimally driving large capacitive loads
- Logic Effort
- Elmore Delay
- Power Dissipation

Overdrive Factors



Scaling widths of ALL devices by constant (W_{scaled}=WxOD) will change "drive" capability relative to that of the reference inverter but not change relative value of t_{HL} and t_{LH}

$$R_{PD}=\frac{L_1}{\mu_n C_{OX} W_1 (V_{DD}-V_{Tn})} \rightarrow R_{PDOD}=\frac{L_1}{\mu_n C_{OX} [OD \bullet W_1](V_{DD}-V_{Tn})}=\frac{R_{PD}}{OD}$$

$$R_{PU}=\frac{L_2}{\mu_p C_{OX} W_2 (V_{DD}+V_{Tp})} \rightarrow R_{PUOD}=\frac{L_2}{\mu_p C_{OX} [OD \bullet W_2](V_{DD}+V_{Tp})}=\frac{R_{PU}}{OD}$$

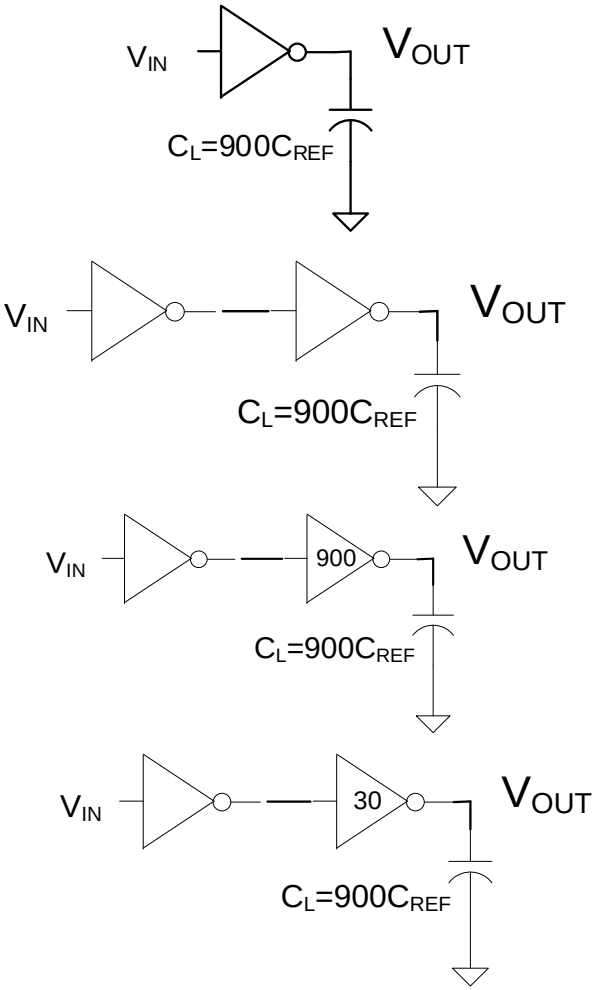
Scaling widths of ALL devices by constant will change FI by OD

$$C_{IN}=C_{OX}(W_1 L_1+W_2 L_2) \rightarrow C_{INOD}=C_{OX}([OD \bullet W_1]L_1+[OD \bullet W_2]L_2)=OD \bullet C_{IN}$$

Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don't worry about the extra inversion at this time.



$$t_{PROP} = 900t_{REF}$$

$$t_{PROP} = t_{REF} + 900t_{REF} = 901t_{REF}$$

$$t_{PROP} = 900t_{REF} + t_{REF} = 901t_{REF}$$

$$t_{PROP} = 30t_{REF} + 30t_{REF} = 60t_{REF}$$

Note: Dramatic reduction in t_{PROP} is possible
Will later determine what optimal number of stages and sizing is

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- **Equal rise/fall (no overdrive)**
- **Equal rise/fall with overdrive**
- **Minimum Sized**
- **Asymmetric Overdrive**
- **Combination of equal rise/fall, minimum size and overdrive**

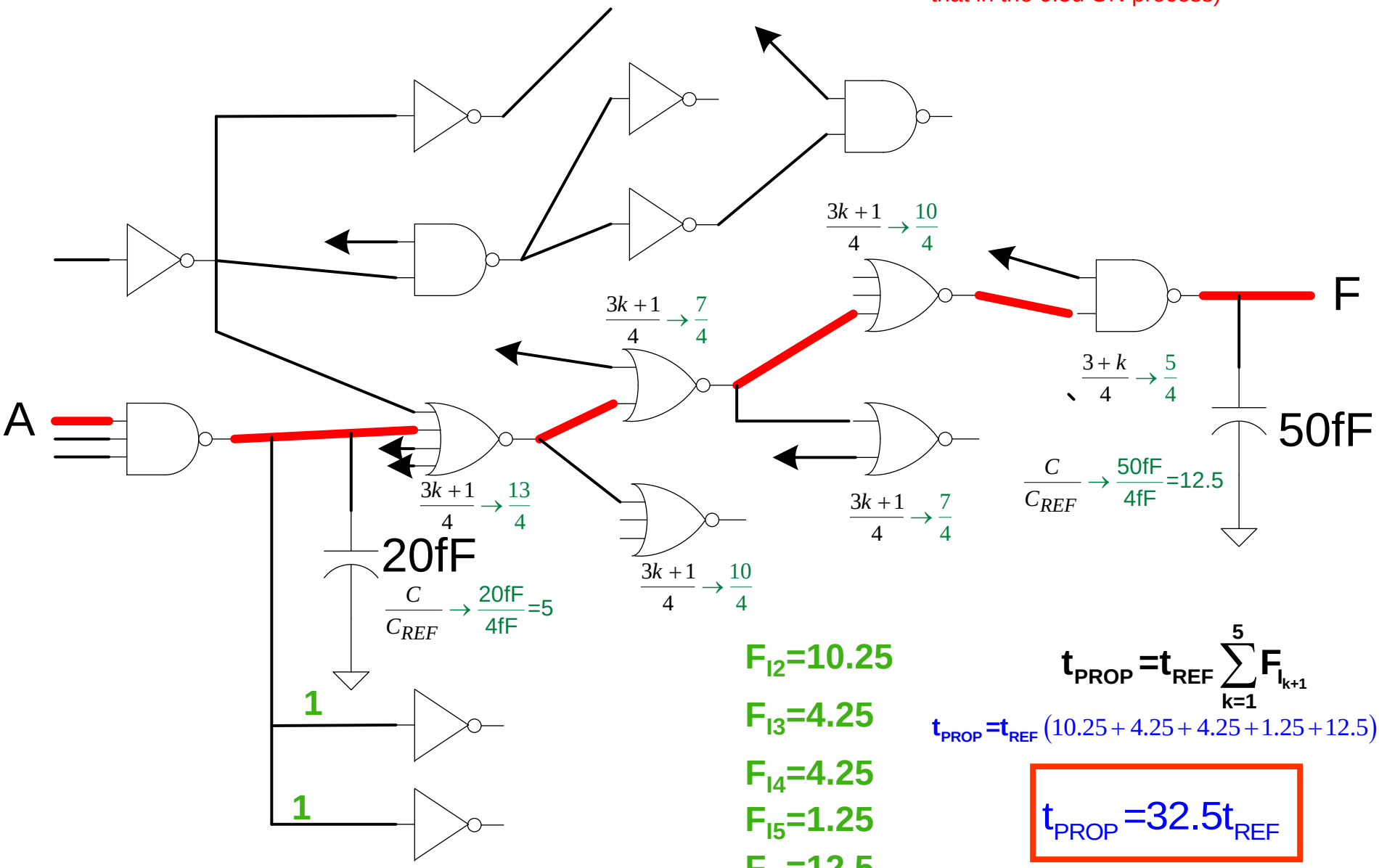
Will develop the analysis methods as needed

Review from Last Time

Equal rise-fall gates, no overdrive

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



F_{I2}=10.25

F_{I3}=4.25

F_{I4}=4.25

F_{I5}=1.25

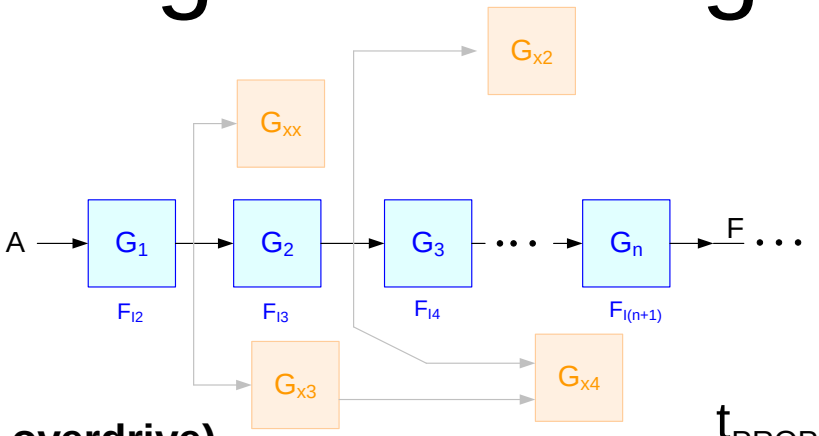
F_{I6}=12.5

$$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{I_{k+1}}$$

$$t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)$$

$$t_{PROP} = 32.5 t_{REF}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Asymmetric overdrive**

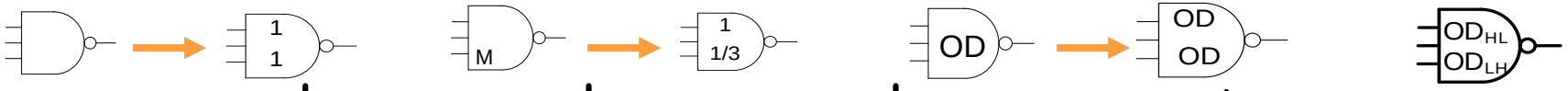
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Review from Last Time

Summary: Propagation Delay in Multiple-Levels of Logic with Stage Loading



	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
      - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

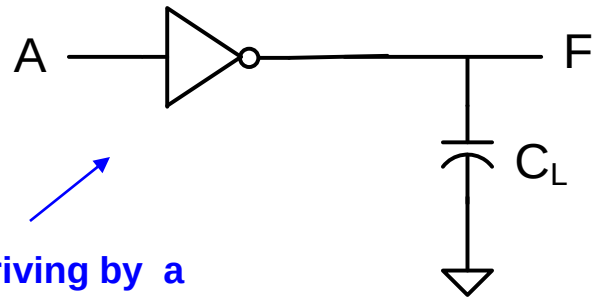
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial

Driving Large Capacitive Loads

Example



Assume driving by a reference inverter

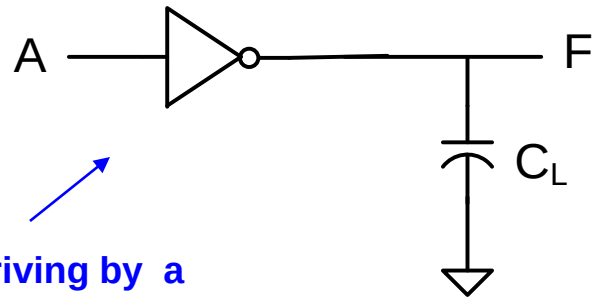
Assume $C_L=1000C_{REF}$

t_{PROP}=?

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

Driving Large Capacitive Loads

Example



Assume driving by a reference inverter

Assume $C_L=1000C_{REF}$

$t_{PROP}=1000t_{REF}$

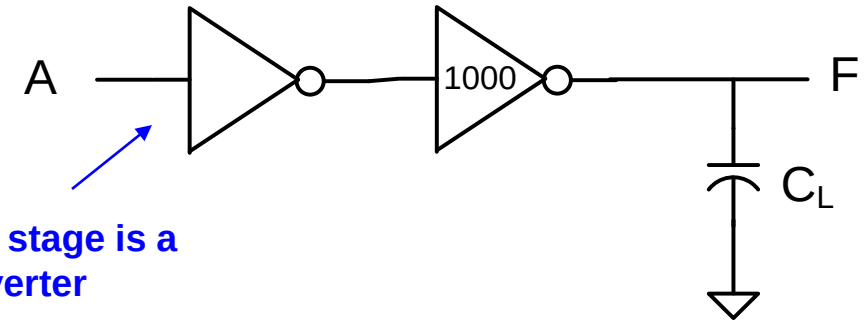
t_{PROP} is too long !

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

Driving Large Capacitive Loads

Example

Assume $C_L = 1000 C_{REF}$



Assume first stage is a reference inverter

$$t_{PROP} = ?$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{2} \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \left(\frac{1}{1} 1000 + \frac{1}{1000} 1000 \right) = t_{REF} \left(1000 + 1 \right)$$

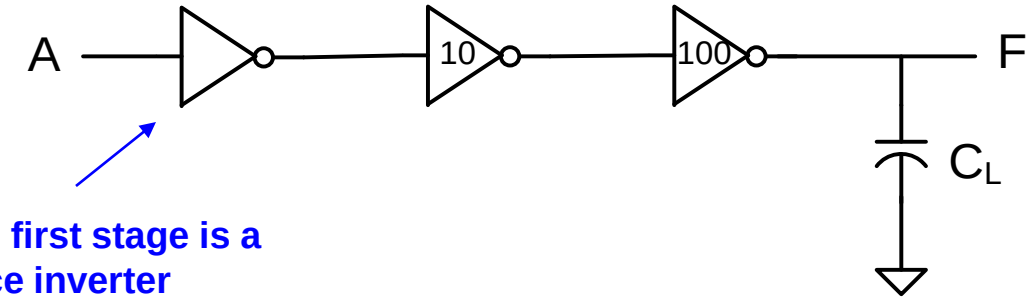
$$t_{PROP} = t_{REF} \left(1001 \right)$$

Delay of second inverter is really small but overall delay is even longer than before!

Driving Large Capacitive Loads

Example

Assume $C_L=1000C_{REF}$



Assume first stage is a reference inverter

$$t_{PROP}=t_{REF}\sum_{k=1}^{3}\frac{F_{I(k+1)}}{OD_k}$$

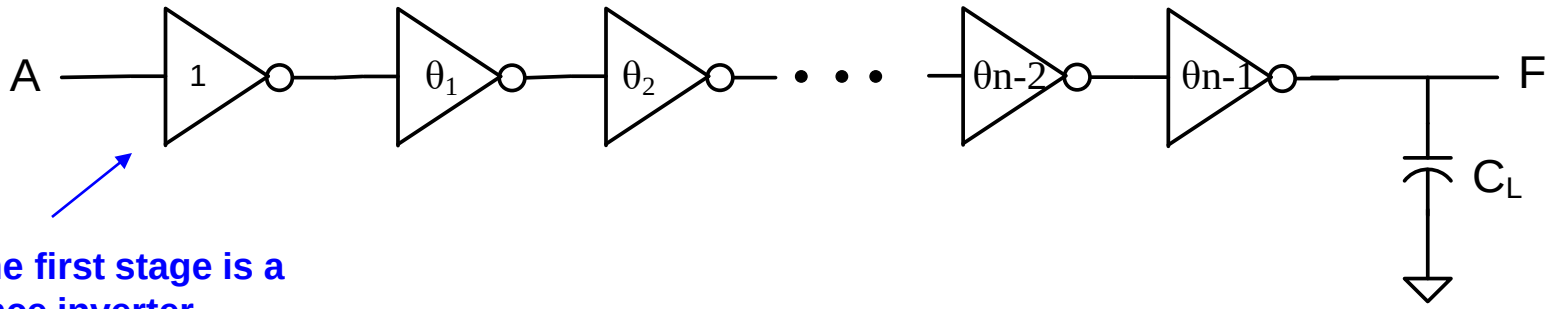
$$t_{PROP}=t_{REF}\left(\frac{1}{1}10+\frac{1}{10}100+\frac{1}{100}1000\right)=t_{REF}\left(10+10+10\right)$$

$$t_{PROP}=30t_{REF}$$

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?

Optimal Driving of Capacitive Loads



Assume first stage is a reference inverter

Need to determine the number of stages, n, and the OD factors for each stage to minimize t_{PROP}.

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \quad \rightarrow \quad t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}$$

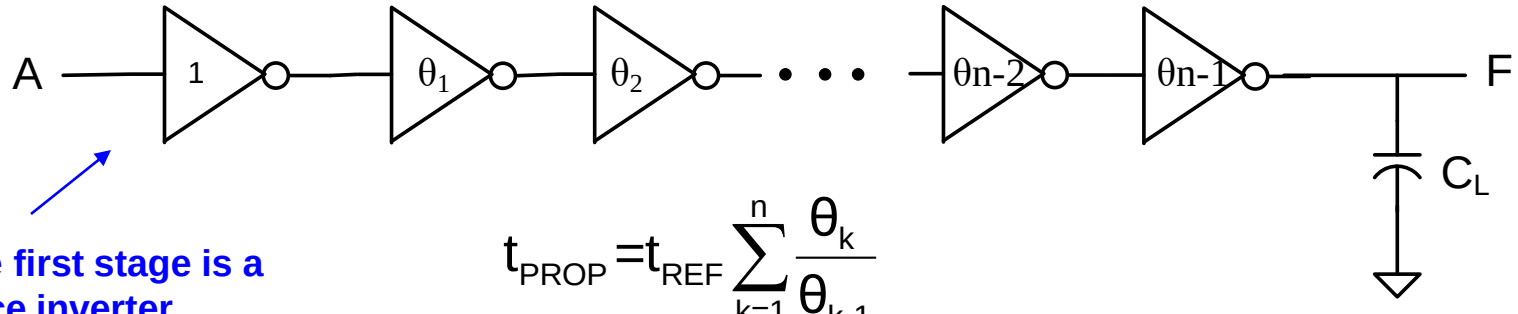
where $\theta_0 = 1$, $\theta_n = C_L / C_{REF}$

This becomes an n-parameter optimization (minimization) problem !

Unknown parameters: $\{\theta_1, \theta_2, \ldots \theta_{n-1}, n\}$

An n-parameter nonlinear optimization problem is generally difficult !!!!

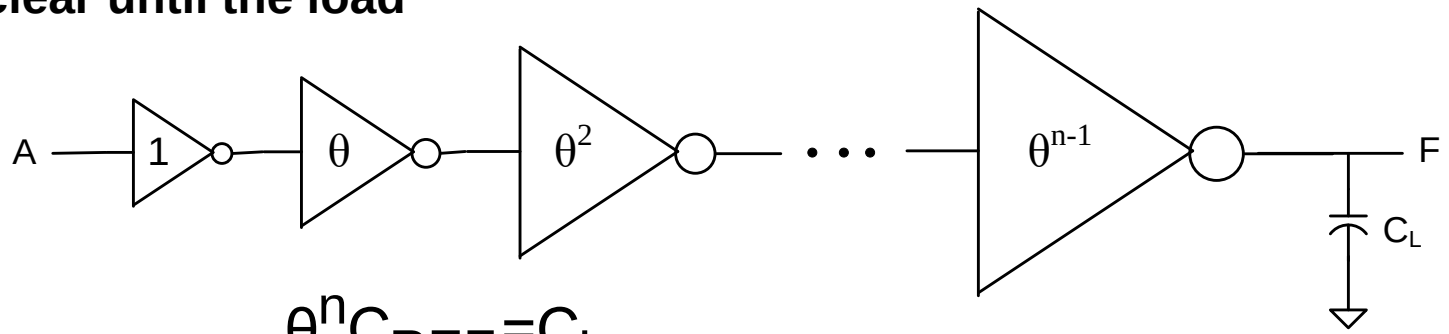
Optimal Driving of Capacitive Loads



Assume first stage is a reference inverter

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}$$

Order reduction strategy : Assume overdrive of stages increases by the same factor clear until the load



$$\theta^n C_{REF} = C_L$$

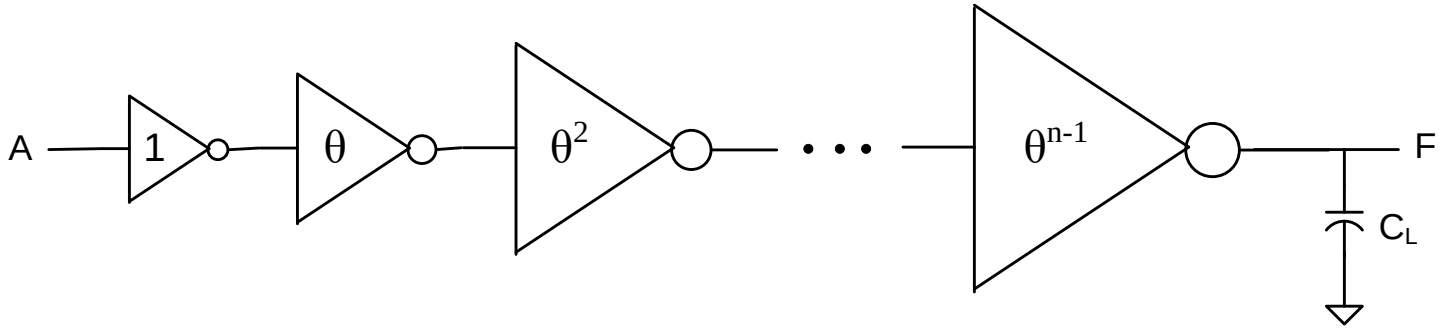
This becomes a 2-parameter optimization (minimization) problem !

Unknown parameters: $\{\theta, n\}$

One degree of freedom

One constraint : $\theta^n C_{REF} = C_L$

Optimal Driving of Capacitive Loads



$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \quad \rightarrow \quad t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta^k}{\theta^{k-1}} \qquad \theta^n C_{REF} = C_L$$

$$t_{PROP} = t_{REF} n\theta$$

$$\left.\begin{aligned} t_{PROP} &= t_{REF} n\theta \\ \theta^n C_{REF} &= C_L \end{aligned}\right\}$$

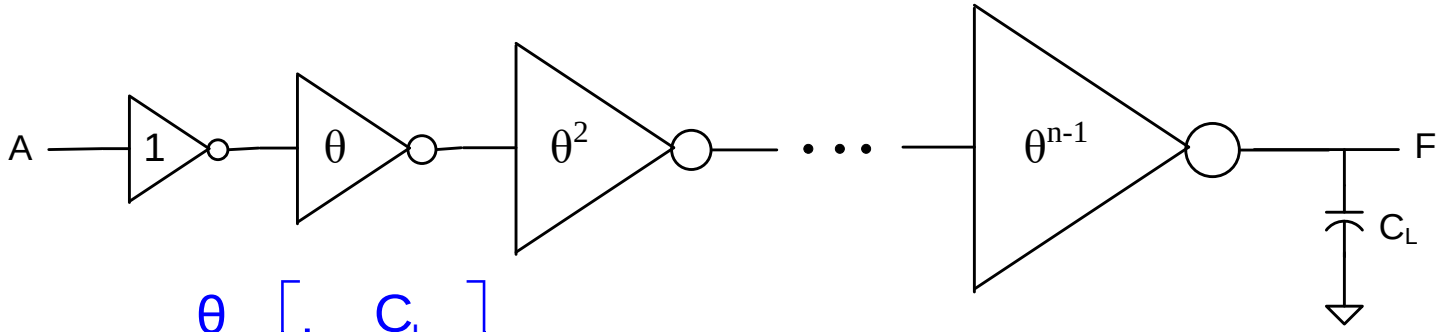
Unknown parameters: $\{\theta, n\}$

$$\theta^n C_{REF} = C_L \quad \rightarrow \quad n = \frac{1}{\ln(\theta)} \ln\left(\frac{C_L}{C_{REF}}\right)$$

Thus obtain an expression for t_{PROP} in terms of only θ

$$t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[\ln \frac{C_L}{C_{REF}}\right]$$

Optimal Driving of Capacitive Loads



$$t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[\ln \frac{C_L}{C_{REF}} \right]$$

$$\theta^n C_{REF} = C_L$$

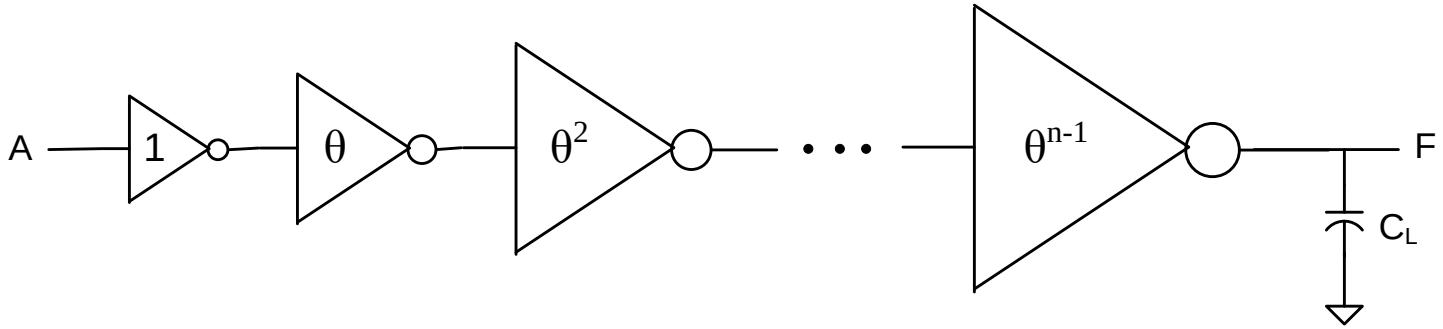
Is suffices to minimize the function $f(\theta) = \frac{\theta}{\ln(\theta)}$

$$\frac{df}{d\theta} = \frac{\ln(\theta) - \theta \bullet \left(\frac{1}{\theta}\right)}{(\ln(\theta))^2} = 0$$

$$\ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e$$

$$n = \frac{1}{\ln(\theta)} \ln\left(\frac{C_L}{C_{REF}}\right) \quad \rightarrow \quad n = \ln\left(\frac{C_L}{C_{REF}}\right)$$

Optimal Driving of Capacitive Loads



$$\theta_{OPT} = e$$

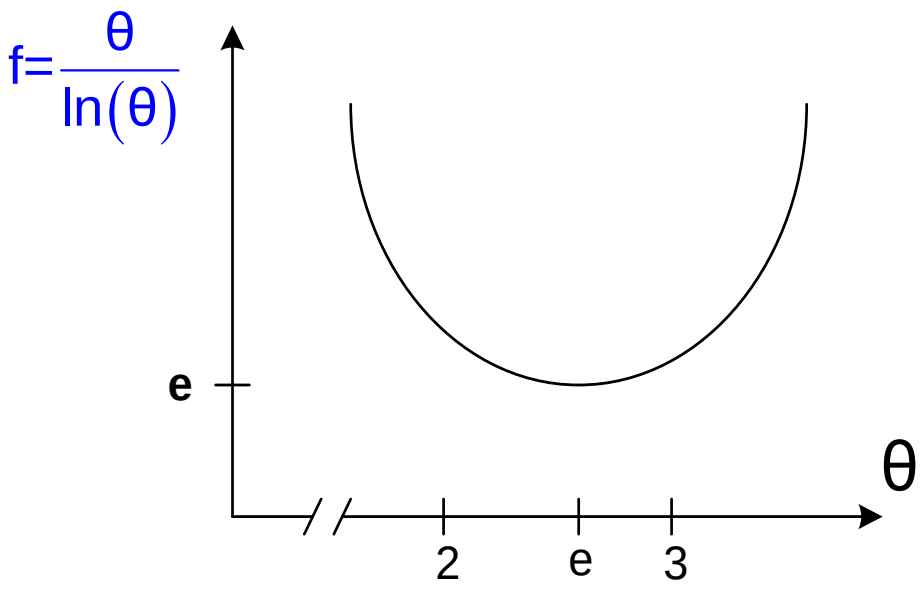
$$\theta^n C_{REF} = C_L$$

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right)$$

$$t_{PROP} = t_{REF}\frac{\theta}{\ln(\theta)}\left[\ln\frac{C_L}{C_{REF}}\right]$$

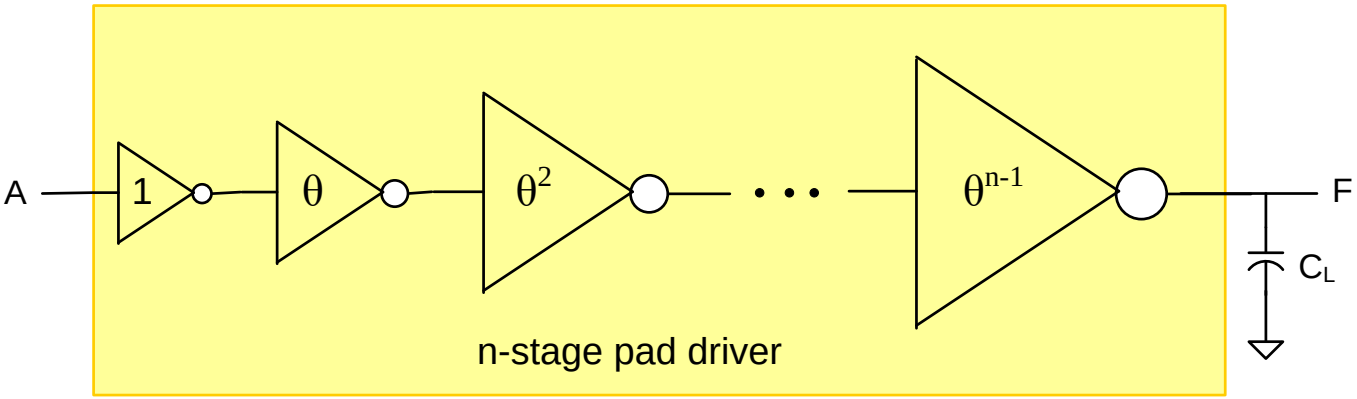
$$t_{PROP} = t_{REF}\, e\left[\ln\frac{C_L}{C_{REF}}\right] = n\theta t_{REF}$$

Optimal Driving of Capacitive Loads



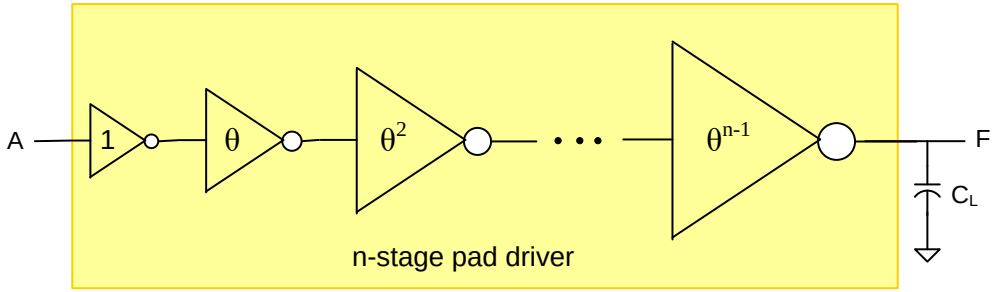
- **minimum at θ=e but shallow inflection point for 2<θ<3**
- **practically pick θ=2, θ=2.5, or θ=3**
- **since optimization may provide non-integer for n, must pick close integer**

Optimal Driving of Capacitive Loads



- **Often termed a pad driver**
- **Often used to drive large internal busses as well**
- **Generally included in standard cells or in cell library**
- **Device sizes can become very large**
- **Odd number of stages will cause signal inversion but usually not a problem**

Optimal Driving of Capacitive Loads



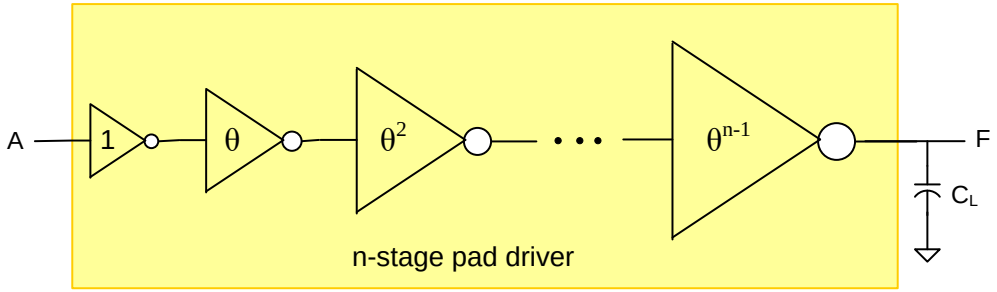
Example: Design a pad driver for driving a load capacitance of 10pF, determine t_{PROP} for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter. In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln\left(\frac{10pF}{4fF}\right) = 7.8$$

Select n=8, θ=2.5

$$W_{nk} = 2.5^{k-1} \bullet W_{REF}, \qquad W_{pk} = 3 \bullet 2.5^{k-1} \bullet W_{REF}$$

Optimal Driving of Capacitive Loads



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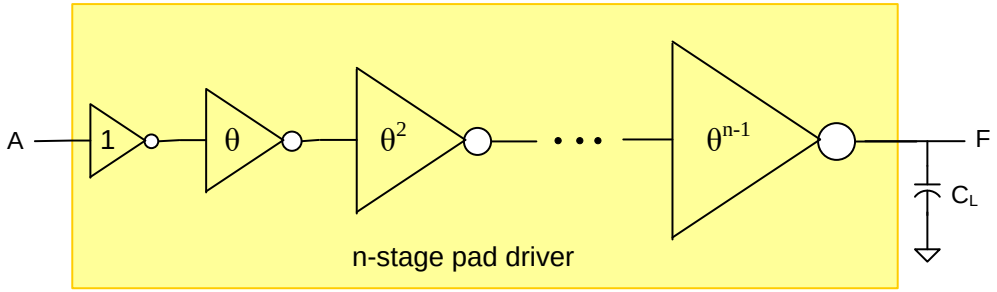
$$W_{nk}=2.5^{k-1}\bullet W_{REF},\qquad W_{pk}=3\bullet 2.5^{k-1}\bullet W_{REF}$$

$$W_{REF}=W_{MIN}\qquad L_n=L_p=L_{MIN}$$

k	n-channel		p-channel	
1	1	WMIN	3	WMIN
2	2.5	WMIN	7.5	WMIN
3	6.25	WMIN	18.75	WMIN
4	15.6	WMIN	46.9	WMIN
5	39.1	WMIN	117.2	WMIN
6	97.7	WMIN	293.0	WMIN
7	244.1	WMIN	732.4	WMIN
8	610.4	WMIN	1831.1	WMIN

Note devices in last stage are very large !

Optimal Driving of Capacitive Loads



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In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

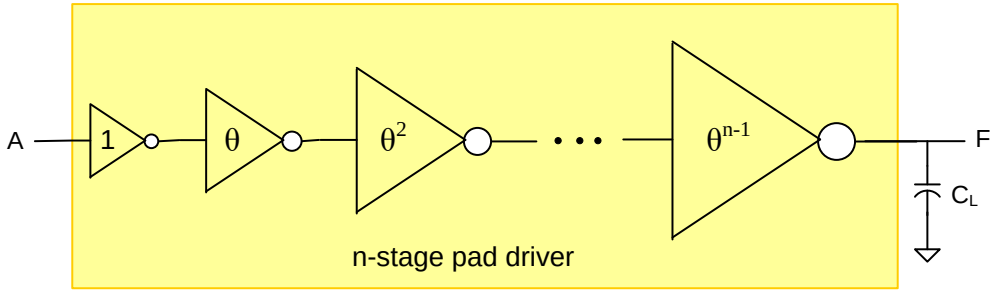
$W_{nk}=2.5^{k-1}\bullet W_{REF}$, $W_{pk}=3\bullet 2.5^{k-1}\bullet W_{REF}$

$$t_{PROP} \cong n\theta t_{REF} = 8\bullet 2.5\bullet t_{REF} = 20t_{REF}$$

More accurately:

$$t_{PROP}=t_{REF}\left(\sum_{k=1}^{7}\theta+\frac{1}{\theta^7}\frac{C_L}{C_{REF}}\right)=t_{REF}\left(17.5+\frac{1}{610}2500\right)=21.6t_{REF}$$

Optimal Driving of Capacitive Loads



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In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

$W_{nk}=2.5^{k-1} \bullet W_{REF}$, $W_{pk}=3 \bullet 2.5^{k-1} \bullet W_{REF}$

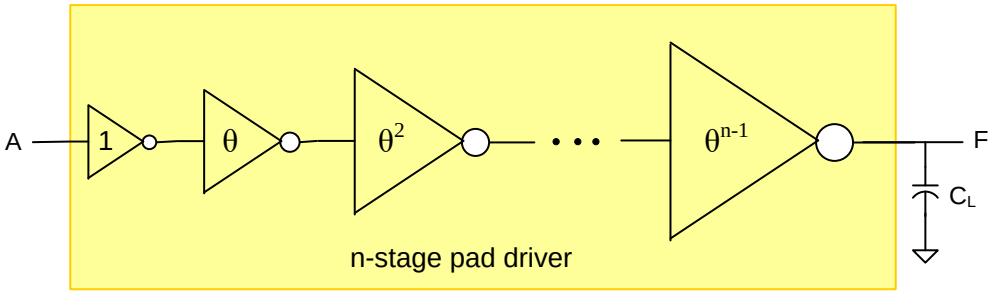
If driven directly with the minimum-sized reference inverter

$$t_{PROP}=t_{REF}\frac{C_L}{C_{REF}}=2500t_{REF}$$

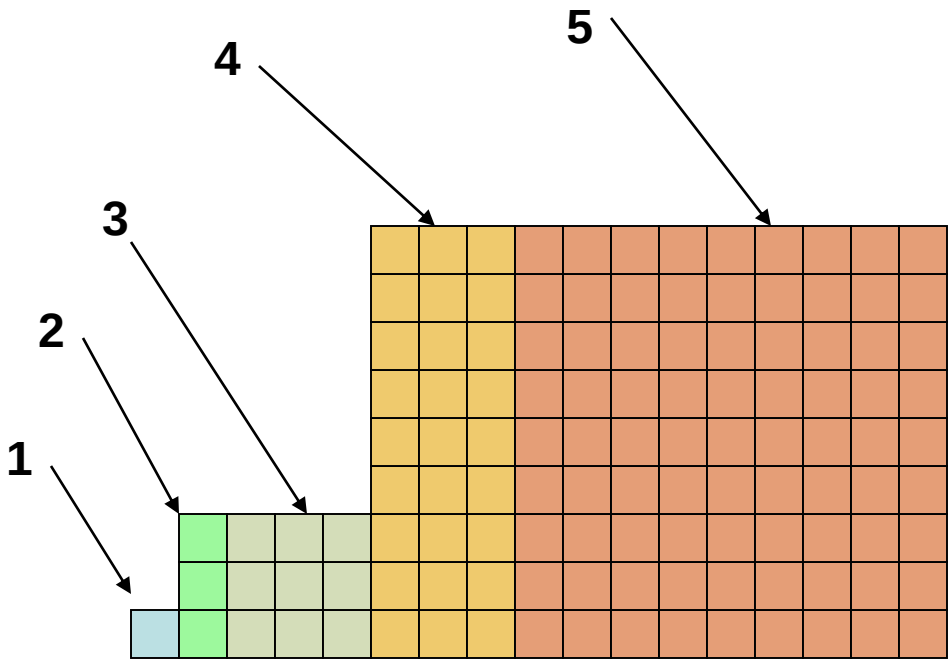
Note an improvement in speed by a factor of

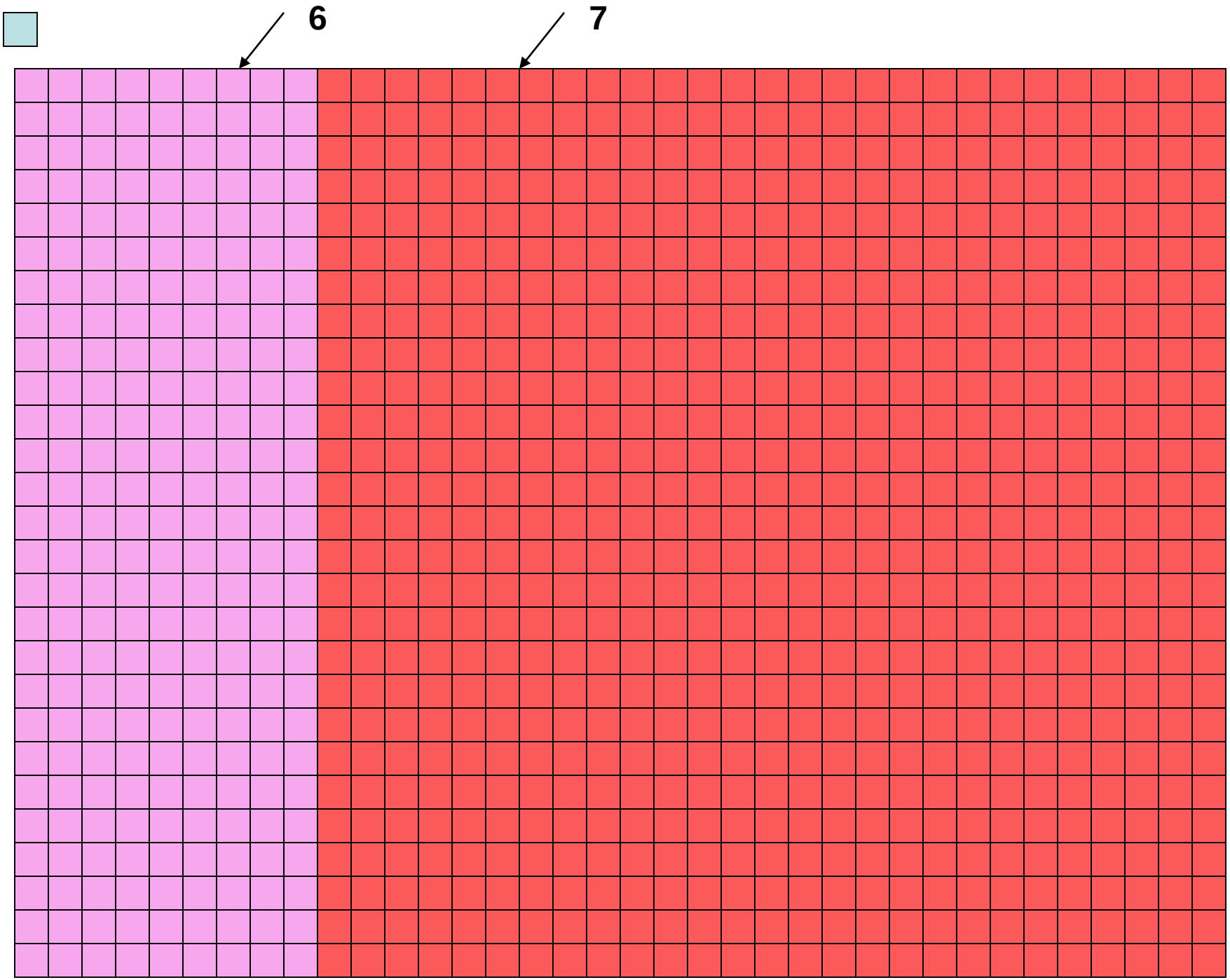
$$r=\frac{2500}{20}=125$$

Pad Driver Size Implications

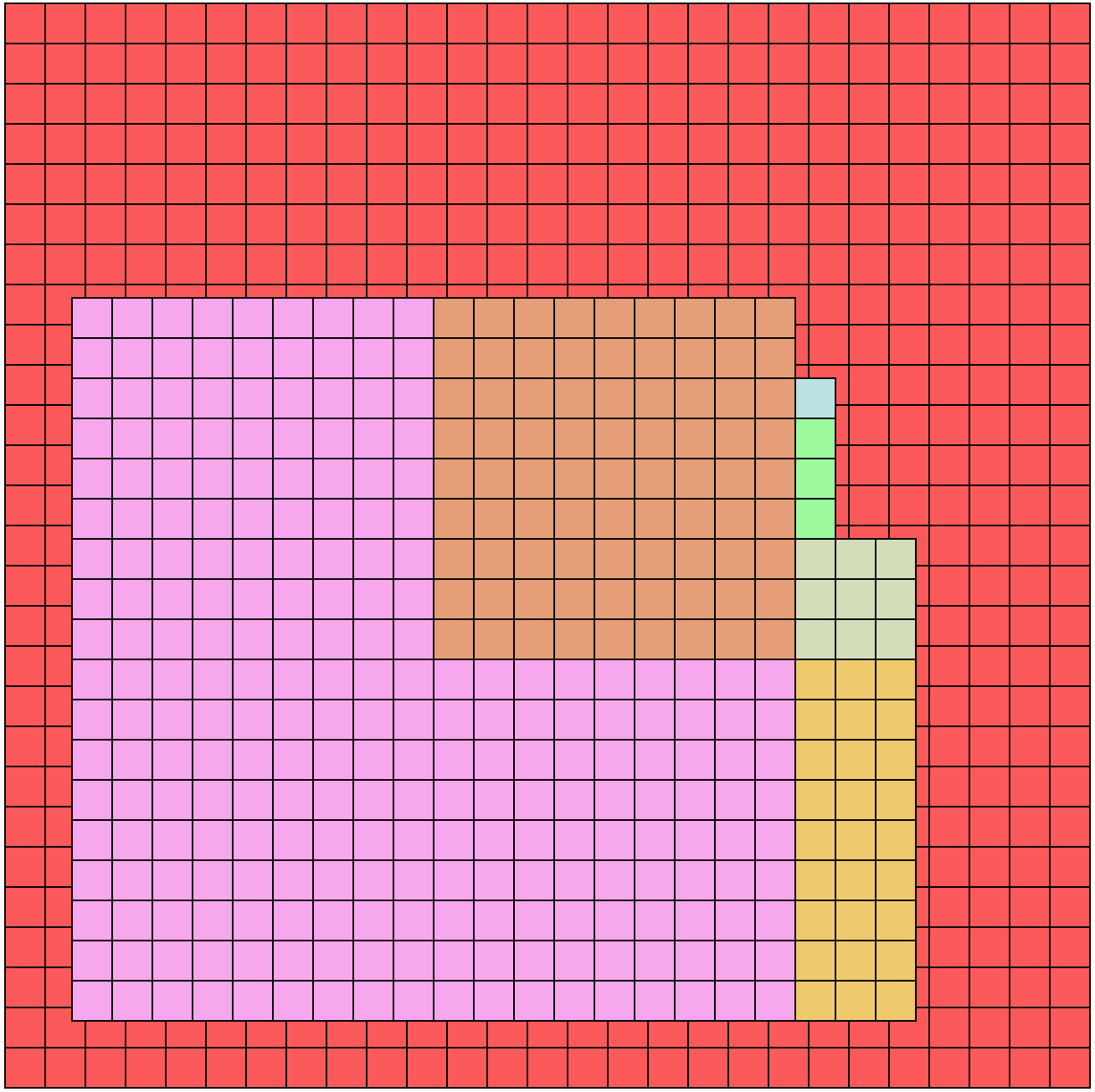


Consider a 7-stage pad driver and assume θ = 3




6
7

Area of Last Stage Larger than that of all previous stages combined!



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done

partial

Propagation Delay in "Logic Effort" approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

Propagation delay for equal rise/fall gates was derived to be

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

Delay calculations with "logical effort" approach

Logical effort delay approach:

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k$$

(t_{REF} scaling factor not explicitly stated in W_H textbook. As defined in W_H, f_k is dimensionless

where f_k is the "effort delay" of stage k

$$f_k = g_k h_k$$

g_k=logical effort

h_k=electrical effort

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

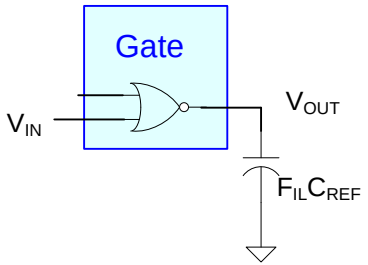
f_k = “effort delay” of stage k

g_k=logical effort

h_k=electrical effort

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate

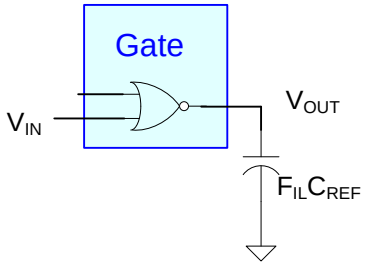


Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

Logic Effort (g) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort (h) is the ratio of the gate load capacitance to the input capacitance of a gate



$$g_k = \frac{C_{IN_k}}{C_{REF} \bullet OD_k} \qquad h_k = \frac{C_{REF} \bullet FI_{k+1}}{C_{IN_k}}$$

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

$$g_k = \frac{C_{IN_k}}{C_{REF} \bullet OD_k} \qquad h_k = \frac{C_{REF} \bullet F_{I(k+1)}}{C_{IN_k}}$$

$$f_k = \left(\frac{C_{IN_k}}{C_{REF} \bullet OD_k} \right) \left(\frac{C_{REF} \bullet F_{I(k+1)}}{C_{IN_k}} \right)$$

$$f_k = \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k = t_{REF} \sum_{k=1}^{n} g_k h_k = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k = t_{REF} \sum_{k=1}^{n} g_k h_k = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Note this expression is identical to what we have derived previously**
  (t_{REF} scaling factor not included in W_H text)

- **Probably more tedious to use the “Logical Effort” approach**
- **Extensions to asymmetric overdrive factors may not be trivial**
- **Extensions to include parasitics may be tedious as well**
- **Logical Effort is widely used throughout the industry**

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial

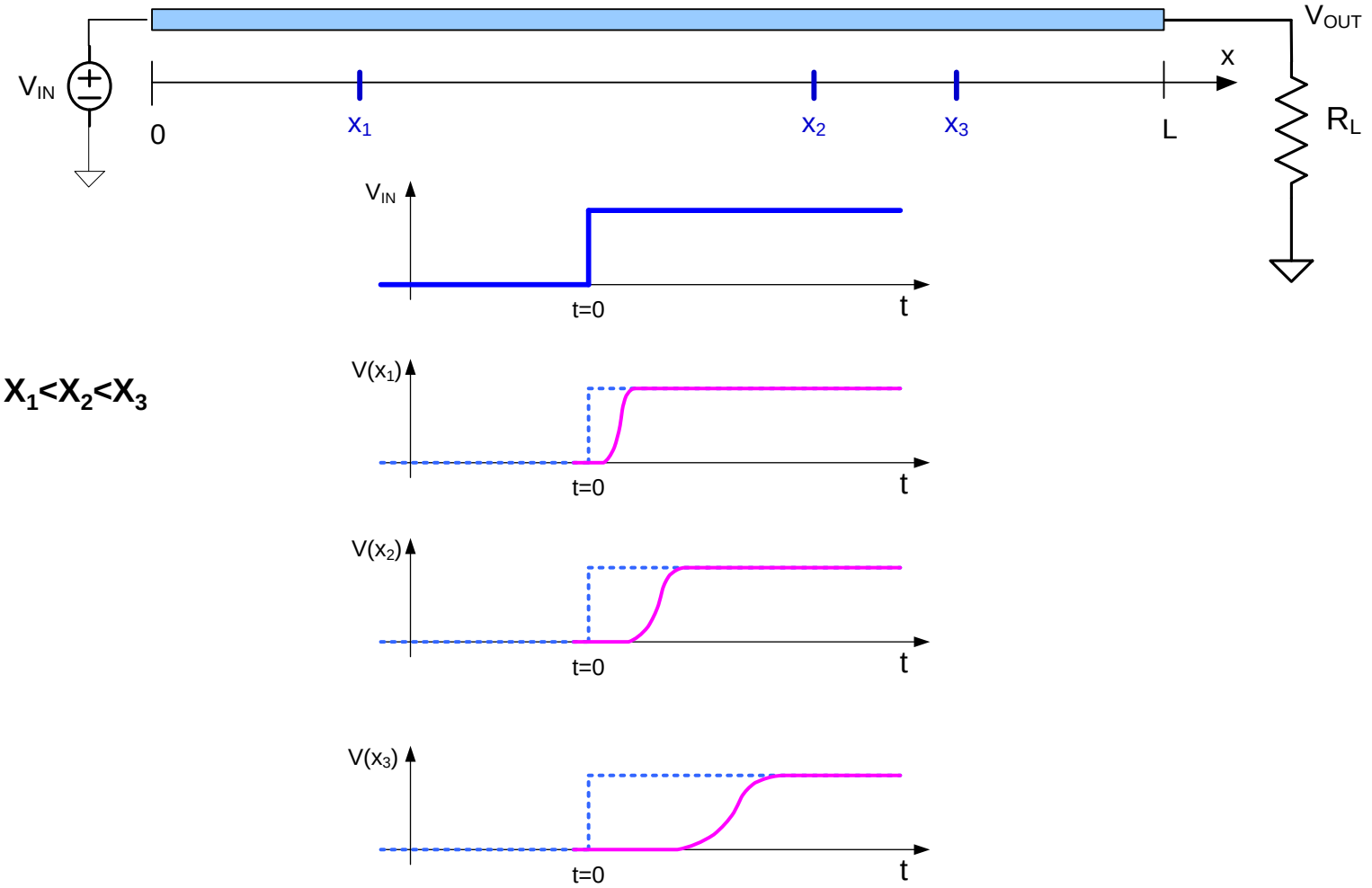
Elmore Delay Calculations

- **Interconnects have a distributed resistance and a distributed capacitance**
  - **Often modeled as resistance/unit length and capacitance per unit length**
- **These delay the propagation of the signal**
- **Effectively a transmission line**
  - **analysis is really complicated**
- **Can have much more complicated geometries**

Elmore Delay Calculations

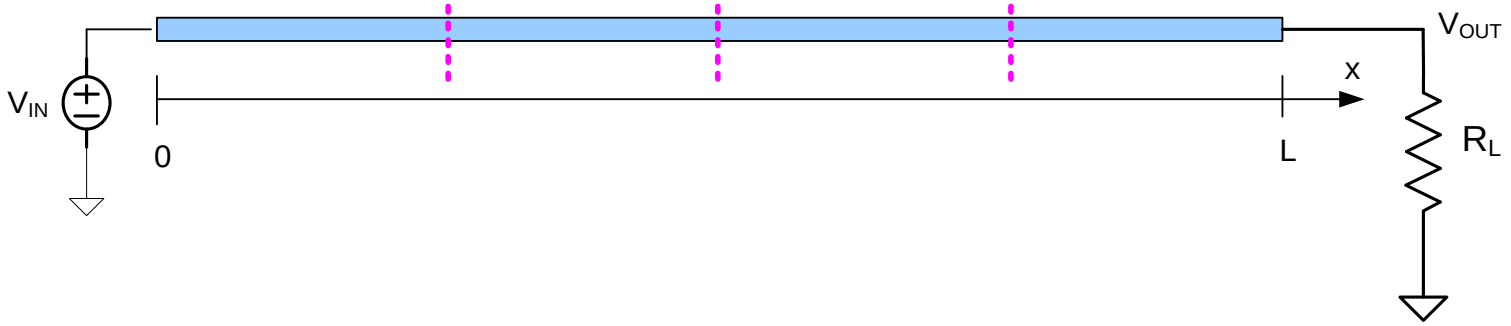
Can have much more complicated geometries

Elmore Delay Calculations

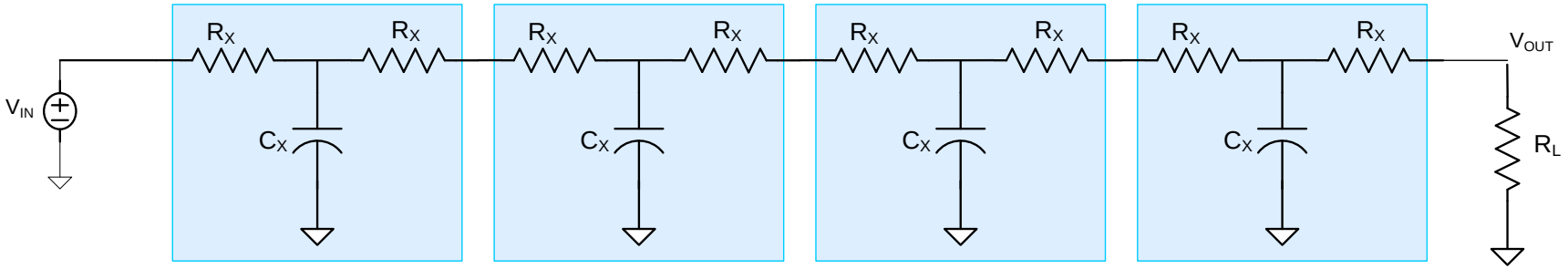


For $X_1<X_2<X_3$

Elmore Delay Calculations



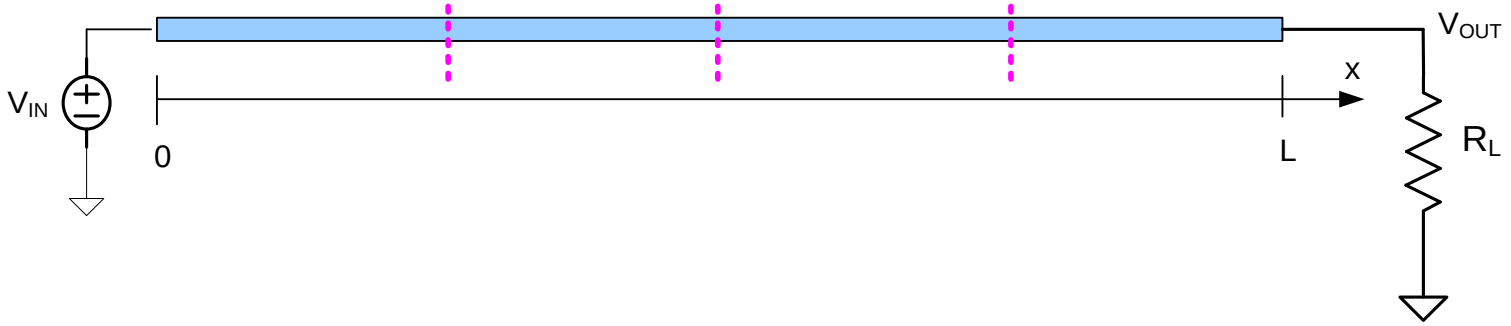
A lumped element model of transmission line



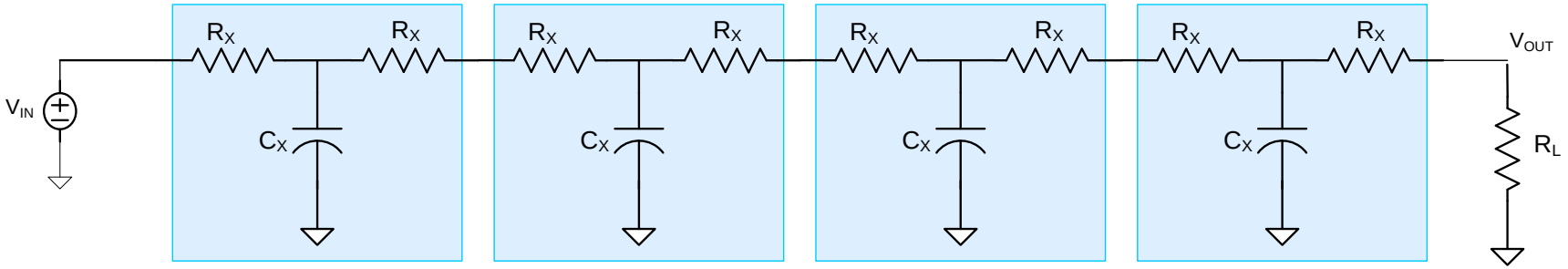
Even this lumped model is 4-th order and a closed-form solution is very tedious

Need a quick (and reasonably good) approximation to the delay of a delay line

Elmore Delay Calculations



A lumped element model of transmission line



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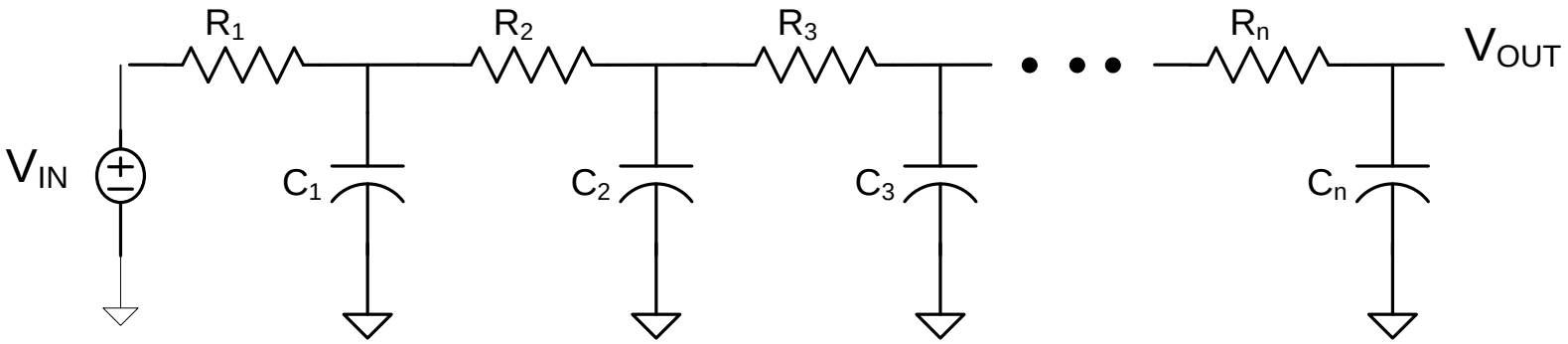
Elmore Delay Calculations



Elmore delay: $t_{PD} = \sum_{i=1}^{n} \left(C_i \sum_{j=1}^{i} R_j \right)$

- **It can be shown that this is a reasonably good approximation to the actual delay**
- **Numbering is critical (resistors and capacitors numbered from input to output)**
- **As stated, only applies to this specific structure**

Elmore Delay Calculations

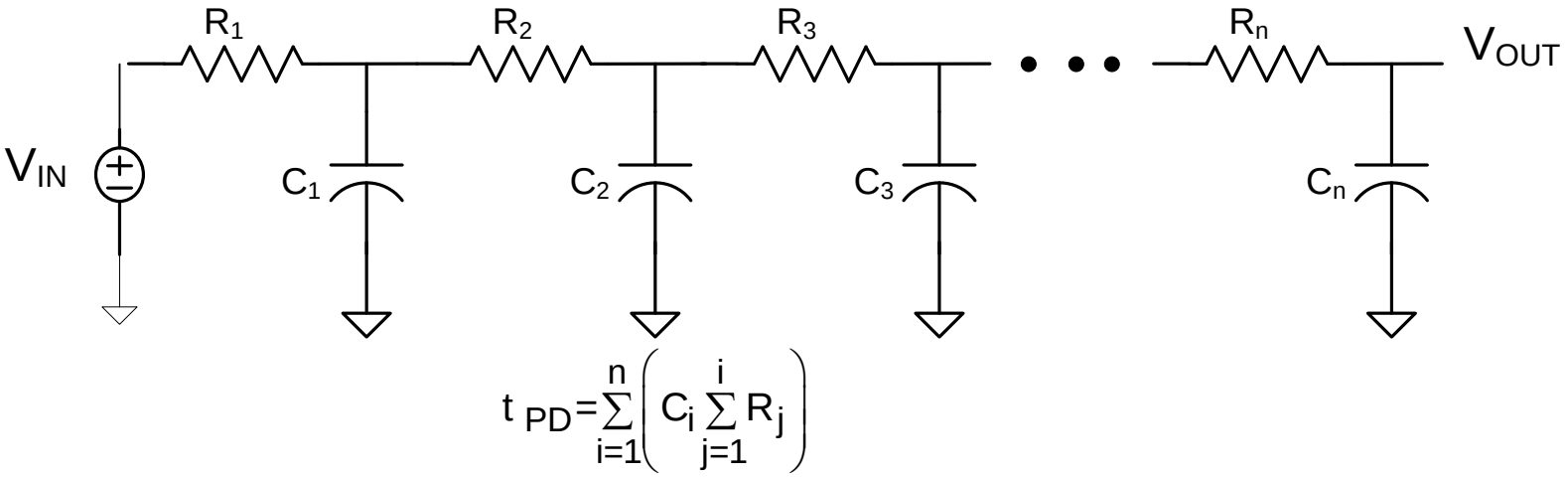
Elmore delay: $t_{PD} = \sum_{i=1}^{n} \left(C_i \sum_{j=1}^{i} R_j \right)$

- **Note error in text on Page 161 of first edition of WH**

$$t_{pd} = \sum_{i} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j$$

- **Not detailed definition on Page 150 of second edition of WH**

Elmore Delay Calculations



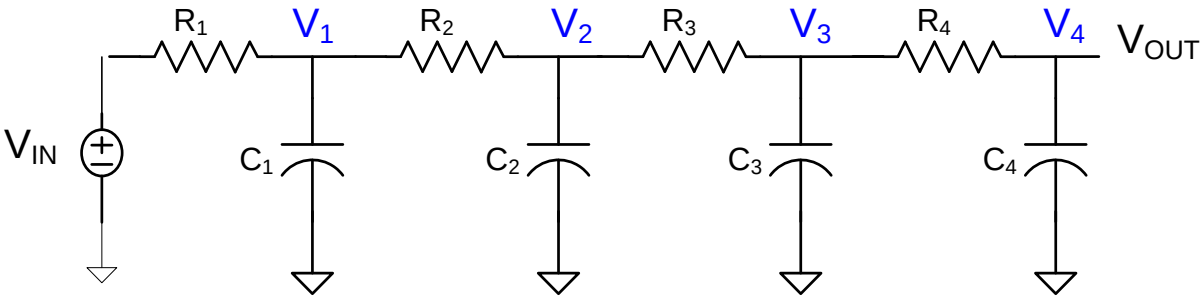
From Wikipedia:

Elmore delay[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

[1] W.C. Elmore. *The Transient Analysis of Damped Linear Networks with Particular Regard to Wideband Amplifiers*. J. Applied Physics, vol. 19(1), 1948.

Elmore Delay Calculations

Example:



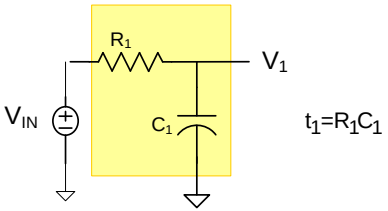
Elmore delay:

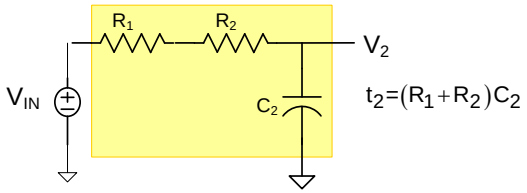
$$t_{PD} = \sum_{i=1}^{4} \left(C_i \sum_{j=1}^{i} R_j \right)$$

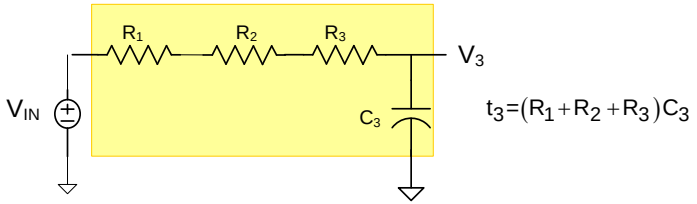
$$t_{PD} = \sum_{i=1}^{4} (t_i)$$

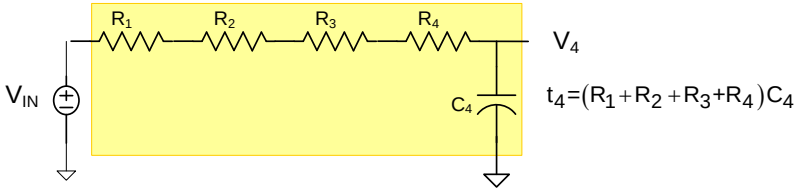
where

$$t_i = C_i \sum_{j=1}^{i} R_j \qquad j = 1,2,3,4$$









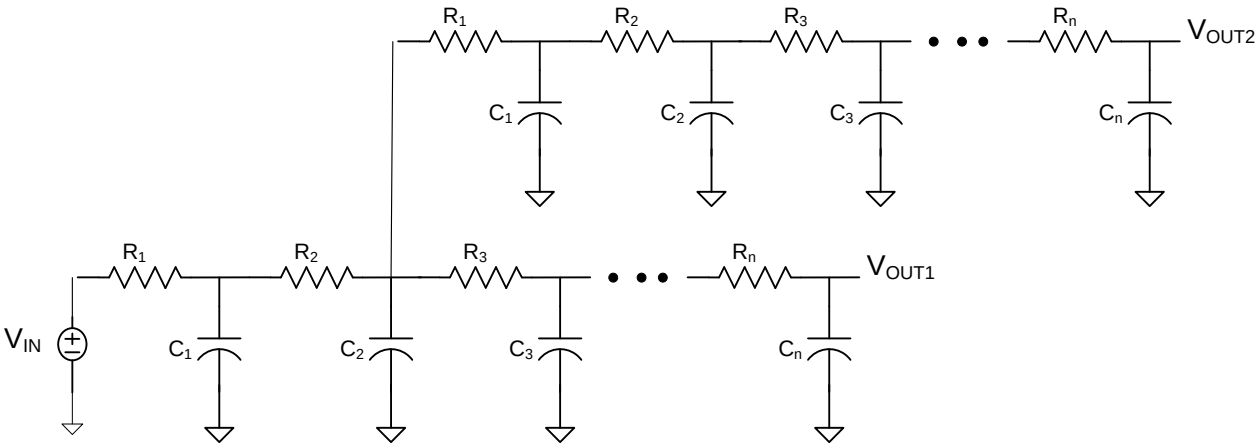
What is really happening?

- **Creating 4 first-order circuits**
- **Delay to V_1, V_2, V_3 and V_4 calculated separately by considering capacitors one at a time and assuming others are 0**

Elmore Delay Calculations

Extensions:

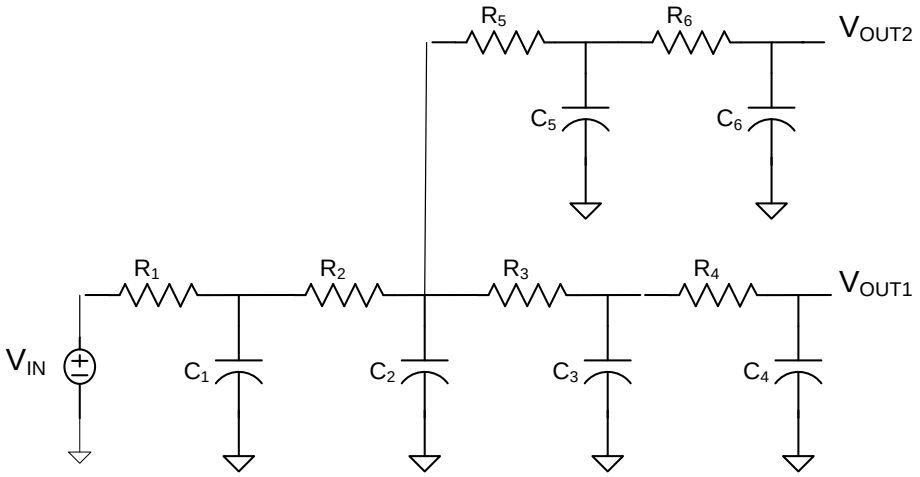
Lumped Network Model:



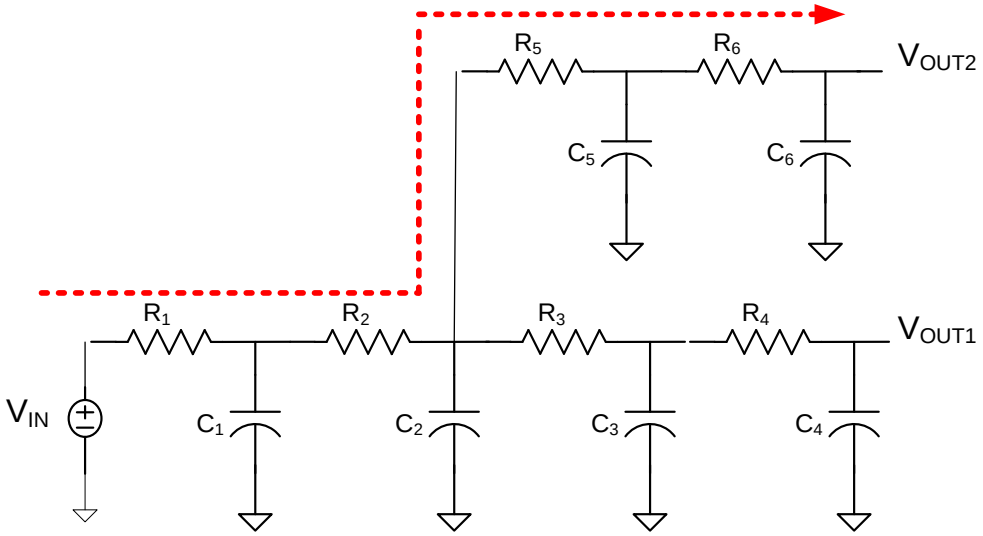
Elmore Delay Calculations

Extensions:

1. **Create a lumped element model**



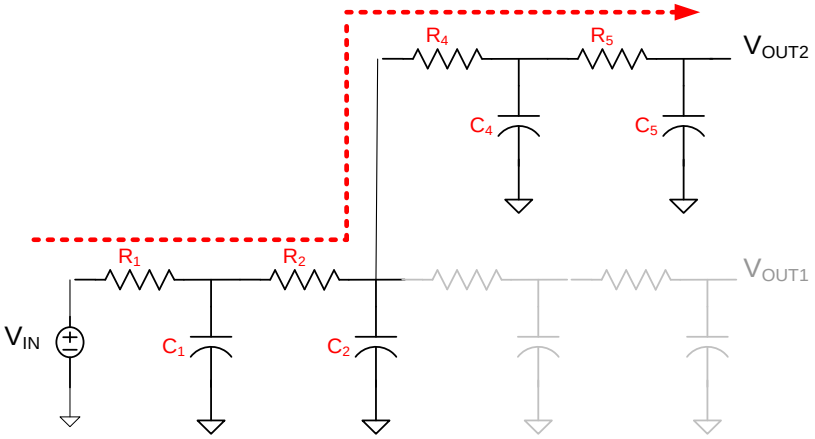
2. **Identify te a path from input to output**



Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elem



4. Use Elmore Delay equation for elements on this RC network

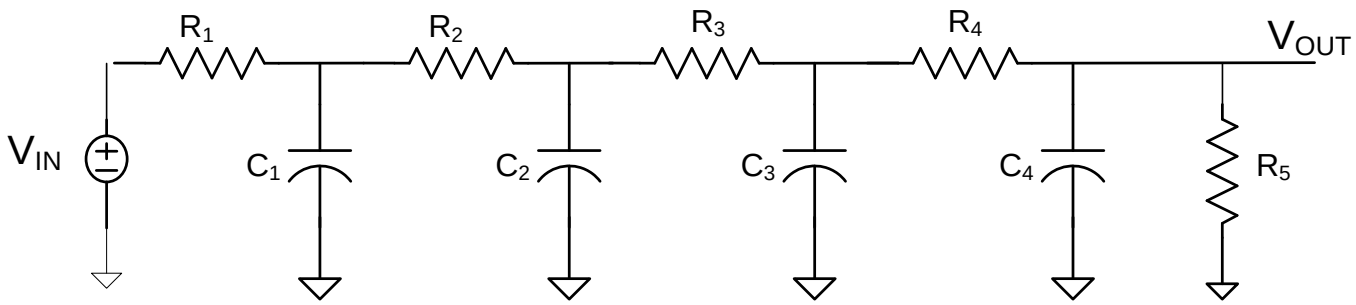
$$t_{PD} = \sum_{i=1}^{4} \left(C_i \sum_{j=1}^{i} R_j \right)$$

Elmore Delay Calculations

How is a resistive load handled?

Elmore Delay Calculations

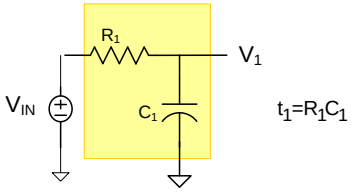
Example with resistive load:

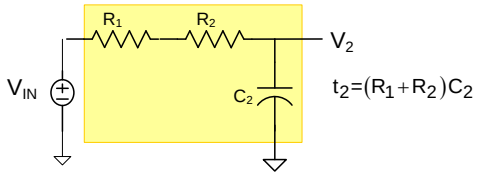


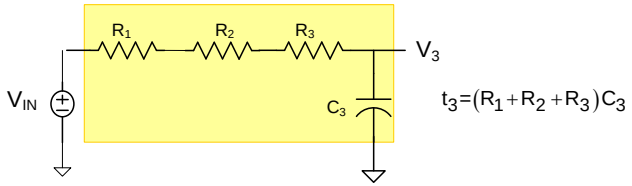
Elmore delay:

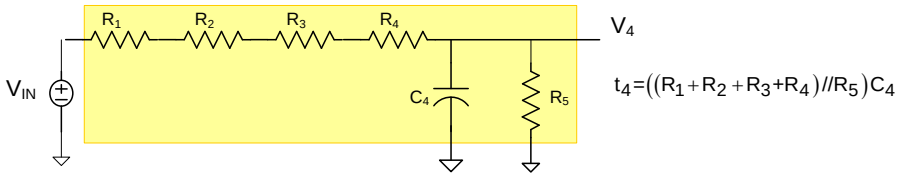
$$t_{PD} = \sum_{i=1}^{4} \left(C_i \sum_{j=1}^{i} R_j \right)$$

where









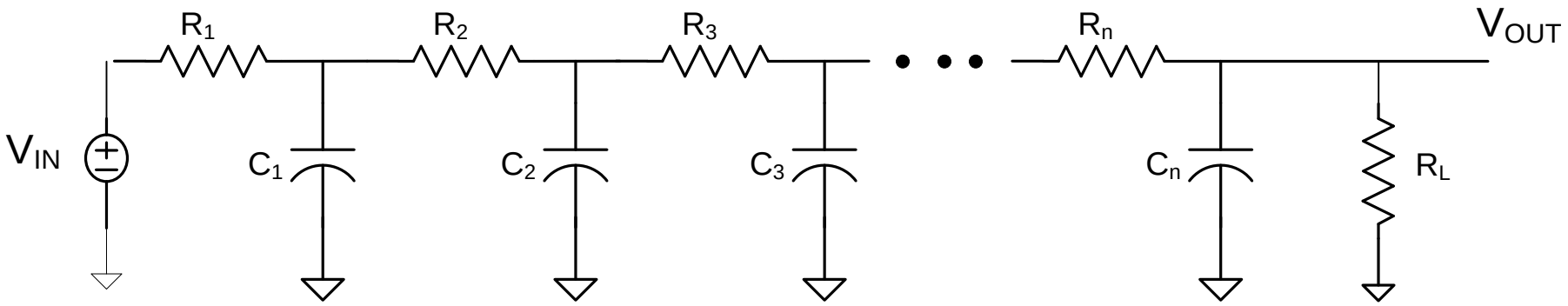
$$t_{PD} = \sum_{i=1}^{4} (t_i)$$

$$t_i = C_i \sum_{j=1}^{i} R_j \qquad j = 1,2,3$$

$$t_4 = C_4 \left(\left[\sum_{j=1}^{4} R_j \right] // R_5 \right)$$

Elmore Delay Calculations

With resistive load:

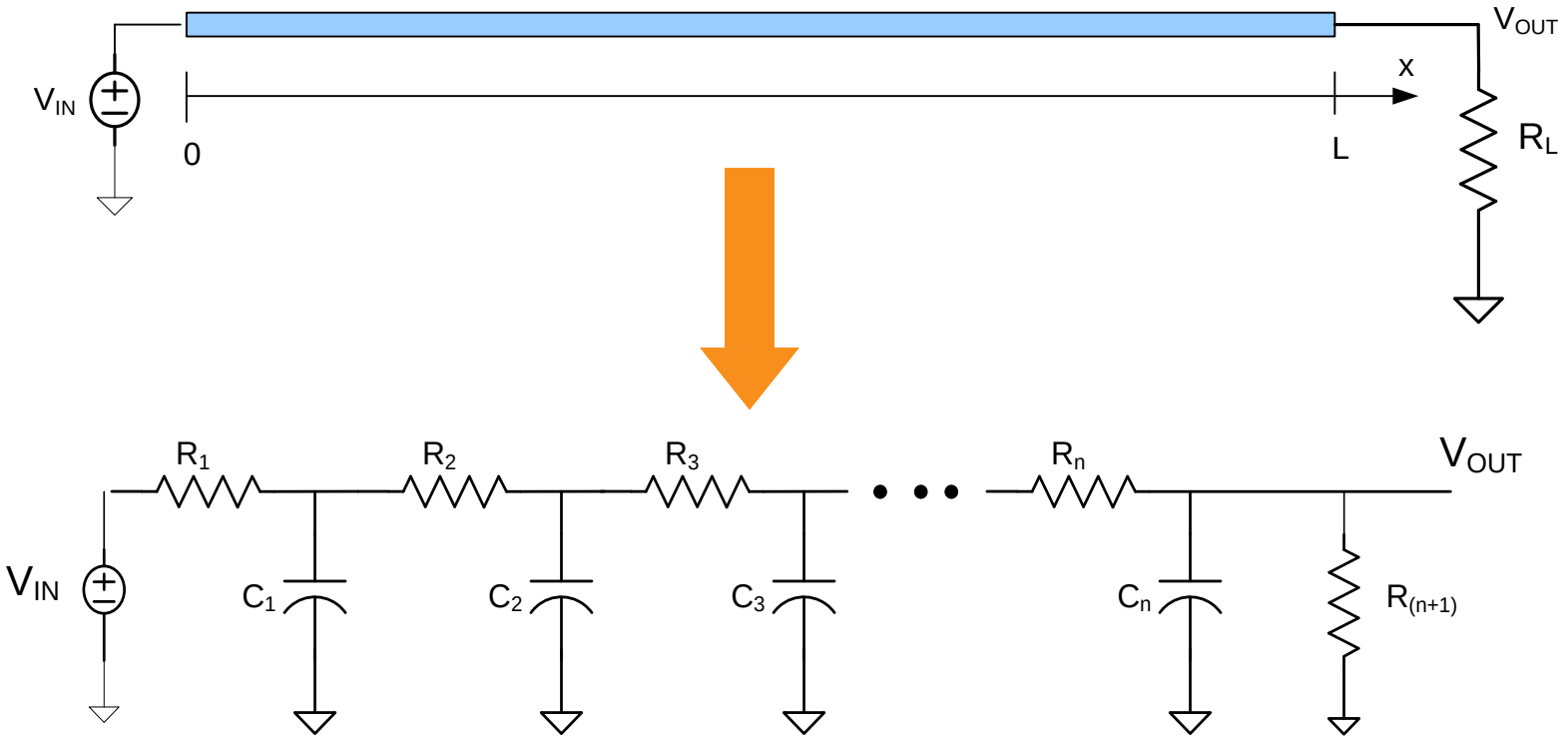


Simple Elmore delay:

$$t_{PD} = \sum_{i=1}^{n-1} \left(C_i \sum_{j=1}^{i} R_j \right) + C_n \left(\left(\sum_{j=1}^{n} R_j \right) // R_L \right)$$

Actually, R_L affects all of the delays and a modestly better but modestly more complicated delay model is often used

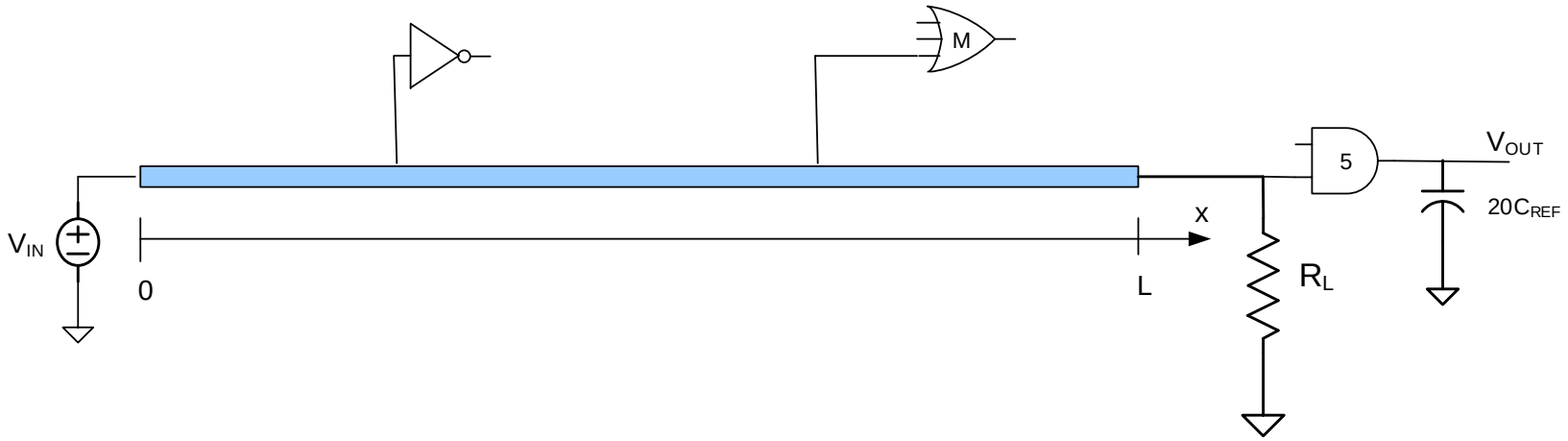
Elmore Delay Calculations



How are the number of stages chosen?

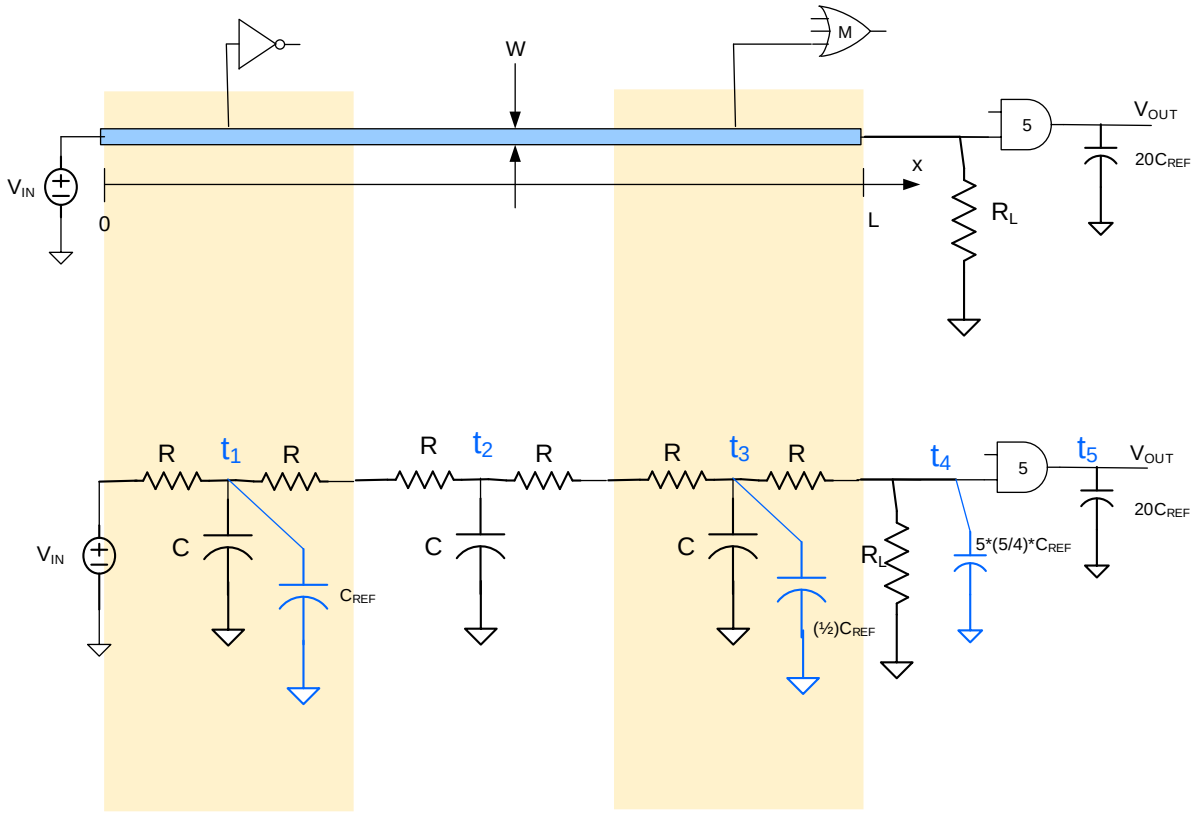
- **For hand analysis, keep number of stages small (maybe 3 or 4 for simple delay line) if possible**
- **If "faithfulness" is important, should keep the number of stages per unit length constant**

Elmore Delay Calculations



?

Elmore Delay Calculations



$$R = \frac{1}{6} R_{\square} \frac{L}{W}$$

$$C = \frac{1}{3} C_D$$

$$t_1 = R\left(C + C_{REF}\right) \qquad t_2 = 3RC \qquad t_3 = 5R\left(C + \frac{1}{2}C_{REF}\right) \qquad t_4 = \left[6R \,/\!/\!/\, R_L\right]\frac{25}{4}C_{REF} \qquad t_5 = t_{REF}\frac{20}{5}$$

$$t_{PROP} = \sum_{i=1}^{5} t_i$$

End of Lecture 43