EE 330
Homework 10
Spring 2018 Due Monday March 26.

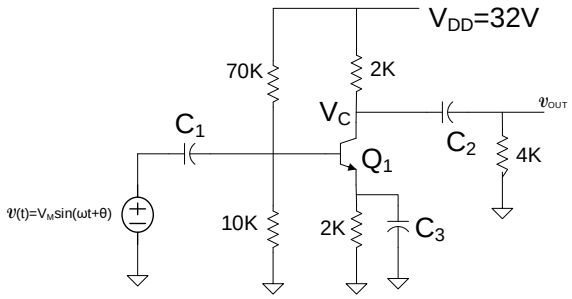
All problems are weighted equally. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$ ,$V_{Tn} = 0.5V$, and $\lambda=0$, and all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$ ,$V_{Tp}= -0.5V$, and $\lambda=0$. Correspondingly, assume all BJT transistors are from a process with $J_S$ at 300°K of $0.25fA/\mu^2$, $\beta_n=100$ and $\beta_p=25$. If the emitter area of a BJT is not given, assume it is $100\mu m^2$.

## Problem 1

Assume the capacitors are all very large.

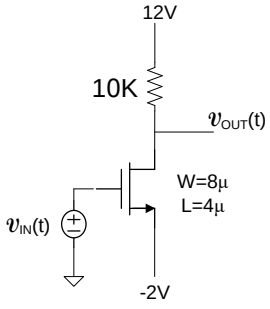
a) Obtain the small-signal voltage gain

b) Determine the small-signal output voltage $v_{OUT}$ if $V_M=1mV$ and $\omega=2000\pi$



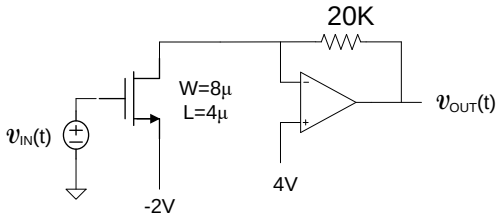

## Problem 2

Obtain the quiescent output voltage and the small signal voltage gain.




## Problem 3

Determine the small signal output voltage if the small signal input voltage is a sinusoidal 1KHz signal with 0-P amplitude of 25mV.

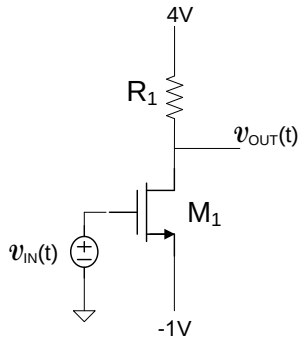


## Problem 4

a) Determine the maximum value of $R_1$ that will keep $M_1$ in saturation. $M_1$ has dimensions W=18u and L=2u.

b) If $R_1$ is 1/3 of the value determined in Part a), determine the small signal voltage gain of this circuit

c) With the value of $R_1$ used in part b), determine the total output voltage if $v_{IN}(t)=.001\sin(5000t+75^o)$.

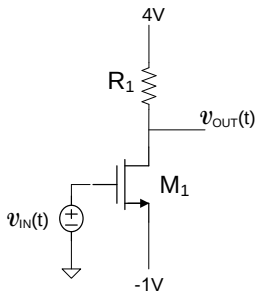



## Problem 5

Consider the following circuit where $R_1$=20K.

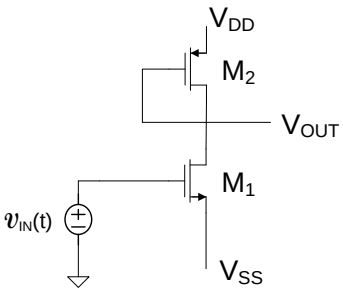
a) Size the device so that the amplifier has a voltage gain of -8.

b) With the sizing obtained for part a) determine the quiescent value of the output voltage (the voltage on the drain node of $M_1$)



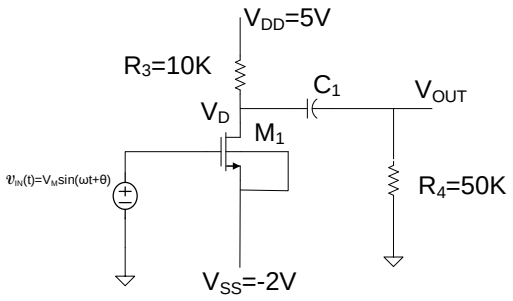

## Problem 6

Obtain an expression for the small signal output voltage in terms of the small signal parameters for the following circuit if the input is given by the expression $v_{IN}(t)=V_M\cos(\omega t+\theta)$. Assume $M_1$ is operating in the saturation region.



**Problem 7** In the circuit shown the dimensions of the transistor are W=8u and L=12u. Assume $C_1$ is very large.

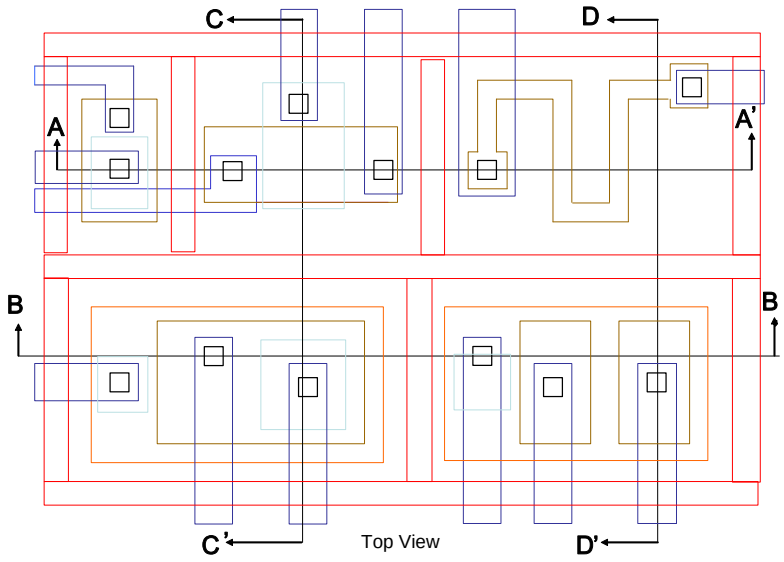
a) Draw the small signal equivalent circuit for the amplifier
b) Determine the quiescent value of $V_D$ and $V_{OUT}$
c) Obtain the small-signal voltage gain
d) Determine the small-signal output voltage $v_{OUT}$ if $V_M$=20mV

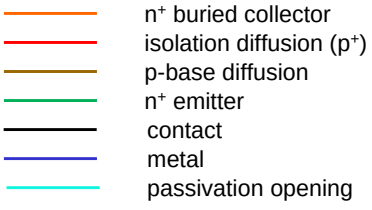



**Problem 8** Design an amplifier using only BJT transistors, resistors, capacitors and voltage sources that has a voltage gain of -5 when driving a 2K resistor.

**Problem 9** Design an amplifier using only MOS transistors, capacitors, and voltage sources that has a voltage gain of -10 when driving an external 10K resistor.

**Problem 10** Sketch a cross-section of the bipolar die along the BB' and CC' section lines for this bipolar layout.

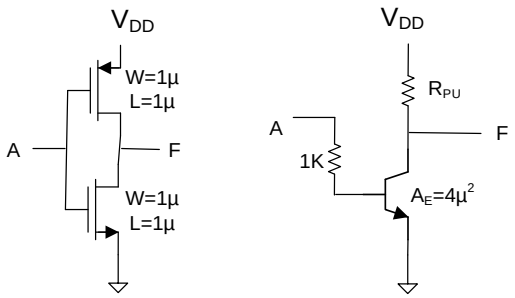


Problem 11 Two circuits that can perform as digital inverters are shown below. One is suitable for operation in a CMOS process and the other is for operation in a bipolar process (though the bipolar circuit will work, there are much better bipolar architectures). Assume $V_{DD}$ for both inverters is 5V and the λ parameter in the design rules for both processes is 0.5µm. Design rules and relevant device characteristics for both MOS and bipolar processes are attached to this assignment.

a) Determine minimum value of $R_{PU}$ that will assure that the BJT is operating in saturation when the A input is $V_{DD}$.

b) Quantitatively compare (with 10% accuracy) the area required for the layout of both inverters.



# Bipolar Process Characteristics

| Parameter | Typical | Tolerance[b] | Units |
|---|---|---|---|
| **Resistance and resistivity** | | | |
| Substrate resistivity | 16 | ±25% | Ω · cm |
| $n^+$ buried collector diffusion | 17 | ±35% | Ω / □ |
| Epitaxial layer | 1.6 | ±20% | Ω · cm |
| p-base diffusion | 160 | ±20% | Ω / □ |
| p-resistive diffusion (optional) | 1500 | ±40% | Ω / □ |
| $n^+$ emitter diffusion | 4.5 | ±30% | Ω / □ |
| Metal | 0.003 | | Ω / □ |
| Contacts ($3\mu \times 3\mu$) | <4 | | Ω |
| Metal-$n^+$ emitter (contact plus series resistance to BE junction) | <1 | | Ω |
| Metal-p-base[c] (contact plus series resistance) | 70 | | Ω |
| Metal-Epitaxial[d] (contact plus series resistance to BC junction) | 120 | | Ω |
| **Breakdown voltages, leakage currents, migration currents, and operating conditions** | | | |
| Reverse breakdown voltages | | | |
| $n^+$ emitter to p-base | 6.9 | ±50 mV | V |
| p-base to epitaxial | 70 | ±10 | V |
| Epitaxial to substrate | >80 | | V |
| Maximum operating voltage | 40 | | V |
| Substrate leakage current | 0.16 | | $fA/\mu^2$ |
| Maximum metal current density | 0.8 | | mA/$\mu$ width |
| Maximum device operating temperature (design) | 125 | | °C |
| Maximum device operating temperature (physical) | 225 | | °C |

**Capacitances**

| | | | |
|---|---|---|---|
| Metal to epitaxial | 0.022 | ±30% | fF/$\mu^2$ |
| Metal to p-base diffusion | 0.045 | ±30% | fF/$\mu^2$ |
| Metal to $n^+$ emitter diffusion | 0.078 | ±30% | fF/$\mu^2$ |
| $n^+$ buried collector to substrate (junction, bottom) | 0.062 | ±30% | fF/$\mu^2$ |
| Epitaxial to substrate (junction, bottom) | 0.062 | ±30% | fF/$\mu^2$ |
| Epitaxial to substrate (junction, sidewall) | 1.6 | ±30% | fF/$\mu$ perimeter |
| Epitaxial to p-base diffusion (junction, bottom) | 0.14 | ±30% | fF/$\mu^2$ |
| Epitaxial to p-base diffusion (junction, sidewall) | 7.9 | ±30% | fF/$\mu$ perimeter |
| p-base diffusion to $n^+$ emitter diffusion (junction, bottom) | 0.78 | ±30% | fF/$\mu^2$ |
| p-base diffusion to $n^+$ emitter diffusion (junction, sidewall) | 3.1 | ±30% | fF/$\mu$ perimeter |

| | Dimension |
|---|---|
| 1. $n^+$ buried collector diffusion (Yellow, Mask #1) | |
| 1.1 Width | 3λ |
| 1.2 Overlap of p-base diffusion (for vertical npn) | 2λ |
| 1.3 Overlap of $n^+$ emitter diffusion (for collector contact of vertical npn) | 2λ |
| 1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp) | 2λ |
| 1.5 Overlap of $n^+$ emitter diffusion (for base contact of lateral pnp) | 2λ |
| 2. Isolation diffusion (Orange, Mask #2) | |
| 2.1 Width | 4λ |
| 2.2 Spacing | 24λ |
| 2.3 Distance to $n^+$ buried collector | 14λ |
| 3. p-base diffusion (Brown, Mask #3) | |
| 3.1 Width | 3λ |
| 3.2 Spacing | 5λ |
| 3.3 Distance to isolation diffusion | 14λ |
| 3.4 Width (resistor) | 3λ |
| 3.5 Spacing (as resistor) | 3λ |
| 4. $n^+$ emitter diffusion (Green, Mask #4) | |
| 4.1 Width | 3λ |
| 4.2 Spacing | 3λ |
| 4.3 p-base diffusion overlap of $n^+$ emitter diffusion (emitter in base) | 2λ |
| 4.4 Spacing to isolation diffusion (for collector contact) | 12λ |
| 4.5 Spacing to p-base diffusion (for base contact of lateral pnp) | 6λ |
| 4.6 Spacing to p-base diffusion (for collector contact of vertical npn) | 6λ |
| 5. Contact (Black, Mask #5) | |
| 5.1 Size (exactly) | 4λ × 4λ |
| 5.2 Spacing | 2λ |
| 5.3 Metal overlap of contact | λ |
| 5.4 $n^+$ emitter diffusion overlap of contact | 2λ |
| 5.5 p-base diffusion overlap of contact | 2λ |
| 5.6 p-base to $n^+$ emitter | 3λ |
| 5.7 Spacing to isolation diffusion | 4λ |

| | |
|---|---|
| 6. Metalization (Blue, Mask #6) | |
| 6.1 Width | $2\lambda$ |
| 6.2 Spacing | $2\lambda$ |
| 6.3 Bonding pad size | $100\ \mu \times 100\ \mu$ |
| 6.4 Probe pad size | $75\ \mu \times 75\ \mu$ |
| 6.5 Bonding pad separation | $50\ \mu$ |
| 6.6 Bonding to probe pad | $30\ \mu$ |
| 6.7 Probe pad separation | $30\ \mu$ |
| 6.8 Pad to circuitry | $40\ \mu$ |
| 6.9 Maximum current density | $0.8\ \text{mA}/\mu$ width |
| 7. Passivation (Purple, Mask #7) | |
| 7.1 Minimum bonding pad opening | $90\ \mu \times 90\ \mu$ |
| 7.2 Minimum probe pad opening | $65\ \mu \times 65\ \mu$ |

# CMOS Process Characteristics

**Process parameters for a typical[a] p-well CMOS process**

| | Typical | Tolerance[b] | Units |
|---|---|---|---|
| **Square law model parameters** | | | |
| $V_{T0}$ (threshold voltage) | | | |
| n-channel ($V_{TN0}$) | 0.75 | ± 0.25 | V |
| p-channel ($V_{TP0}$) | −0.75 | ± 0.25 | V |
| $K'$(conduction factor) | | | |
| n-channel | 24 | ± 6 | $\mu A/V^2$ |
| p-channel | 8 | ± 1.5 | $\mu A/V^2$ |
| $\gamma$(body effect) | | | |
| n-channel | 0.8 | ± 0.4 | $V^{1/2}$ |
| p-channel | 0.4 | ± 0.2 | $V^{1/2}$ |
| $\lambda$(channel length modulation) | | | |
| n-channel | 0.01 | ± 50% | $V^{-1}$ |
| p-channel | 0.02 | ± 50% | $V^{-1}$ |
| $\phi$(surface potential) | | | |
| n- and p-channel | 0.6 | ± 0.1 | V |
| **Process parameters** | | | |
| $\mu$ (channel mobility) | | | |
| n-channel | 710 | | $cm^2/(V \cdot s)$ |
| p-channel | 230 | | $cm^2/(V \cdot s)$ |
| **Doping[c]** | | | |
| $n^+$ active | 5 | ±4 | $10^{18}/cm^3$ |
| $p^+$ active | 5 | ±4 | $10^{17}/cm^3$ |
| p-well | 5 | ±2 | $10^{16}/cm^3$ |
| n-substrate | 1 | ±0.1 | $10^{16}/cm^3$ |

| Physical feature sizes | | | |
|---|---|---|---|
| $T_{ox}$ (gate oxide thickness) | 500 | ± 100 | Å |
| Total lateral diffusion | | | |
| n-channel | 0.45 | ± 0.15 | $\mu$ |
| p-channel | 0.6 | ± 0.3 | $\mu$ |
| Diffusion depth | | | |
| $n^+$ diffusion | 0.45 | ± 0.15 | $\mu$ |
| $p^+$ diffusion | 0.6 | ± 0.3 | $\mu$ |
| p-well | 3.0 | ± 30% | $\mu$ |
| **Insulating layer separation** | | | |
| POLY I to POLY II | 800 | ± 100 | Å |
| Metal 1 to Substrate | 1.55 | ± 0.15 | $\mu$ |
| Metal 1 to Diffusion | 0.925 | ± 0.25 | $\mu$ |
| POLY I to Substrate (POLY I on field oxide) | 0.75 | ± 0.1 | $\mu$ |
| Metal 1 to POLY I | 0.87 | ± 0.7 | $\mu$ |
| Metal 2 to Substrate | 2.7 | ± 0.25 | $\mu$ |
| Metal 2 to Metal I | 1.2 | ± 0.1 | $\mu$ |
| Metal 2 to POLY I | 2.0 | ± 0.07 | $\mu$ |
| **Capacitances**[d] | | | |
| $C_{OX}$ (gate oxide capacitance, n- and p-channel) | 0.7 | ±0.1 | fF/$\mu^2$ |
| POLY I to substrate, poly in field | 0.045 | ±0.01 | fF/$\mu^2$ |
| POLY II to substrate, poly in field | 0.045 | ±0.01 | fF/$\mu^2$ |
| Metal 1 to substrate, metal in field | 0.025 | ±0.005 | fF/$\mu^2$ |
| Metal 2 to substrate, metal in field | 0.014 | ±0.002 | fF/$\mu^2$ |
| POLY I to POLY II | 0.44 | ±0.05 | fF/$\mu^2$ |
| POLY I to Metal 1 | 0.04 | ±0.01 | fF/$\mu^2$ |
| POLY I to Metal 2 | 0.039 | ±0.003 | fF/$\mu^2$ |
| Metal 1 to Metal 2 | 0.035 | ±0.01 | fF/$\mu^2$ |
| Metal 1 to diffusion | 0.04 | ±0.01 | fF/$\mu^2$ |
| Metal 2 to diffusion | 0.02 | ±0.005 | fF/$\mu^2$ |
| $n^+$ diffusion to p-well (junction, bottom) | 0.33 | ±0.17 | fF/$\mu^2$ |
| $n^+$ diffusion sidewall (junction, sidewall) | 2.6 | ±0.6 | fF/$\mu$ |
| $p^+$ diffusion to substrate (junction, bottom) | 0.38 | ±0.12 | fF/$\mu^2$ |
| $p^+$ diffusion sidewall (junction, sidewall) | 3.5 | ±2.0 | fF/$\mu$ |
| p-well to substrate (junction, bottom) | 0.2 | ±0.1 | fF/$\mu^2$ |
| p-well sidewall (junction, sidewall) | 1.6 | ±1.0 | fF/$\mu$ |
| **Resistances** | | | |
| Substrate | 25 | ±20% | Ω-cm |
| p-well | 5000 | ±2500 | Ω/□ |
| $n^+$ diffusion | 35 | ±25 | Ω/□ |
| $p^+$ diffusion | 80 | ±55 | Ω/□ |
| Metal | 0.003 | ±25% | Ω/□ |
| Poly | 25 | ±25% | Ω/□ |
| Metal 1–Metal 2 via (3 $\mu$ × 3 $\mu$ contact) | <0.1 | | Ω |
| Metal 1 contact to POLY I (3 $\mu$ × 3 $\mu$ contact) | <10 | | Ω |
| Metal 1 contact to $n^+$ or $p^+$ diffusion (3 $\mu$ × 3 $\mu$ contact) | <5 | | Ω |

| | | Dimensions | |
|---|---|---|---|
| | | **Microns** | **Scalable** |
| 1. | p-well (CIF Brown, Mask #1[a]) | | |
| 1.1 | Width | 5 | 4λ |
| 1.2 | Spacing (different potential) | 15 | 10λ |
| 1.3 | Spacing (same potential) | 9 | 6λ |
| 2. | Active (CIF Green, Mask #2) | | |
| 2.1 | Width | 4 | 2λ |
| 2.2 | Spacing | 4 | 2λ |
| 2.3 | $p^+$ active in n-subs to p-well edge | 8 | 6λ |
| 2.4 | $n^+$ active in n-subs to p-well edge | 7 | 5λ |
| 2.5 | $n^+$ active in p-well to p-well edge | 4 | 2λ |
| 2.6 | $p^+$ active in p-well to p-well edge | 1 | λ |
| 3. | Poly (POLY I) (CIF Red, Mask #3) | | |
| 3.1 | Width | 3 | 2λ |
| 3.2 | Spacing | 3 | 2λ |
| 3.3 | Field poly to active | 2 | λ |
| 3.4 | Poly overlap of active | 3 | 2λ |
| 3.5 | Active overlap of poly | 4 | 2λ |
| 4. | $p^+$ select (CIF Orange, Mask #4) | | |
| 4.1 | Overlap of active | 2 | λ |
| 4.2 | Space to $n^+$ active | 2 | λ |
| 4.3 | Overlap of channel[b] | 3.5 | 2λ |
| 4.4 | Space to channel[b] | 3.5 | 2λ |
| 4.5 | Space to $p^+$ select | 3 | 2λ |
| 4.6 | Width | 3 | 2λ |

| | | | | |
|---|---|---|---|---|
| 7. | Via [e](CIF Purple Hatched, Mask #C1) | | | |
| | 7.1 | Size, exactly | 3 × 3 | 2λ × 2λ |
| | 7.2 | Separation | 3 | 2λ |
| | 7.3 | Space to poly edge | 4 | 2λ |
| | 7.4 | Space to contact | 3 | 2λ |
| | 7.5 | Overlap by metal 1 | 2 | λ |
| | 7.6 | Overlap by metal 2 | 2 | λ |
| | 7.7 | Space to active edge | 3 | 2λ |
| 8. | Metal 2 (CIF Orange Hatched, Mask #C2) | | | |
| | 8.1 | Width | 5 | 3λ |
| | 8.2 | Spacing | 5 | 3λ |
| | 8.3 | Bonding pad size | 100 × 100 | 100 μ × 100 μ |
| | 8.4 | Probe pad size | 75 × 75 | 75 μ × 75 μ |
| | 8.5 | Bonding pad separation | 50 | 50 μ |
| | 8.6 | Bonding to probe pad | 30 | 30 μ |
| | 8.7 | Probe pad separation | 30 | 30 μ |
| | 8.8 | Pad to circuitry | 40 | 40 μ |
| | 8.9 | Maximum current density | 0.8 mA/μ | 0.8 mA/μ |
| 9. | Passivation[f] (CIF Purple Dashed, Mask #8) | | | |
| | 9.1 | Bonding pad opening | 90 × 90 | 90 μ × 90 μ |
| | 9.2 | Probe pad opening | 65 × 65 | 65 μ × 65 μ |
| 10. | Metal 2 crossing coincident metal 1 and poly[g] | | | |
| | 10.1 | Metal 1 to poly edge spacing when crossing metal 2 | 2 | λ |
| | 10.2 | Rule domain | 2 | λ |
| 11. | Electrode (POLY II)[h] (CIF Purple Hatched, Mask #A1) | | | |
| | 11.1 | Width | 3 | 2λ |
| | 11.2 | Spacing | 3 | 2λ |
| | 11.3 | POLY I overlap of POLY II | 2 | λ |
| | 11.4 | Space to contact | 3 | 2λ |