EE 330 Fall 2012
Homework 4

Due Friday September 14 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

Problem 1 (10 points):
Please solve problem 3.1 of Weste and Harris (WH)

Problem 2 (10 points):
Please solve problem 3.2 of WH

Problem 3 (10 points):
Please solve problem 3.5 of WH

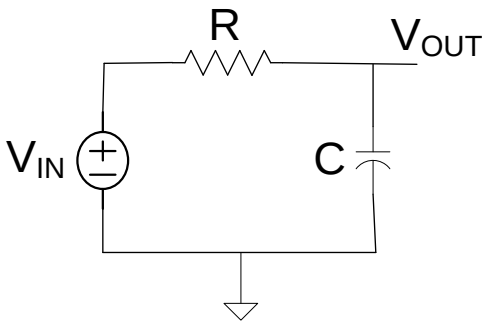
Problem 4 (10 points):
Please solve problem 3.7 of WH

Problem 5 (15 points):

A first-order RC filter is shown. The 3dB bandwidth of this filter is given by $\omega_{3dB} = \frac{1}{RC}$.

Assume Poly 1 is used to make the resistor and that the capacitor is a Poly-Insulator-Poly (PIP) capacitor. This filter is to be fabricated in the ON 0.5u CMOS process that is characterized by the parameters given at:
http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t6au-params.txt.

a) Design this circuit and estimate the area required to implement this filter in your design if the 3dB bandwidth is to be located at 5K rad/sec.
b) If the resistor is too big or the capacitor is too big, the area required to realize this filter becomes very large. Determine the value of R and C that will minimize the total area and compare this minimum area with the area you arrived at in part (a).

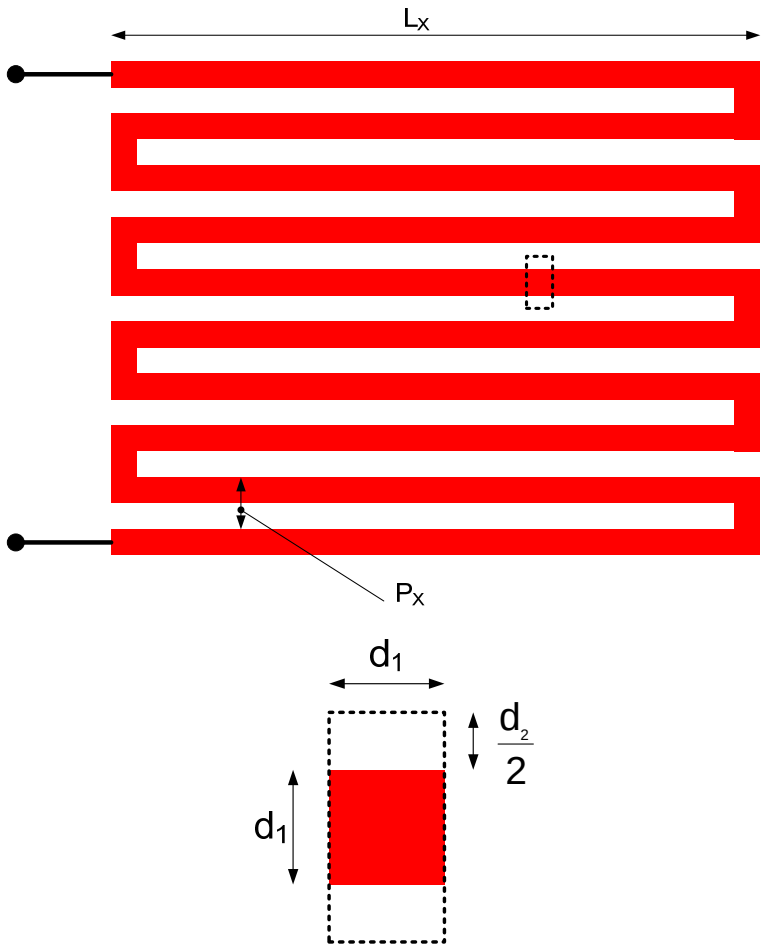


Problem 6 (5 points):
Thermal oxide growth of field oxide causes the wafer surface to become somewhat nonplanar. If 8000Å of field oxide is thermally grown, what is the difference in the thickness of the wafer between regions where field oxide is present and where it is absent?

Problem 7 (15 points):
Compare the area required for the layout of a 100k resistor using Poly-2 to that required using p+ diffusion in the ON 0.5u CMOS process. Use a serpentine layout with minimum width and minimum spacing for the resistive elements and be sure that you meet the design rules of the process. The sheet resistance is characterized in the parameter file located at:
http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t6au-params.txt
(A brief discussion of a serpentine layout appears below).

Serpentine layout:

A serpentine layout is shown below. For large valued resistors, the length LX is generally much larger than the pitch, PX. The dashed box which includes exactly one square of resistance is expanded below. The dimension d1 corresponds to the minimum width of the resistor and d2 to the minimum spacing.



Problem 8 & 9 (20 points):
Implement the 3-input NAND or NOR gate from your Lab 4 in Verilog. Also, implement your logic function. Clearly state what your logic function was and whether you chose to do a NAND or NOR gate. Show correct function with sufficient simulation.

Problem 10 (5 points):
The term dual damascene refers to a particular type of interconnect. What does this refer to and what are the benefits of a process that provides dual damascene interconnects?