EE 330
Homework 1
Fall 2018

Due Friday August 24

Problem 1 Assume a simple circuit requires 2,000 MOS transistors on a die and that all transistors are minimum sized. If the transistors are fabricated in a 7nm CMOS process (the dimensions of a minimum-sized transistor are 7nm x 7nm) and the spacing overhead for the transistors is a factor of 10 (Spacing overhead is needed to allow for electrical separation between devices. With a spacing overhead of 10, often designated as 10x, the average area per transistor is assumed to be 10 times larger than the transistor itself.), determine the number of die that can be fabricated on a 12" silicon wafer. Neglect the area required for the bonding pads of the circuit (bonding pad area actually dominates the die area for integrated circuits with a small number of small MOS transistors but is neglected in this problem).

Problem 2 If the cost of a 12 inch wafer (actually 300mm) is $3500, determine the cost/die for the circuit in Problem 1.

Problem 3 How many 7 nm transistors can be placed on a die that has the same area as a single ink drop from an ink-jet printer? Assume a 10x spacing overhead.

Problem 4 The clock frequency of microprocessors has not increased appreciably for the past several years yet performance is improving through the parallelism offered by multiple cores. Why is it more energy efficient to use multiple cores on a die each operating at a lower clock rate than to have a single core operating at a higher clock frequency?

Problem 5 How does the feature size (minimum gate length) in a 7nm process compare to the approximate "diameter" of a silicon atom? To a SiO_2 molecule? To the diameter of a human hair?

Problem 6 How do the annual sales of Samsung compare to the annual sales of Saudi Aramco, the largest oil producing company in the world and Nestle's, the largest food producing company in the world? Be quantitative.

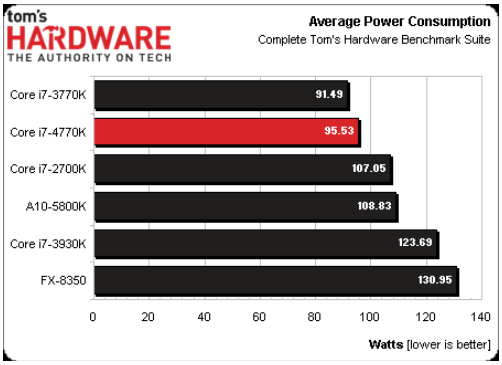
Problem 7
What is the feature size used in the Intel Cannon Lake processor?

Problem 8 The current flow into a microprocessor can be quite large. There are various methods for connecting a power supply to an integrated circuit but one way is with gold wires that are termed "bonding wires". Assuming the average supply voltage of the Quad Core Intel i7 3930K is 1.2V and the power dissipation is 95 watts.

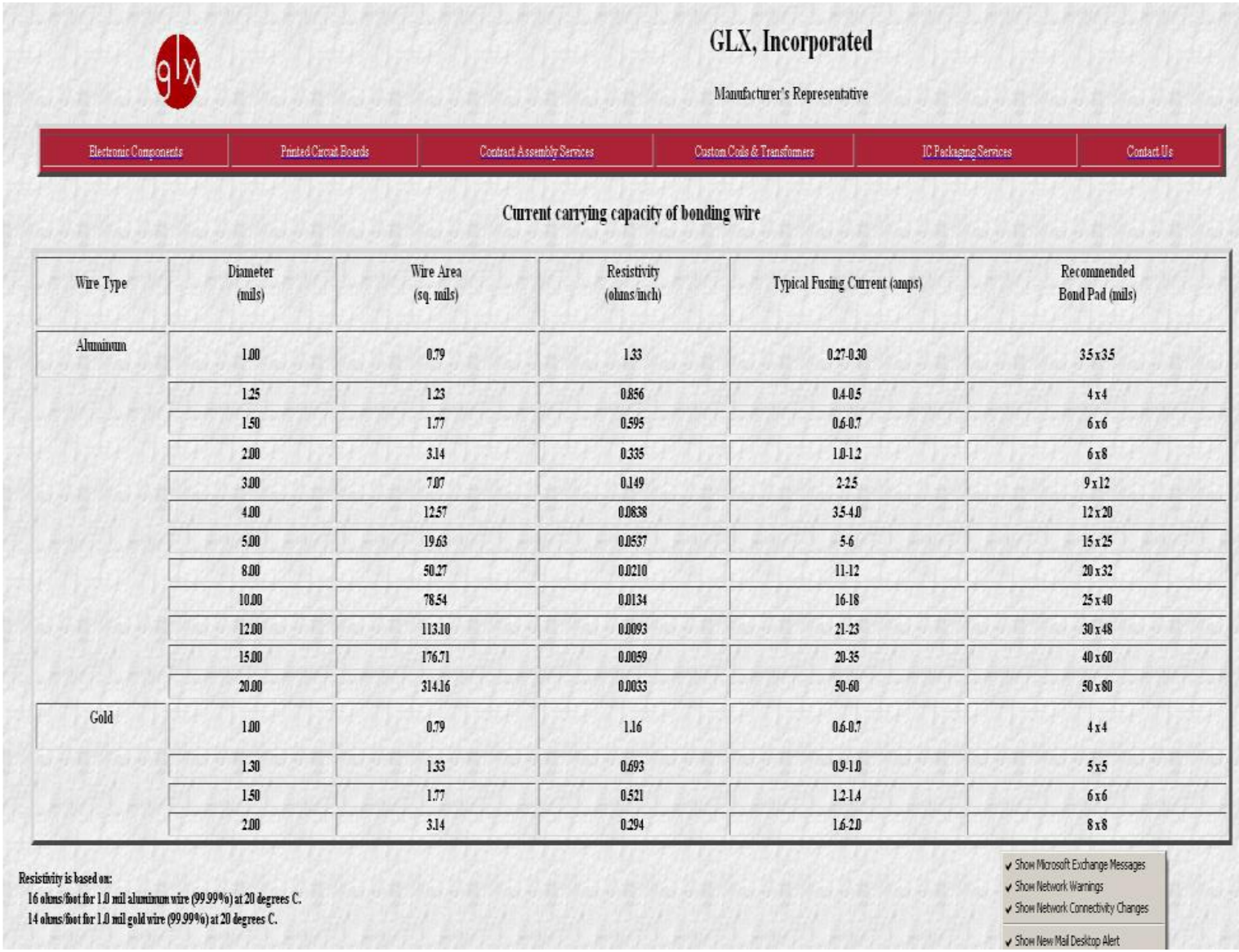
a) What is the current draw from the 1.2V supply?
b) What would be the voltage drop in a bonding wire if a single gold wire that is 25.5um (1 mil) in diameter and ½ inch long is used to bring power into the processor?

c) What would be the power dissipated in this wire?

d) How many parallel gold wires that are 25.5um in diameter would be needed to guarantee that the current in these interconnects is at most 10% of the fusing current? (Power requirements for some Intel processors and some properties of bonding wires are attached).



Some Properties of Gold and Aluminum Wires



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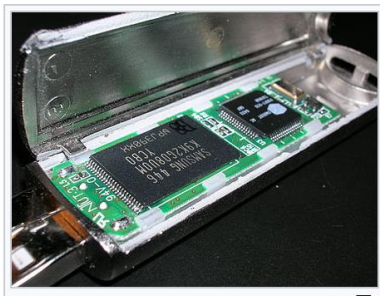
Current carrying capacity of bonding wire

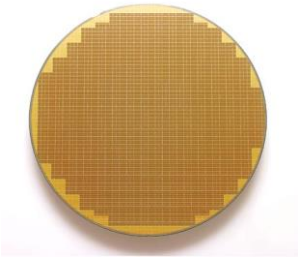
Wire Type	Diameter (mils)	Wire Area (sq. mils)	Resistivity (ohms/inch)	Typical Fusing Current (amps)	Recommended Bond Pad (mils)
Aluminum	1.00	0.79	1.33	0.27-0.30	3.5 x 3.5
	1.25	1.23	0.856	0.4-0.5	4 x 4
	1.50	1.77	0.595	0.6-0.7	6 x 6
	2.00	3.14	0.335	1.0-1.2	6 x 8
	3.00	7.07	0.149	2-2.5	9 x 12
	4.00	12.57	0.0838	3.5-4.0	12 x 20
	5.00	19.63	0.0537	5-6	15 x 25
	8.00	50.27	0.0210	11-12	20 x 32
	10.00	78.54	0.0134	16-18	25 x 40
	12.00	113.10	0.0093	21-23	30 x 48
	15.00	176.71	0.0059	20-35	40 x 60
	20.00	314.16	0.0033	50-60	50 x 80
Gold	1.00	0.79	1.16	0.6-0.7	4 x 4
	1.30	1.33	0.693	0.9-1.0	5 x 5
	1.50	1.77	0.521	1.2-1.4	6 x 6
	2.00	3.14	0.294	1.6-2.0	8 x 8

Resistivity is based on:
16 ohms/foot for 1.0 mil aluminum wire (99.99%) at 20 degrees C.
14 ohms/foot for 1.0 mil gold wire (99.99%) at 20 degrees C.

Problem 9-10 Data is stored in many different ways but today the most popular strategies for storage that can be rapidly retrieved are CDs, DVDs, Blu Ray DVDs, hard disks, static memory (SRAM), dynamic memory (DRAM), and Flash Memory. The first three store data physically on metal/plastic media and retrieve it optically. Hard disks store data magnetically. SRAMs and DRAMs store data electronically in semiconductor materials. Flash memory devices store data electronically in floating gate transistors. Using a table, make a comparison of the storage density (bits per cm^2) and the commercial cost of storage per bit in these 7 different media. In making this comparison, try to use state of the art parts or components and, when appropriate, state which part you are using and the approximate cost for the component or device.

Based upon this comparison, what is the lowest cost method for storing data and what is the ratio in the cost/bit between the most expensive and the least expensive data storage approaches in this comparison?





Problem 11 There are varying estimates by presumably reputable sources on the number of people that will be using smart phones on a global basis by the year 2020. What are the prediction extremes? Give the sources of your data.

Problem 12 What percent of the smart phones today use the Android OS?, the Apple OS?, any other OS?

Problem 13 Compare the number of smart phones sold in 2016 to the number of smart phone users in 2016. Comment on the useful "life" of a smart phone and the corresponding market potential.

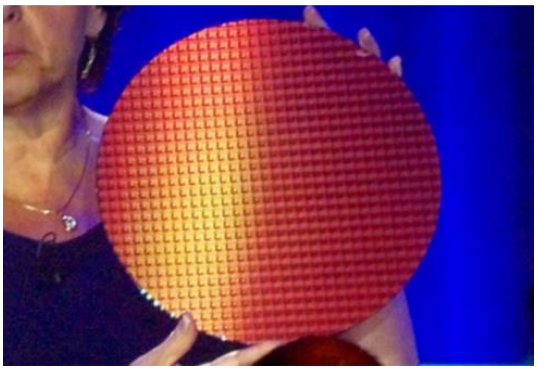
Problem 14 A major engineering effort is required to support the mobile-phone industry. This includes engineers that work all the way from the infrastructure level down to the process development level. Using the number of smart phone users in the world and worldwide annual

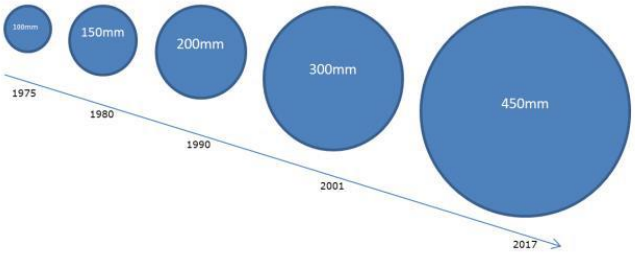
smart-phone sales obtained in the previous problem, obtain a very approximate estimate of the level of the engineering workforce that is needed to support the smart phone industry. In making this assessment, make the following basic simplifying assumptions. Assume the average smart-phone selling price is $500 (this is not the "plan" price) and the average salary of engineers is $60,000 (of course some get paid much more and some much less in different parts of the world). If 10% of the total mobile-phone sales revenue is invested in the salary of engineers responsible for development of the mobile-phone infrastructure, how many full-time engineers are needed worldwide to support the growing mobile-phone industry?

Problem 15 A picture of a woman holding a wafer of Intel Skylane chips is shown below on the left. Standard wafer sizes in the industry are shown below on the right.

a) Determine the approximate number of Skylane chips on this wafer

b) If the yield is 90% and the manufacturing costs for the wafer are $2500, what is the cost of manufacturing a Skylane chip?





Problem 16 Using ModelSim create a 3-input **AND** and a 2-input **NOR** gate. Create a test bench for the code to verify the operation of the design. Provide both your code and the test bench results (appropriate results/waveforms). Use the same input signals for verifying the operation of the **AND** and **NOR** gates in the test bench.