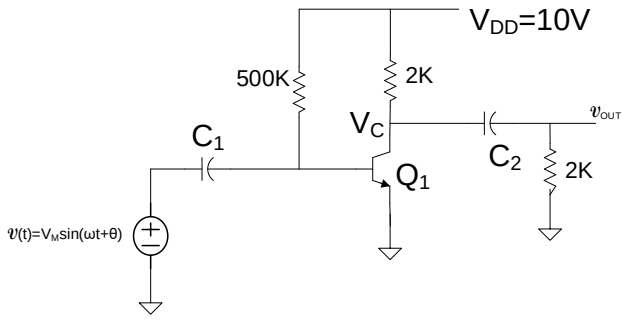
EE 330
Homework 9
Spring 2018
Due Wed March 7 at the beginning of class (no late HW accepted)

All problems are worth 10 points except Problems 8-9 which are worth 20 points. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$ and $V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$ and $V_{Tp} = -0.5V$. Correspondingly, assume all npn BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. If parameters are needed for CMOS process characterization beyond what is given, use the measured parameters from the TSMC 0.18μ process given below as model parameters. Assume all diodes are characterized by the model parameters $J_{SX}=0.5A/\mu m^2$, $V_{G0}=1.17V$, and $m=2.3$.

Problem 1

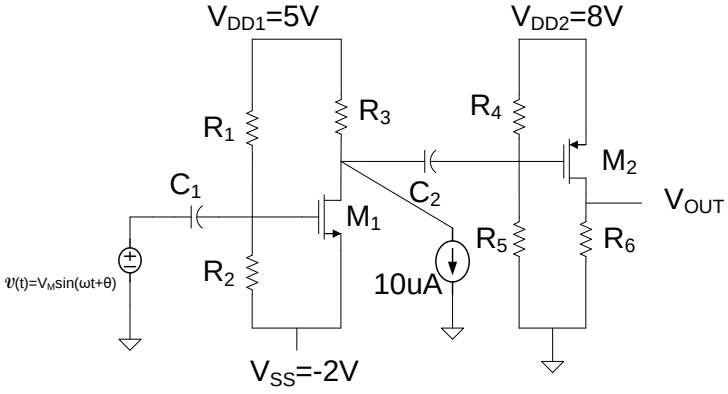
Assume the capacitors are very large and V_M is small.

a) Draw the small signal equivalent circuit for the amplifier shown
b) Determine the quiescent value of V_C and V_{OUT}
c) Determine the voltage gain in terms of the small-signal y-parameters for the transistor. Assume the parameter y_{21} in the model of the transistor is 0.



Problem 2

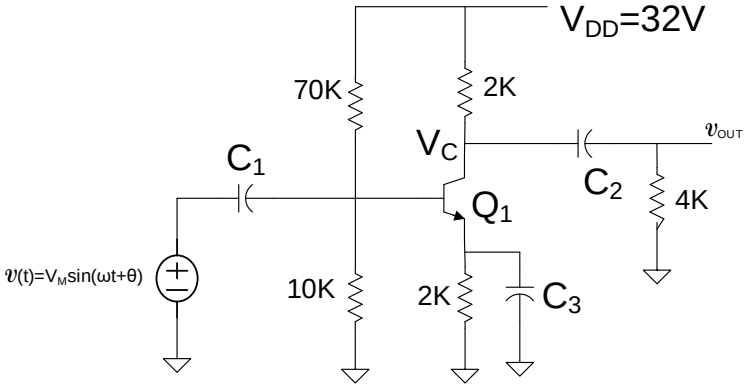
Obtain the small signal equivalent circuit for the following network. Assume the transistors are operating in the saturation region, all capacitors are large, and V_M is small. You need not solve the circuit.



Problem 3 Assume the capacitors are all very large and V_m is small.

a) Draw the small signal equivalent circuit for the amplifier shown

b) Determine the quiescent value of V_C and V_{OUT}



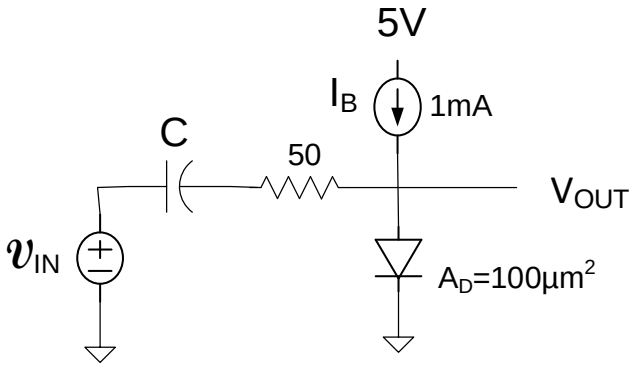
Problem 4 Consider the following circuit operating at T=300K. Assume the capacitor C is very large and the v_{IN} is a small-signal input.

a) Determine the quiescent output voltage.

b) Draw the small-signal equivalent circuit

c) Determine the small-signal voltage gain from the input to the output.

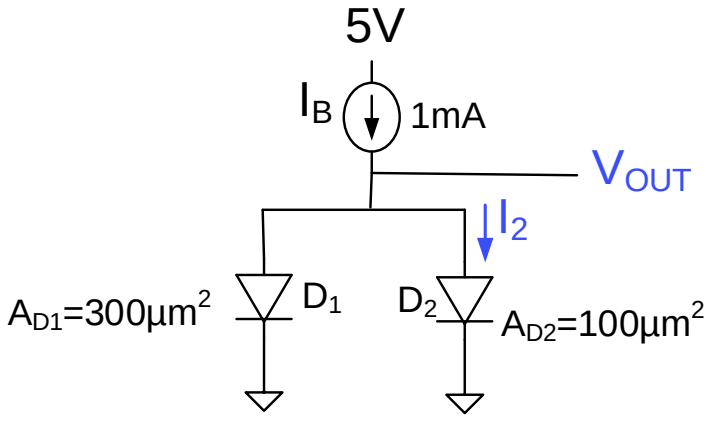
d) Repeat part c) if the current I_B is increased to 5mA



Problem 5 Consider the following circuit operating at T=300K.

a) Determine I_2

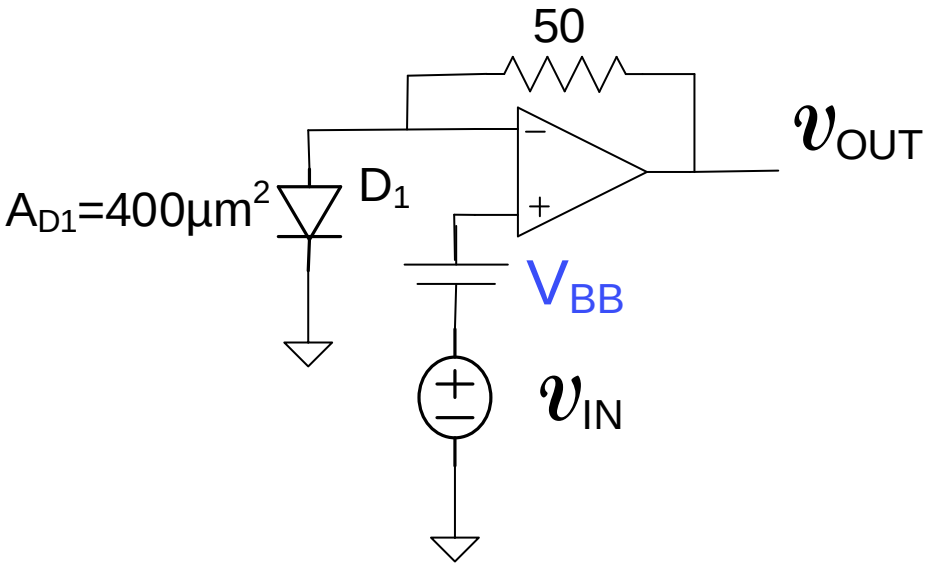
b) Accurately determine the voltage V_{OUT}



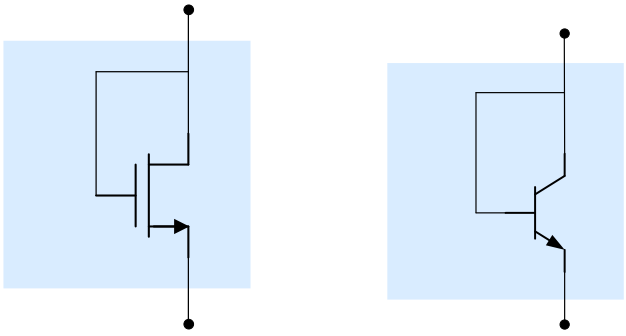
Problem 6 Consider the following circuit operating at T=300K. Assume v_{IN} is a small-signal voltage source.

a) If the voltage V_{BB} is adjusted so that the quiescent diode current is 1mA, determine the small signal voltage gain $A_V = \frac{v_{OUT}}{v_{IN}}$

b) Repeat part a) if V_{BB} is adjusted so that the quiescent diode current is 10mA



Problem 7 Obtain the small signal impedance between the two terminals exiting the box. Assume the MOSFET is operating in the Saturation region and the BJT in the Forward Active region and that the quiescent currents are both 1mA.



Problems 8-9 Use Modelsim to create a 4-bit register. The register should only change its value on a positive clock edge. Include an enable bit and make the register only change its's value if the enable bit is high during the positive clock edge. Create a test bench to test the correct operation of the register. Include screenshots of your Verilog code, and simulation waveforms.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.51	volts
SHORT	20.0/0.18			
Idss		547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE	20.0/0.18			
Ids0		14.4	-4.7	pA/um
LARGE	50/50			
Vth		0.43	-0.42	volts
Vjbkd		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS

Sheet Resistance	6.7	7.8	8.0	59.7	313.6	0.08	0.08	ohms/sq
Contact Resistance	10.6	11.0	10.0				4.79	ohms
Gate Oxide Thickness	41							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08		0.08	0.08	0.03	930	ohms/sq
Contact Resistance	9.24		14.05	18.39	20.69		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34				984	aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235	41	35	29	21	14							aF/um
Fringe (poly)			70	39	29	23	20	17						aF/um
Fringe (metal1)				52	34		22	19						aF/um
Fringe (metal2)					48	35	27	22						aF/um
Fringe (metal3)						53	34	27						aF/um
Fringe (metal4)							58	35						aF/um
Fringe (metal5)								55						aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.72	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		300.36	MHz
DIV1024 (31-stg,1.8V)		363.77	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate