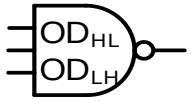
EE 330
Lecture 43

Digital Circuits

- Logic Effort
- Elmore Delay
- Power Dissipation
- Other Logic Styles
- Dynamic Logic Circuits

Propagation Delay in Multiple-Levels of Logic with Stage Loading

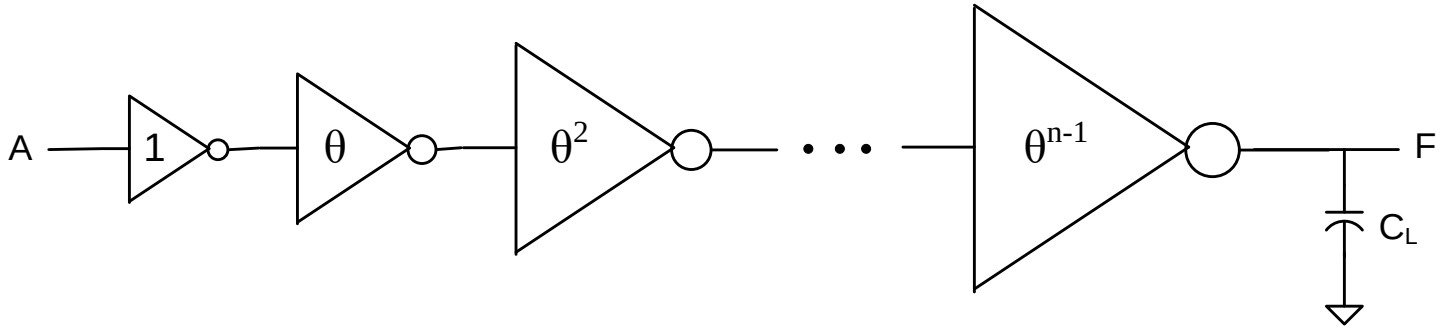
Asymmetric-sized gates



	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2}\sum_{k=1}^{5} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)\right)$$

Optimal Driving of Capacitive Loads



$$\theta_{OPT} = e$$

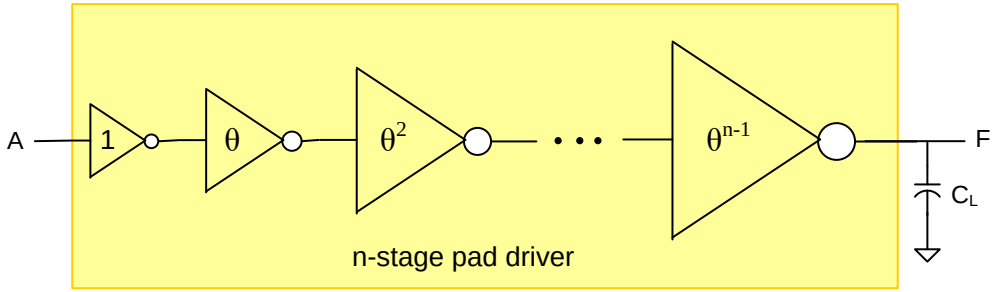
$$\theta^n C_{REF} = C_L$$

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right)$$

$$t_{PROP} = t_{REF}\frac{\theta}{\ln(\theta)}\left[\ln\frac{C_L}{C_{REF}}\right]$$

$$t_{PROP} = t_{REF}\, e\left[\ln\frac{C_L}{C_{REF}}\right] = n\theta t_{REF}$$

Optimal Driving of Capacitive Loads



Example: Design a pad driver for driving a load capacitance of 10pF, determine t_{PROP} for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

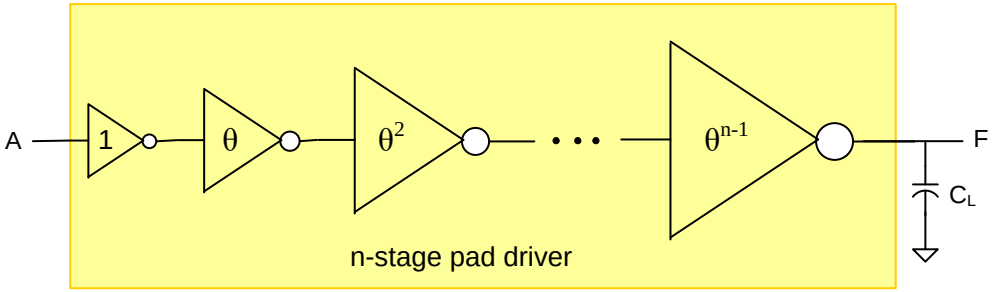
$W_{nk}=2.5^{k-1}$, $W_{pk}=3\bullet 2.5^{k-1}$

$L_n=L_p=L_{MIN}$

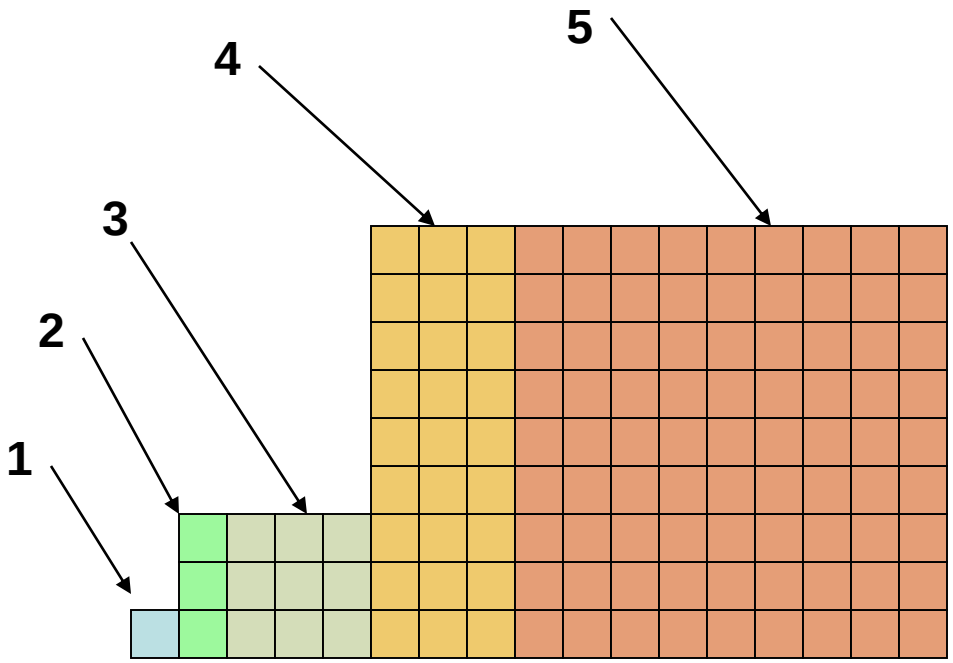
k	n-channel		p-channel	
1	1	WMIN	3	WMIN
2	2.5	WMIN	7.5	WMIN
3	6.25	WMIN	18.75	WMIN
4	15.6	WMIN	46.9	WMIN
5	39.1	WMIN	117.2	WMIN
6	97.7	WMIN	293.0	WMIN
7	244.1	WMIN	732.4	WMIN
8	610.4	WMIN	1831.1	WMIN

Note devices in last stage are very large !

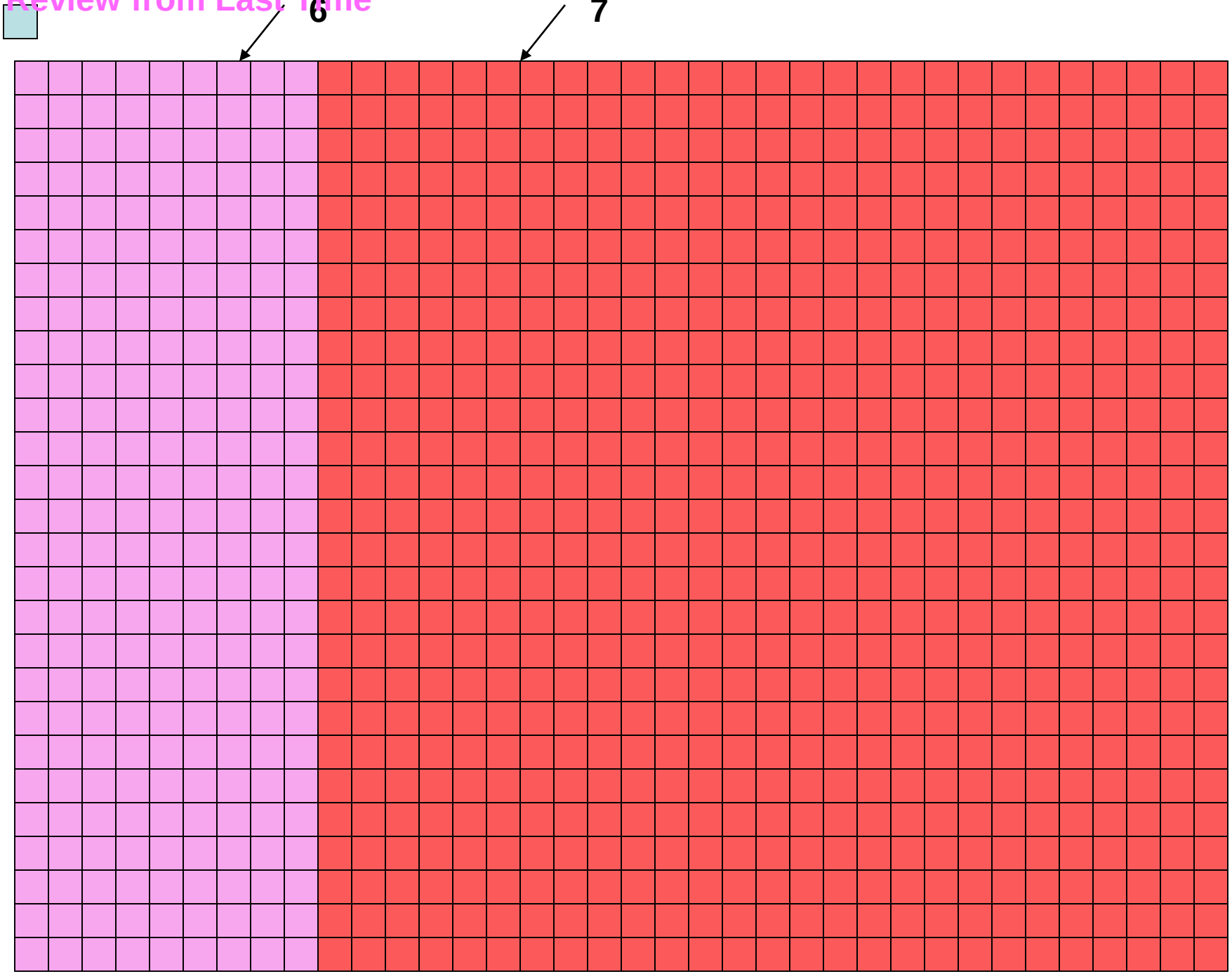
Pad Driver Size Implications



Consider a 7-stage pad driver and assume θ = 3

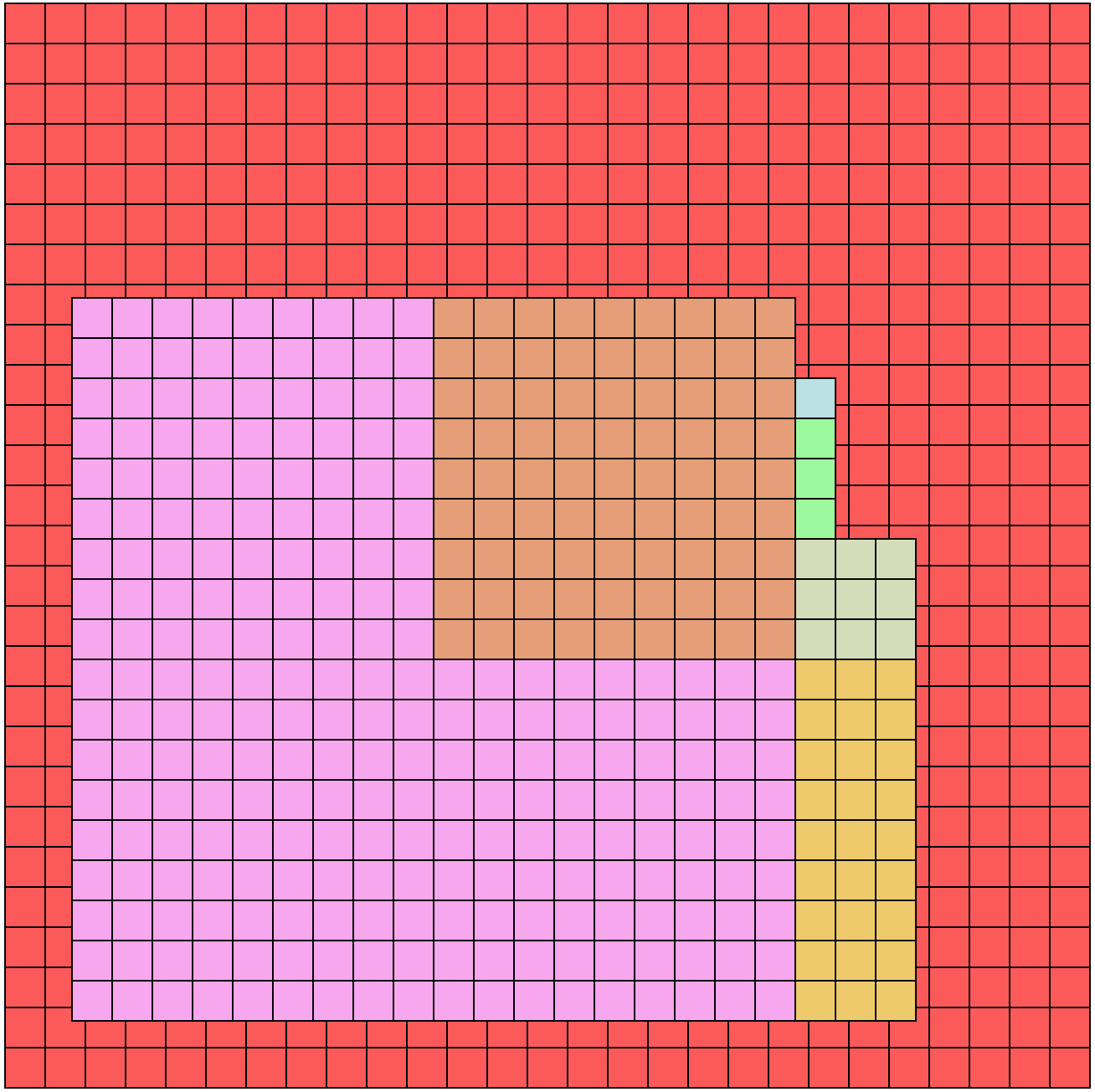


Review from Last Time



Review from Last Time

Area of Last Stage Larger than that of all previous stages combined!



Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial

Propagation Delay in "Logic Effort" approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

Propagation delay for equal rise/fall gates was derived to be

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

Delay calculations with "logical effort" approach

Logical effort delay approach:

$$t_{PROP} = \sum_{k=1}^{n} f_k$$

(t_{REF} scaling factor not explicitly stated)

where f_k is the "effort delay" of stage k

$$f_k = g_k h_k$$

g_k=logical effort

h_k=electrical effort

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

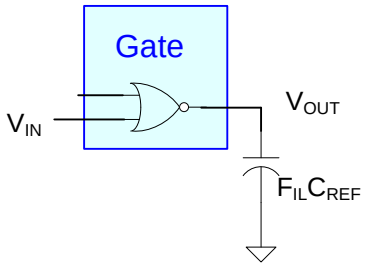
f_k = “effort delay” of stage k

g_k=logical effort

h_k=electrical effort

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate

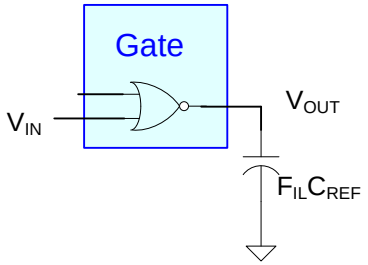


Propagation Delay in “Logic Effort” approach

$$t_{PROP} = \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

Logic Effort (g) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort (h) is the ratio of the gate load capacitance to the input capacitance of a gate



$$g_k = \frac{C_{IN_k}}{C_{REF} \bullet OD_k} \qquad h_k = \frac{C_{REF} \bullet FI_{k+1}}{C_{IN_k}}$$

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

$$g_k = \frac{C_{IN_k}}{C_{REF} \cdot OD_k} \qquad h_k = \frac{C_{REF} \bullet F_{I(k+1)}}{C_{IN_k}}$$

$$f_k = \left(\frac{C_{IN_k}}{C_{REF} \cdot OD_k} \right) \left(\frac{C_{REF} \cdot F_{I(k+1)}}{C_{IN_k}} \right)$$

$$f_k = \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Note with the exception of the t_{REF} scaling factor, this expression is identical to what we have derived previously**
- **Probably more tedious to use the “Logical Effort” approach**
- **Extensions to asymmetric overdrive factors may not be trivial**
- **Extensions to include parasitics may be tedious as well**
- **Logical Effort is widely used throughout the industry**

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  - **done**
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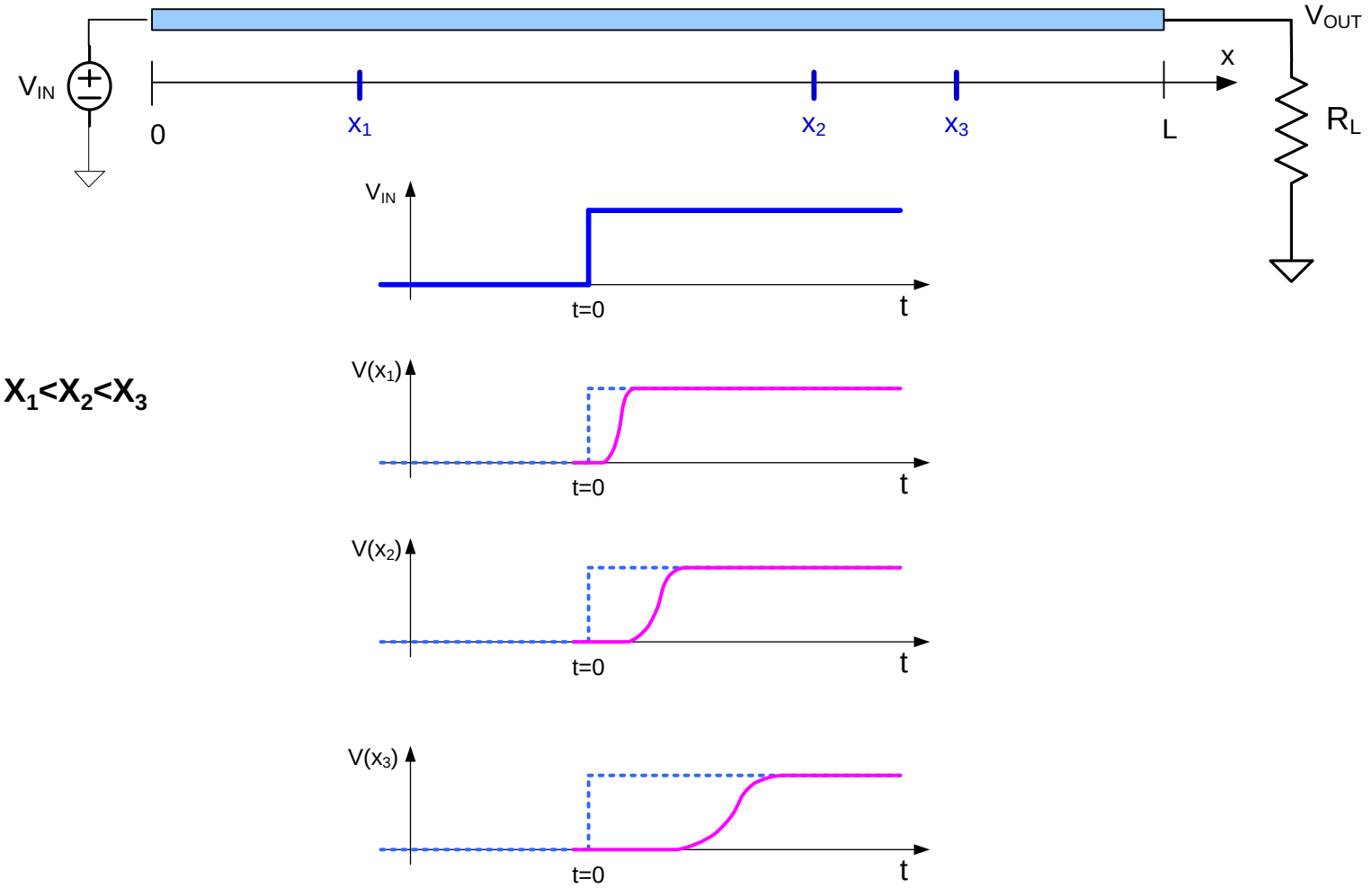
Elmore Delay Calculations

- **Interconnects have a distributed resistance and a distributed capacitance**
  - **Often modeled as resistance/unit length and capacitance per unit length**
- **These delay the propagation of the signal**
- **Effectively a transmission line**
  - **analysis is really complicated**
- **Can have much more complicated geometries**

Elmore Delay Calculations

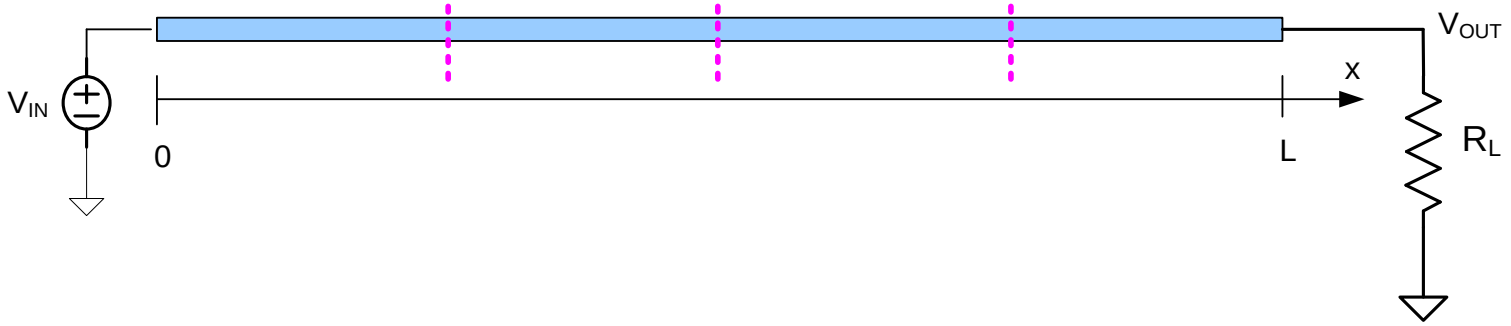
Can have much more complicated geometries

Elmore Delay Calculations

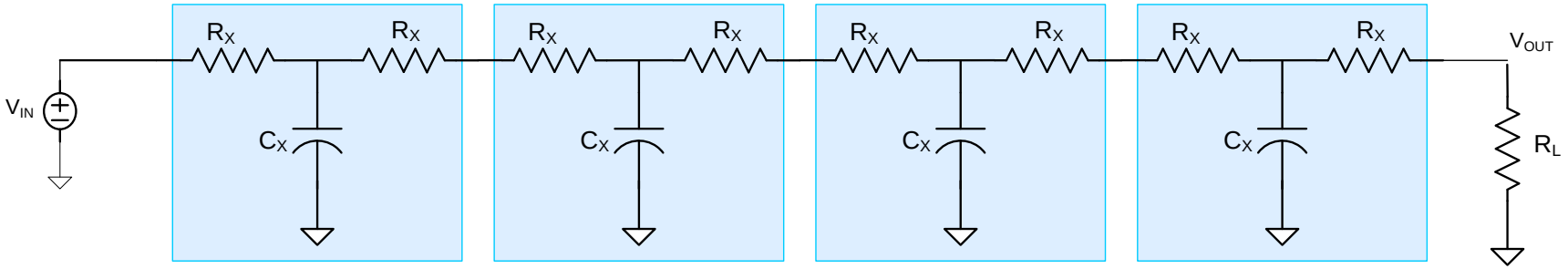


For $X_1<X_2<X_3$

Elmore Delay Calculations



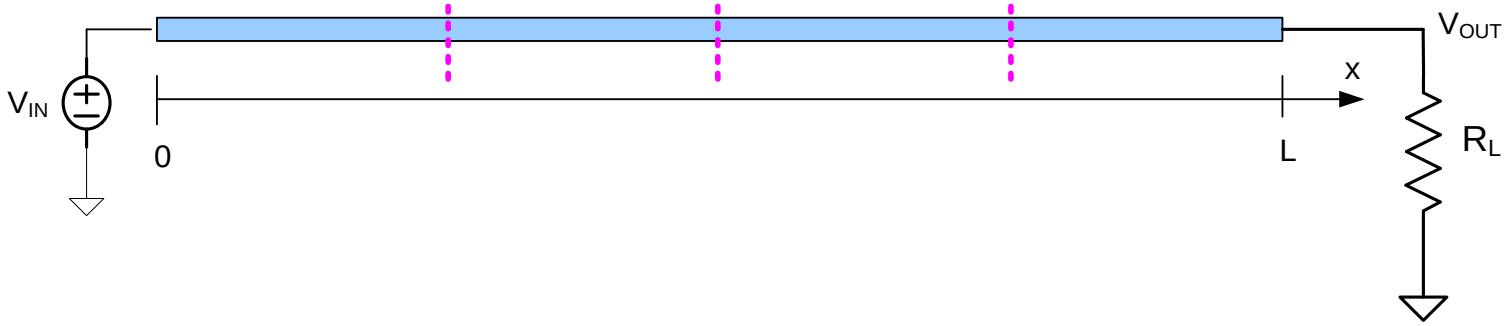
A lumped element model of transmission line



Even this lumped model is 4-th order and a closed-form solution is very tedious

Need a quick (and reasonably good) approximation to the delay of a delay line

Elmore Delay Calculations



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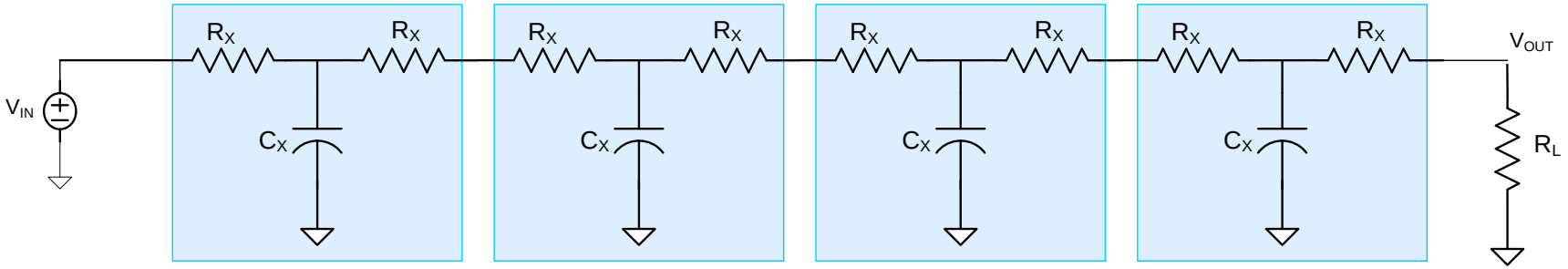

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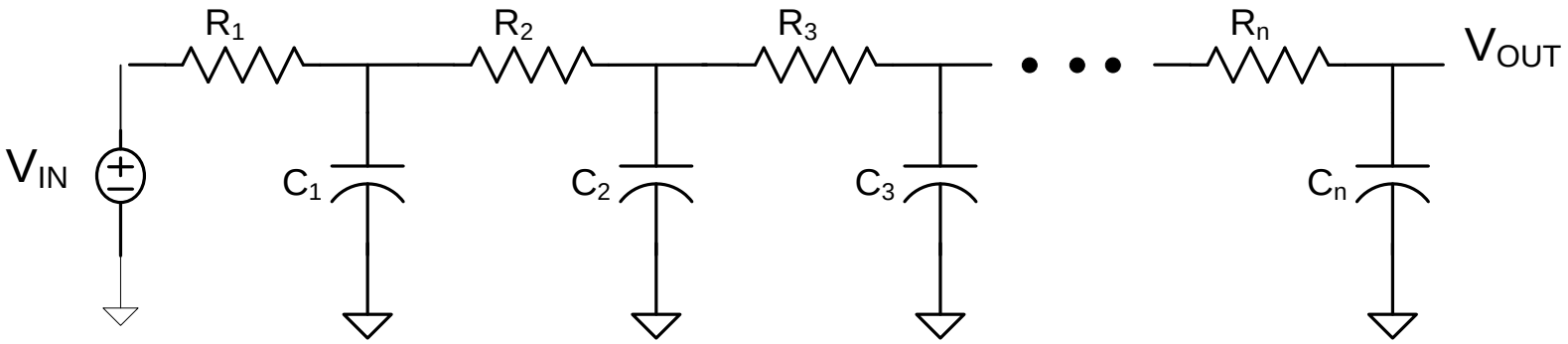
Elmore Delay Calculations



Elmore delay: $t_{PD} = \sum_{i=1}^{n} \left(C_i \sum_{j=1}^{i} R_j \right)$

- **It can be shown that this is a reasonably good approximation to the actual delay**
- **Numbering is critical (resistors and capacitors numbered from input to output)**
- **As stated, only applies to this specific structure**

Elmore Delay Calculations

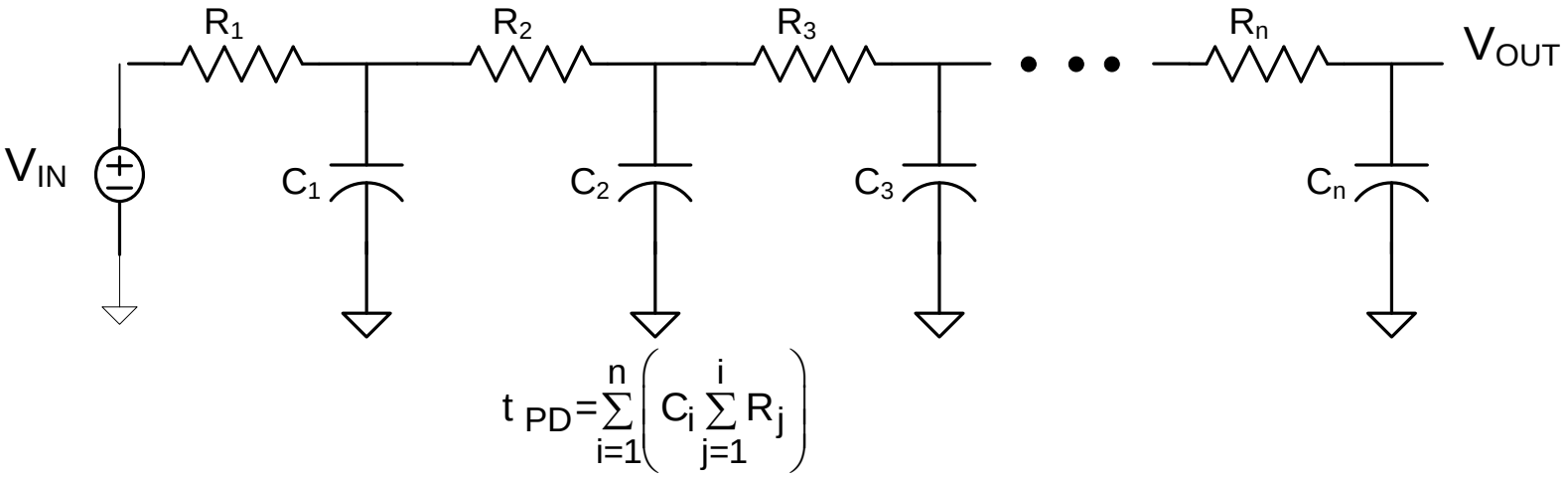
Elmore delay: $t_{PD} = \sum_{i=1}^{n} \left(C_i \sum_{j=1}^{i} R_j \right)$

- **Note error in text on Page 161 of first edition of WH**

$$t_{pd} = \sum_{i} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j$$

- **Not detailed definition on Page 150 of second edition of WH**

Elmore Delay Calculations



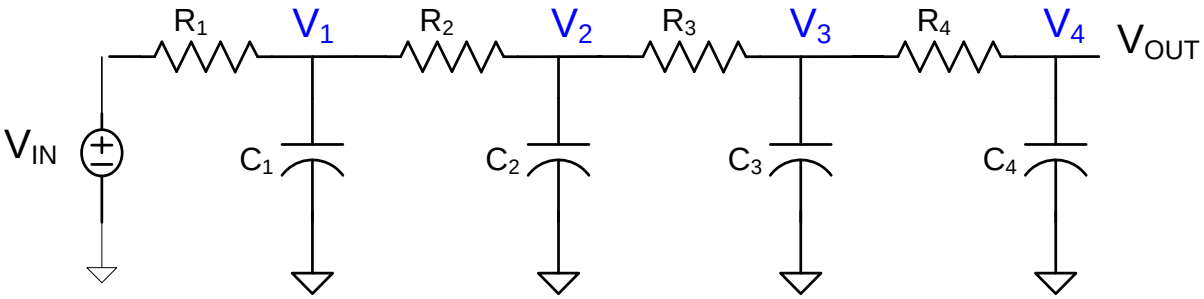
From Wikipedia:

Elmore delay[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

[1] W.C. Elmore. *The Transient Analysis of Damped Linear Networks with Particular Regard to Wideband Amplifiers*. J. Applied Physics, vol. 19(1), 1948.

Elmore Delay Calculations

Example:



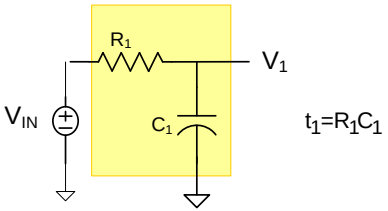
Elmore delay:

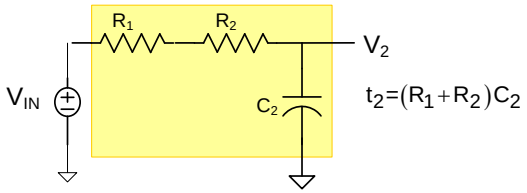
$$t_{PD} = \sum_{i=1}^{4} \left(C_i \sum_{j=1}^{i} R_j \right)$$

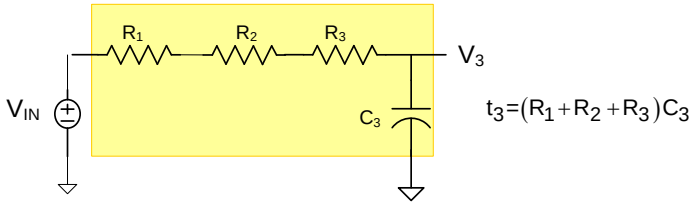
$$t_{PD} = \sum_{i=1}^{4} (t_i)$$

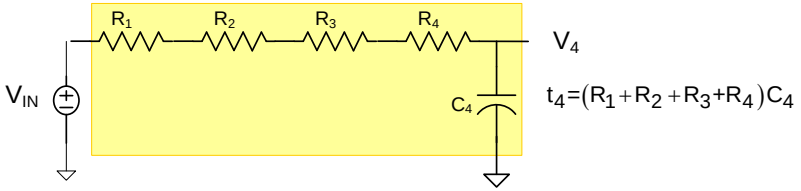
where

$$t_i = C_i \sum_{j=1}^{i} R_j \qquad j = 1,2,3,4$$









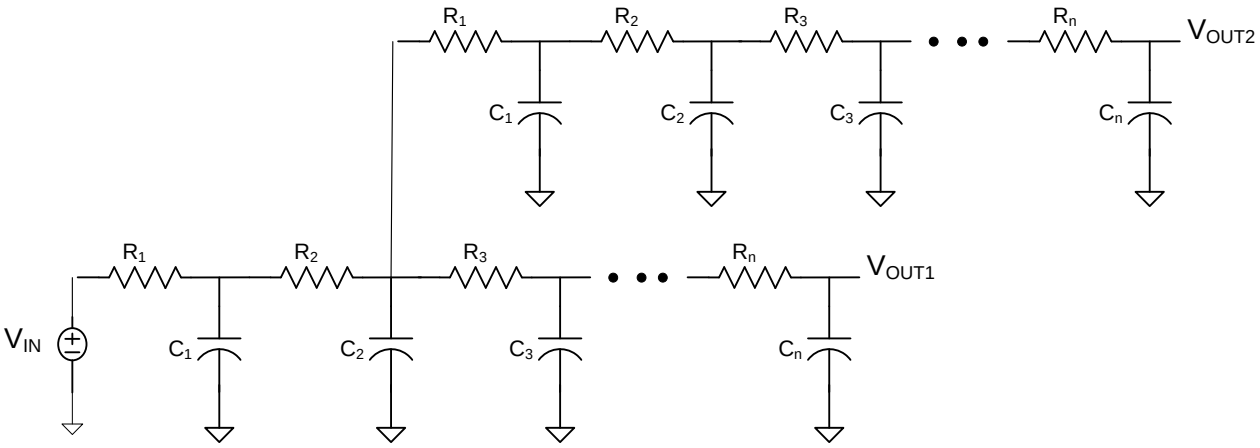
What is really happening?

- **Creating 4 first-order circuits**
- **Delay to V_1, V_2, V_3 and V_4 calculated separately by considering capacitors one at a time and assuming others are 0**

Elmore Delay Calculations

Extensions:

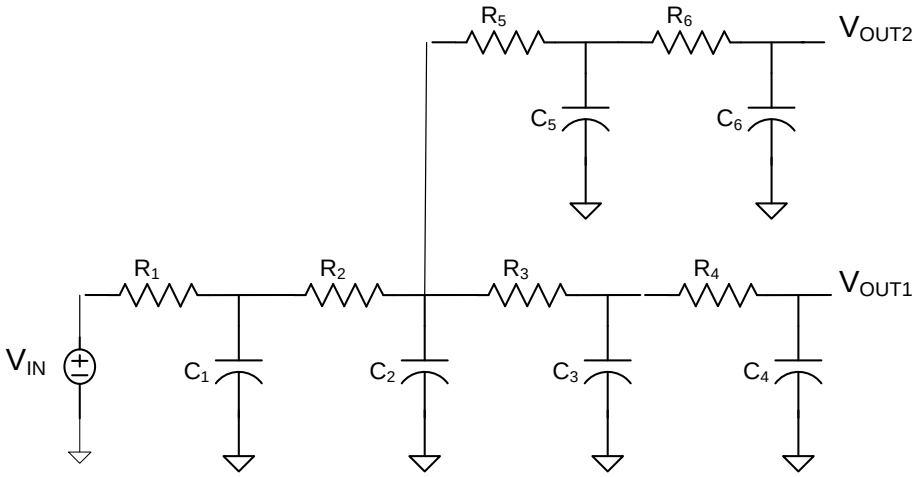
Lumped Network Model:



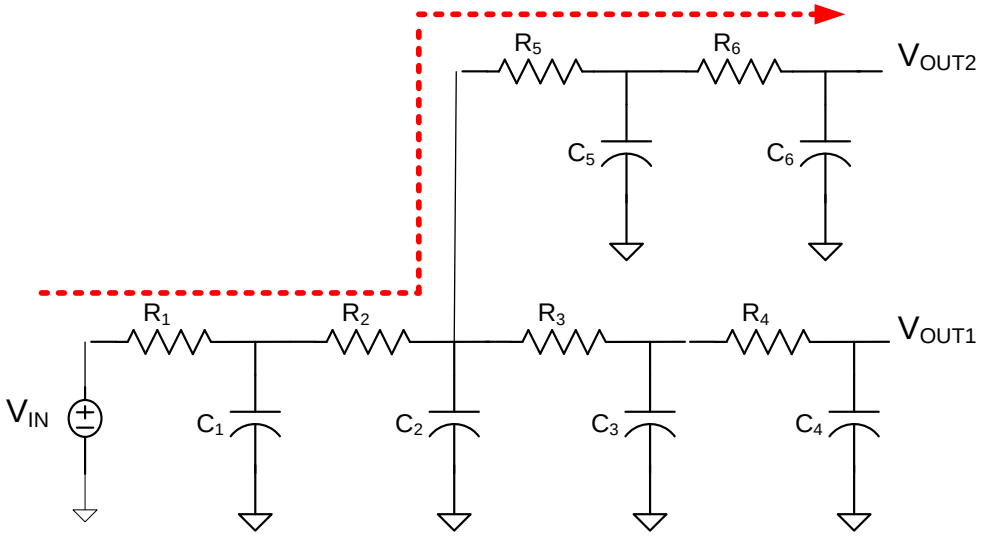
Elmore Delay Calculations

Extensions:

1. **Create a lumped element model**



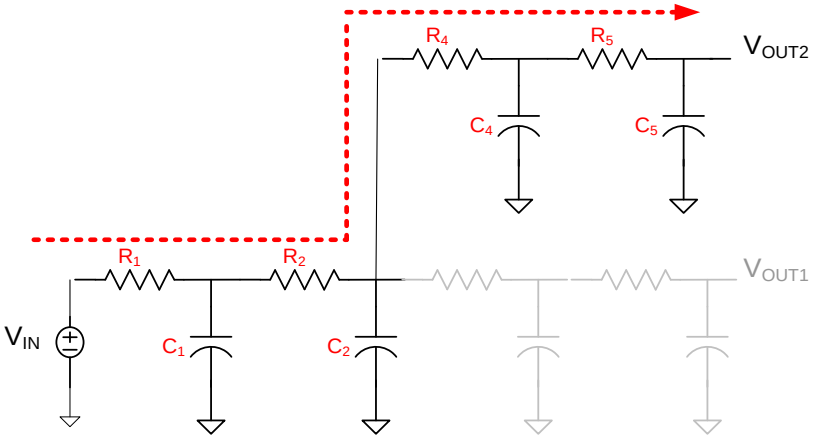
2. **Identify te a path from input to output**



Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elem



4. Use Elmore Delay equation for elements on this RC network

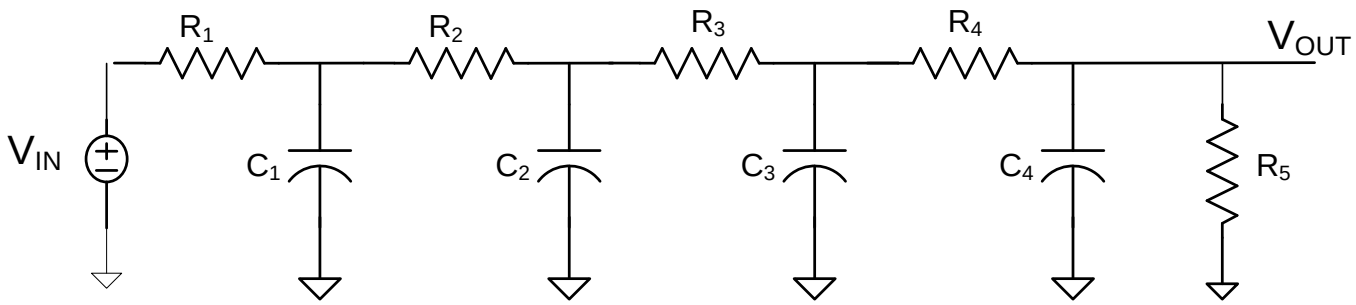
$$t_{PD} = \sum_{i=1}^{4} \left(C_i \sum_{j=1}^{i} R_j \right)$$

Elmore Delay Calculations

How is a resistive load handled?

Elmore Delay Calculations

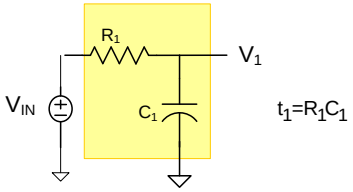
Example with resistive load:

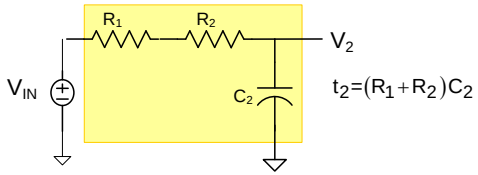


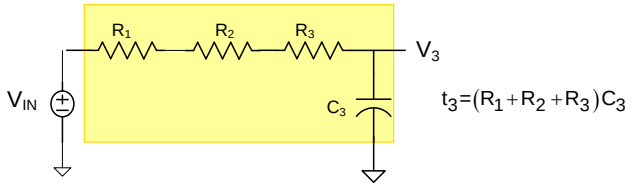
Elmore delay:

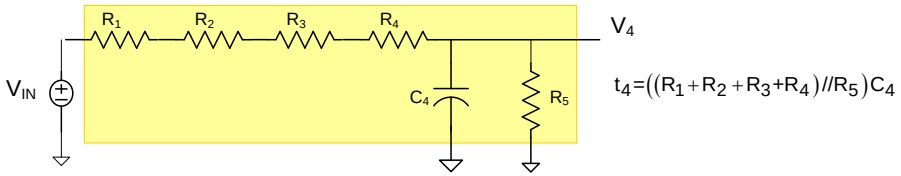
$$t_{PD} = \sum_{i=1}^{4} \left(C_i \sum_{j=1}^{i} R_j \right)$$

where









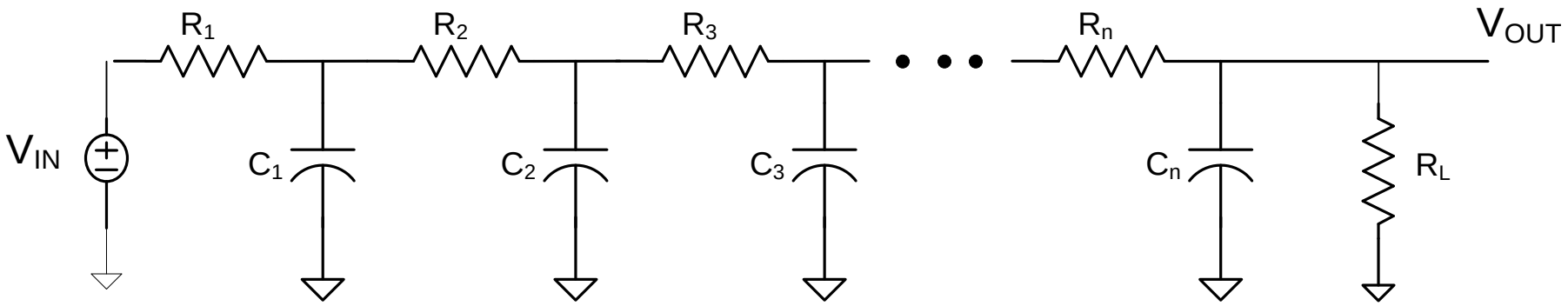
$$t_{PD} = \sum_{i=1}^{4} (t_i)$$

$$t_i = C_i \sum_{j=1}^{i} R_j \qquad j = 1,2,3$$

$$t_4 = C_4 \left(\left[\sum_{j=1}^{4} R_j \right] // R_5 \right)$$

Elmore Delay Calculations

With resistive load:

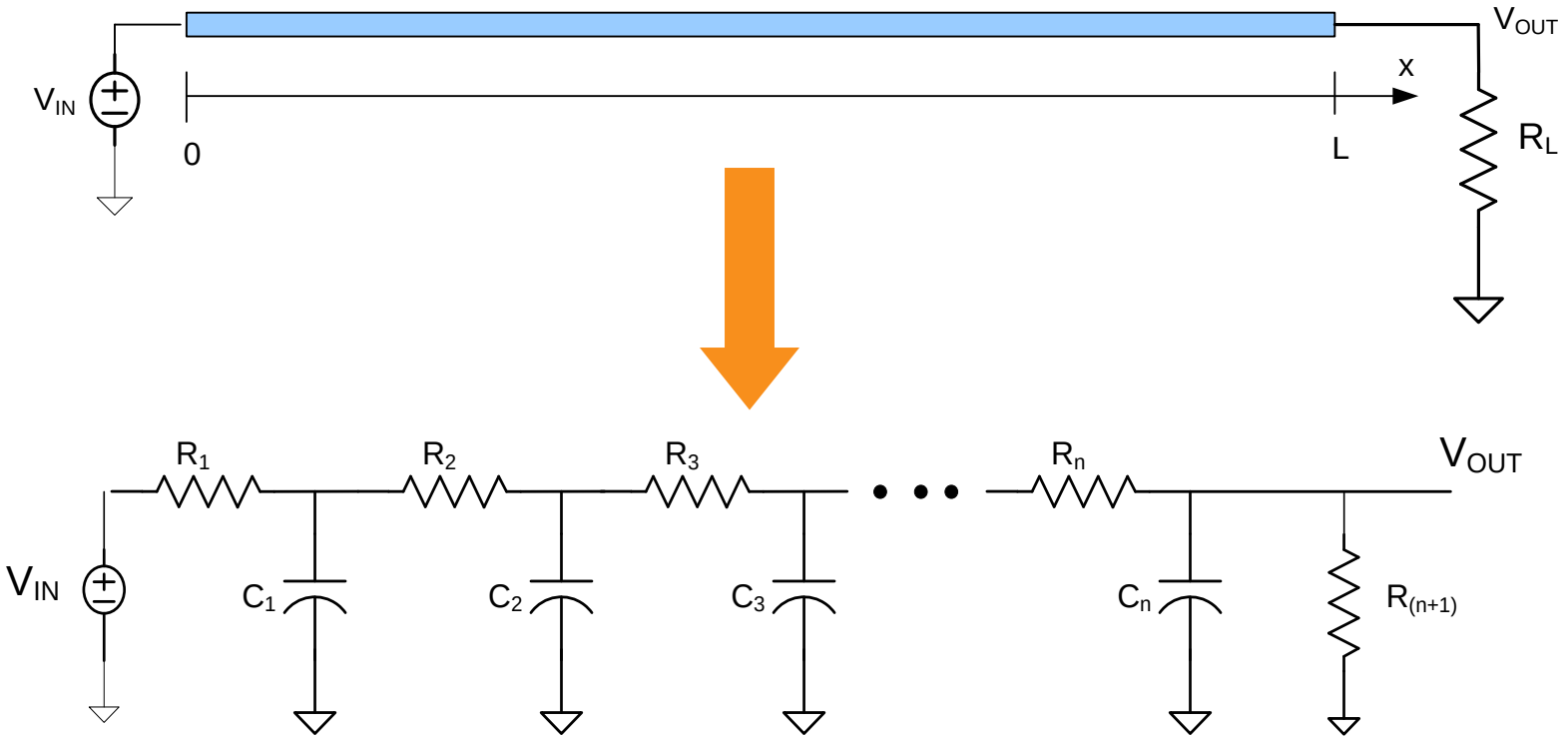


Simple Elmore delay:

$$t_{PD} = \sum_{i=1}^{n-1} \left(C_i \sum_{j=1}^{i} R_j \right) + C_n \left(\left(\sum_{j=1}^{n} R_j \right) // R_L \right)$$

Actually, R_L affects all of the delays and a modestly better but modestly more complicated delay model is often used

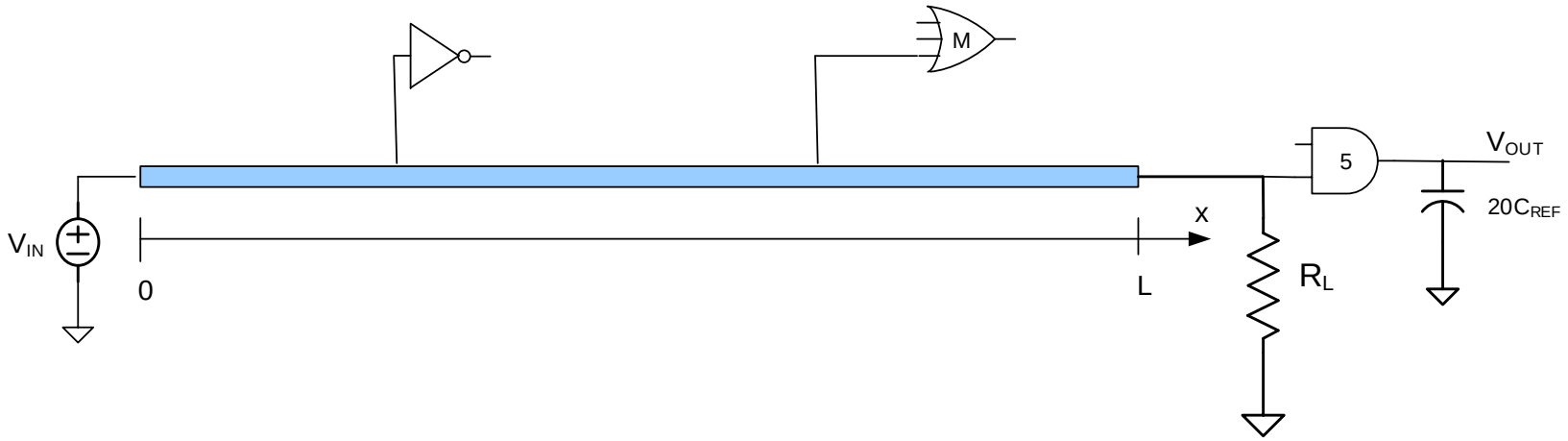
Elmore Delay Calculations



How are the number of stages chosen?

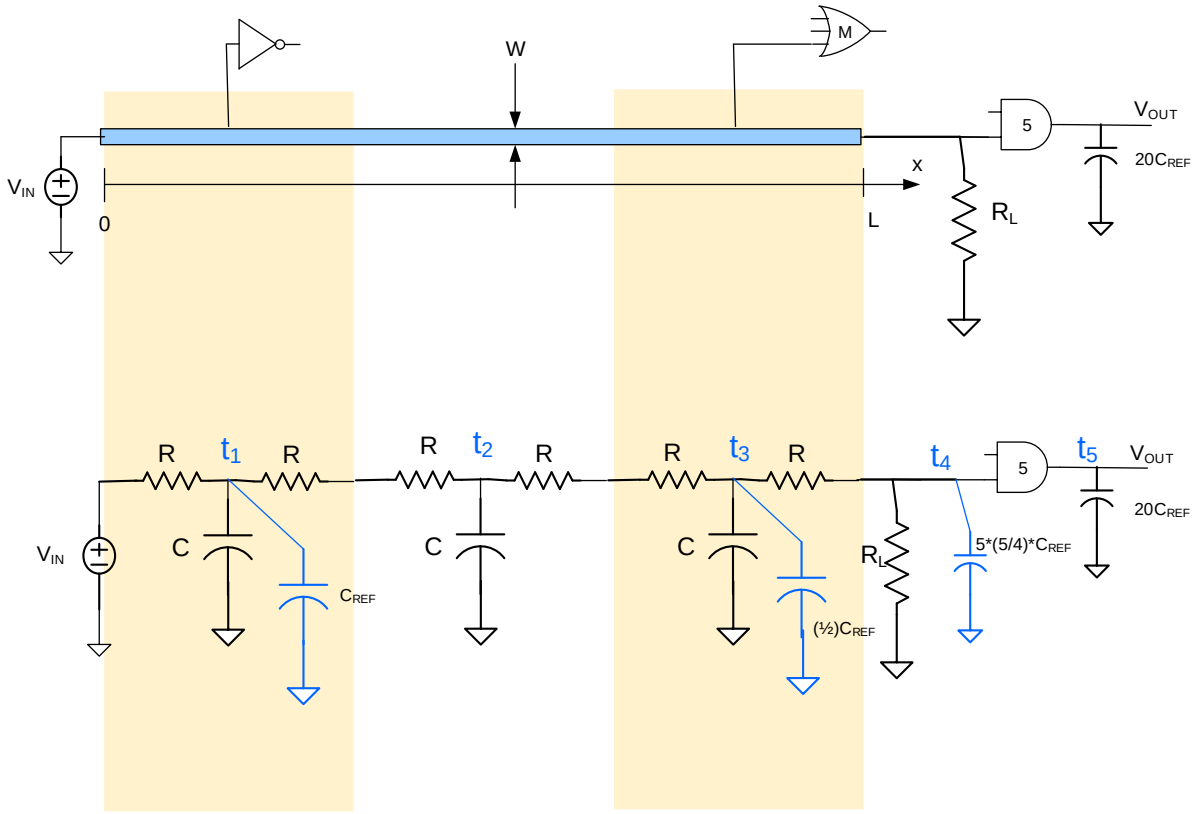
- **For hand analysis, keep number of stages small (maybe 3 or 4 for simple delay line) if possible**
- **If "faithfulness" is important, should keep the number of stages per unit length constant**

Elmore Delay Calculations



?

Elmore Delay Calculations



$$R = \frac{1}{6} R_{\square} \frac{L}{W}$$

$$C = \frac{1}{3} C_D$$

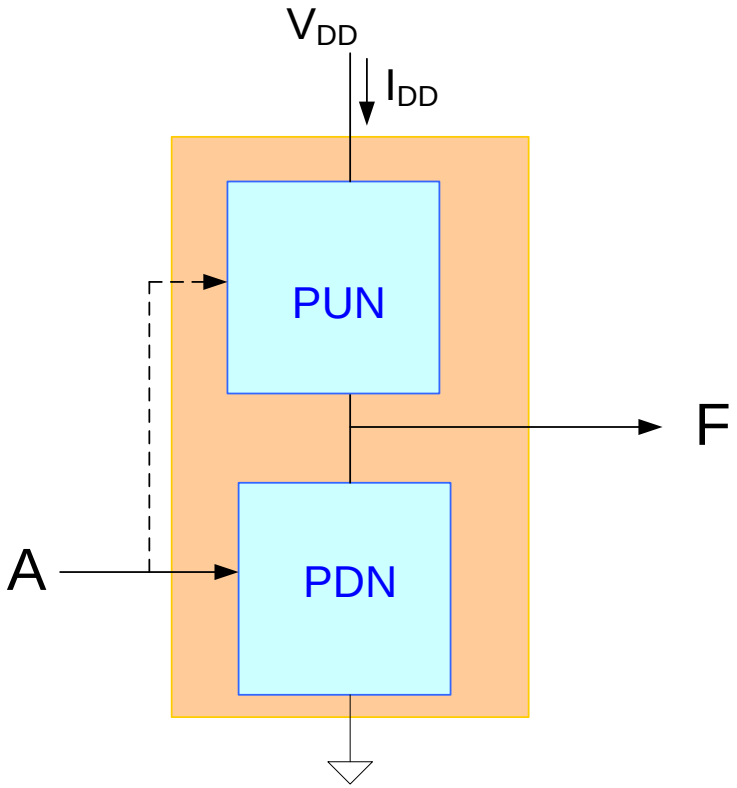
$$t_1 = R\left(C + C_{REF}\right) \qquad t_2 = 3RC \qquad t_3 = 5R\left(C + \frac{1}{2}C_{REF}\right) \qquad t_4 = \left[6R \,/\!/\!/\, R_L\right]\frac{25}{4}C_{REF} \qquad t_5 = t_{REF}\frac{20}{5}$$

$$t_{PROP} = \sum_{i=1}^{5} t_i$$

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - **done**
  - **partial**
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

Power Dissipation in Logic Circuits



Assume current periodic with period T_{CL}

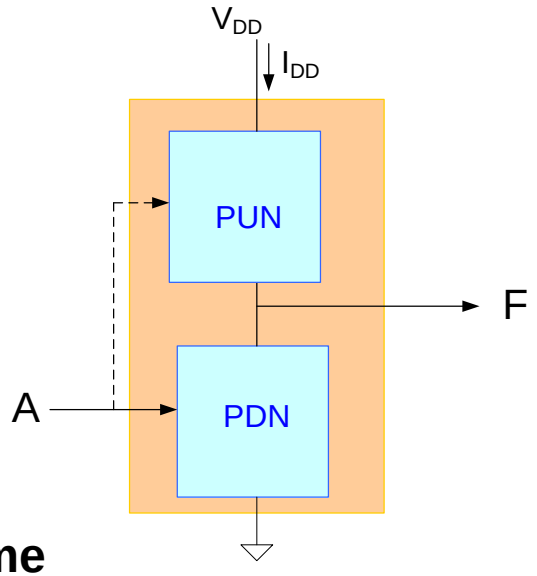
$$P_{AVG,T} = \frac{1}{T_{CL}} \int_{t_1}^{t_1+T_{CL}} V_{DD} I_{DD}(t)\,dt$$

Power Dissipation in Logic Circuits

Types of Power Dissipation

- **Static**
- **Pipe**
- **Dynamic**
- **Leakage**
  - **Gate**
  - **Diffusion**
  - **Drain**

Static Power Dissipation



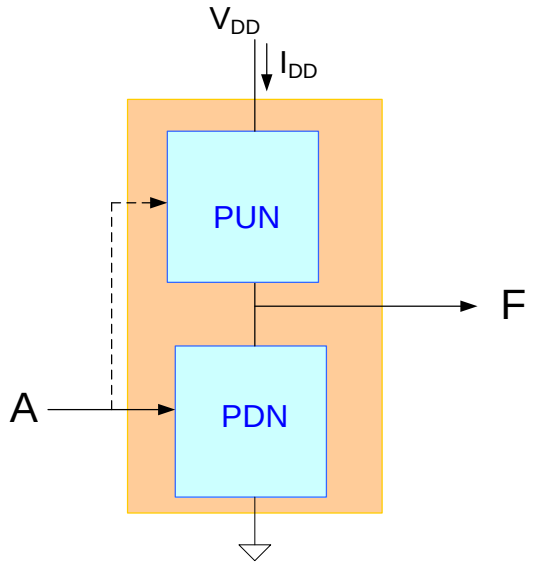
If Boolean output averages H and L 50% of the time

$$P_{STAT,AVG} = \frac{P_H + P_L}{2}$$

$$P_{STAT,AVG} = \frac{V_{DD}(I_{DDH} + I_{DDL})}{2}$$

- **Generally decreases with V_{DD}**
- **I_{DDH}=I_{DDL}=0 for static CMOS gates so P_{STAT}=0**
- **A major source of power dissipation in ratio logic circuits and the major reason CMOS is so widely used**

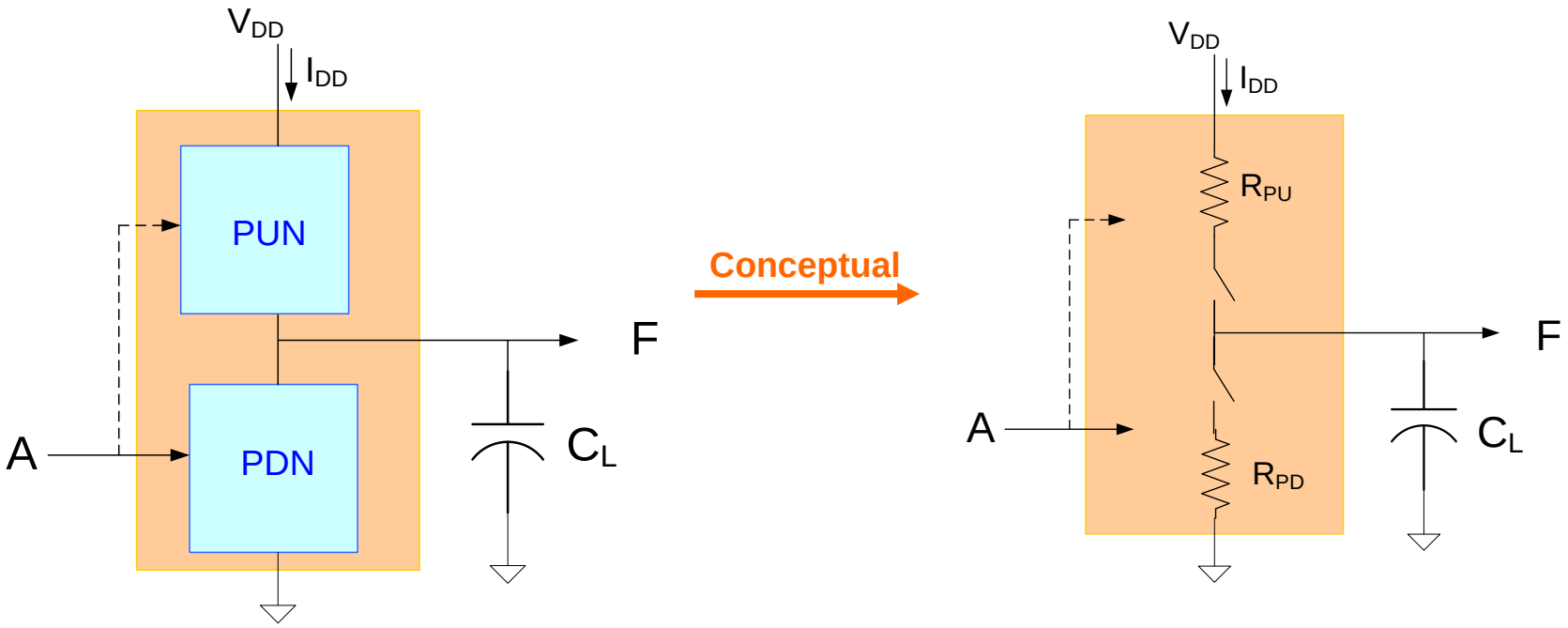
Pipe Power Dissipation



Due to conduction of both PUN and PDN during transitions

- **Can be made small if transitions are fast**
- **Usually negligible in Static CMOS circuits**

Dynamic Power Dissipation



Due to charging and discharging C_L on logic transitions

C_L dissipates no power but PUN and PDN dissipate power during charge and discharge of C_L

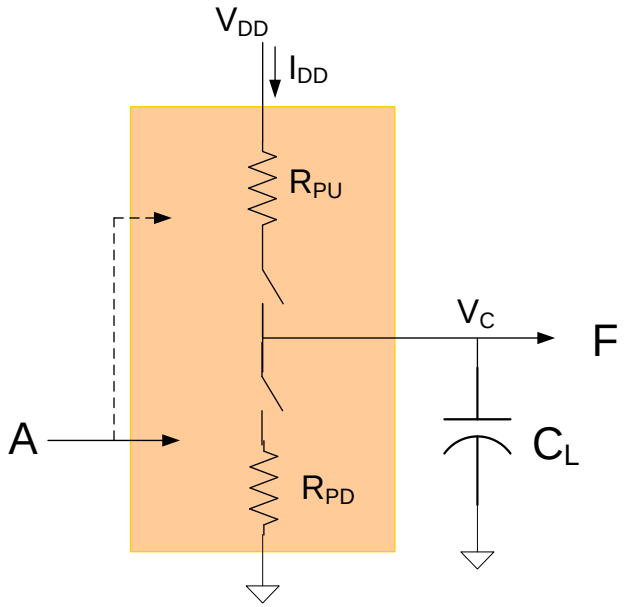
C_L includes all gate input capacitances of loads and interconnect capacita

Dynamic Power Dissipation

Energy supplied by V_{DD} when C_L charges

$$E = \int_{t_1}^{\infty} V_{DD} I_{DD}(t)\,dt$$

$$I_{DD} = C_L \frac{dV_C}{dt}$$



$$E = \int_{t_1}^{\infty} V_{DD} C_L \frac{dV_C}{dt}\,dt$$

$$E = \int_{V_C=0}^{V_{DD}} V_{DD} C_L\,dV_C = V_{DD} C_L \int_{V_C=0}^{V_{DD}} dV_C = V_{DD} C_L\, V_C\Big|_{V_C=0}^{V_{DD}} = V_{DD}^2 C_L$$

Energy stored in C_L after C_L is charged to V_{DD}:

$$E = \frac{1}{2} C_L V_{DD}^2$$

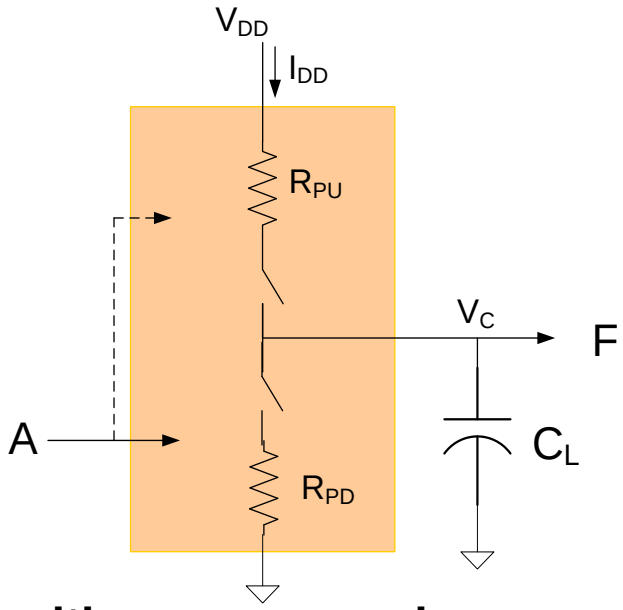
Dynamic Power Dissipation

Energy supplied by V_{DD} and dissipated in R_{PU} when C_L charges

$$E_{DIS} = \frac{1}{2} C_L V_{DD}^2$$

Energy stored on C_L after L-H transition

$$E_{STORE} = \frac{1}{2} C_L V_{DD}^2$$



Thus, energy from V_{DD} for one L-H: H-L output transition sequence is

$$E = E_{DIS} + E_{STORE} = C_L V_{DD}^2$$

When the output transitions from H to L, energy stored on C_L is dissipated in PDN

If f is the average transition rate of the output, determine P_{AVG}

End of Lecture 43