EE 330
Lecture 28

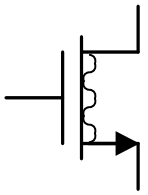
Bipolar Processes

- Device Sizes
- Parasitic Devices
  - JFET
  - Thyristors

Thyristors

- SCR – Basic operation

How does g_m vary with I_{DQ}?



$$g_m = \sqrt{\frac{2\mu C_{OX} W}{L}} \sqrt{I_{DQ}}$$

Varies with the square root of I_{DQ}

$$g_m = \frac{2I_{DQ}}{V_{GSQ} - V_T} = \frac{2I_{DQ}}{V_{EBQ}}$$

Varies linearly with I_{DQ}

$$g_m = \frac{\mu C_{OX} W}{L}\left(V_{GSQ} - V_T\right)$$

Doesn't vary with I_{DQ}

How does g_m vary with I_{DQ}?

All of the above are true – but with qualification

g_m is a function of more than one variable (I_{DQ}) and how it varies depends upon how the remaining variables are constrained

Topical Coverage Change

Will have several additional lectures on amplifier structures but will temporarily suspend discussion of amplifiers to consider Thyristors

This is being done to get ready for the Thyristor laboratory experiments

Outline

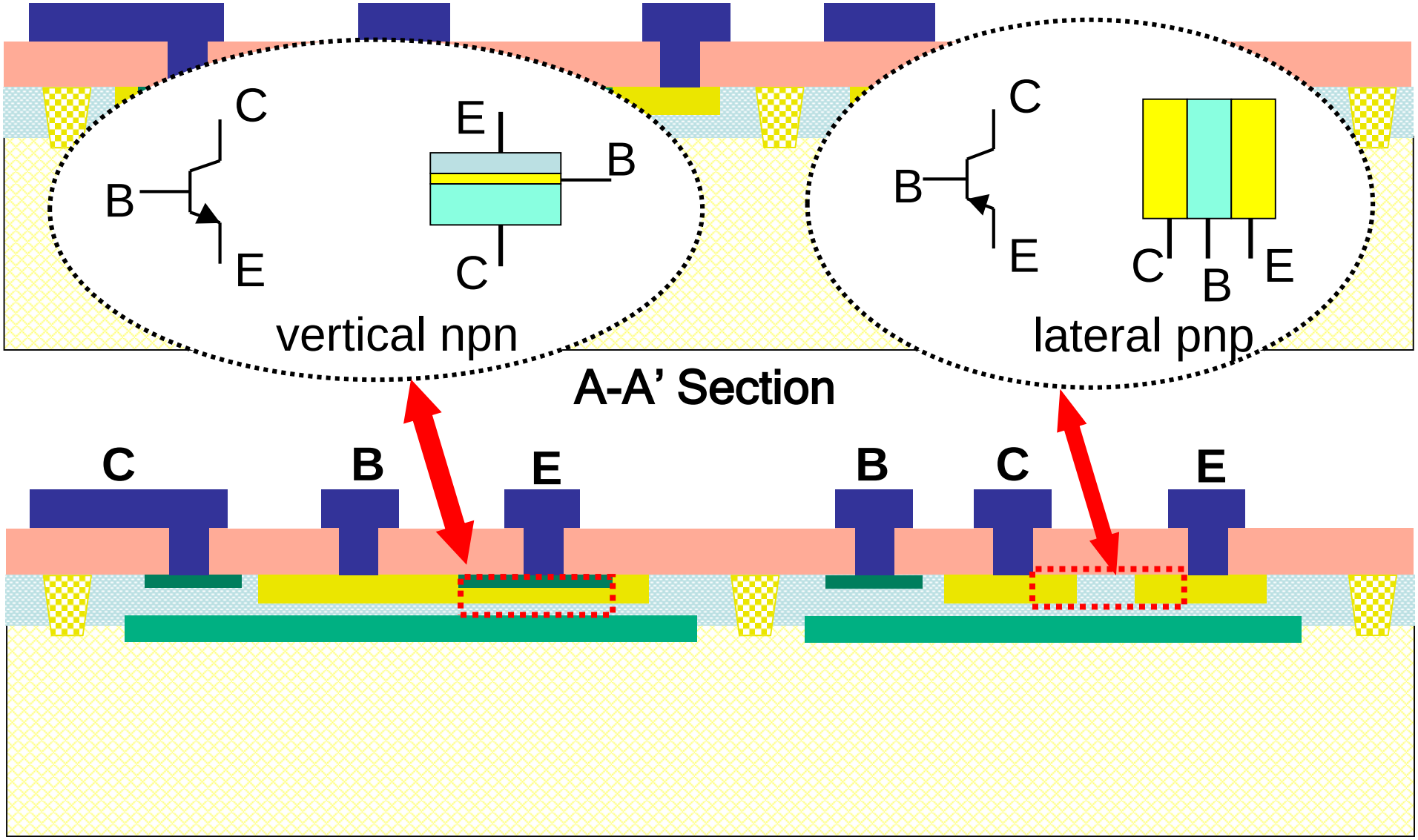
Bipolar Processes

- Comparison of MOS and Bipolar Process
- Parasitic Devices in CMOS Processes
- JFET

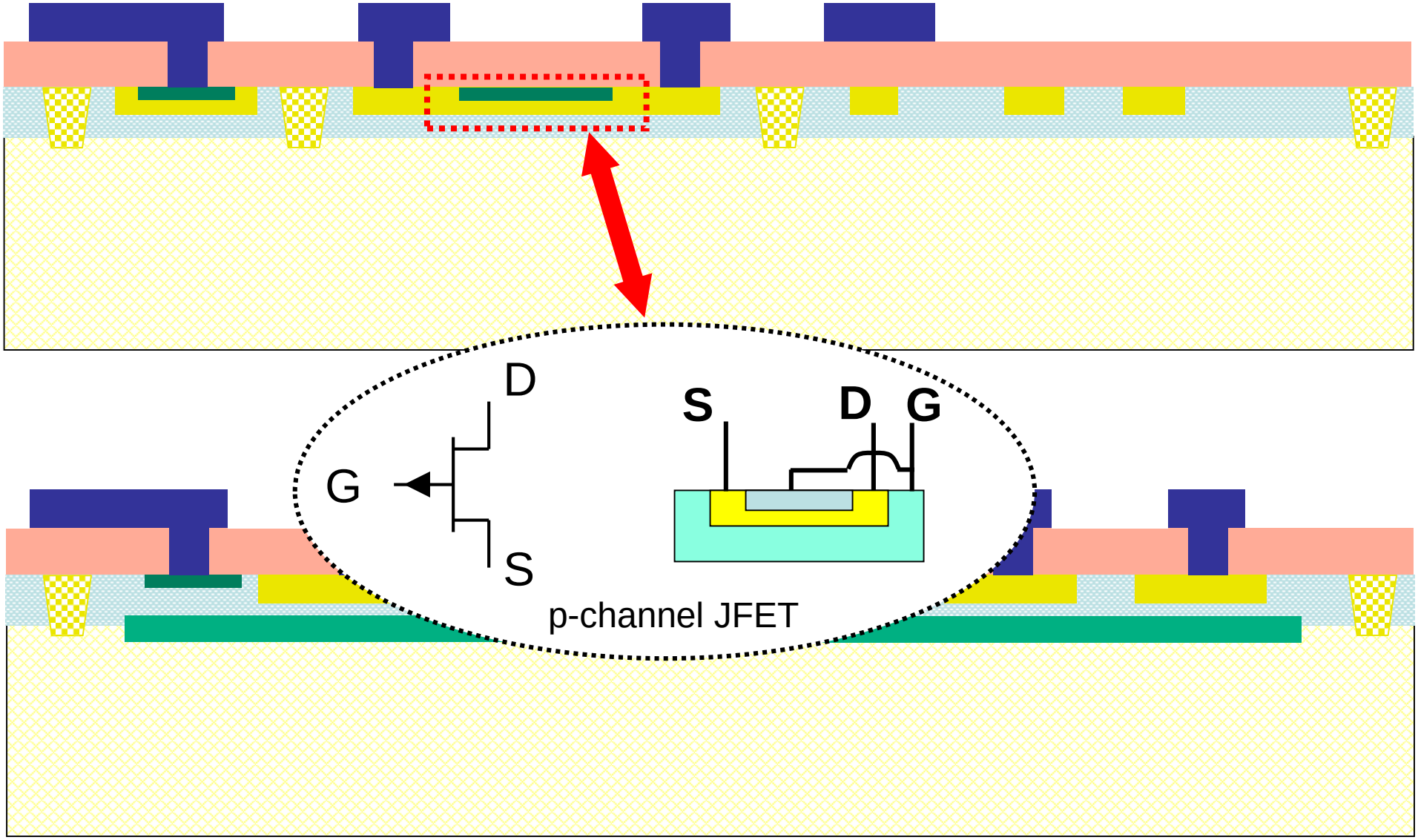
Special Bipolar Processes

- Thyristors
  - SCR
  - TRIAC

Review from a Previous Lecture

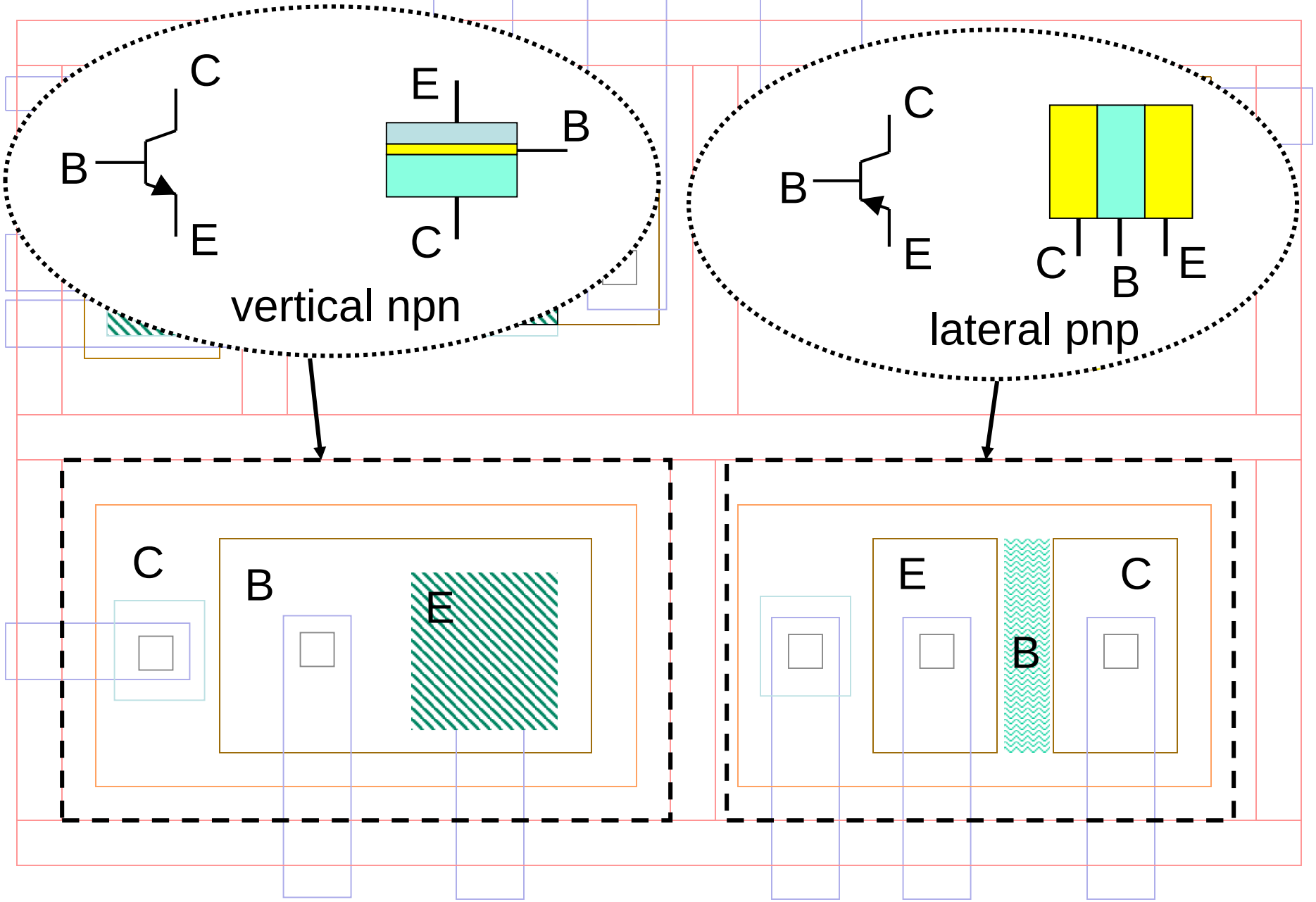


Review from a Previous Lecture

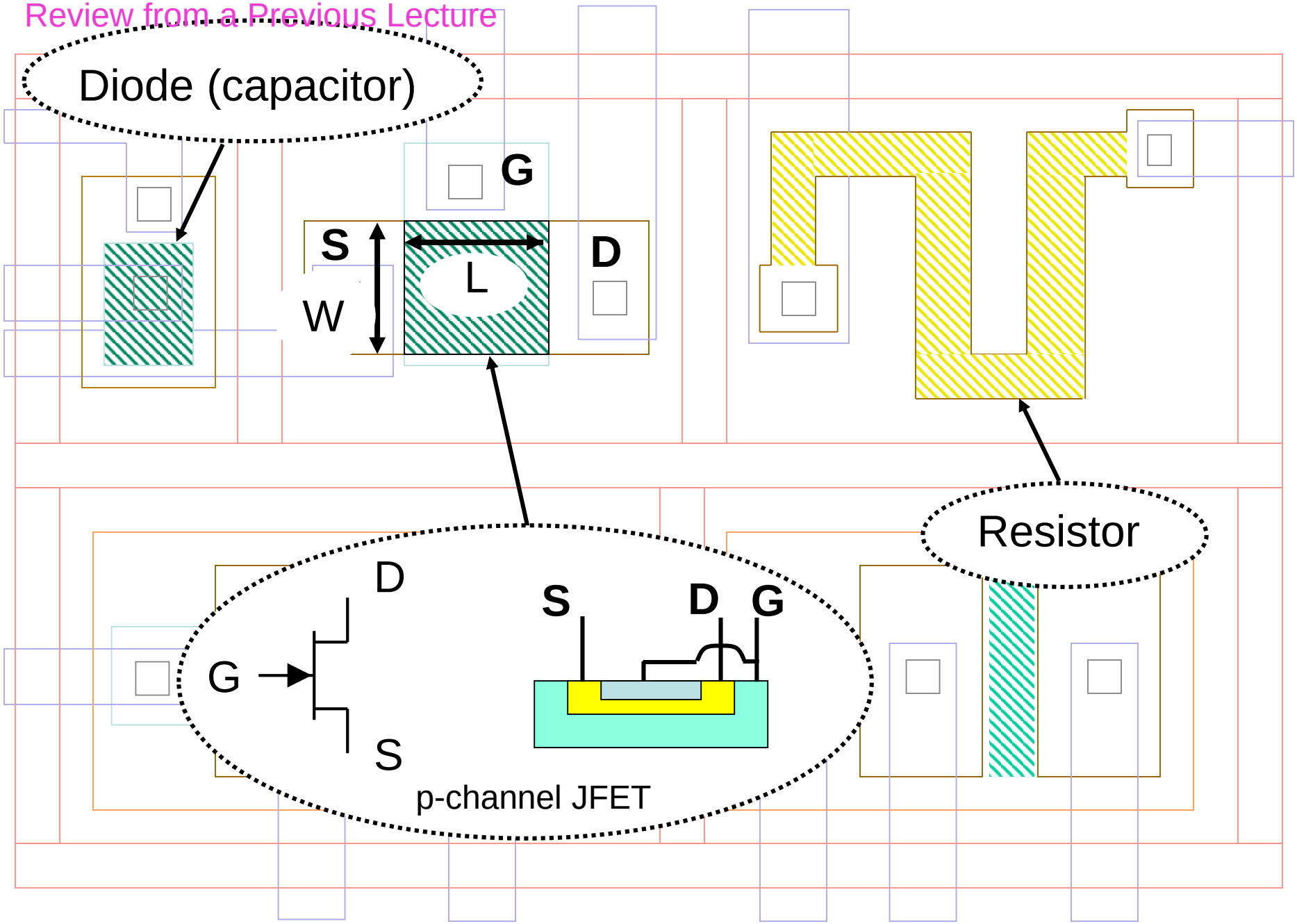


B-B' Section

Review from a Previous Lecture



Review from a Previous Lecture



Will consider next the JFET but first some additional information about MOS Devices

Enhancement and Depletion MOS Devices

- Enhancement Mode n-channel devices

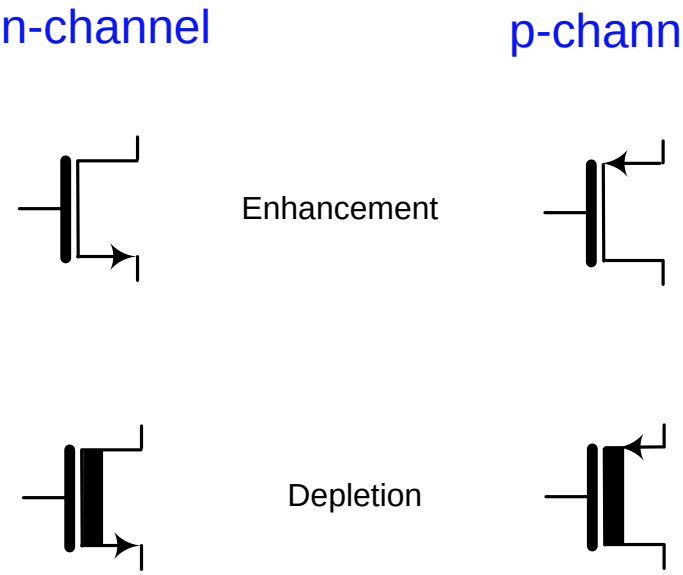
  $V_T > 0$
- Enhancement Mode p-channel devices

  $V_T < 0$
- Depletion Mode n-channel devices

  $V_T < 0$
- Depletion Mode p-channel devices

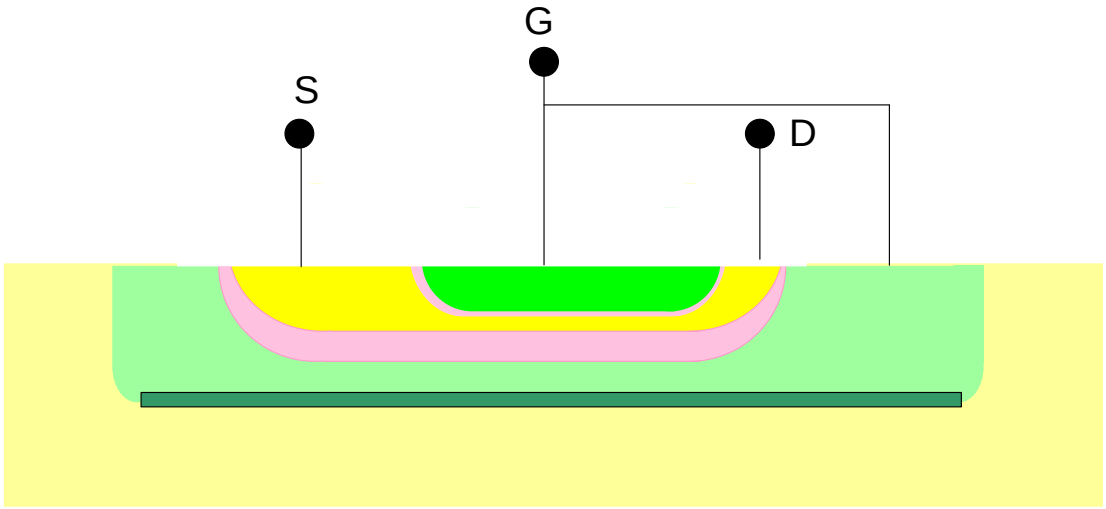
  $V_T > 0$

Enhancement and Depletion MOS Devices

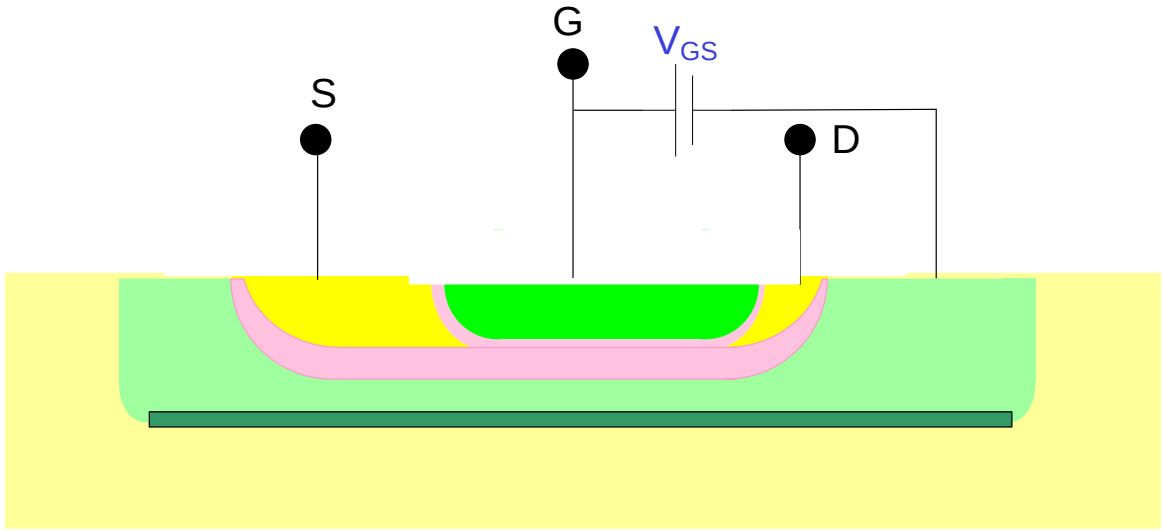


- Depletion mode devices require only one additional mask step
- Older n-mos and p-mos processes usually had a depletion device and an enhancement device
- Depletion devices usually not available in CMOS because applications usually do not justify the small increasing costs in processing
- The threshold voltage of either n-channel or p-channel devices is adjusted to a desired value by doing a channel implant before gate oxide is applied

The JFET

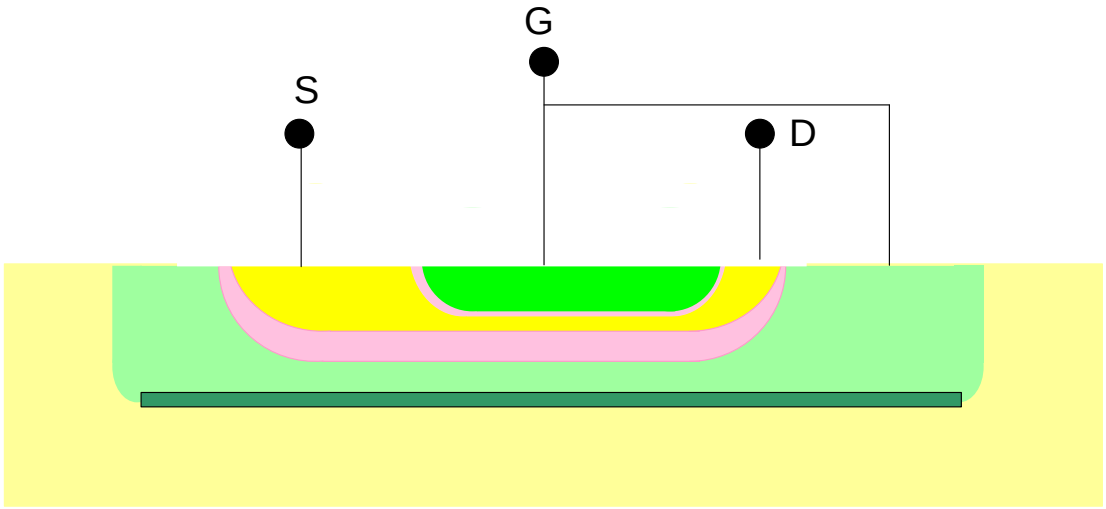


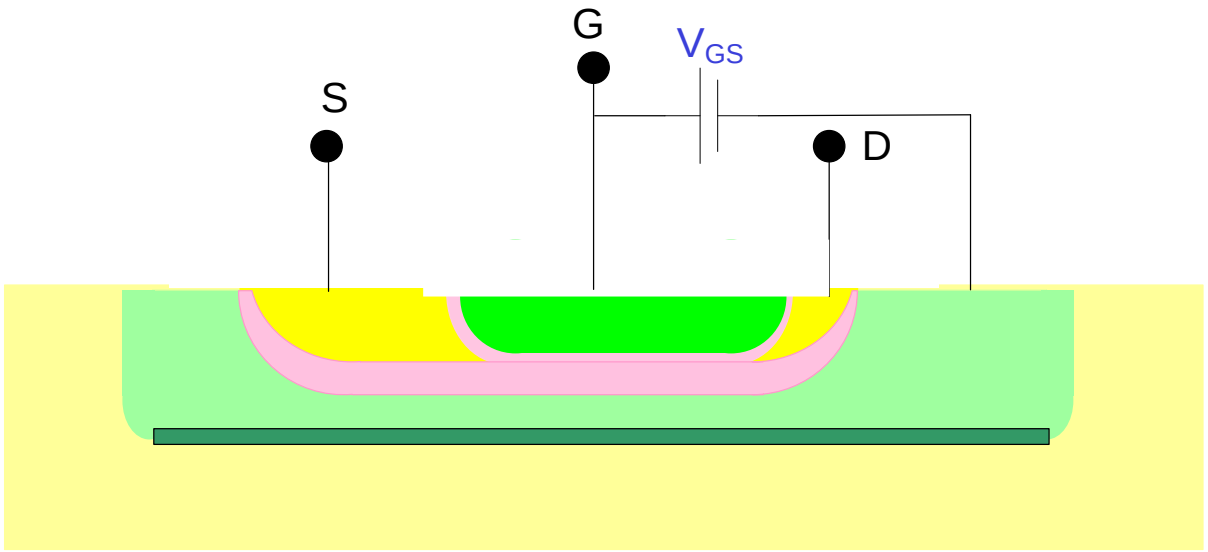
With V_{GS}=0, channel exists under gate between D and S



Under sufficiently large reverse bias (depletion region widens and channel disappears - “pinches off”)

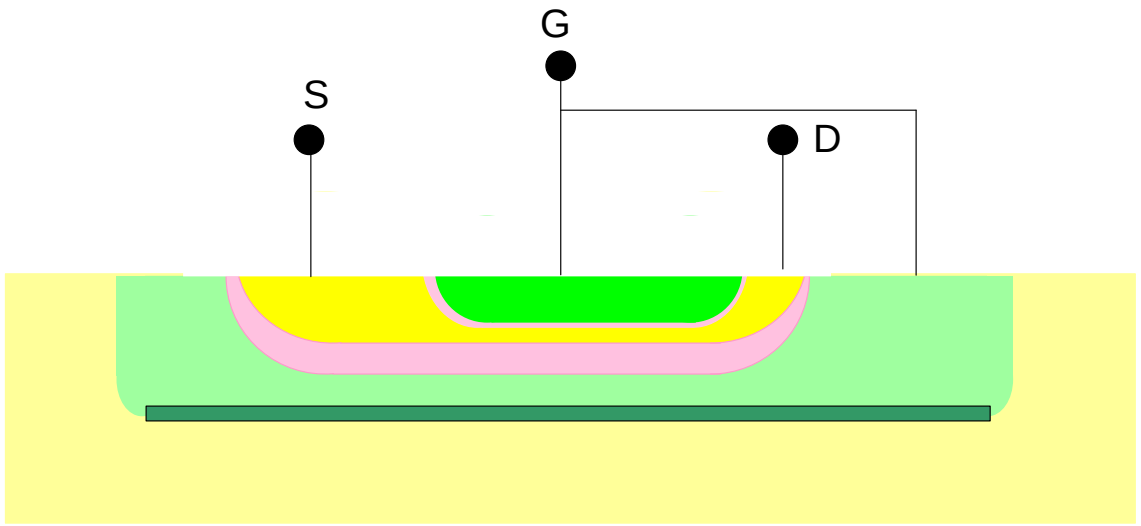
The JFET

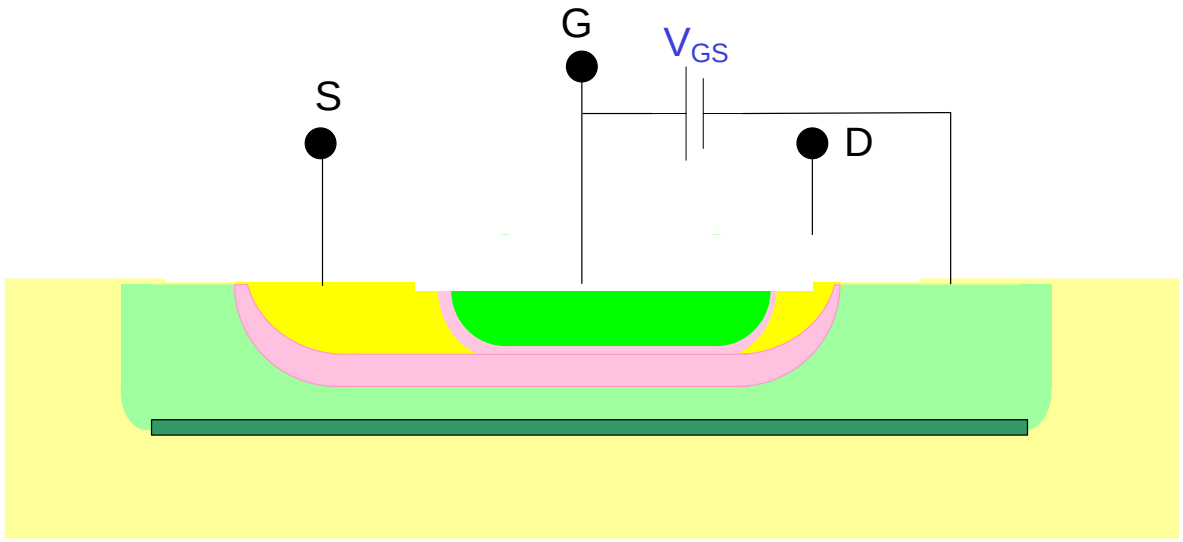




Under smaller reverse bias (depletion region widens and channel thins)

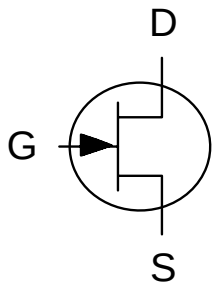
The JFET



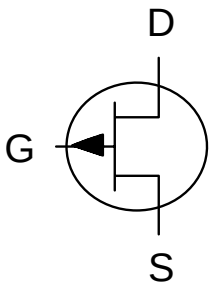


Under small reverse bias and large negative V_{DS} (channel pinches off)

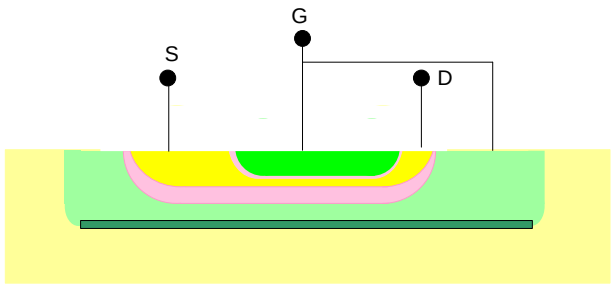
The JFET



n-channel



p-channel



p-channel JFET

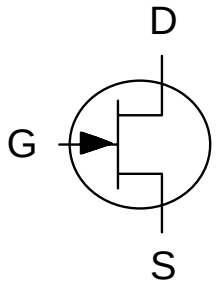
Square-law model of p-channel JFET

$$I_D = \begin{cases} 0 & V_{GS} > V_P \\ \dfrac{2I_{DSSp}}{V_P^2}\left(V_{GS}-V_P-\dfrac{V_{DS}}{2}\right)V_{DS} & -0.3 < V_{GS} < V_P \quad V_{GS}+0.3 > V_{DS} > V_{GS}-V_P \\ I_{DSSp}\left(1-\dfrac{V_{GS}}{V_P}\right)^2 & -0.3 < V_{GS} < V_P \quad V_{DS} < V_{GS}-V_P \end{cases}$$

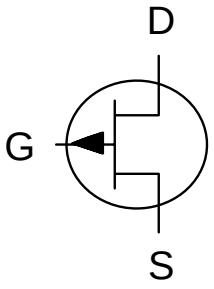
(I_{DSSp} carries negative sign)

- Functionally identical to the square-law model of MOSFET
- Parameters I_{DSS} and V_P characterize the device
- I_{DSS} proportional to W/L where W and L are width and length of n+ diff
- V_P is negative for n-channel device, positive for p-channel device thus JFET is depletion mode device
- Must not forward bias GS junction by over about 300mV or excessive base current will flow (red constraint)
- Widely used as input stage for bipolar op amps

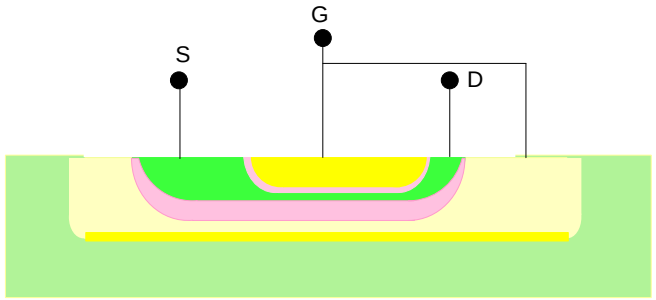
The JFET



n-channel



p-channel



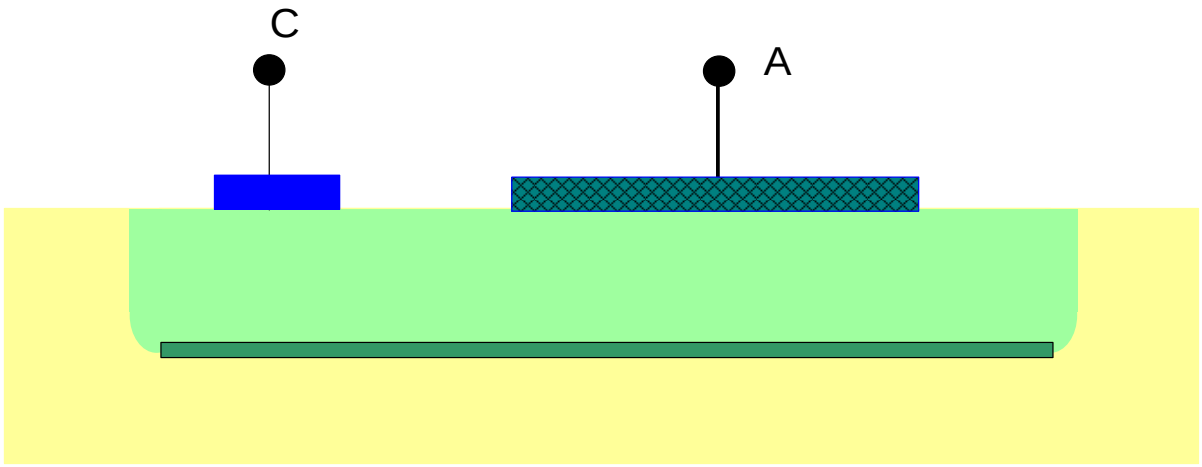
n-channel JFET
(not available in this process)

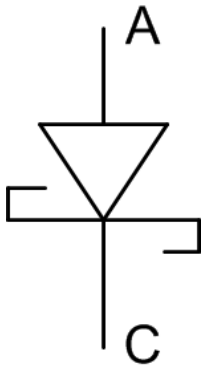
Square-law model of n-channel JFET

$$I_D = \begin{cases} 0 & V_{GS} < V_P \\ \frac{2I_{DSS}}{V_P^2}\left(V_{GS}-V_P-\frac{V_{DS}}{2}\right)V_{DS} & 0.3 > V_{GS} > V_P \quad V_{GS}-0.3 < V_{DS} < V_{GS}-V_P \\ I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 & 0.3 > V_{GS} > V_P \quad V_{DS} > V_{GS}-V_P \end{cases}$$

- Functionally identical to the square-law model of MOSFET
- Parameters I_{DSS} and V_P characterize the device
- I_{DSS} proportional to W/L where W and L are width and length of n+ diff
- V_P is negative for n-channel device, positive for p-channel device thus JFET is depletion mode device
- Must not forward bias GS junction by over about 300mV or excessive base current will flow (red constraint)
- Widely used as input stage for bipolar op amps

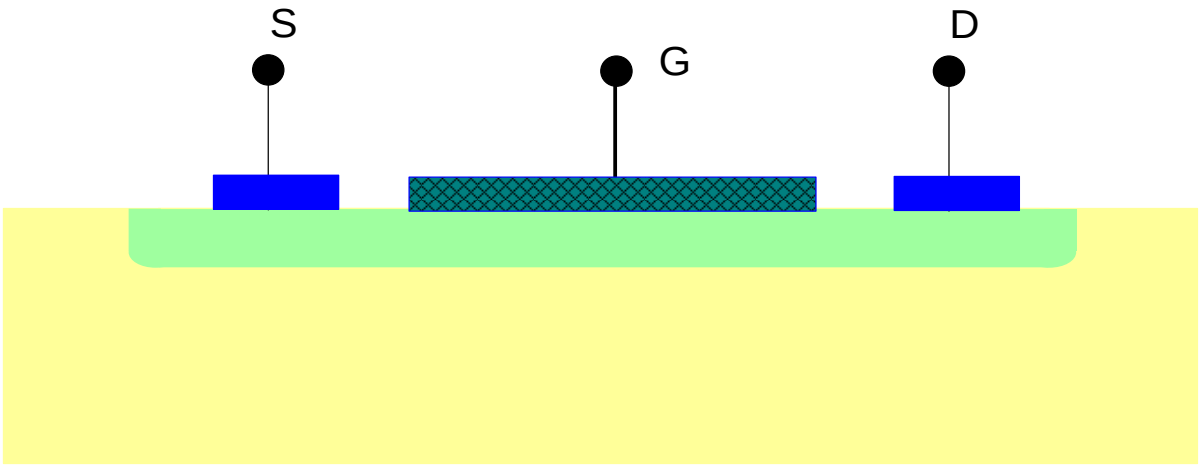
The Schottky Diode





- Metal-Semiconductor Junction
- One contact is ohmic, other is rectifying
- Not available in all processes
- Relatively inexpensive adder in some processes
- Lower cut-in voltage than pn junction diode
- High speed

The MESFET

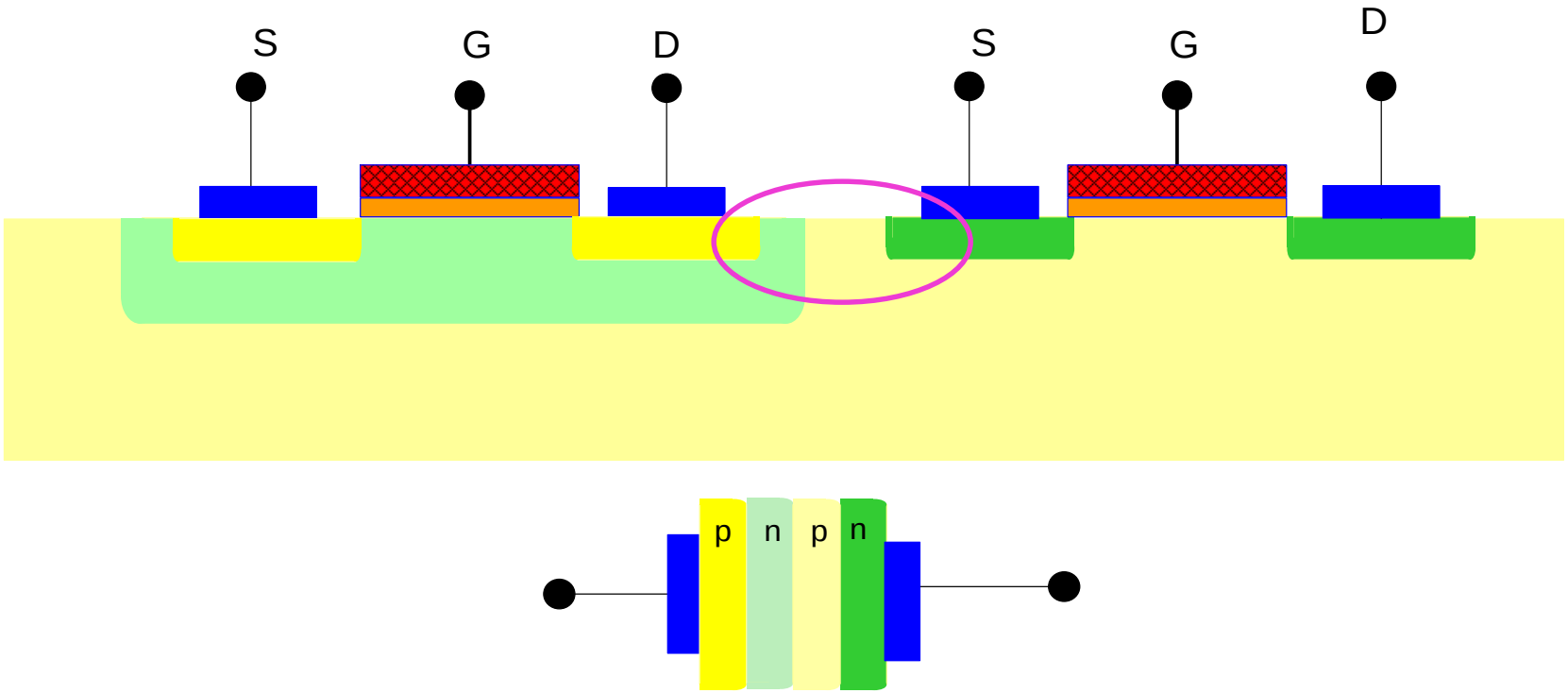


- Metal-Semiconductor Junction for Gate
- Drain and Source contacts ohmic, other is rectifying
- Usually not available in standard CMOS processes
- Must not forward bias very much
- Lower cut-in voltage than pn junction diode
- High speed

The Thyristor

A bipolar device in CMOS Processes

Consider a Bulk-CMOS Process



Have formed a lateral pnpn device !

Will spend some time studying pnpn devices

Outline

Two-Port Amplifier Models

Bipolar Processes

- Comparison of MOS and Bipolar Process
- Parasitic Devices in CMOS Processes
- JFET

Special Bipolar Processes

- Thyristors
  - SCR
  - TRIAC

Thyristors

The good and the bad!

Thyristors

The good

SCRs
Triacs

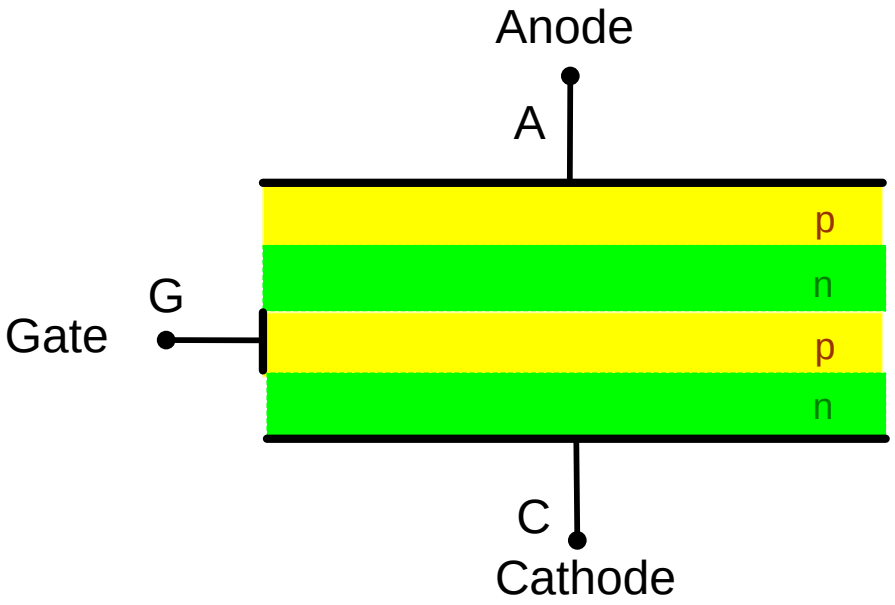
The bad

Parasitic Device that can destroy integrated circuits

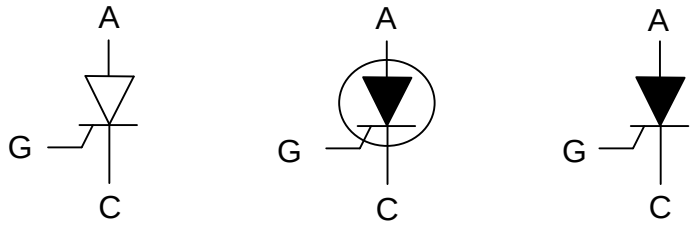
The SCR

Silicon Controlled Rectifier

- Widely used to switch large resistive or inductive loads
- Widely used in the power electronics field
- Widely used in consumer electronic to interface between logic and power



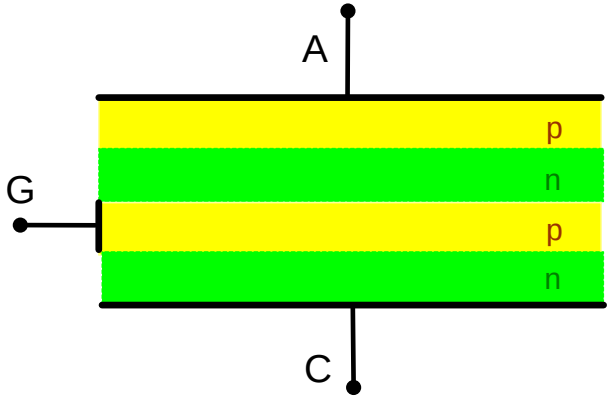
Usually made by diffusions in silicon

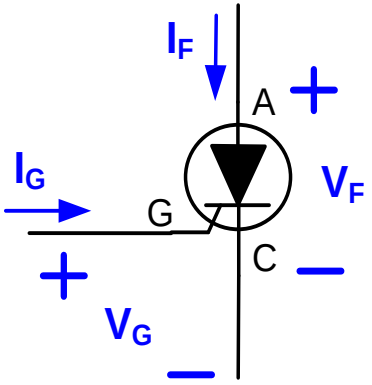


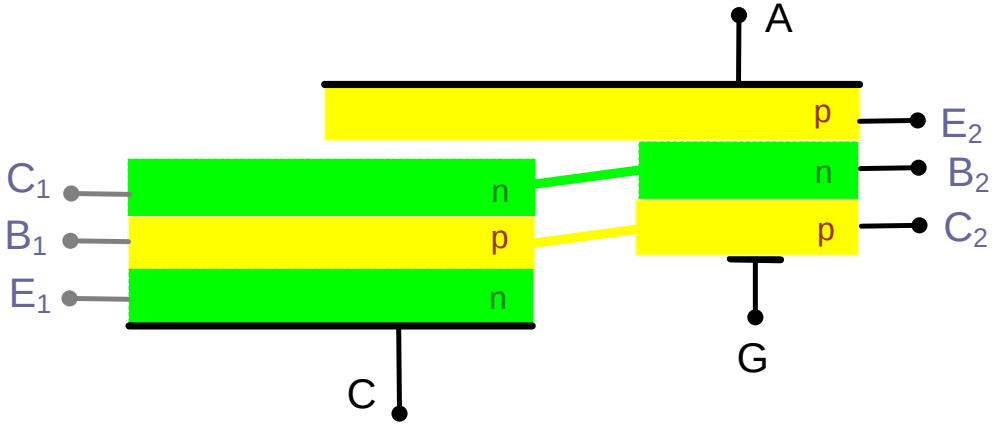
Symbols

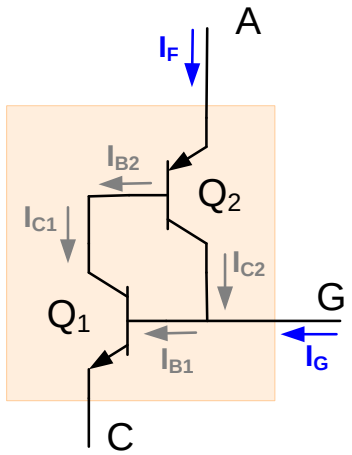
Consider first how this 4-layer 3-junction device operates

Operation of the SCR









Not actually separated but useful for describing operation

Variation of Current Gain (β) with Bias for BJT

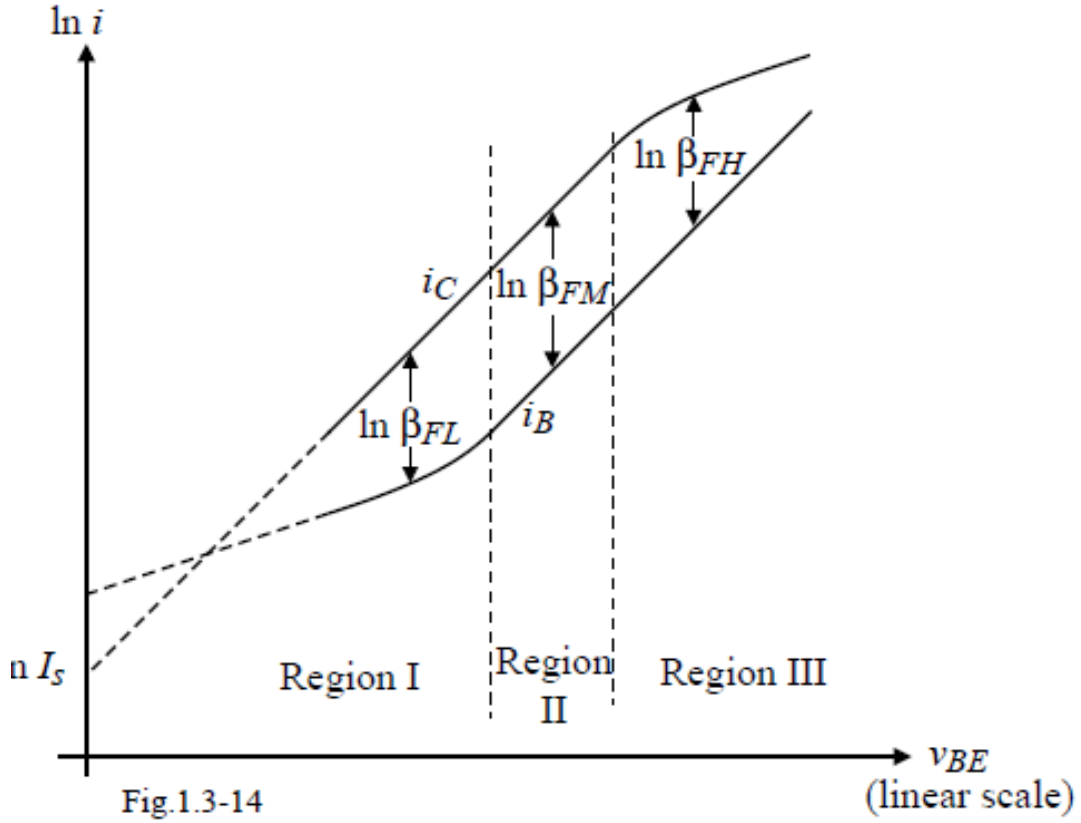
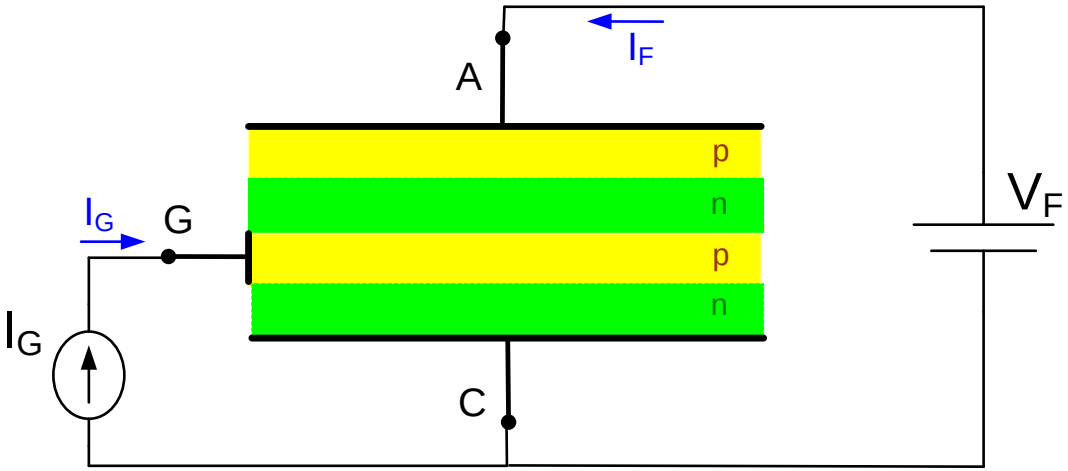
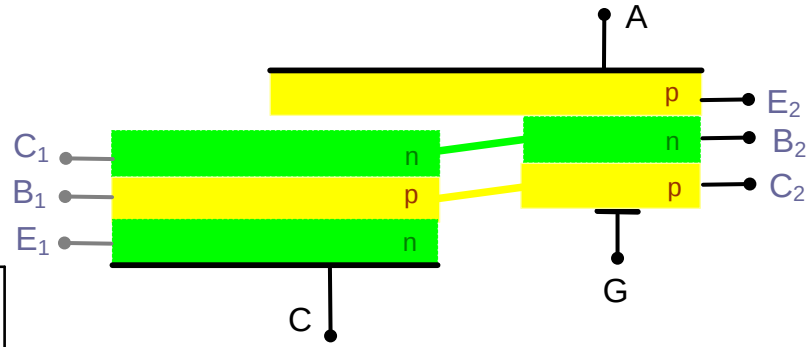


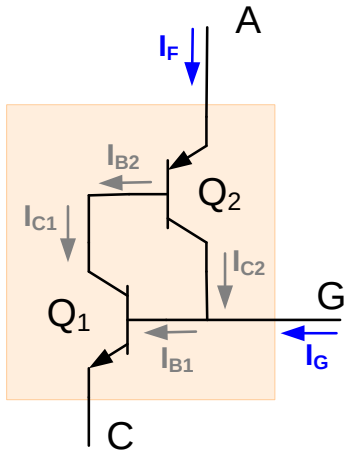
Fig.1.3-14

Note that current gain gets very small at low base current levels

Operation of the SCR







Consider a small positive bias (voltage or current) on the gate (V_{GC}<0.5V) and a positive and large voltage V_F

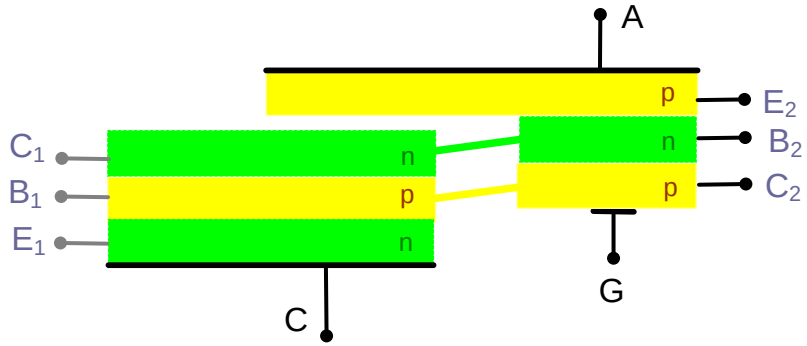
Will have $V_{C1} \geq V_F - 0.5V$

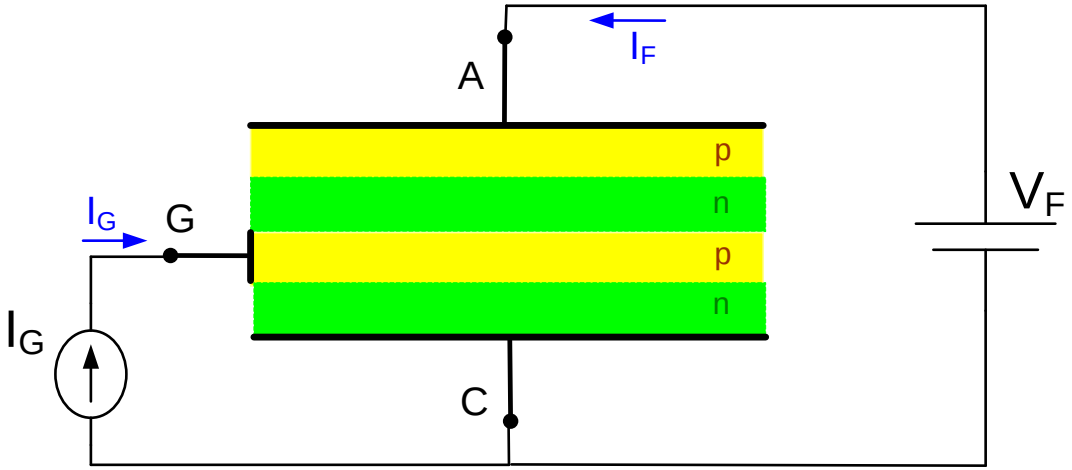
Thus Q_1 has a large positive voltage on its collector

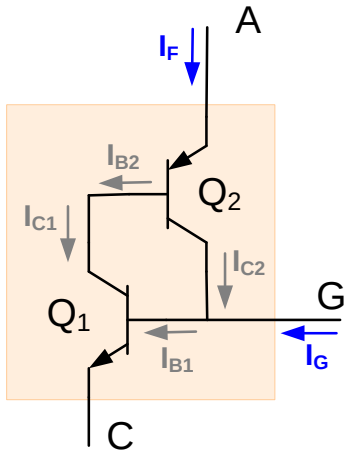
Since VB_{E1} is small, I_{C1} will be small as will I_{C2} so diode equation governs BE junction of Q_1

I_F will be very small

Operation of the SCR







Now let bias on the gate increase (V_{GC} around 0.6V) so Q_1 and Q_2 in FA $V_{C1} \geq V_F - 0.5V$

From diode equation, base voltage V_{BE1} will increase and collector current I_{C1} will increase

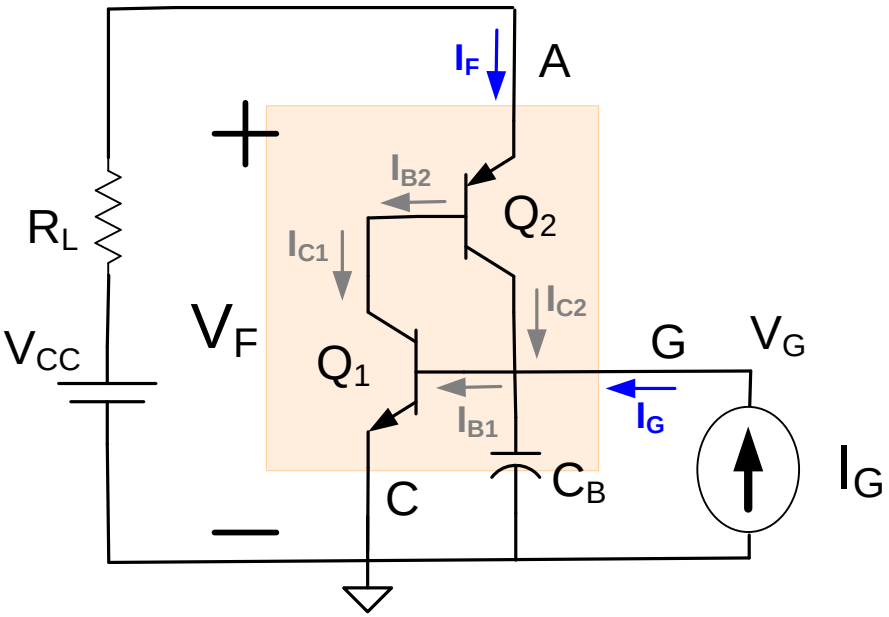
Thus base current I_{B2} will increase as will the collector current of I_{C2}

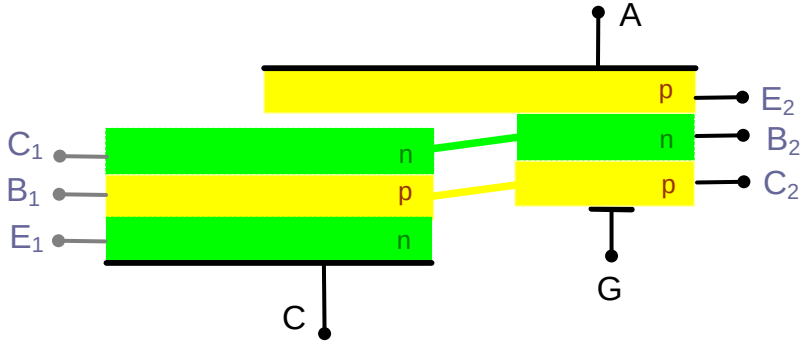
Under assumption of operation in FA region get expression

$$I_{B1} = I_G + \beta_1\beta_2 I_{B1}$$

This is regenerative feedback (actually can show pole in RHP)

Very Approximate Analysis Showing RHP Pole





$$V_G = I_G \frac{R_{BE}}{sR_{BE}C_B + 1 - \beta_1\beta_2}$$

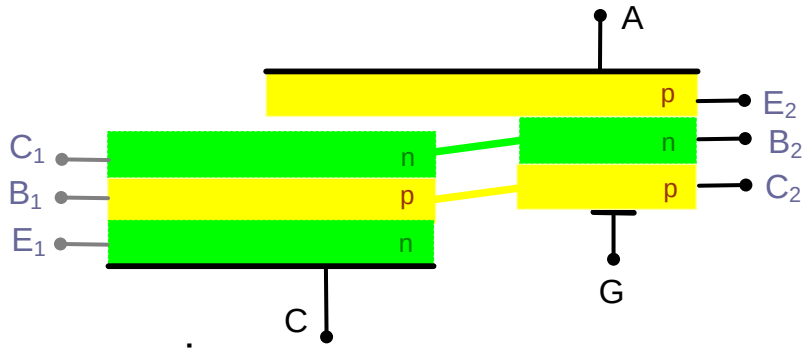
$$V_G sC_B + I_{B1} = I_{C2} + I_G$$

$$I_{C2} = \beta_1\beta_2 I_{B1}$$

$$I_{B1}R_{BE} = V_G$$

$$p = \frac{\beta_1\beta_2 - 1}{R_{BE}C_B}$$

Operation of the SCR



$V_{C1} \cong V_F - 0.6V$

Under assumption of operation in FA region get expression

$$I_{B1} = I_G + \beta_1\beta_2 I_{B1}$$

What will happen with this is regenerative feedback?

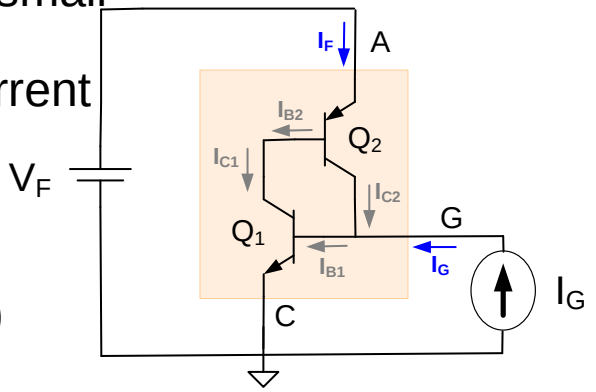
If I_G is small (and thus β_1 and β_2 are small) I_F will be very small

If I_G larger but less than $\beta_1\beta_2 I_{B1}$ it can be removed and current will continue to flow

I_{C1} will continue to increase and drive Q_1 into SAT

This will try to drive V_A towards 0.9V (but forced to be V_F!)

The current in V_F will go towards ∞

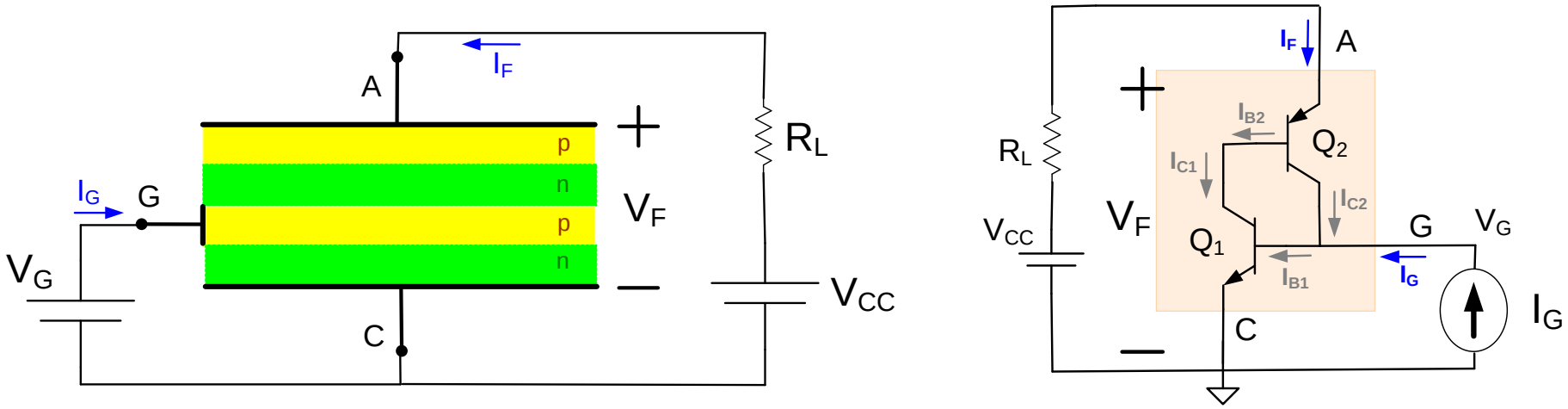


The SCR will self-destruct because of excessive heating !

Too bad the circuit self-destructed because the small gate current was able to control a lot of current!

Operation of the SCR

Consider a modified application by adding a load (depicted as R_L)

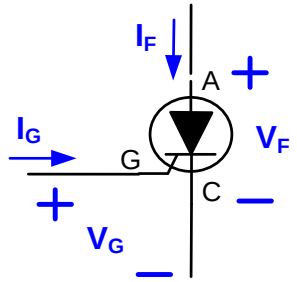


All operation is as before, but now, after the triggering occurs, the voltage V_F will drop to approximately 0.8 V and the voltage V_{CC}-.8 will appear across R_L

If V_{CC} is very large, the SCR has effectively served as a switch putting V_{CC} across the load and after triggering occurs, I_G can be removed!

But, how can we turn it off? Will discuss that later

Operation of the SCR



SCR model

$$\left.\begin{aligned} I_F &= f_1(V_F, V_G) \\ I_G &= f_2(V_G) \end{aligned}\right\}$$

As for MOSFET, Diode, and BJT, several models for SCR can be developed

The Ideal SCR Model

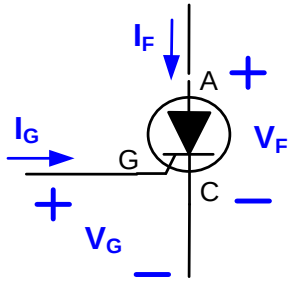
$$\left.\begin{aligned} I_F &= f_{1\mathrm{I}}(V_F, I_G) \\ I_G &= f_{2\mathrm{I}}(V_G) \end{aligned}\right\}$$

or

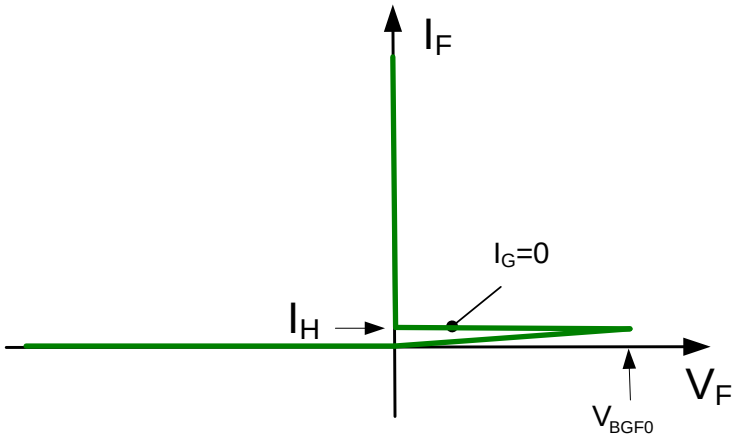
$$\left.\begin{aligned} I_F &= f_{1IA}(V_F, V_G) \\ I_G &= f_{2I}(V_G) \end{aligned}\right\}$$

Operation of the SCR

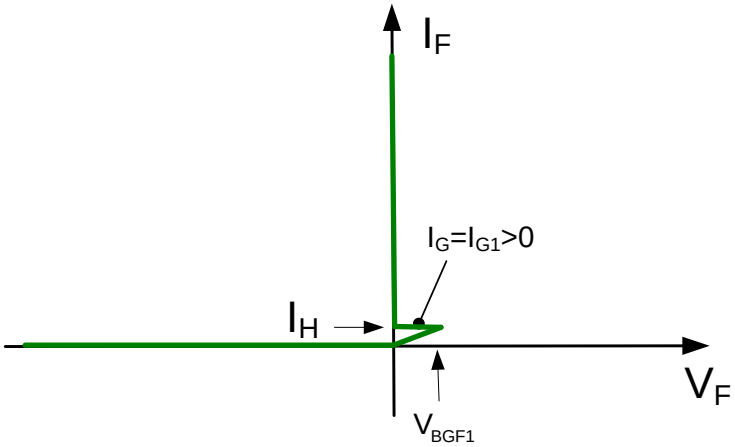
Consider the Ideal SCR Model



$$I_F = f_{1I}(V_F, I_G)$$
$$I_G = f_{2I}(V_G)$$



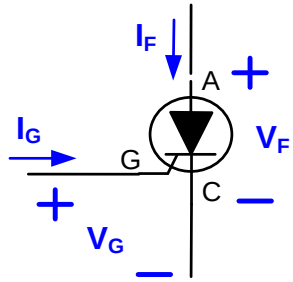
I_H is very small



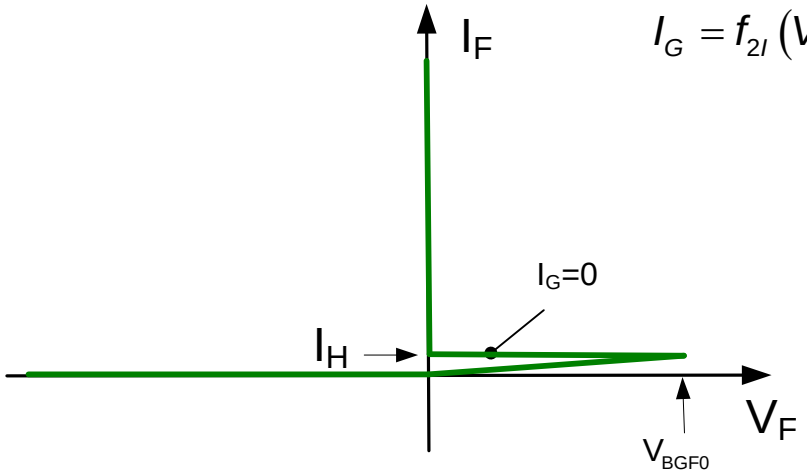
I_{G1} is small (but not too small)

Operation of the SCR

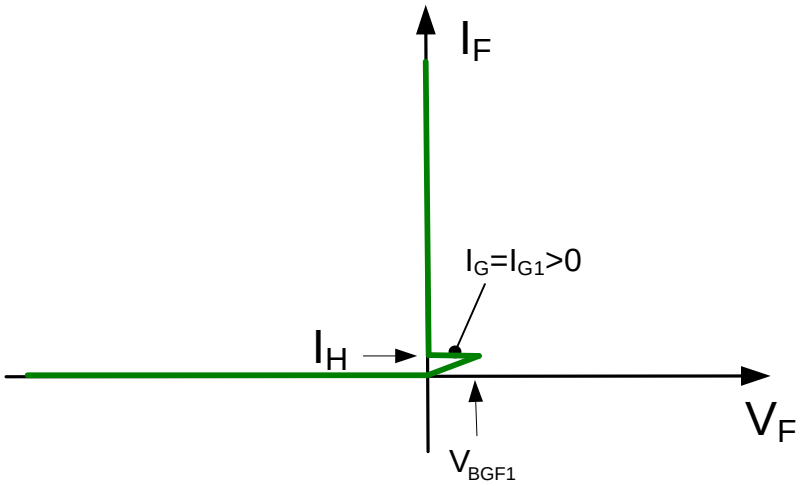
Consider the Ideal SCR Model



$$I_F = f_{1I}(V_F, I_G)$$
$$I_G = f_{2I}(V_G)$$



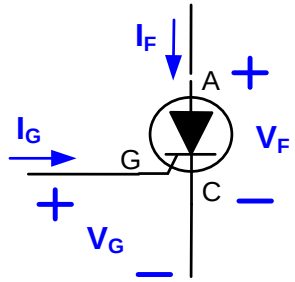
I_H is very small



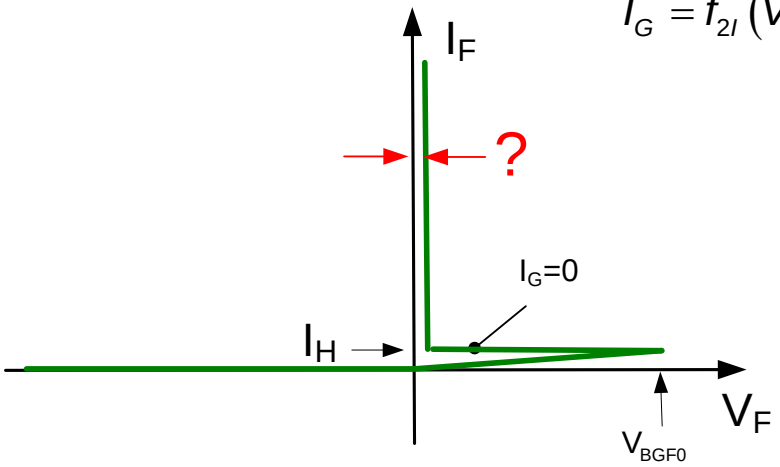
I_{G1} is small (but not too small)

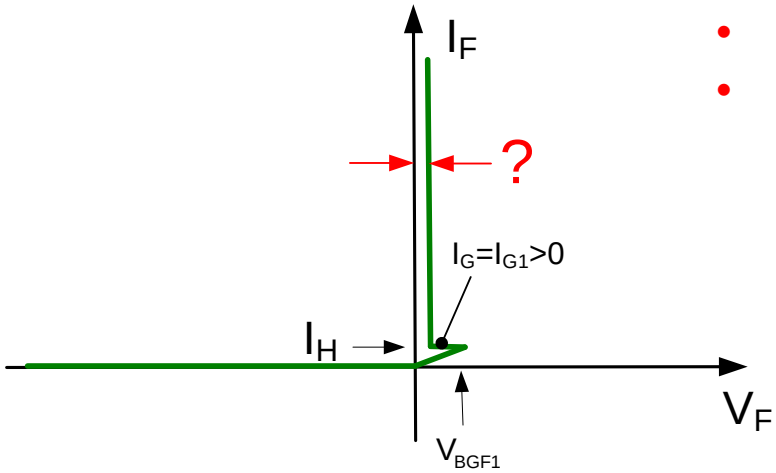
Operation of the SCR

Consider nearly Ideal SCR Model



$$I_F = f_{1I}(V_F, I_G)$$
$$I_G = f_{2I}(V_G)$$



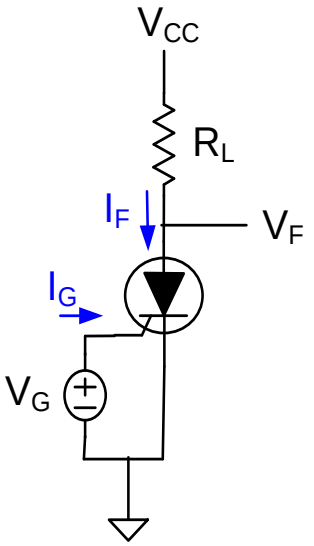


- On voltage approximately 0.9V
- Major contributor to ON-state power dissipatio
- Even with large currents, P_{ON} is quite small

Operation of the SCR

Operation with the Ideal SCR

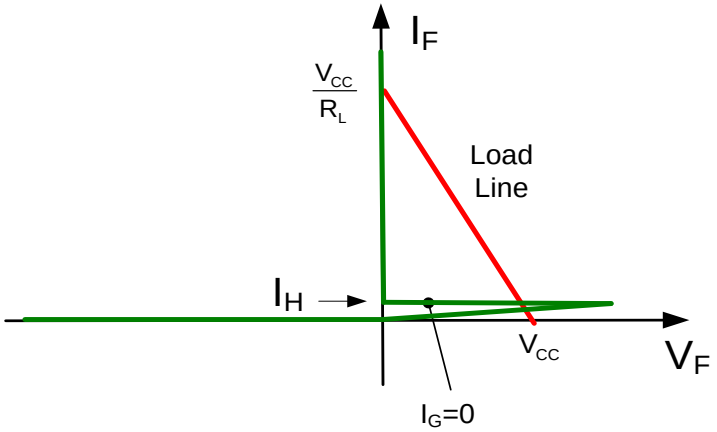
$$I_F = f_1(V_F, V_G)$$
$$I_G = f_2(V_G)$$



Load Line: $V_{CC} = I_F R_L + V_F$

Analysis:
$$V_{CC} = I_F R_L + V_F$$
$$I_F = f_{1I}(V_F, V_G)$$

The solution of these two equations is at the intersection of the load line and the device characteristics



when I_G=0

Note three intersection points
Two (upper and lower) are stable equilibrium points, one is not

When operating at upper point, V_F=0 so V_{CC} appears across R_L We say SCR is ON

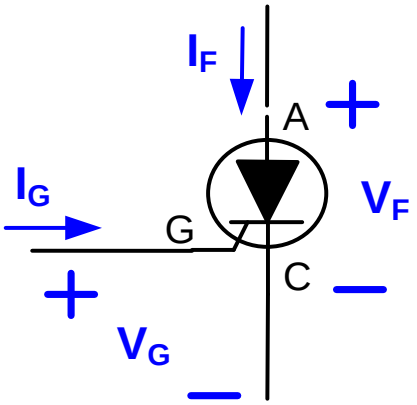
When operating at lower point, I_F approx 0 so no signal across R_L We say SCR is OFF

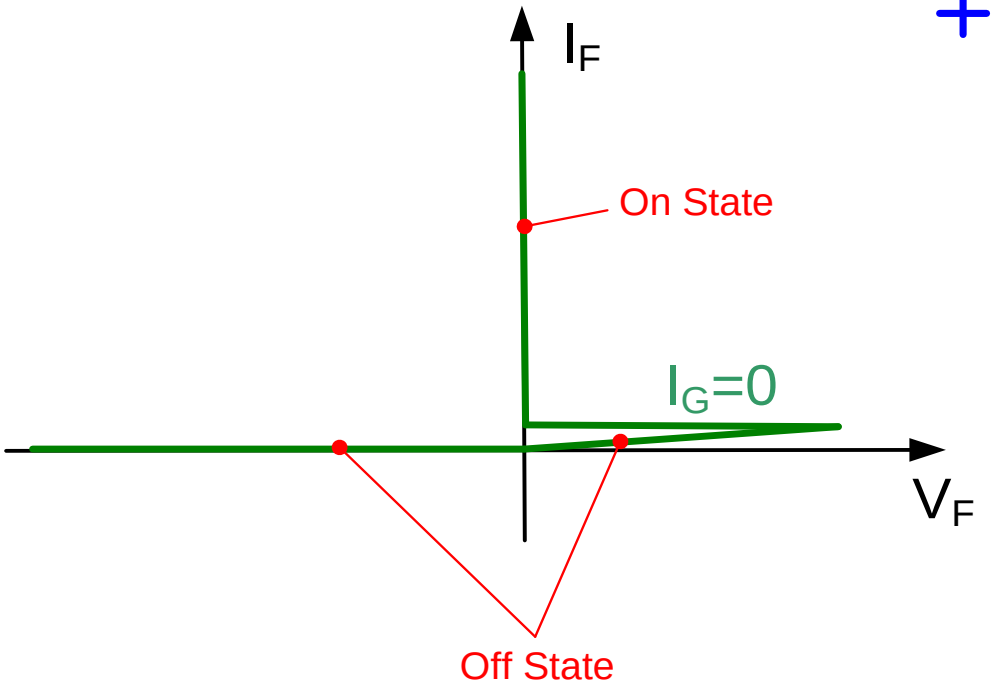
When I_G=0, will stay in whatever state it was in

Operation of the SCR

Operation with the Ideal SCR

$$I_F = f_{1I}(V_F, I_G)$$





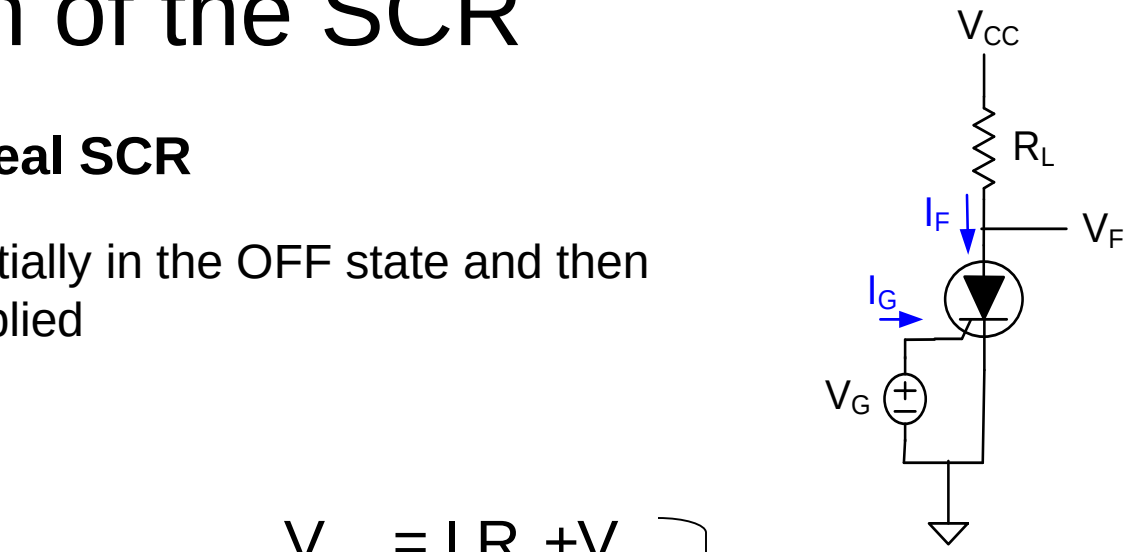
For notational convenience will drop subscript unless emphasis is needed

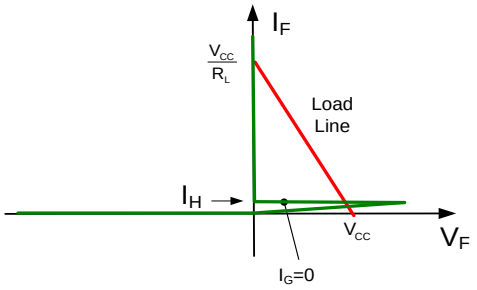
$$I_F = f_{1I}(V_F, I_G) \quad \Rightarrow \quad I_F = f(V_F, I_G)$$

Operation of the SCR

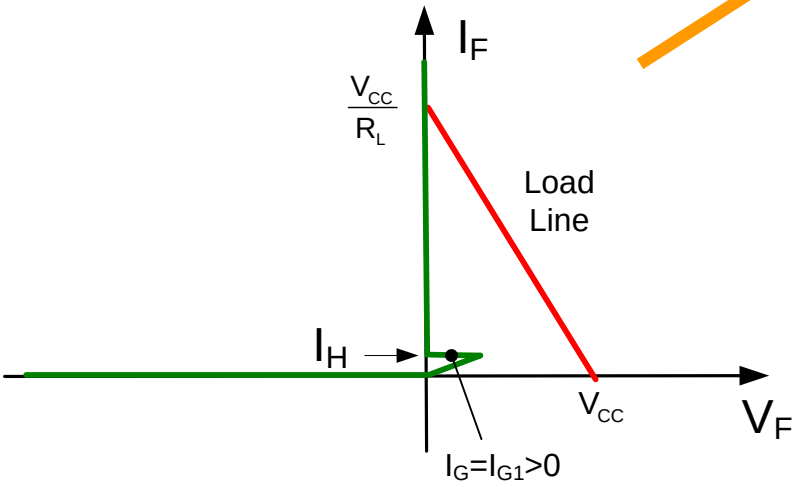
Operation with the Ideal SCR

Now assume it was initially in the OFF state and then a gate current was applied





$$V_{CC} = I_F R_L + V_F$$
$$I_F = f\left(V_F, I_G\right)$$



Now there is a single intersection point so a unique solution

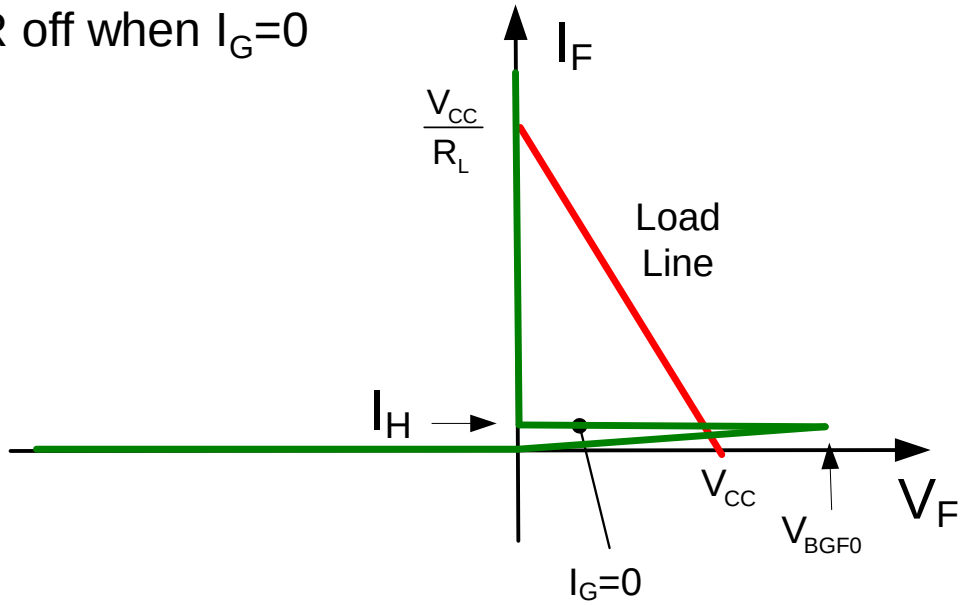
The SCR is now ON

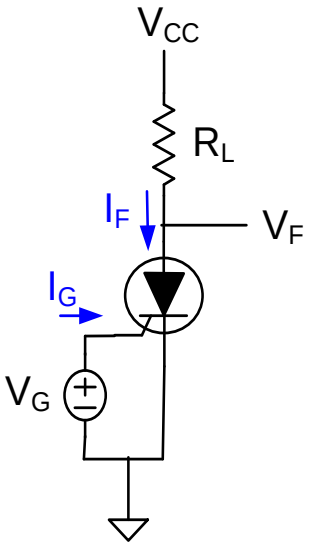
Removing the gate current will return to the previous solution (which has 3 intersection points) but it will remain in the ON state

Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G=0$





Reduce V_{CC} so that V_{CC}/R_L goes below I_H

This will provide a single intersection point

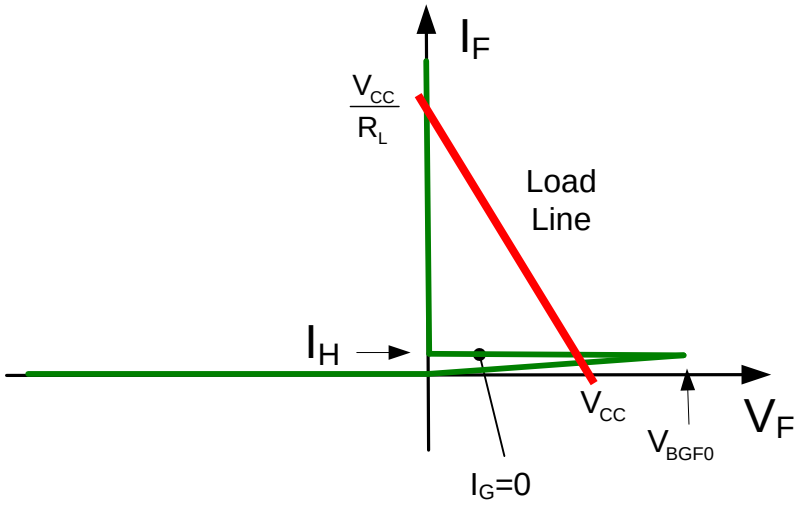
V_{CC} can then be increased again and SCR will stay off

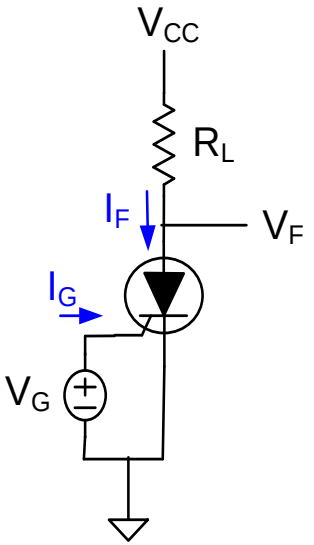
Must not increase V_{CC} much above V_{BGF0} else will turn on

Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G=0$



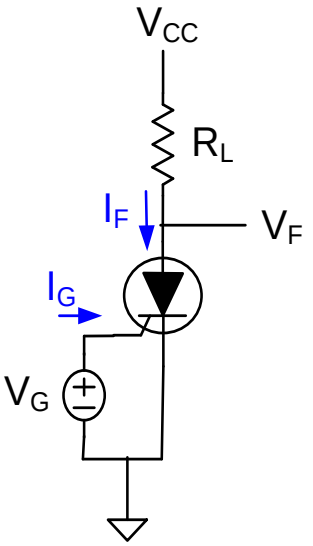


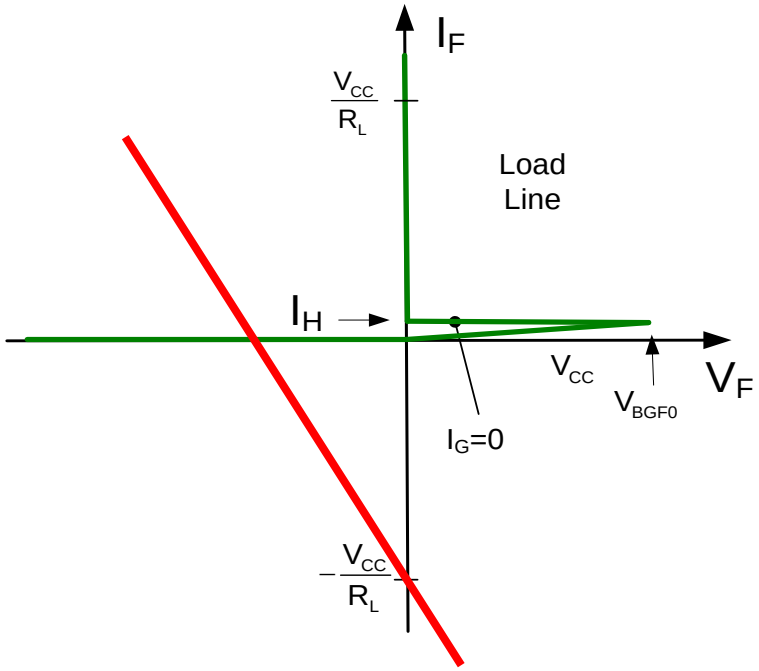
Operation of the SCR

Operation with the Ideal SCR

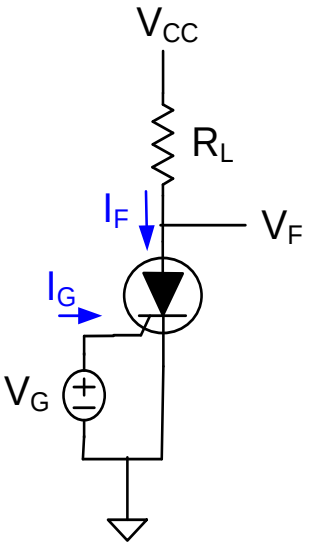
Often V_{CC} is an AC signal (often 110V)

SCR will turn off whenever AC signal goes negative





Operation of the SCR



Operation with the Ideal SCR

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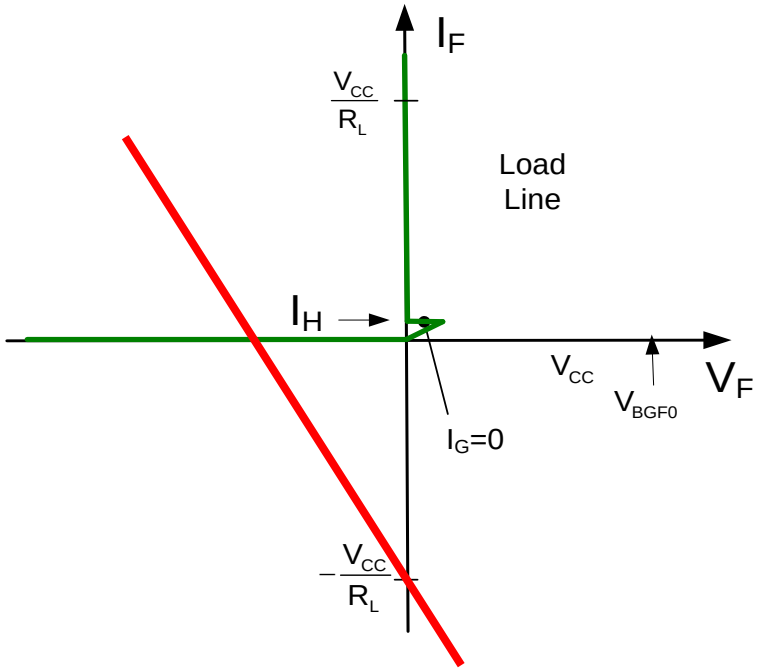
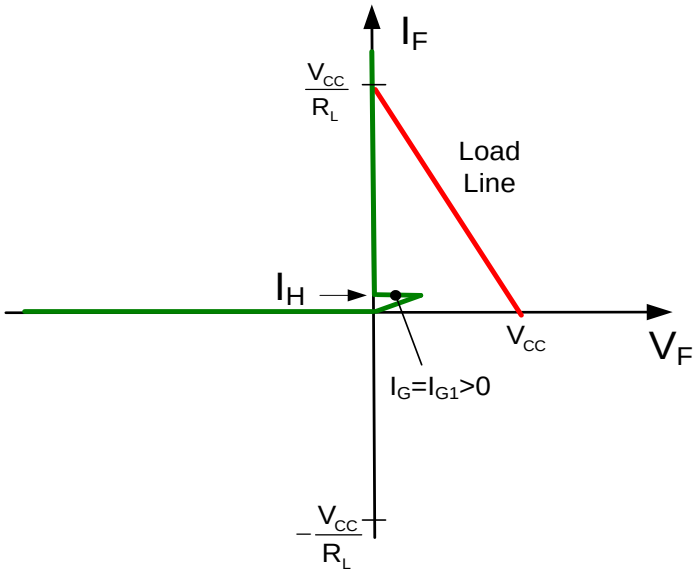
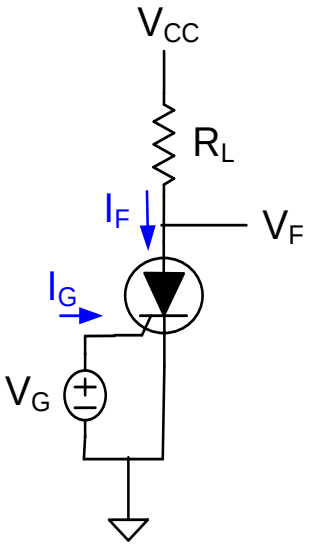


Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G>0$





Reduce V_{CC} so that V_{CC}/R_L goes below I_H

This will provide a single intersection point

But when V_{CC} is then increased SCR will again turn on

Will not turn off if I_G is very large

End of Lecture 28