Name _____

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Lab Section (circle one): A (T 6-9), **B** (W 3-6), **C** (R 4-7), **D** (F 12-3), **E** (R 12-3), **F** (T 12-3), **G** (W 6-9), **J** (W 12-3), **K** (T 3-6), **L** (T 9-12), **M** (R 9-12), **N** (R 12-3)

CprE 281

Digital Logic

Mock Examination #2

Time limit: 50 minutes

Directions: There are 8 questions in this exam. Each question is worth points indicated along with the problem. You should roughly spend 1 minute for every two point. So plan accordingly. If a problem appears to be hard, move on. Please read the questions carefully. Do not write more than what is required.

Problem	**Score**
1	_____ **/ 12 points**
2	_____ **/ 8 points**
3	_____ **/ 12 points**
4	_____ **/ 14 points**
5	_____ **/ 16 points**
6	_____ **/ 14 points**
7	_____ **/ 8 points**
8	_____ **/ 16 points**
Total	_____ (out of 100 points)

1. (Total 12 points) Assume 5-bit 2's complement representation is used.
   (a) Convert the following binary numbers to decimal numbers.
      i) 01010

      ii) 10011

   (b) Convert the following decimal numbers to binary numbers.
      i) 10

      ii) –5

   (c) Negate the following numbers:
      i) 01010

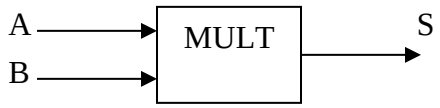
      ii) 10011

   (d) Perform the operations below and indicate whether or not overflow occurs in each case.

01000	10001	10001
+01000	+11111	-10000

2. (Total 8 points) Convert -4.625×2^9 into IEEE single-precision floating point format.

3. (Total 12 points) Consider the following n-bit multipler block which compute S=A*B. Assume that you do not have any overflow problem.



(a) How can you use one MULT block to compute A^2?

(b) How can you use two MULT blocks to compute A^4?

(c) How can you compute A^8 with the smallest number of MULT blocks?

(d) Construct a circuit using the minimum number of MULT blocks to compute A^9.

4. (Total 14 points) You are given a 3-bit full adder, and several 2-to-1 multiplexers. Suppose A is a 3-bit input number. Design a circuit which can perform the following Operations based on a 2-bit control code S1 S0. Ignore any overflow problem. Show clearly how the control signals S1 and S0 are used. Make your design as simple as possible.

S1	**S0**	**Operations**
0	0	A
0	1	A+1
1	0	A+2
1	1	A+3

5. (Total 16 points) In this question, we will compare two different ways to construct a 4-to-1 multiplexer.
   (a) Design a 4-to-1 multiplexer as a SOP expression using **only** 2-input AND gates, 2-input OR gates, and NOT gates.

   (b) How many AND gates, OR gates, and NOT gates are used for the design in (a)?

   (c) First design a 2-to-1 multiplexer as a SOP expression using **only** 2-input AND gates, 2-input OR gates, and NOT gates. Then design a 4-to-1 multiplexer using the 2-to-1 multiplexers constructed as building blocks.

   (d) How many AND gates, OR gates, and NOT gates are used for the design in (b)?

   (e) Which design is better in terms of number of gates used?

6. (Total 14 points)
   (a) Implement the following function by a 4-to-1 MUX and a minimal number of basic logic gates. Please label your circuit diagram clearly.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

   (b) Based on Shannon's expansion, implement the following function by a 4-to-1 MUX and a minimal number of basic logic gates. Please label your circuit diagram clearly.

$F(A,B,C) = (A'+B').(B+A.C)$

7. (Total 8 points) Construct a 3-to-8 decoder using AND gates, OR gates, and NOT gates **only**. Please label your circuit diagram clearly.

8. (Total 16 points) Show how to construct a JK flip-flop using:
   (a) one T flip-flop and a minimal number of AND, OR and NOT gates.

   (b) one D flip-flop and a minimal number of AND, OR and NOT gates.

(END OF EXAM)

Extra Exercises

1. At least how many bits are required to represent each set of objects below:
   (a) All integers from –1 to 255.
   (b) The 340 students in a classroom.
   (c) Numbers: 2, 3, 5, 7, 11, 13.

2. At least how many trits (trinary digits) are required to represent each set in question 1 above?

3. What is the range of integer that can be represented by a 10-bit word if
   (a) Representation of non-negative numbers is used?
   (b) Sign-magnitude representation is used?
   (c) 1's complement representation is used?
   (d) 2's complement representation is used?

4. Convert the number -19 into binary in the following representation:
   (a) 6-bit unsigned representation.
   (b) 6-bit sign-magnitude representation.
   (c) 6-bit 1's complement representation.
   (d) 6-bit 2's complement representation.

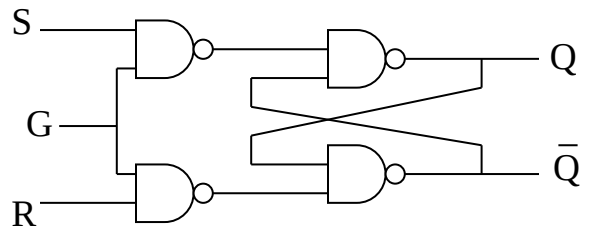
5. Notice that 4-to-1 multiplexer is a function with 6 inputs (S1, S0, I3, I2, I1, and I0) and 1 output (F).
   (a) Write the truth table in uncompact form for a 4-to-1 multiplexer.
   (b) Draw the K-map for a 4-to-1 multiplexer.
   (c) From the K-map, write the simplest sum-of-product expression of F.
   (d) Write a sum-of-product expression of F from the compact form truth table. Is this expression or the expression in part (c) above simpler?

6. The parity function is defined as follows. The output is '0' if the number of '1's in the input is even, and is '1' if the number of '1's in the input is odd. A 4-bit parity P(W,X,Y,Z) is given in the following truth table. Implement the 4-bit parity function using a multiplexer. You may determine the size of the multiplexer.

W	**X**	**Y**	**Z**	**P**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

7. Construct a 4-to-2 priority decoder using a minimal number of basic logic gates.

8. Show the next state for the following gated SR latch with control input (G). The choices for the next state are: NC (no change), Q = 0, Q = 1, U (undefined).



G	S	R	Next state
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

9. Construct a register file consisting of eight 10-bit registers, one input port, and two output ports. You may use parallel-access registers of any size, multiplexers of any size, and any kind of decoders with any size.