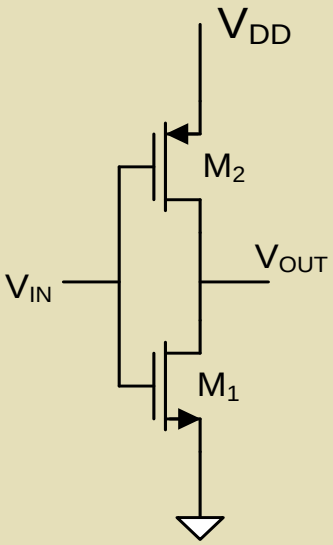
EE 330
Lecture 42

Digital Circuits

- Propagation Delay With Multiple Levels of Logic
- Optimally Driving Large Capacitive Loads
  - Overdrive
  - Sizing for optimal driving

The Reference Inverter

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, $R_{PDREF}=R_{PUREF}$=2.5K

$$R_{PDREF}=R_{PUREF}$$

$$\mathbf{C_{REF}=C_{IN}=4C_{OX}W_{MIN}L_{MIN}}$$

$$R_{PDREF}=\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$\mathbf{t_{HLREF}=t_{LHREF}=R_{PDREF}C_{REF}}$$

$$\mathbf{t_{REF}=t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}}$$

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

Question:

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes ?

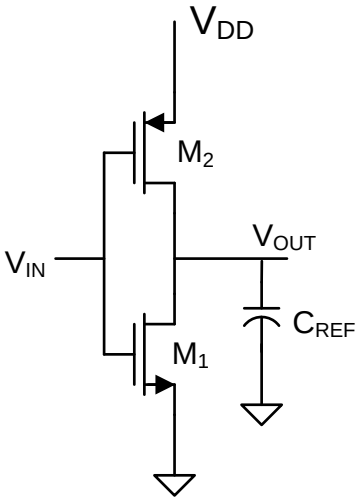
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy

-- (same as $V_{TRIP}=V_{DD}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p=3$ **How many degrees of freedom were available?**

$L_n=L_p=L_{MIN}$

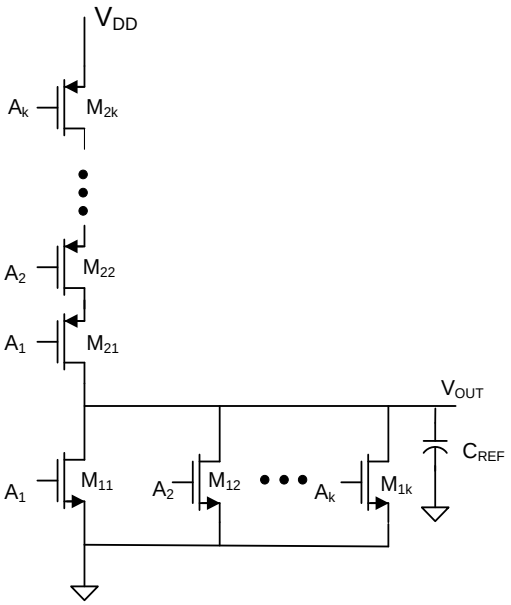


INV

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$C_{IN}=C_{REF}$

FI=1

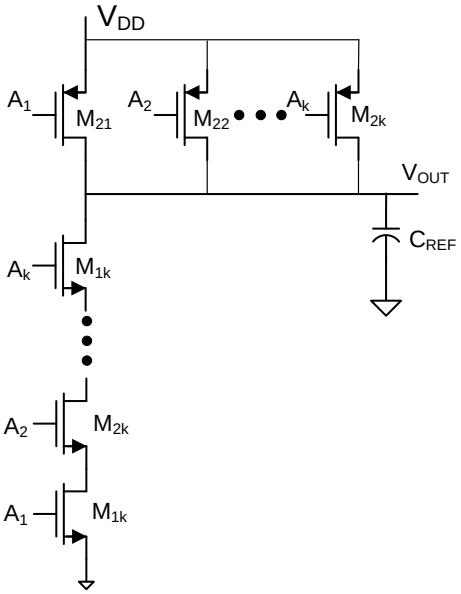


k-input NOR

$W_n=W_{MIN}$, $W_p=3kW_{MIN}$

$$C_{IN}=\left(\frac{3k+1}{4}\right)C_{REF}$$

$$FI=\left(\frac{3k+1}{4}\right)$$



k-input NAND

$W_n=kW_{MIN}$, $W_p=3W_{MIN}$

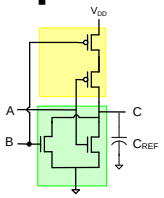
$$C_{IN}=\left(\frac{3+k}{4}\right)C_{REF}$$

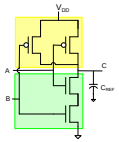
$$FI=\left(\frac{3+k}{4}\right)$$

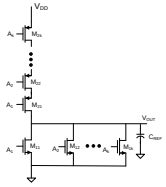
Device Sizing

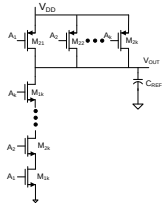
Multiple Input Gates:

2-input NOR **2-input NAND** **k-input NOR** **k-input NAND**









Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Wn=?
Wp=?

Fastest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized (assume driving a load of C_{REF})

Wn=Wmin
Wp=Wmin

Fastest response (t_{HL} or t_{LH}) = ?

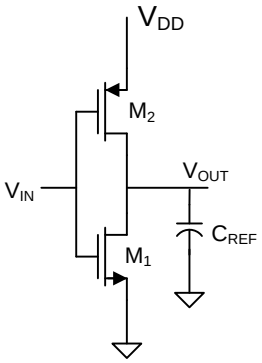
Slowest response (t_{HL} or t_{LH}) = ?

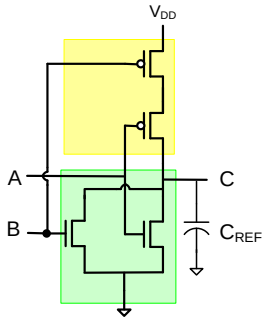
Worst case response (t_{PROP}, usually of most interest)?

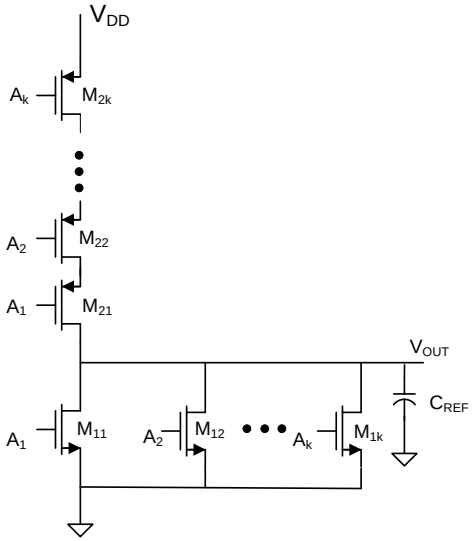
Input capacitance (FI) = ?

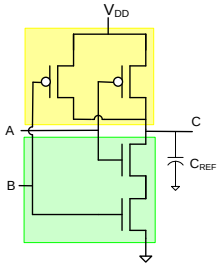
Review from Last Time

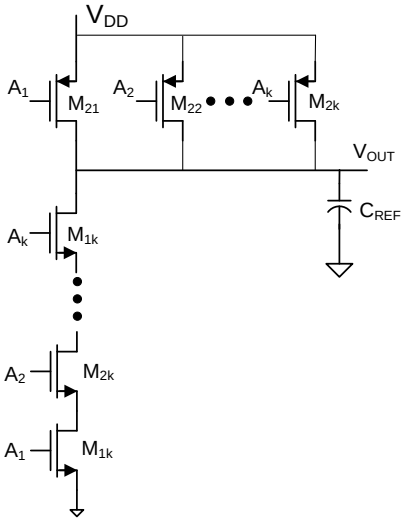
Device Sizing











Minimum Sized **(assume driving a load of C_{REF})** $W_n=W_{min}$ $W_p=W_{min}$

Input capacitance (FI) = ?

$$C_{IN} = C_{OX}W_nL_n + C_{OX}W_pL_p = C_{OX}W_{min}L_{min} + C_{OX}W_{min}L_{min} = 2C_{ox}W_{min}L_{min} = \frac{C_{REF}}{2}$$

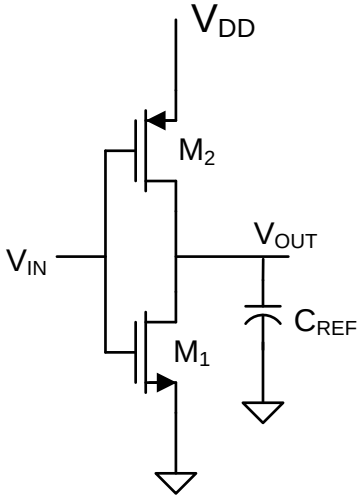
$$FI = \frac{1}{2}$$

Fastest response (t_{HL} or t_{HL}) = ?

Slowest response (t_{HL} or t_{HL}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Device Sizing – minimum size driving C_{REF}



INV

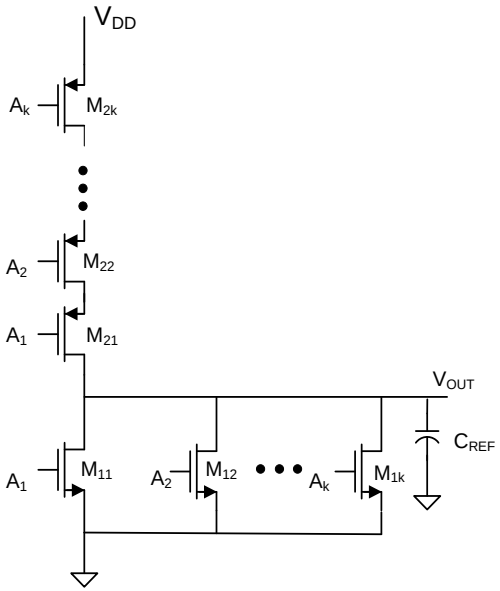
$t_{PROP} = ?$

$$t_{PROP} = 0.5t_{REF} + \frac{3}{2}t_{REF}$$

$$t_{PROP} = 2t_{REF}$$

$$FI = \frac{C_{REF}}{2}$$

$$R_{PU} = R_{PD} = R_{PDREF}$$



k-input NOR

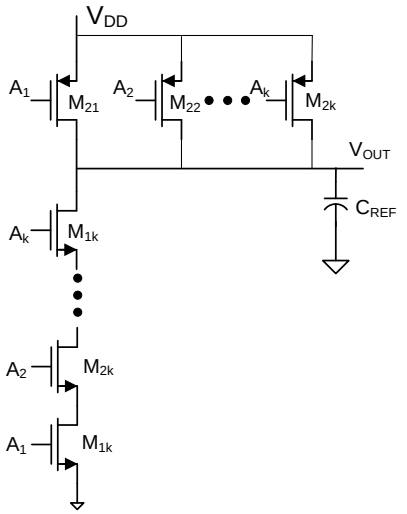
$t_{PROP} = ?$

$$t_{PROP} = 0.5t_{REF} + \frac{3k}{2}t_{REF}$$

$$t_{PROP} = \left(\frac{3k+1}{2}\right)t_{REF}$$

$$FI = \frac{C_{REF}}{2}$$

$$R_{PD} = R_{PDREF} \quad R_{PU} = 3kR_{PDREF}$$



k-input NAND

$t_{PROP} = ?$

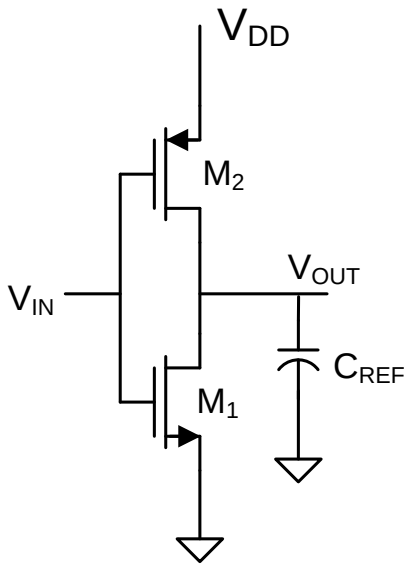
$$t_{PROP} = \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF}$$

$$t_{PROP} = \frac{3+k}{2}t_{REF}$$

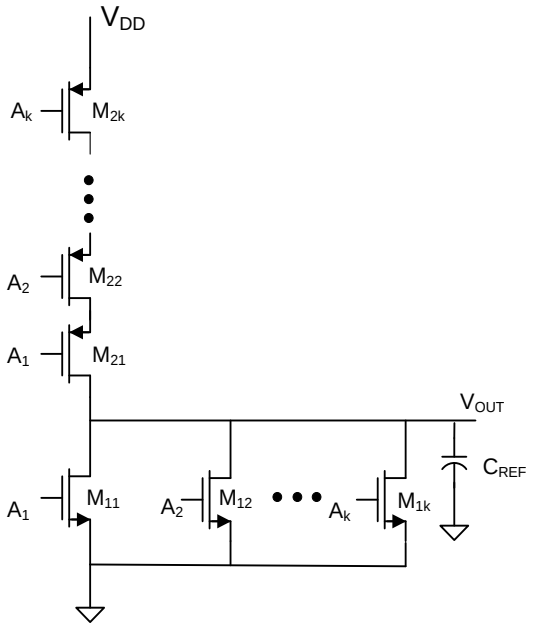
$$FI = \frac{C_{REF}}{2}$$

$$R_{PD} = 3R_{PDREF} \quad R_{PU} = 3R_{PDREF}$$

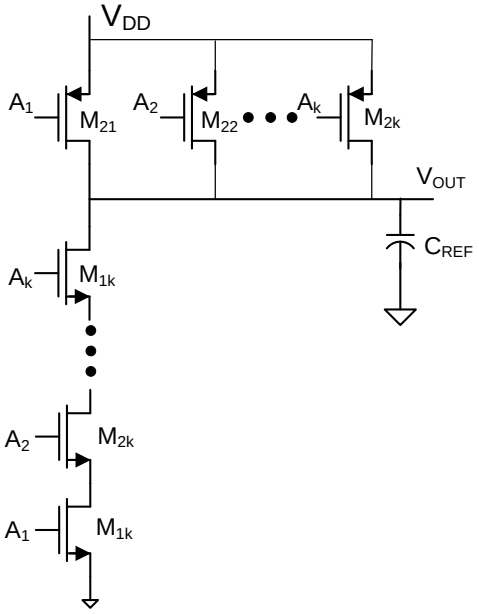
Device Sizing Summary



INV



k-input NOR



k-input NAND

C_{IN} for N_{AND} gates is considerably smaller than for NOR gates for equal worst-case rise and fall times

C_{IN} for minimuim-sized structures is independent of number of inputs and much smaller than C_{IN} for the equal rise/fall time case

R_{PU} gets very large for minimum-sized NOR gate

Digital Circuit Design

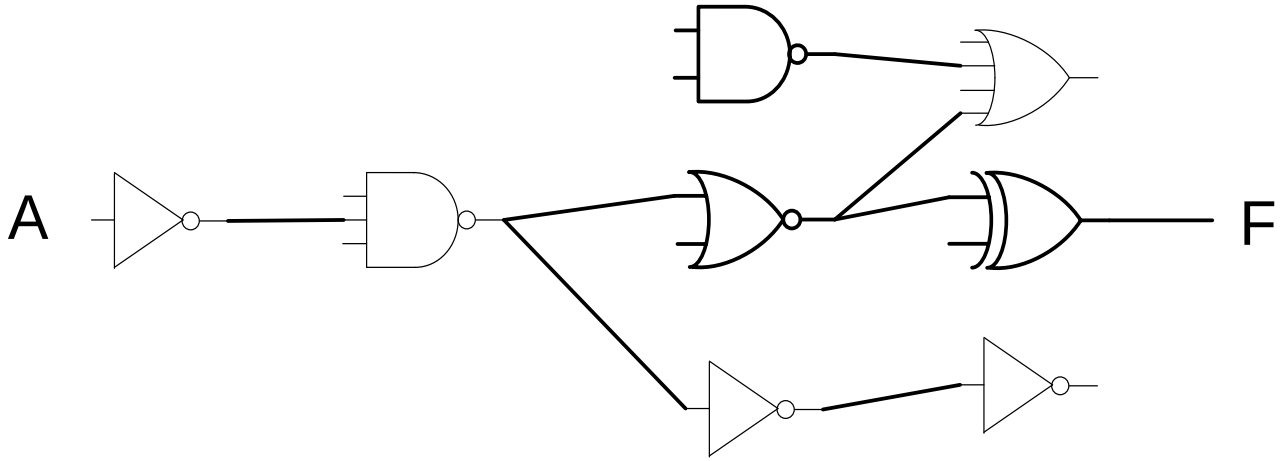
- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial

Propagation Delay in Multiple-Levels of Logic with Stage Loading



Assume all gates sized for equal worst-case rise/fall times

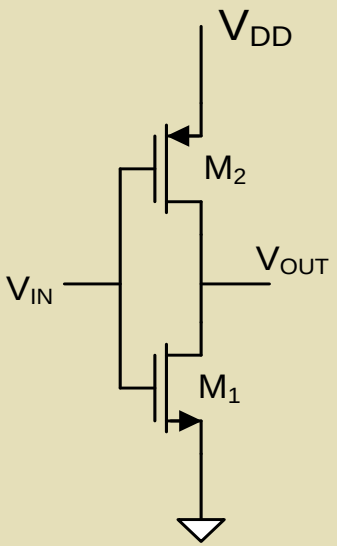
For n levels of logic between A and F

$$t_{PROP} = \sum_{k=1}^{n} t_{PROP}(k)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy : Express delays in terms of those of reference inverter

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

$$C_{REF}=C_{IN}=4C_{OX}W_{MIN}L_{MIN}$$

FI= 1

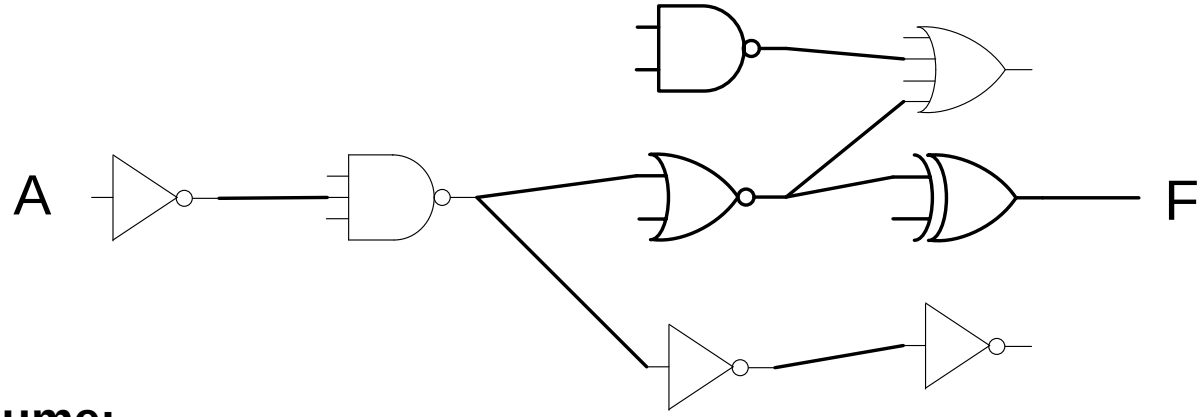
$$R_{PDREF}=\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$t_{REF}=t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}$$

$$L_n=L_p=L_{MIN}$$

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

Propagation Delay in Multiple-Levels of Logic with Stage Loading



Assume:

- **all gates sized for equal worst-case rise/fall times**
- **all gates sized to have rise and fall times equal to that of ref inverter when driving C_{REF}**

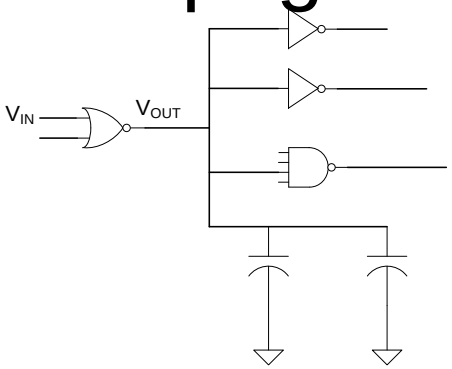
Observe:

- **Propagation delay of these gates will be scaled by the ratio of the total load capacitance on each gate to C_{REF}**

What loading will a gate see?

- **Input capacitance to other gates**
- **Any load capacitors**
- **Parasitic interconnect capacitnaces**

Propagation Delay with Stage Loading



$$t_{REF} = 2R_{PDref}C_{REF}$$

$$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

FI of a capacitor

$$FI_C = \frac{C}{C_{REF}}$$

FI of a gate (input k)

$$FI_G = \frac{C_{INk}}{C_{REF}}$$

FI of an interconnect

$$FI_I = \frac{C_{INI}}{C_{REF}}$$

Overall FI

$$FI = \frac{\sum_{\text{Gates}} C_{INGi} + \sum_{\text{Capacitances}} C_{INCi} + \sum_{\text{Interconnects}} C_{INIi}}{C_{REF}}$$

FI can be expressed either in units of capacitance or normalized to C_{REF}

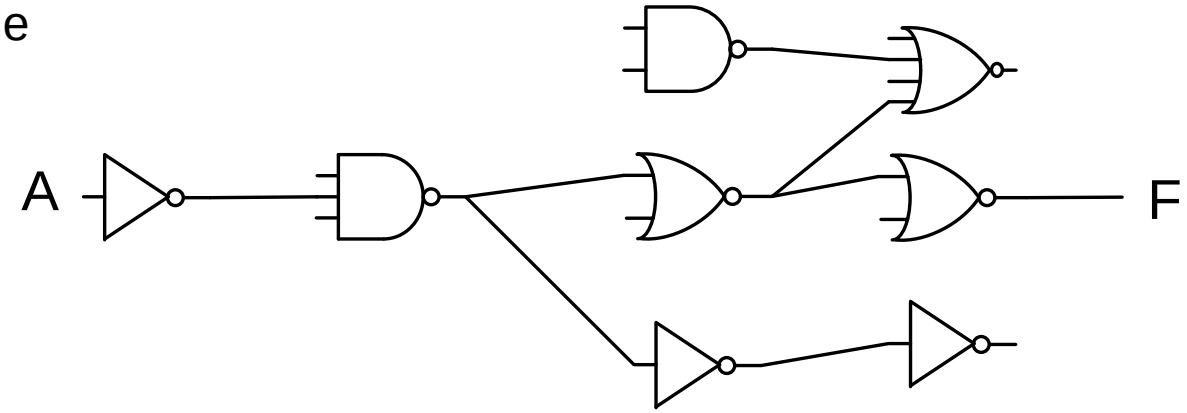
Most commonly FI is normalized but must determine from context

If gates sized to have same drive as ref inverter

$$t_{prop\text{-}k} = t_{REF} \bullet FI_{LOAD\text{-}k}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example



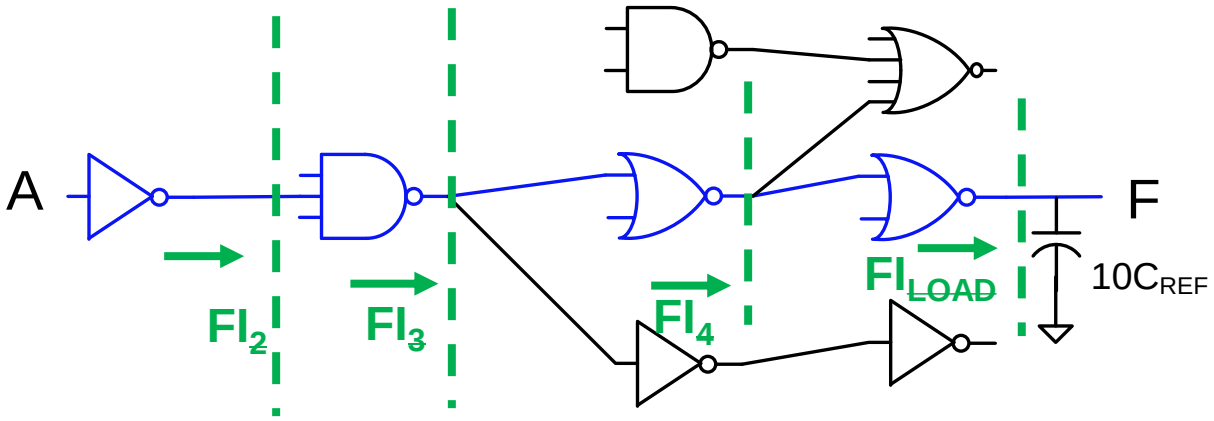
Assume all gates sized for equal worst-case rise/fall times

Assume all gate drives are the same as that of reference inverter

Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F

Propagation Delay in Multiple-Levels of Logic with Stage Loading



$$FI_{NOR} = \left(\frac{3k+1}{4}\right) C_{REF}$$

$$FI_{NAND} = \left(\frac{3+k}{4}\right) C_{REF}$$

Assume all gates sized for equal worst-case rise/fall times

Assume all gate drives are the same as that of reference inverter

Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F

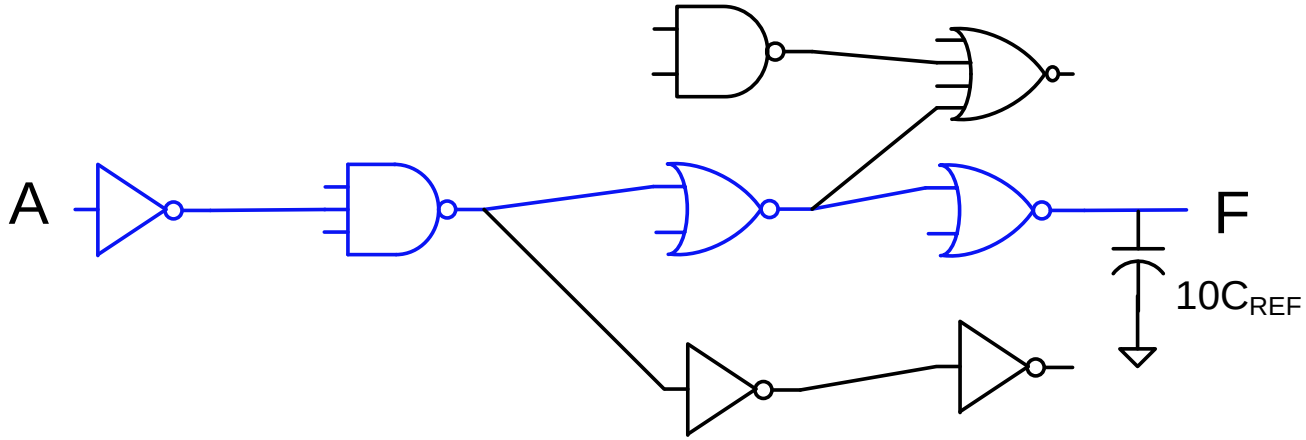
What loading will a gate see?

Derivation:

$$FI_2 = \frac{6}{4} C_{REF} \qquad FI_3 = C_{REF} + \frac{7}{4} C_{REF} \qquad FI_4 = \frac{7}{4} C_{REF} + \frac{13}{4} C_{REF} \qquad FI_{LOAD} = FI_{"5"} = 10C_{REF}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example



Assume all gates sized for equal worst-case rise/fall times

Assume all gate drives are the same as that of reference inverter

Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F

DERIVATIONS

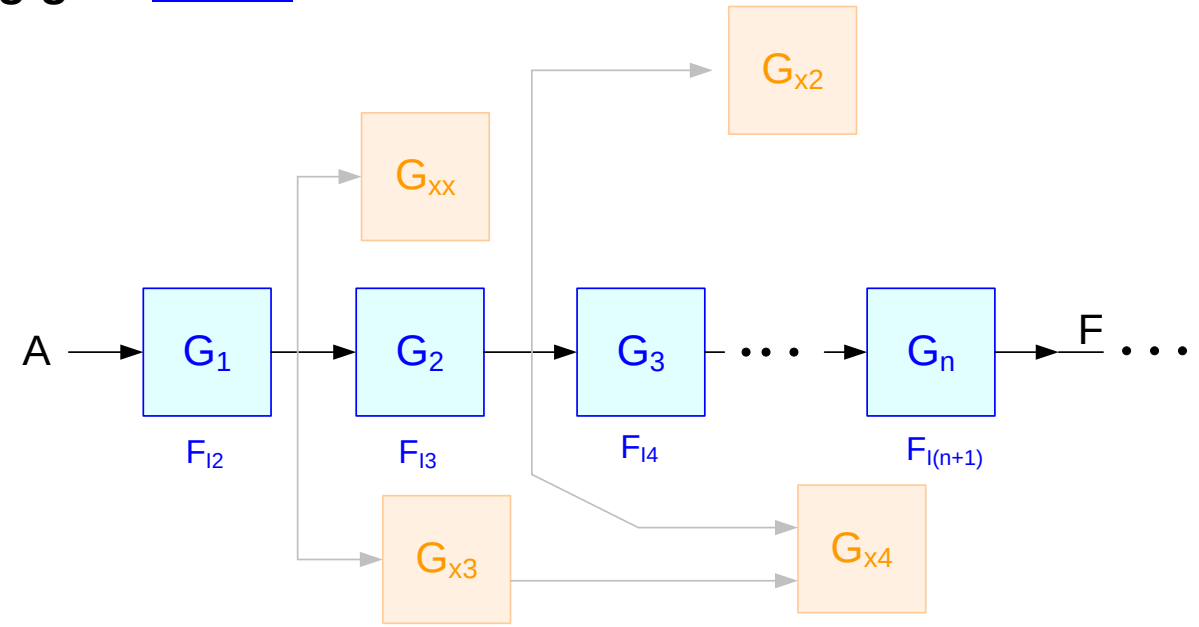
$$FI_2 = \frac{6}{4}C_{REF} \qquad FI_3 = C_{REF} + \frac{7}{4}C_{REF} \qquad FI_4 = \frac{7}{4}C_{REF} + \frac{13}{4}C_{REF} \qquad FI_5 = 10C_{REF}$$

$$t_{PROP1} = \frac{6}{4}t_{REF} \qquad t_{PROP2} = \left(1 + \frac{7}{4}\right)t_{REF} \qquad t_{PROP3} = \left(\frac{7}{4} + \frac{13}{4}\right)t_{REF} \qquad t_{PROP4} = 10t_{REF}$$

$$t_{PROP} = \sum_{k=1}^{n} t_{PROPk} = t_{REF}\sum_{k=1}^{n} FI_{(k+1)} = t_{REF}\left(\frac{6}{4} + \frac{11}{4} + \frac{20}{4} + 10\right) = t_{REF}\left(19.25\right)$$

Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)



Identify the gate path from A to F

$$t_{PROPk} = t_{REF} FI_{(k+1)}$$

Propagation delay from A to F:

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

This approach is analytically manageable, provides modest accuracy and is "faithful"

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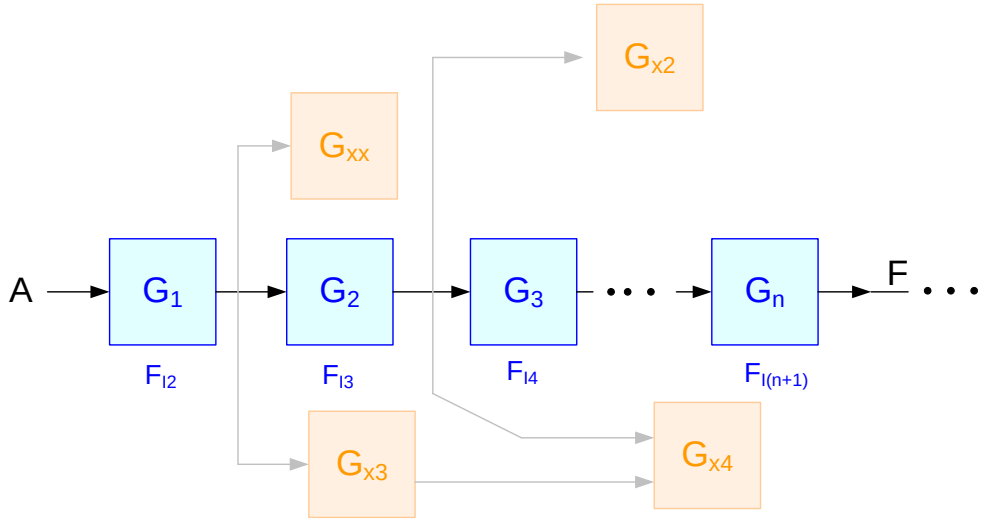
done

partial

What if the propagation delay is too long (or too short)?



Propagation delay from A to F:

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

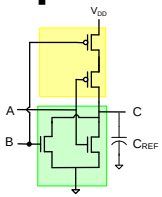
$$\mathbf{t_{PROPk} = t_{REF} FI_{(k+1)}}$$

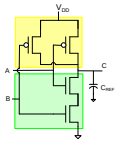
Recall:

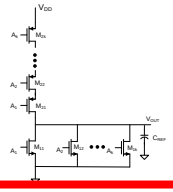
Device Sizing

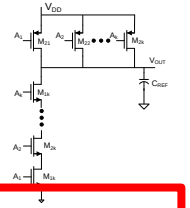
Multiple Input Gates:

2-input NOR **2-input NAND** **k-input NOR** **k-input NAND**









Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

consider the fine print !

W_n=?

W_p=?

Fastest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized **(assume driving a load of C_{REF})**

$W_n=W_{min}$

$W_p=W_{min}$

Fastest response (t_{HL} or t_{LH}) = ?

Slowest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Recall:

Device Sizing

Equal Worst Case Rise/Fall

(and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)

Assume $L_n=L_p=L_{min}$ and driving a load of C_{REF}

W_n=?

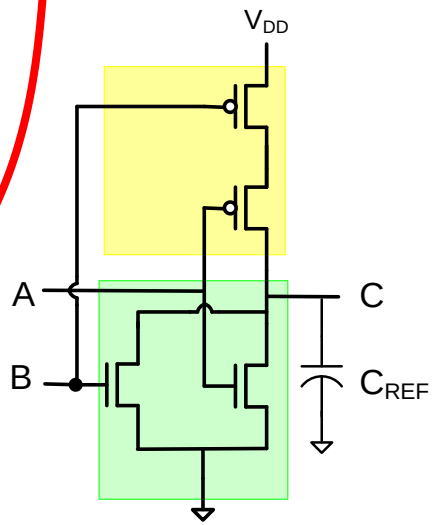
W_p=?

Input capacitance = ?

FI=?

t_{PROP}=? (worst case)

DERIVATIONS



One degree of freedom was used to satisfy the constraint indicated

$W_n=W_{MIN}$

$W_p=6W_{MIN}$

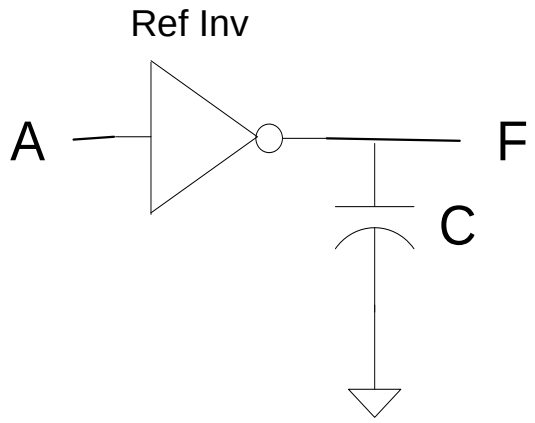
Other degree of freedom was used to achieve equal rise and fall times

$$C_{INA}=C_{INB}=C_{OX}W_{MIN}L_{MIN}+6C_{OX}W_{MIN}L_{MIN}=7C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)4C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)C_{REF}$$

$$FI=\left(\frac{7}{4}\right)C_{REF} \quad or \quad FI=\frac{7}{4}$$

$t_{PROP} = t_{REF}$ (worst case)

Overdrive Factors



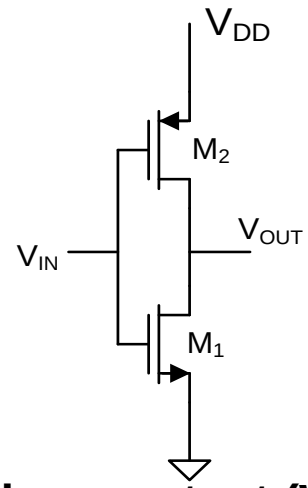
Example: Determine t_{prop} in 0.5u process if C=10pF **In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K**

$$t_{PROP} = t_{REF} \bullet Fl = t_{REF} \bullet \frac{10\,pF}{4\,fF} = t_{REF} \bullet 2500$$

$$t_{PROP} = 20ps \bullet 2500 = 50nsec$$

Note this is unacceptably long !

Overdrive Factors



Scaling widths of ALL devices by constant (W_{scaled}=WxOD) will change "drive" capability relative to that of the reference inverter but not change relative value of t_{HL} and t_{LH}

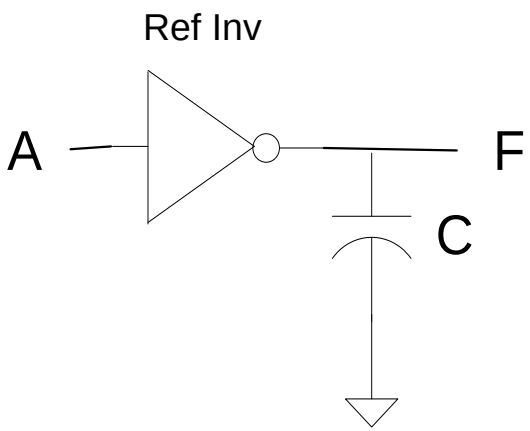
$$R_{PD}=\frac{L_1}{\mu_n C_{OX} W_1 (V_{DD}-V_{Tn})} \rightarrow R_{PDOD}=\frac{L_1}{\mu_n C_{OX} [OD \bullet W_1](V_{DD}-V_{Tn})}=\frac{R_{PD}}{OD}$$

$$R_{PU}=\frac{L_2}{\mu_p C_{OX} W_2 (V_{DD}+V_{Tp})} \rightarrow R_{PUOD}=\frac{L_2}{\mu_p C_{OX} [OD \bullet W_2](V_{DD}+V_{Tp})}=\frac{R_{PU}}{OD}$$

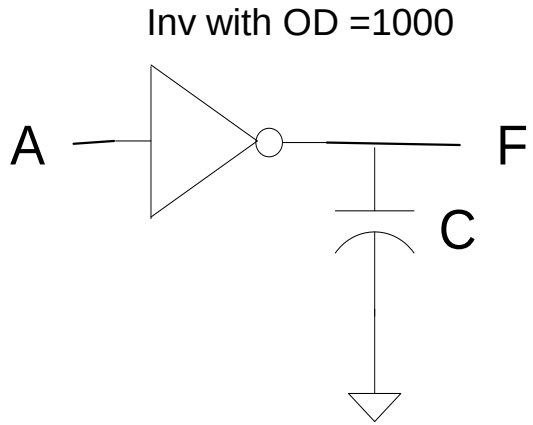
Scaling widths of ALL devices by constant will change FI by OD

$$C_{IN}=C_{OX}(W_1L_1+W_2L_2) \rightarrow C_{INOD}=C_{OX}([OD \bullet W_1]L_1+[OD \bullet W_2]L_2)=OD \bullet C_{IN}$$

Overdrive Factors



t_{PROP}=50nsec



t_{PROP}=?

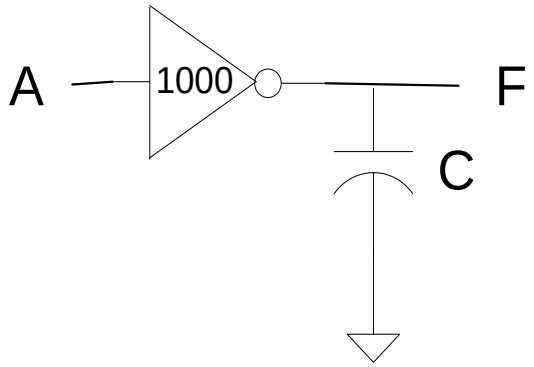
Example: Determine t_{prop} in 0.5u process if C=10pF and OD=1000

$$t_{PROP} = t_{REF} \bullet FI \bullet \frac{1}{OD} = t_{REF} \bullet \frac{10\,pF}{4\,fF} = t_{REF} \bullet 2500$$

$$t_{PROP} = t_{REF} \bullet FI \bullet \frac{1}{OD} = t_{REF} \bullet \frac{10\,pF}{4\,fF} \bullet \frac{1}{1000} = t_{REF} \bullet 2.5$$

Note sizing the inverter with the OD improved delay by a factor of 1000 !

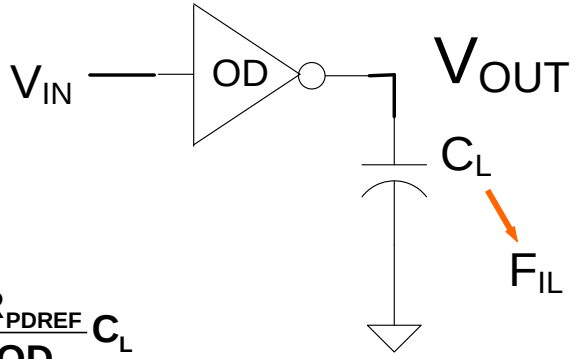
Overdrive Factors



- **By definition, the factor by which the W/L of all devices are scaled above those of the reference inverter is termed the overdrive factor, OD**
- **Scaling widths by overdrive factor DECREASES resistance by same factor**
- **Scaling all widths by a constant does not compromise the symmetry between the rise and fall times (i.e. $t_{HL}=t_{LH}$)**
- **Judicious use of overdrive can dramatically improve the speed of digital circuits**
- **Large overdrive factors are often used**
- **Scaling widths by overdrive factor INCREASES input capacitance by same factor - So is there any net gain in speed?**

Propagation Delay with Over-drive Capability

Overdrive



$$t_{HL}=t_{LH}=\frac{R_{PDREF}}{OD}C_L$$

$$t_{PROP}=t_{HL}+t_{LH}=2\frac{R_{PDREF}C_L}{OD}=\frac{t_{REF}}{OD}$$

Asymmetric Overdrive

Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

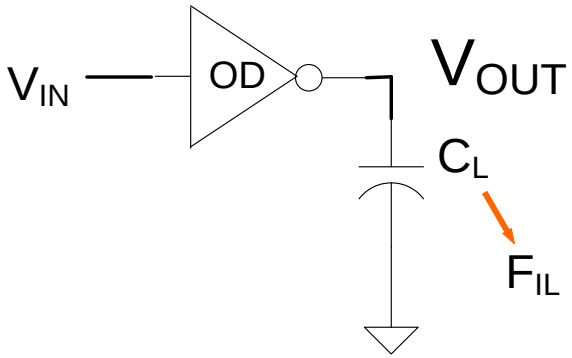
$$R_{PDEFF}=\frac{R_{PDREF}}{OD_{HL}} \qquad R_{PUEFF}=\frac{R_{PUREF}}{OD_{LH}}$$

$$t_{HL}=\frac{R_{PDREF}}{OD_{HL}}C_L \qquad t_{LH}=\frac{R_{PDREF}}{OD_{LH}}C_L$$

$$t_{PROP}=t_{HL}+t_{LH}=\frac{R_{PDREF}}{OD_{HL}}C_L+\frac{R_{PDREF}}{OD_{LH}}C_L=R_{PDREF}C_L\left[\frac{1}{OD_{HL}}+\frac{1}{OD_{LH}}\right]=\frac{t_{REF}}{2}\left[\frac{1}{OD_{HL}}+\frac{1}{OD_{LH}}\right]F_{IL}$$

Propagation Delay with Over-drive Capability

Overdrive



If inverter with OD is sized for equal rise/fall, $OD_{HL}=OD_{LH}=OD$

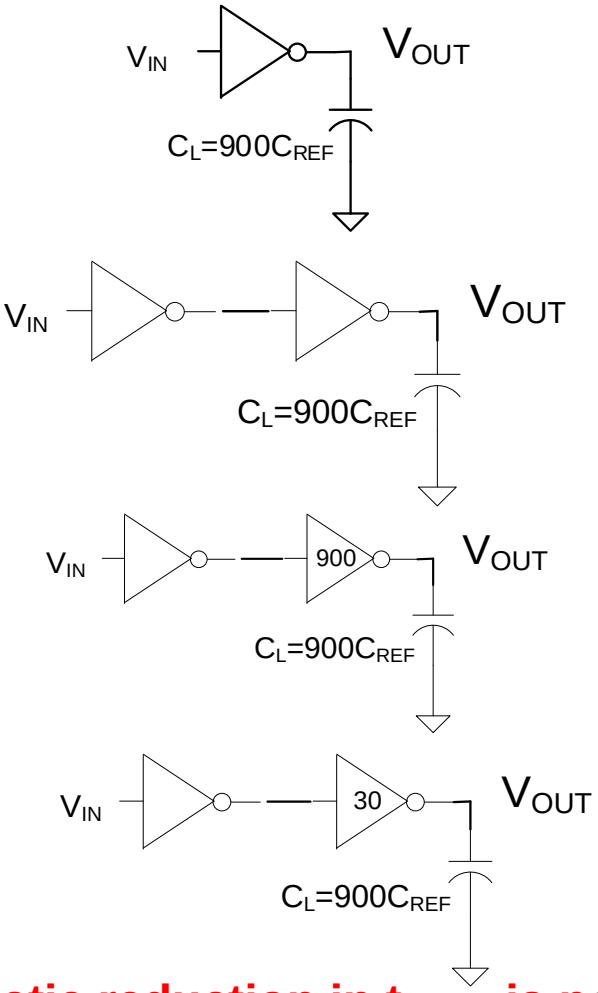
$$t_{PROP}=R_{PDREF}C_L\left[\frac{1}{OD_{HL}}+\frac{1}{OD_{LH}}\right]=R_{PDREF}C_L\frac{2}{OD}=t_{REF}\frac{F_{IL}}{OD}$$

OD may be larger or smaller than 1

Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don't worry about the extra inversion at this time.



$$t_{PROP}=900t_{REF}$$

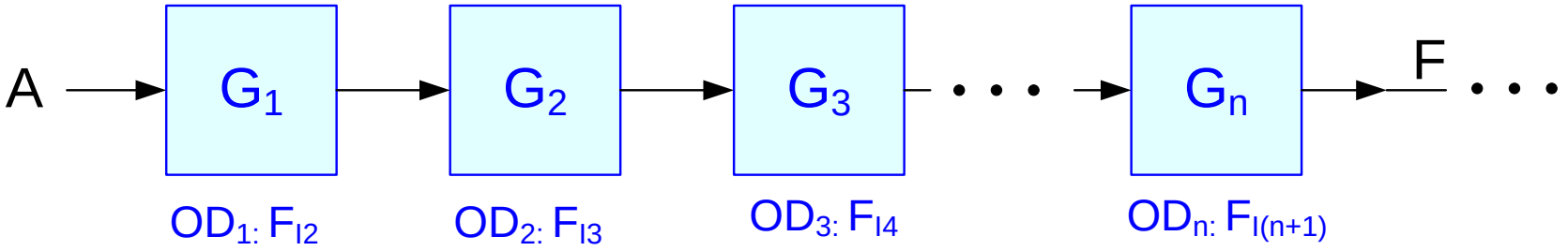
$$t_{PROP}=t_{REF}+900t_{REF}=901t_{REF}$$

$$t_{PROP}=900t_{REF}+t_{REF}=901t_{REF}$$

$$t_{PROP}=30t_{REF}+30t_{REF}=60t_{REF}$$

- **Dramatic reduction in t_{PROP} is possible** (input is driving same in last 3 cases)
- **Will later determine what optimal number of stages and sizing is**

Propagation Delay in Multiple-Levels of Logic with Stage Loading



F_{Ik} denotes the total loading on stage k which is the sum of the F_I of all loading on stage k

Summary: Propagation delay from A to F:

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

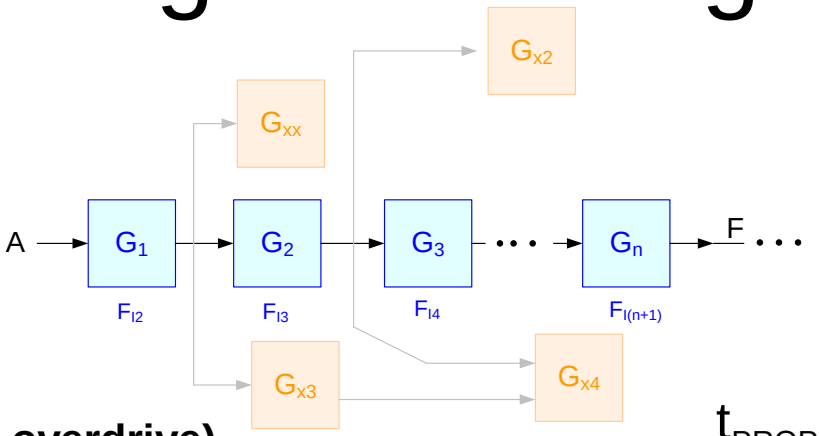
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- **Equal rise/fall (no overdrive)**
- **Equal rise/fall with overdrive**
- **Asymmetric Overdrive**
- **Minimum Sized**
- **Combination of equal rise/fall, minimum size and overdrive**

Will develop the analysis methods as needed

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Asymmetric overdrive**

$$t_{PROP} = \ ?$$

- **Minimum Sized**

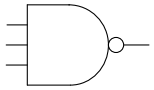
$$t_{PROP} = \ ?$$

- **Combination of equal rise/fall, minimum size and overdrive**

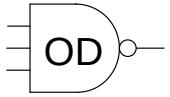
$$t_{PROP} = \ ?$$

Driving Notation

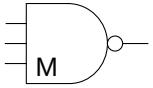
- **Equal rise/fall (no overdrive)**



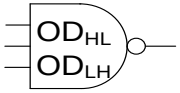
- **Equal rise/fall with overdrive**



- **Minimum Sized**



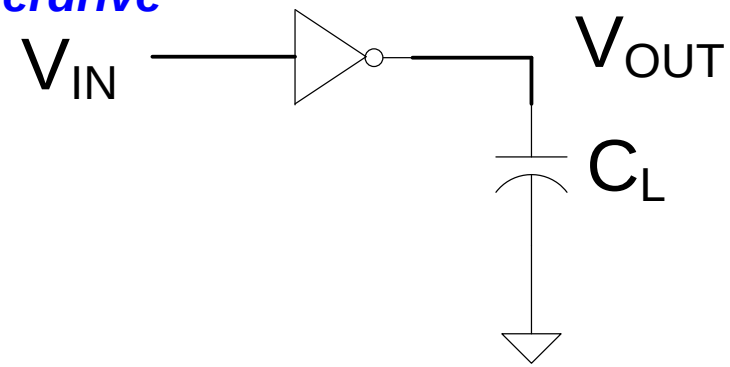
- **Asymmetric Overdrive**



Notation will be used only if it is not clear from the context what sizing is being used

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive



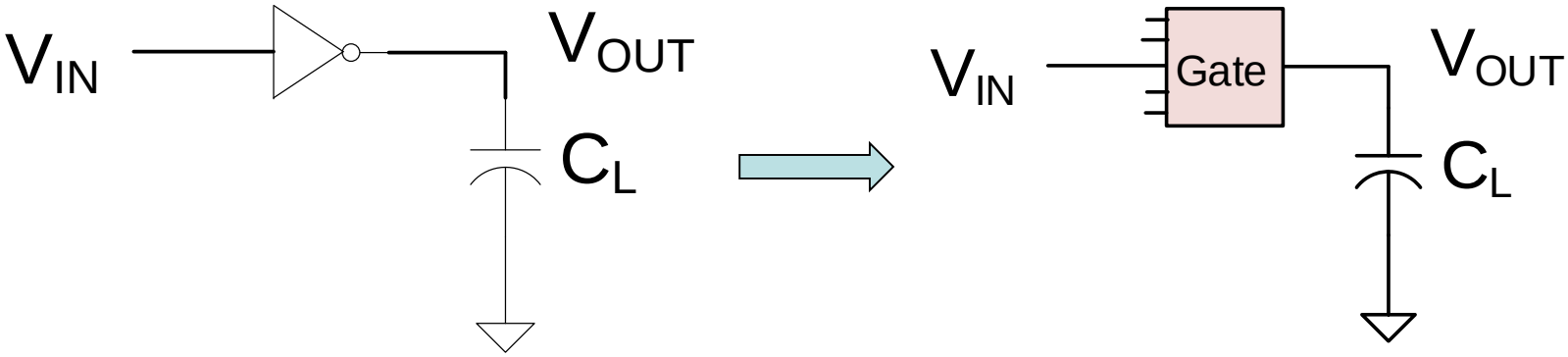
Recall:

Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

$$R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \qquad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive



Recall:

$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

If inverter is not equal rise/fall

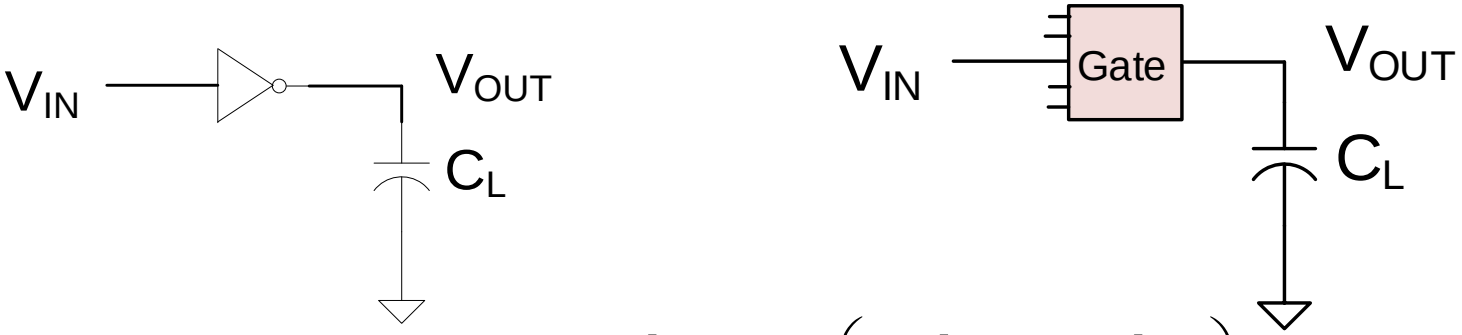
$$t_{HL} = \frac{R_{PDREF}}{OD_{HL}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{HL}}$$

$$t_{LH} = \frac{R_{PUREF}}{OD_{LH}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{LH}}$$

$$t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left(\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right)$$

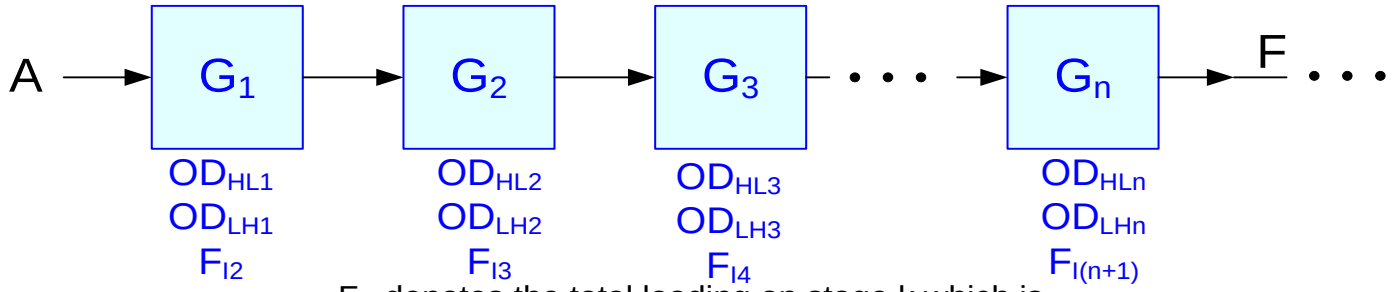
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive



$$t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left(\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right)$$

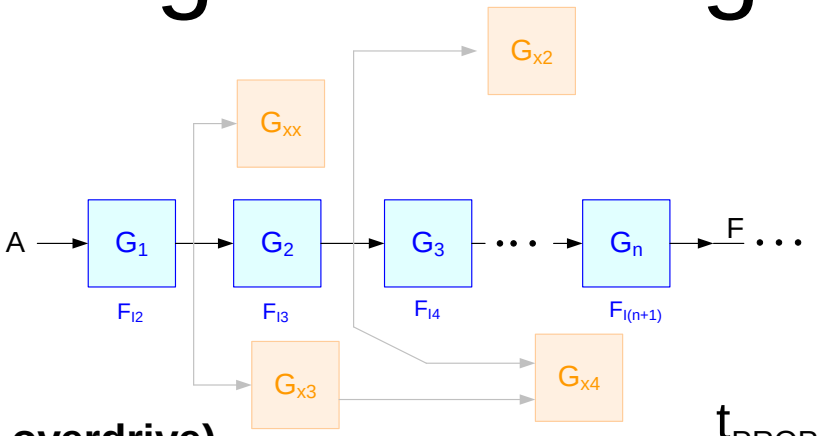
When propagating through n stages:



F_{Ik} denotes the total loading on stage k which is the sum of the F_I of all loading on stage k

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Asymmetric overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Minimum Sized**

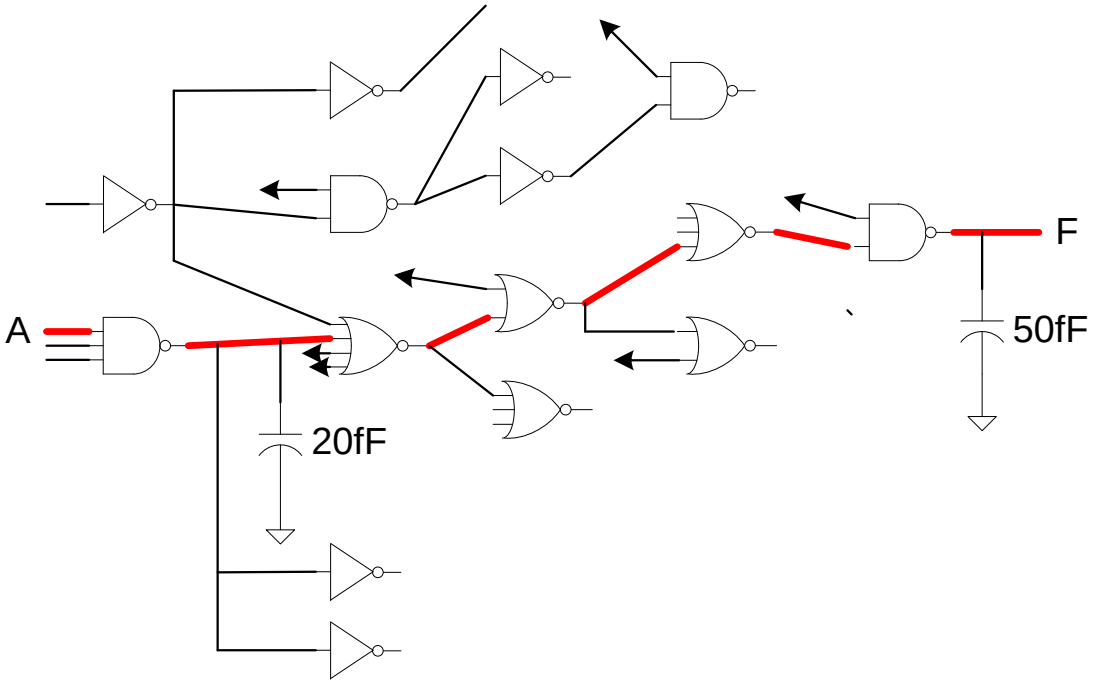
$$t_{PROP} = \ ?$$

- **Combination of equal rise/fall, minimum size and overdrive**

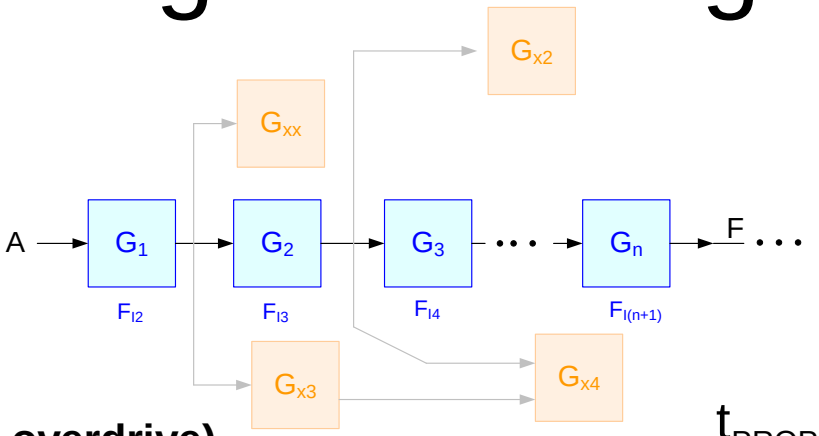
$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading and Overdrives

Will now consider A to F propagation for this circuit as an example with different overdrives



Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Asymmetric overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Minimum Sized**

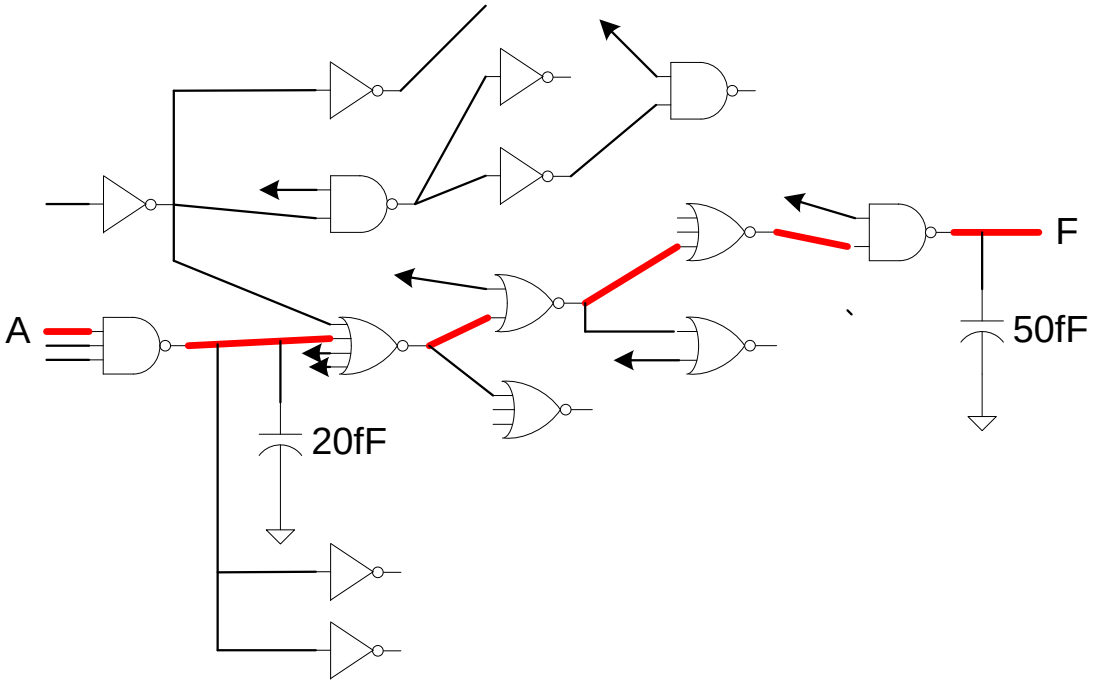
$$t_{PROP} = \ ?$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive



$$t_{REF} = 2t_{HL_{REF}}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I_{k+1}}$$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive

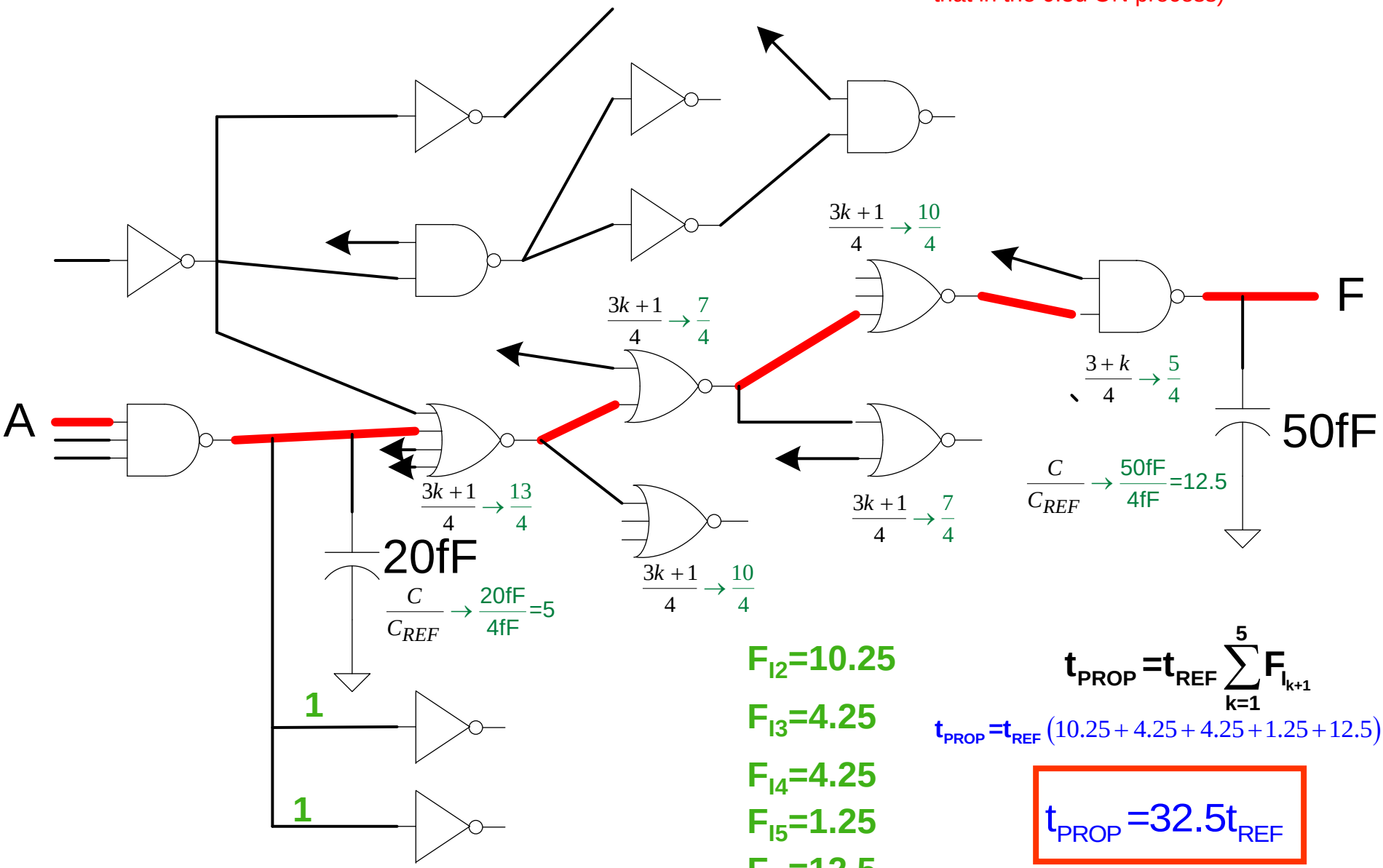
	Equal Rise/Fall
C_{IN}/C_{REF}	
Inverter	1
NOR	$\frac{3k+1}{4}$
NAND	$\frac{3+k}{4}$
Overdrive	
Inverter	
HL	1
LH	1
NOR	
HL	1
LH	1
NAND	
HL	1
LH	1
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$

$$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{I_{k+1}}$$

Equal rise-fall gates, no overdrive

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



F_{I2}=10.25

F_{I3}=4.25

F_{I4}=4.25

F_{I5}=1.25

F_{I6}=12.5

$$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{I_{k+1}}$$

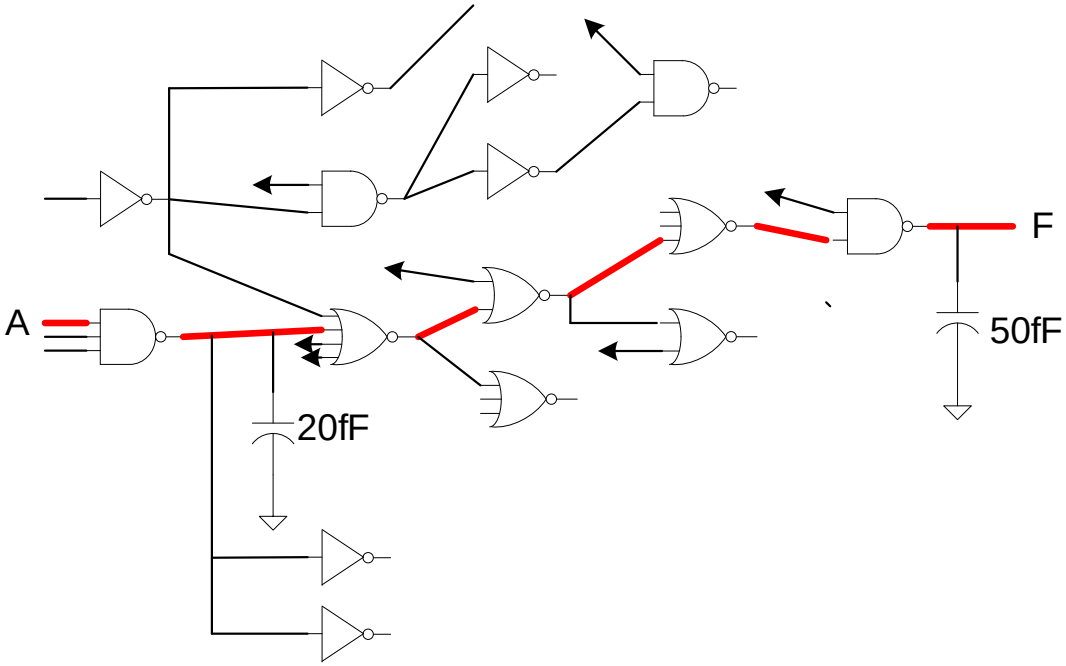
$$t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)$$

$$t_{PROP} = 32.5 t_{REF}$$

Equal rise-fall gates, no overdrive

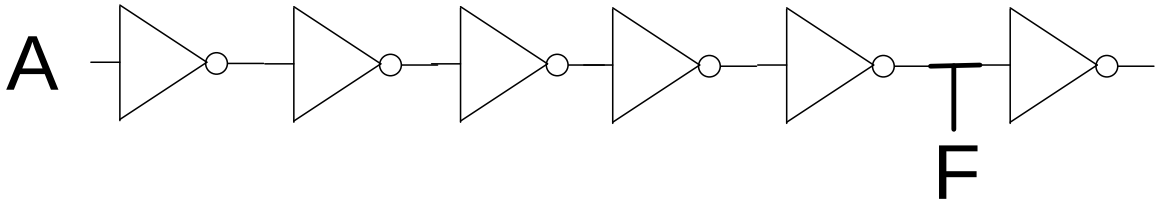
In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



$t_{PROP}=32.5t_{REF}$

How does this propagation delay compare to that required for a propagation of a signal through 5-levels of logic with only reference inverters?

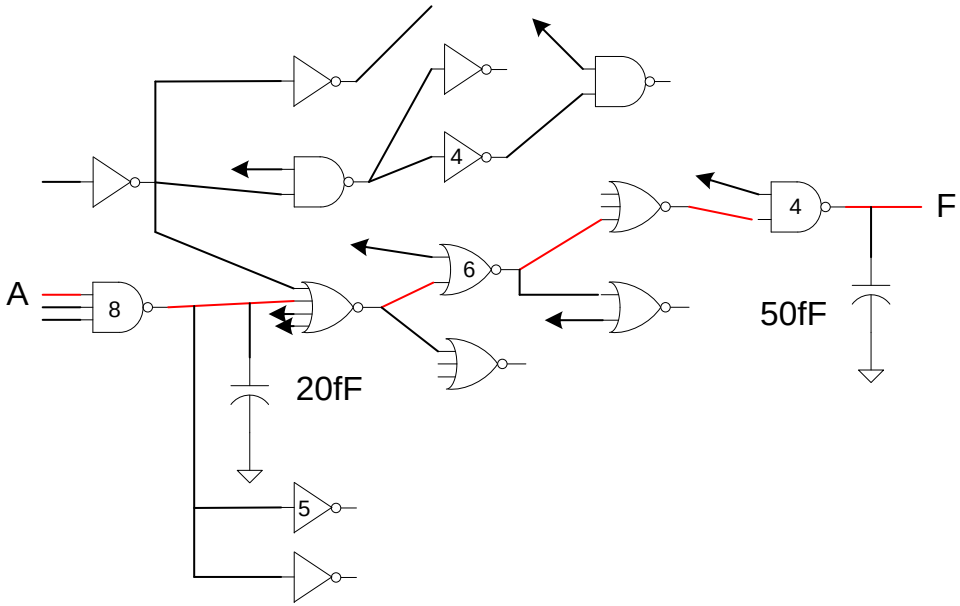


$t_{PROP}=5t_{REF}$

Loading can have a dramatic effect on propagation delay

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive



In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I_{k+1}}}{OD_k}$$

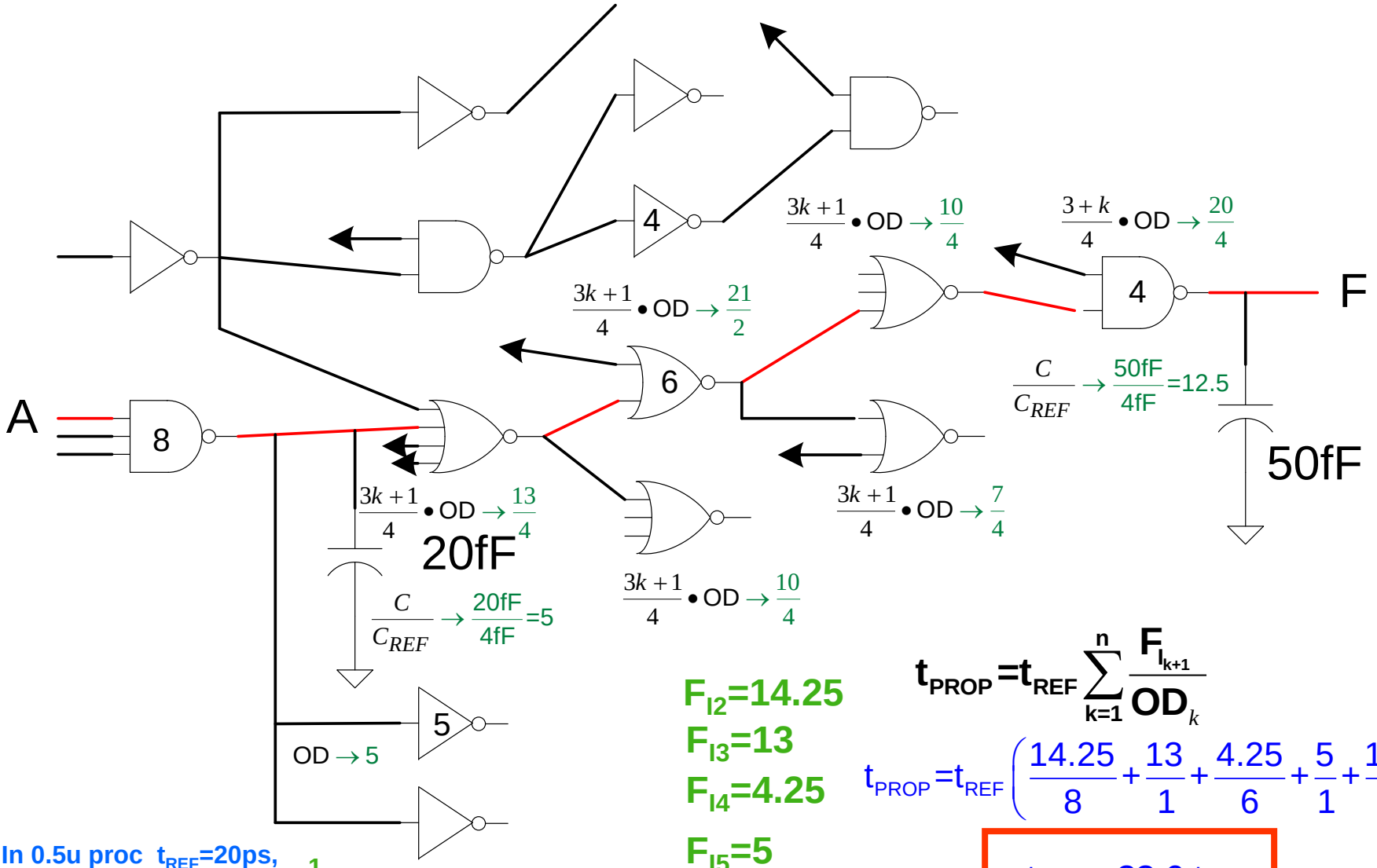
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

	Equal Rise/Fall	Equal Rise/Fall (with OD)
C_{IN}/C_{REF}		
Inverter	1	OD
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$
Overdrive		
Inverter		
HL	1	OD
LH	1	OD
NOR		
HL	1	OD
LH	1	OD
NAND		
HL	1	OD
LH	1	OD
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I_{k+1}}}{OD_k}$$

Equal rise-fall gates, with overdrive



$F_{I2}=14.25$

$F_{I3}=13$

$F_{I4}=4.25$

$F_{I5}=5$

$F_{I6}=12.5$

$$t_{PROP}=t_{REF}\sum_{k=1}^{n}\frac{F_{I_{k+1}}}{OD_k}$$

$$t_{PROP}=t_{REF}\left(\frac{14.25}{8}+\frac{13}{1}+\frac{4.25}{6}+\frac{5}{1}+\frac{12.5}{4}\right)$$

$$t_{PROP}=23.6\ t_{REF}$$

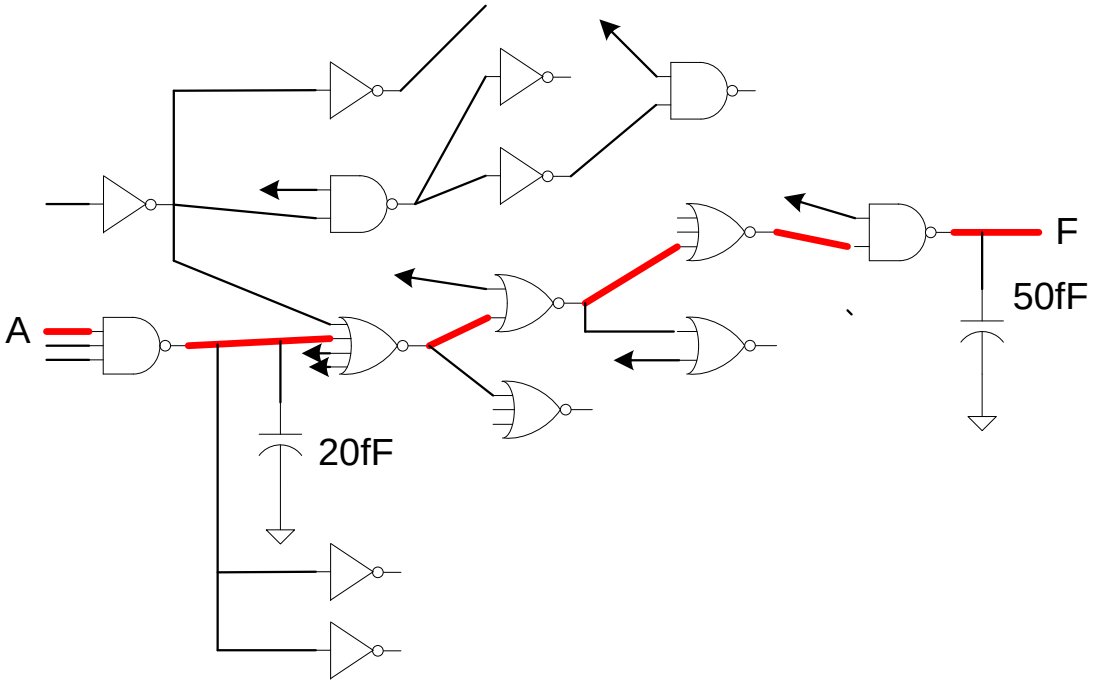
In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

1

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates



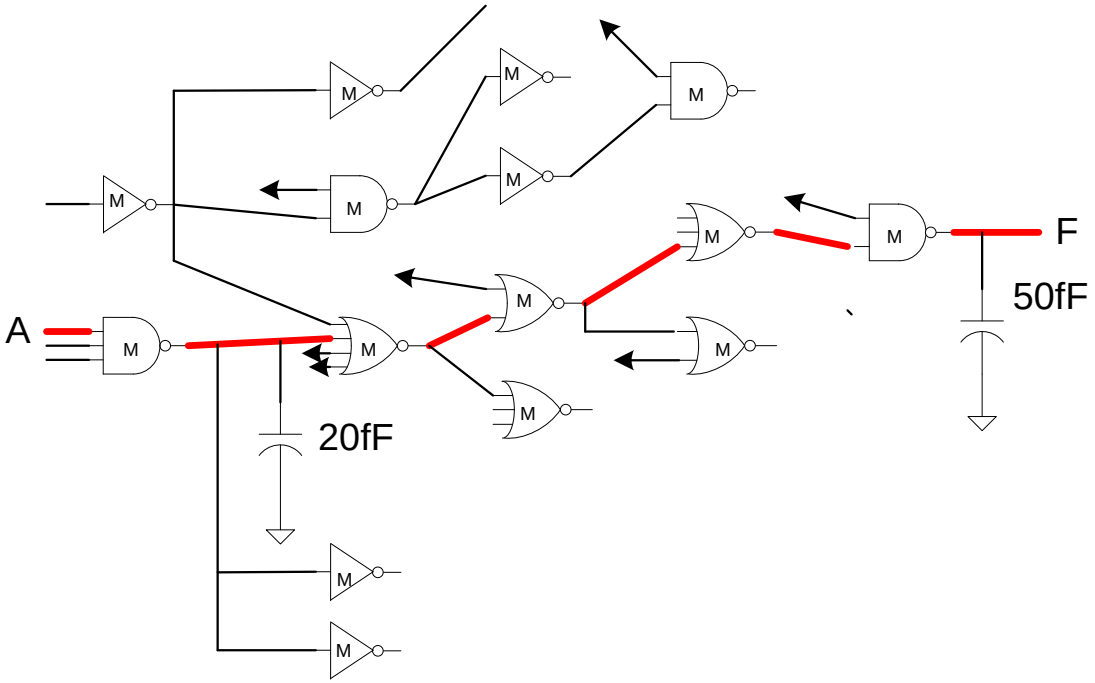
In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

$$t_{PROP} = t_{REF} \bullet ?$$

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

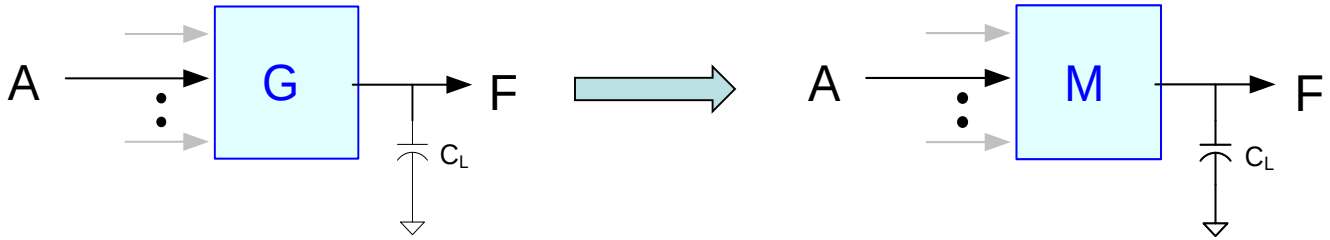


$$t_{PROP} = t_{REF} \bullet ?$$

Observe that a minimum-sized gate is simply a gate with asymmetric overdrive

Recall:

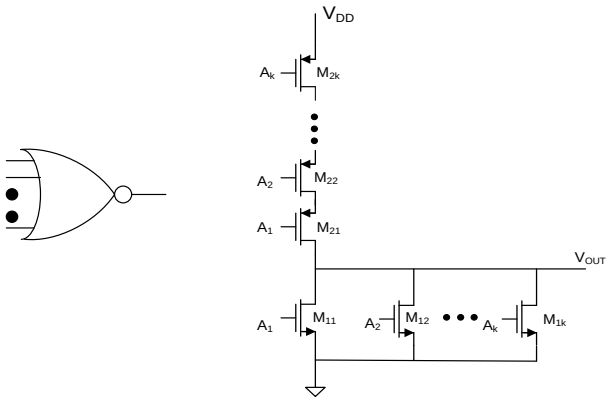
Propagation Delay with Minimum-Sized Gates

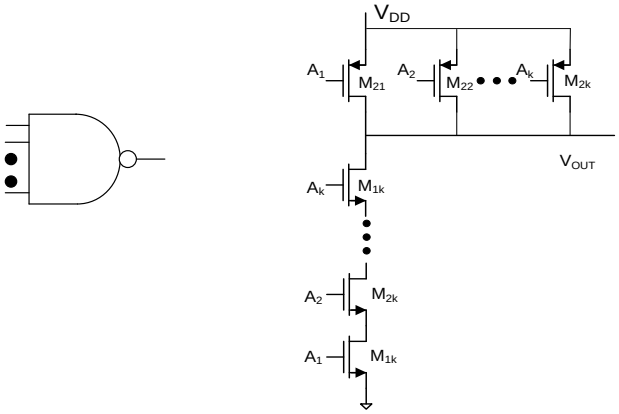


$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Still need OD_{HL} and OD_{LH} for minimum-sized gates**
- **Still need F_I**

Propagation Delay with minimum-sized gates





$OD_{HL}=?$

$OD_{HL}=1$

$OD_{LH}=?$

$OD_{LH}=\frac{1}{3k}$

$OD_{HL}=?$

$OD_{HL}=1/k$

$OD_{LH}=?$

$OD_{LH}=\frac{1}{3}$

$$FI=2C_{OX}W_{MIN}L_{MIN}$$

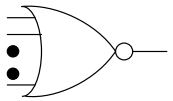
$$C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

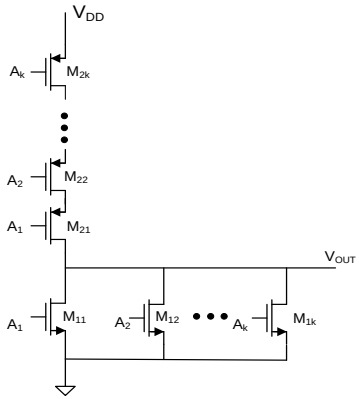
$$FI=\frac{C_{REF}}{2}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

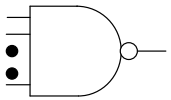
	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
C_{IN}/C_{REF}			
Inverter	1	OD	
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	
Overdrive			
Inverter			
HL	1	OD	
LH	1	OD	
NOR			
HL	1	OD	
LH	1	OD	
NAND			
HL	1	OD	
LH	1	OD	
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	

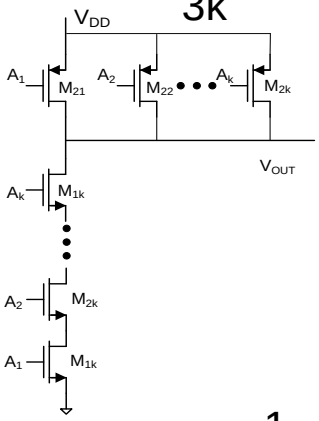




$OD_{HL}=1$

$OD_{LH}=\frac{1}{3k}$





$OD_{HL}=1/k$

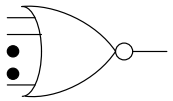
$OD_{LH}=\frac{1}{3}$

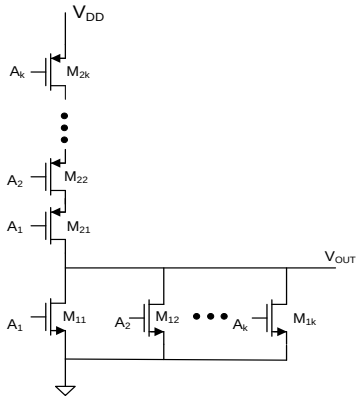
$FI=\frac{C_{REF}}{2}$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

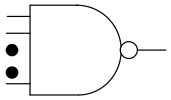
Minimum-sized gates

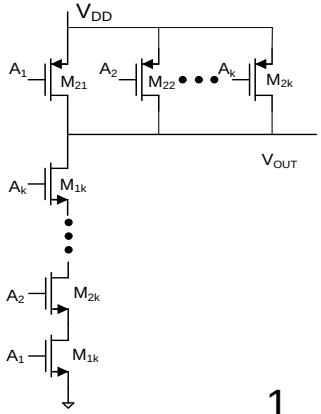
	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
C_{IN}/C_{REF}			
Inverter	1	OD	1/2
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2
Overdrive			
Inverter			
HL	1	OD	1
LH	1	OD	1/3
NOR			
HL	1	OD	1
LH	1	OD	1/(3k)
NAND			
HL	1	OD	1/k
LH	1	OD	1/3
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$





$OD_{HL}=1$ $\quad OD_{LH}=\frac{1}{3k}$

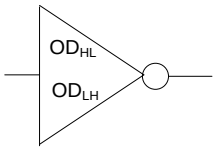




$OD_{HL}=1/k$ $\quad OD_{LH}=\frac{1}{3}$

$FI=\frac{C_{REF}}{2}$

Minimum-sized gates



$F_{I2}=13/2$

$F_{I3}=1$

$F_{I4}=1$

$F_{I5}=1/2$

$F_{I6}=12.5$

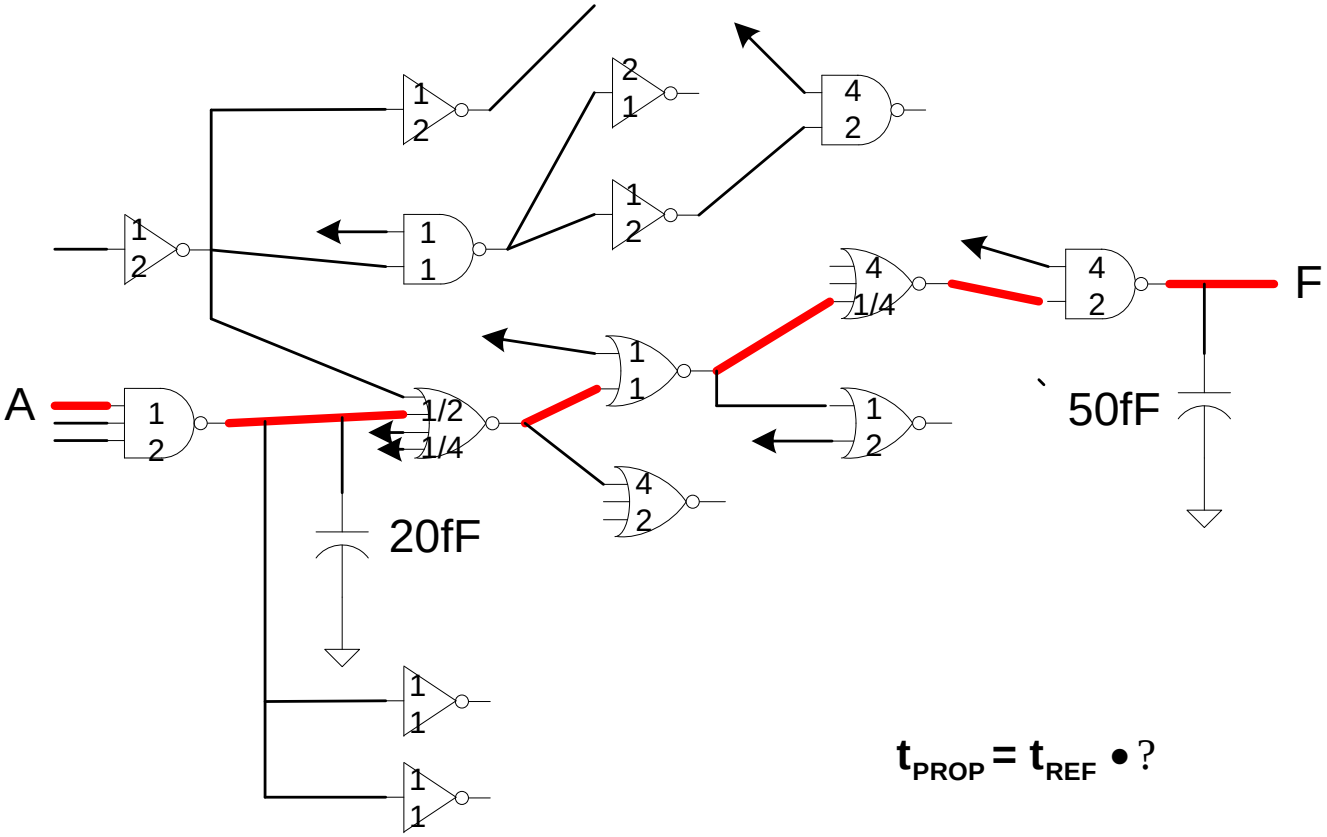
$$t_{PROP}=t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

$$t_{PROP}=t_{REF} \bullet \frac{1}{2}\left(\frac{13}{2}(3+3)+1(12+1)+1(6+10)+\frac{1}{2}(9+1)+12.5(2+3) \right)$$

$$t_{PROP}=63.25 \bullet t_{REF}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

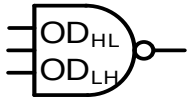
Asymmetric-sized gates



$t_{PROP} = t_{REF} \bullet ?$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

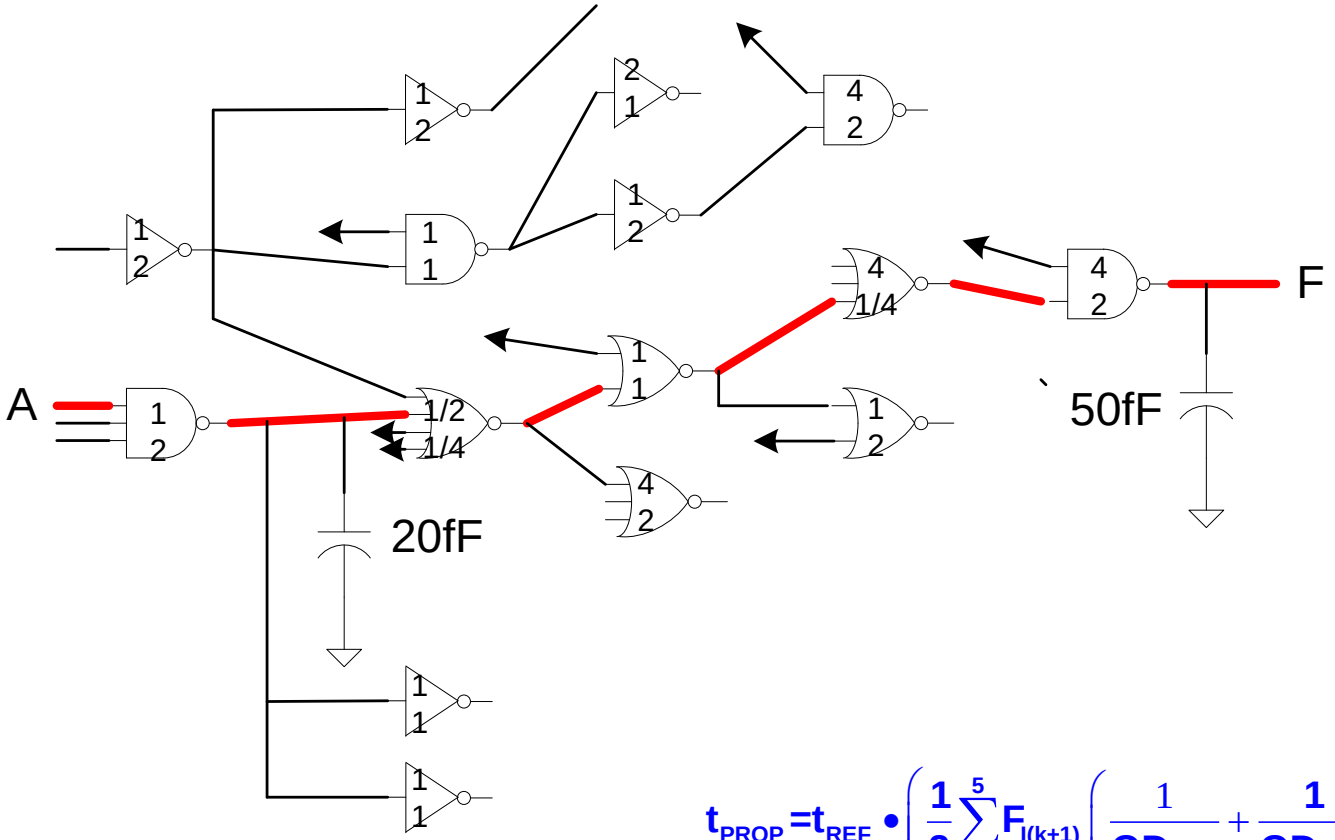


	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2}\sum_{k=1}^{5} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)\right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

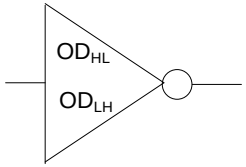
Asymmetric-sized gates



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

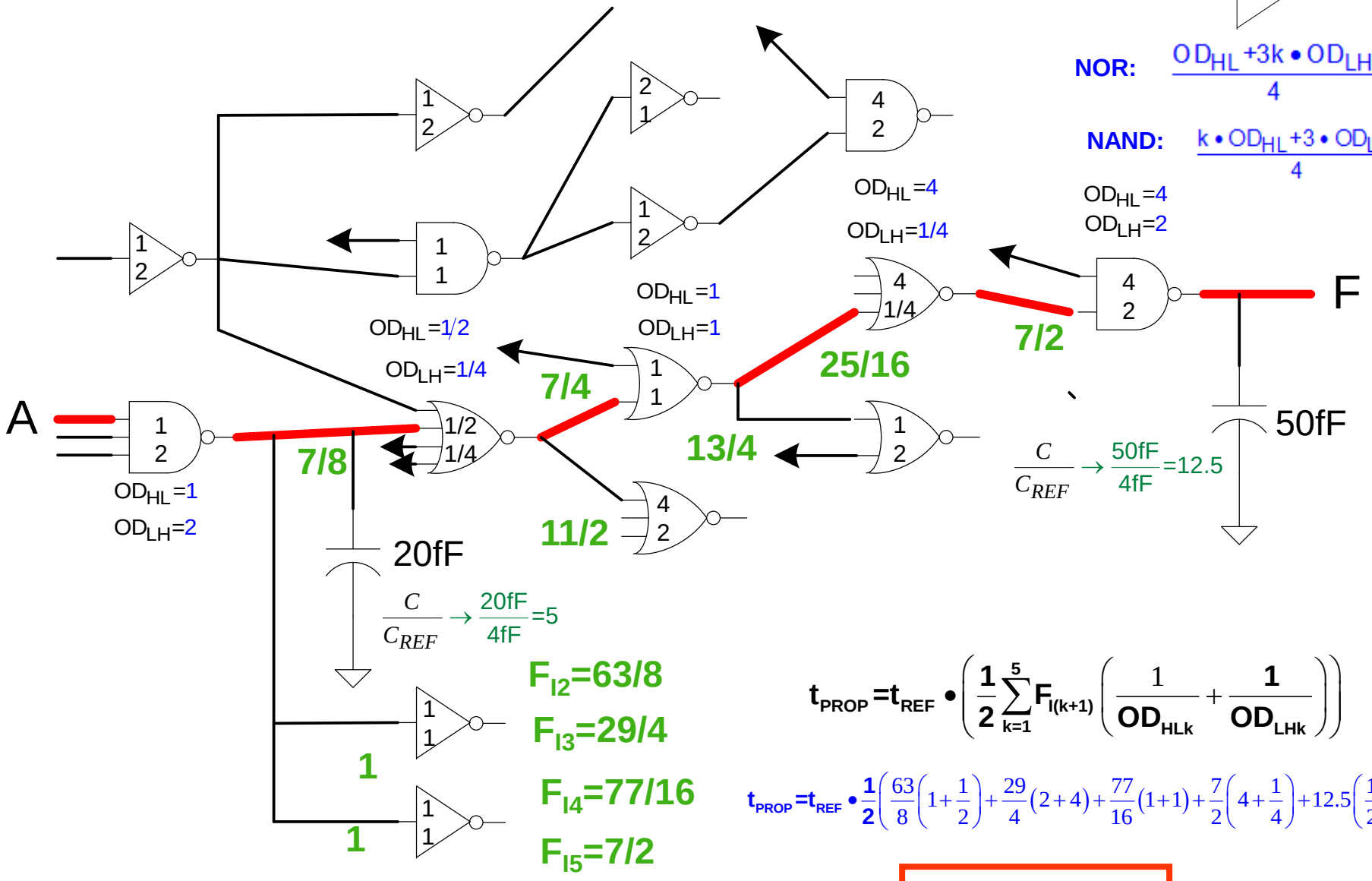
Asymmetric-sized gates

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



NOR: $\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$

NAND: $\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

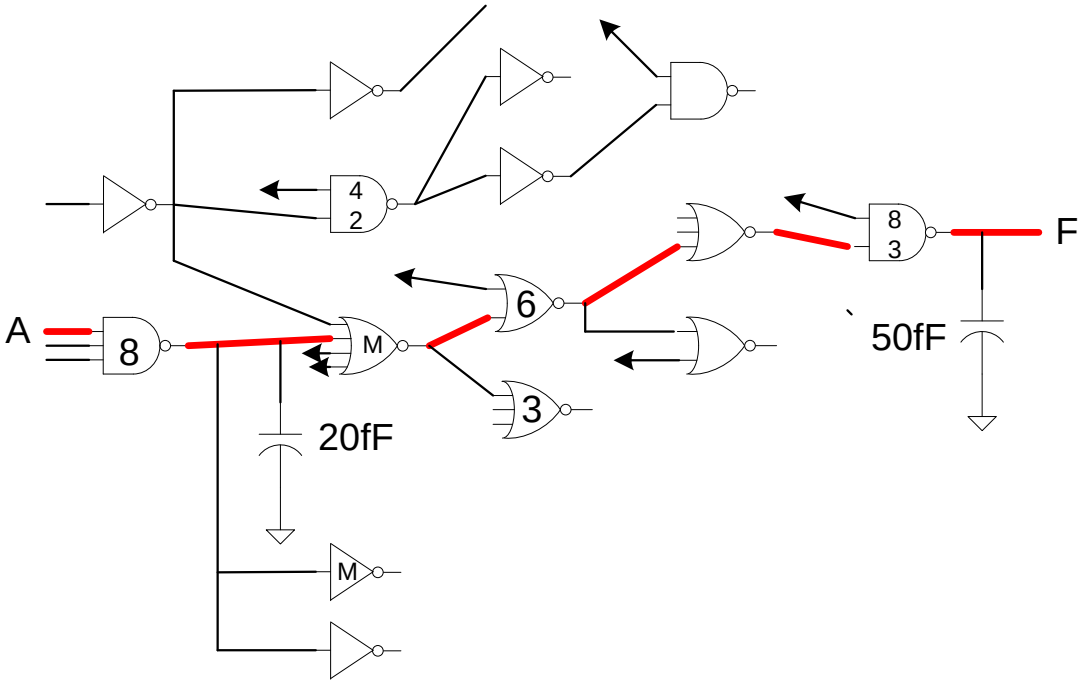
$$t_{PROP} = t_{REF} \bullet \frac{1}{2}\left(\frac{63}{8}\left(1+\frac{1}{2}\right) + \frac{29}{4}(2+4) + \frac{77}{16}(1+1) + \frac{7}{2}\left(4+\frac{1}{4}\right) + 12.5\left(\frac{1}{2}+\frac{1}{4}\right) \right)$$

$t_{PROP} = t_{REF} \bullet ?$

$t_{PROP} = 44.6 \bullet t_{REF}$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

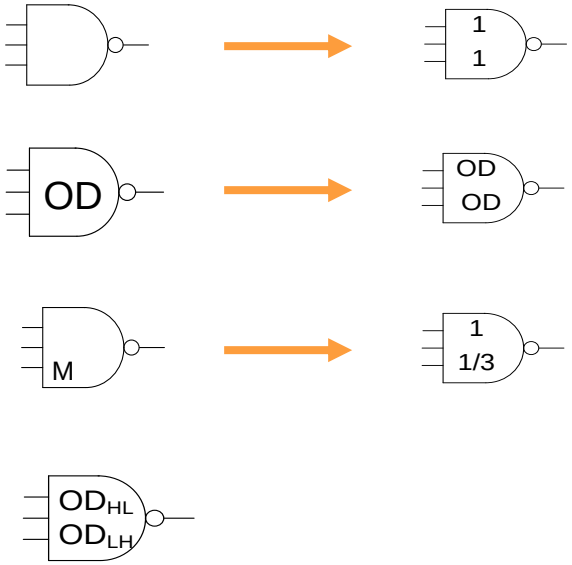
Mixture of Minimum-sized gates, equal rise/fall gates and OD



$t_{PROP} = t_{REF} \bullet ?$

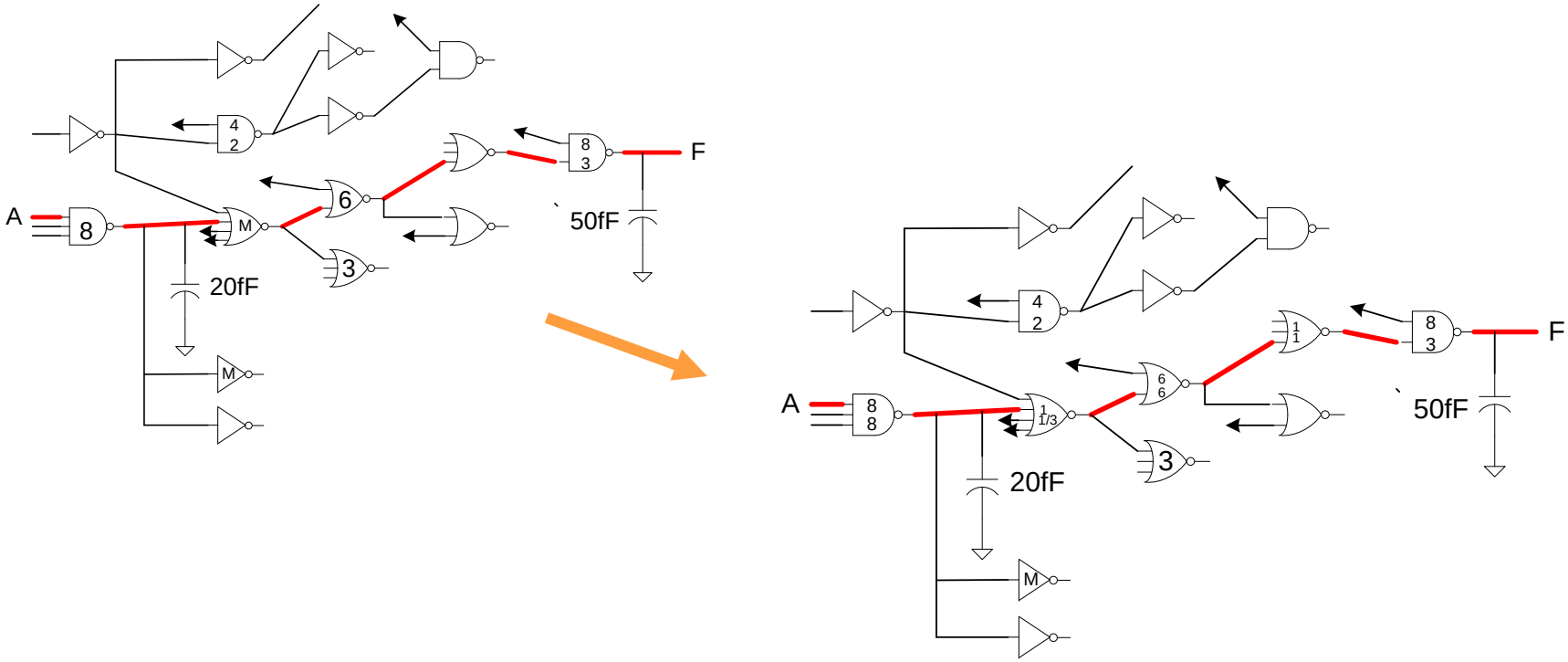
Driving Notation

- **Equal rise/fall (no overdrive)**
- **Equal rise/fall with overdrive**
- **Minimum Sized**
- **Asymmetric Overdrive**



Propagation Delay in Multiple-Levels of Logic with Stage Loading

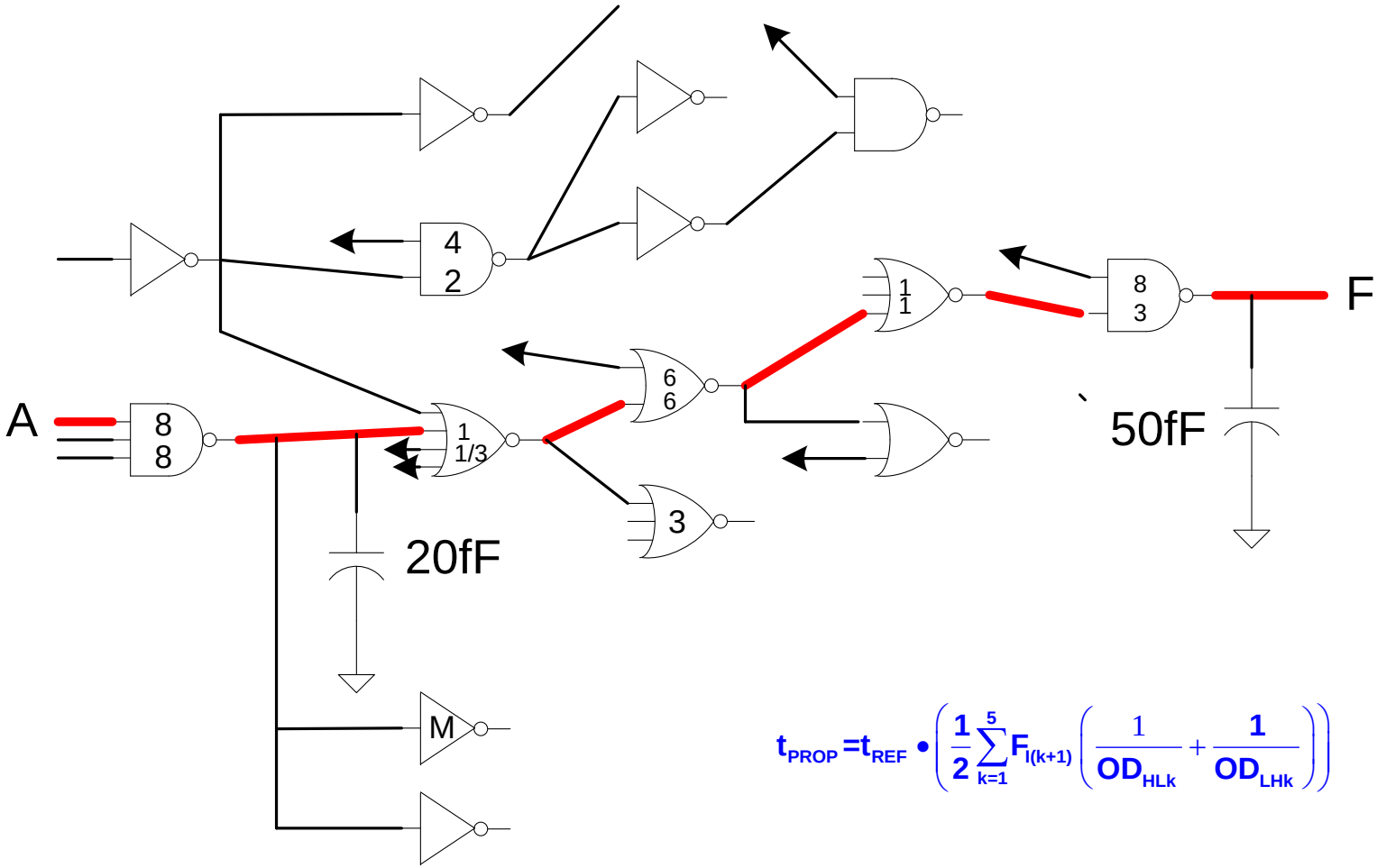
Mixture of Minimum-sized gates, equal rise/fall gates and OD



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

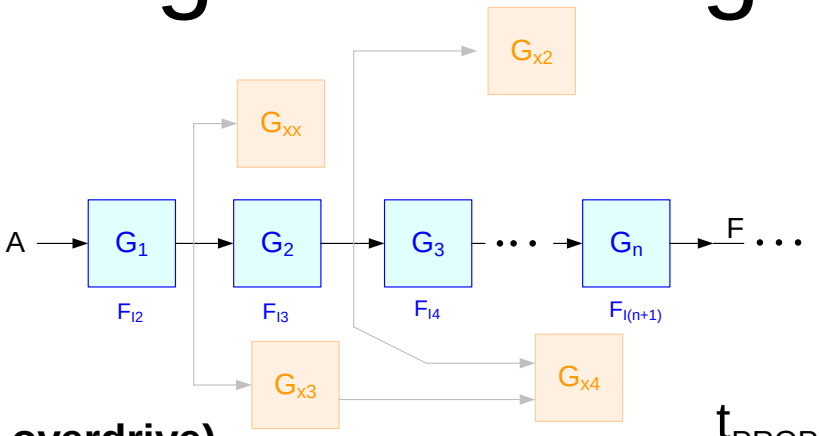
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Mixture of Minimum-sized gates, equal rise/fall gates and OD



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

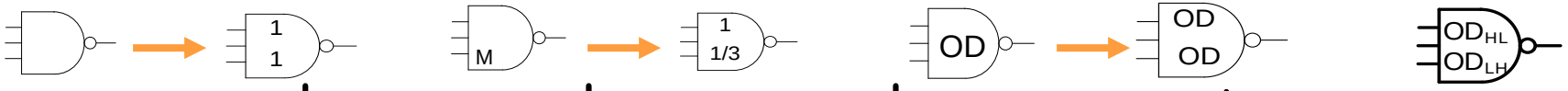
- **Asymmetric overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Summary: Propagation Delay in Multiple-Levels of Logic with Stage Loading



	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

End of Lecture 42