CprE 381: Computer Organization and Assembly Level Programming

Exam 3 Review

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Administrative

- Part 4 due in lab this week
  - WARNING: No work accepted after Midnight tonight

- Please take online course assessment

Concept Map In-Class Assessment

- Help you connect **new information** to your existing knowledge
- Deepen **understanding** and **comprehension**
- Important for this class:
  - Organize the relatively broad topics covered in lecture and homework
  - Help me understand how you are conceptualizing the content of the course
  - Will continue to use during exam reviews

Concept Map In-Class Assessment

1. Brainstorm concepts relating to main concept
2. Organize into categories
3. Draw arrows between related categories (and main concept)
   - Label the connections as well

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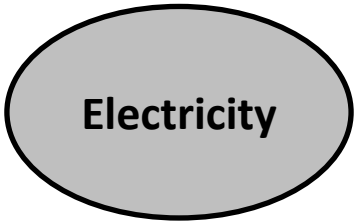

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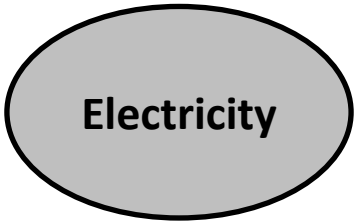
- Energy
- Lightning
- Generator
- Solar panel
- Power
- Computers



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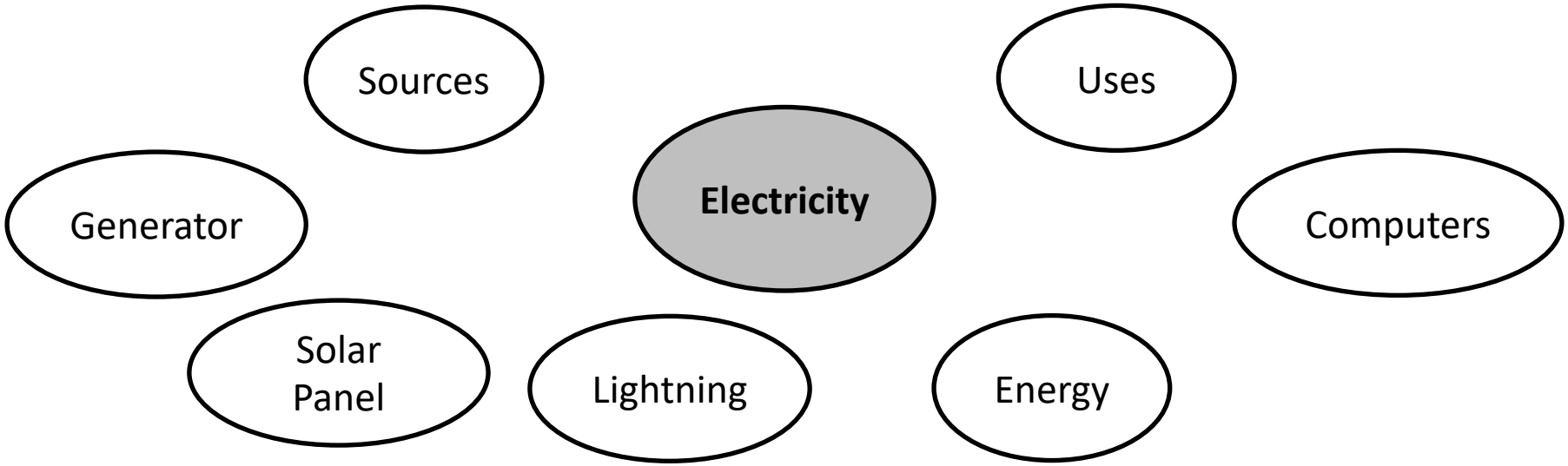

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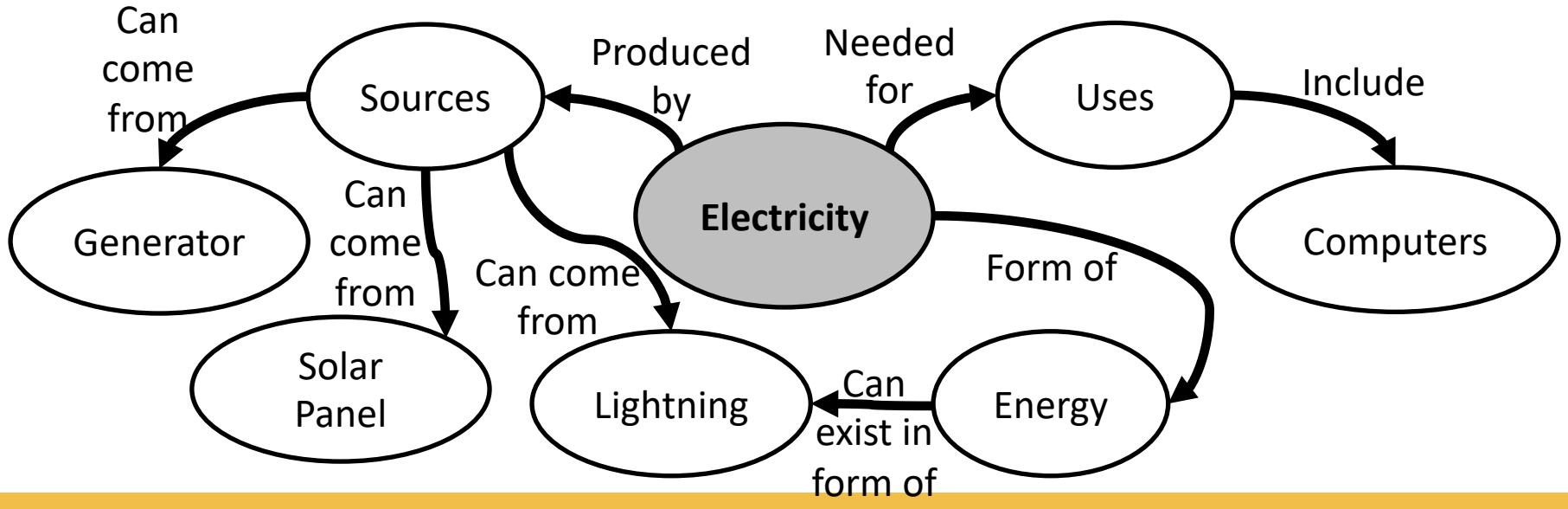

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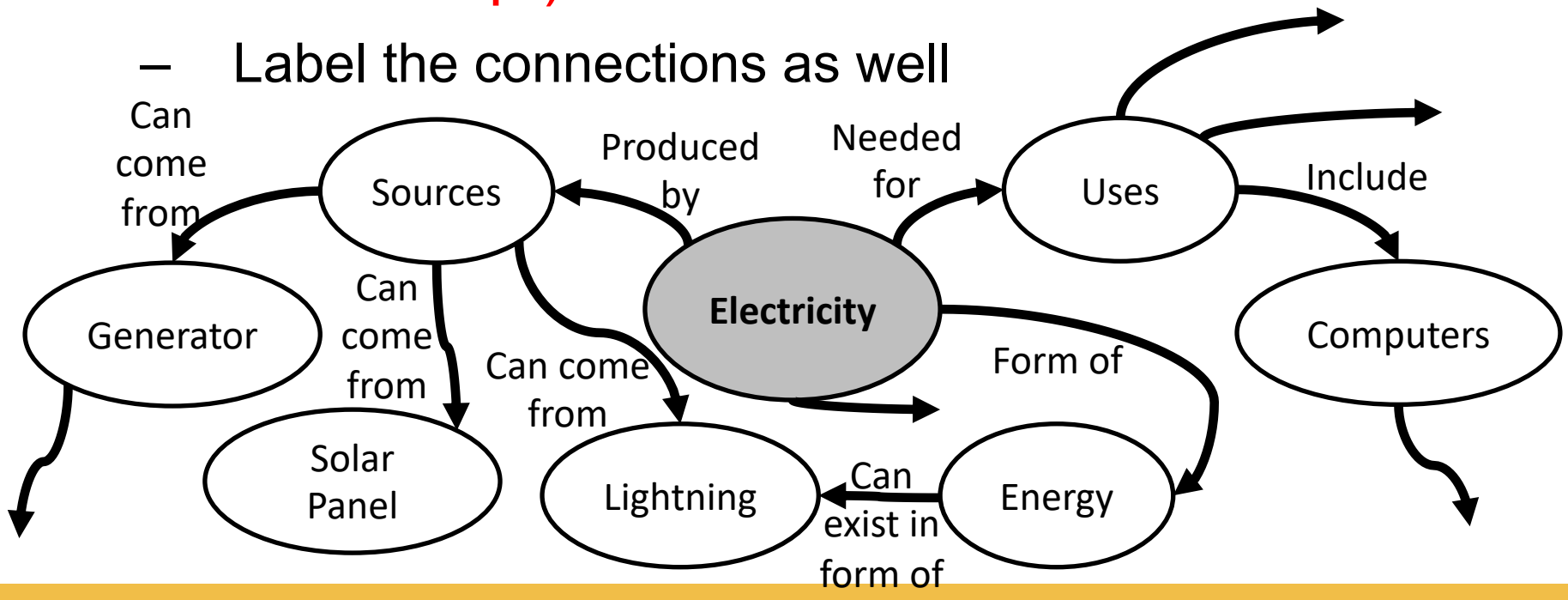

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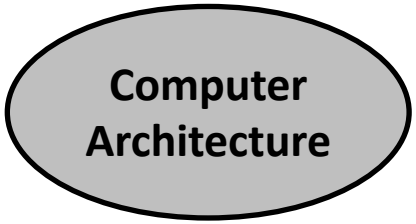
Your 

turn

Exam 3

- Final Exam
  - When: Mon May 6 at 7:30am
  - Where: Marston 2155 (everyone)
  - What: Data forwarding and controla hazards through HW security
    - Note that understanding these topics requires knowledge of previous material (e.g., MIPS ISA, binary, and pipelines)
  - Aids:
    - 1 8.5”x11” notes sheet; double-sided; self-generated; handwritten
    - No electronic devices, including calculators
    - Copy of green sheet will be provided on exam
  - TODOs:
    - Review in-class assessments, HWs, P&H exercises, labs, lecture slides, readings
    - Ask questions here, OH at 1:30pm, and on Canvas

Exam Focus

1. Data Hazard Avoidance (i.e., Forwarding)
2. Control Hazards
   - Branch Predictors
   - BTB
   - Performance impact
3. Memory Systems
   - Memory technology
   - ***Caching***
   - Performance impact
4. Advanced Material
   - GPUs, Multicores, SIMD, and TPU
   - HW Security

Conceptual Knowledge

- Data Forwarding
  - How many inputs does a forwarding mux on the input of EX1 have?
  - What are the possible sources of forwarding paths?
  - How many load use delay slots will various pipelines have?
  - How does forwarding impact performance?

Conceptual Knowledge

- Control Hazards
  - How can you flush the pipeline? How many cycles need to be flushed
  - What is a branch-delay slot?
  - How do control hazards impact performance?

Conceptual Knowledge

- Memory:
  - What is the syntax of load and store instructions in MIPS
  - How are addresses generated in MIPS processors?
  - What is the difference between a register and a memory location?
  - What are the general differences between SRAM, DRAM, and Flash/Disk storage?
    - Structural/functional differences
    - Performance differences
    - Capacity/density differences

Conceptual Knowledge

- Caches:
  - What are the two types of locality that applications have?
  - List the typical levels in a memory hierarchy. Which is fastest and which cheapest?
  - What is a direct mapped cache?
  - How does increasing the block size help? How does it harm?
  - How is the address broken into tag/index for a direct mapped cache?
  - Relationship of parameters: total data size, # ways, # sets, block size, # set index bits, # block offset bits, # tag bits, etc.

Conceptual Knowledge (cont.)

- Caches (cont.)
  - How is the address broken into tag/index for a fully associative cache?
  - What is a replacement policy?
  - What is the difference between a write-through and write-back cache?
  - What is the difference between write-allocate and write-no-allocate caches?
  - What are the trade-offs between the two policies?
  - What is the formula for AMAT?
  - What is the motivation in having separate instruction and data caches?

Conceptual Knowledge (cont.)

- GPUs
  - What kind of parallelism do GPUs take advantage of?
  - Where do GPUs fit within the taxonomy of processors (instruction and data streams)?
  - Why do we have both GPUs and CPUs in one system?
- HW Security
  - Why should a software engineer care about hardware security?
  - Describe the interaction between HW security and Branch Prediction/Exceptions/Caches/Virtual Memory.

Sample Exam Questions

- Look at the code snippet below

```
int grid[4][6];
for(k=0;k<N;k++)
   for(i=0;i<4;i++)
      for(j=0;j<6;j++)
         read(grid[i][j]);
```

- Assuming a direct mapped cache of 64 bytes with 4 word blocks, how many misses do you see? Assume `grid` is stored in row major order

Sample Exam Questions

- The latest processor in the market has two levels of data caches, with the characteristics shown below. You can also assume that it takes 50 clock cycles to request and complete a 32-byte transfer between main memory and the L2 cache.

- Find the average memory access time (AMAT) for both the L2 and L1 cache. Also find the number of storage bits required for each cache assuming 48 bit addresses.

Level	L1	L2
Data Size	32KB	256KB
Block Size	8bytes	32bytes
Associativity	1-way	4-way
Hit Time	1 cycle	19 cycles
Miss Rate	5%	2%

Sample Exam Questions

- Assuming our standard 5-stage pipeline, indicate all the control hazards in the code below

```
loop:  sub $t3, $t3, 1
       add $t0, $t0, 4
       add $t1, $a0, $t0
       lw   $t2, 0($t1)
       add $t2, $t2, 1
       sw   $t2, 0($t1)
       bgt $t3, $zero, loop
       sw   $t2, 0($t1)
```

- How many stalls does one iteration of the above loop incur? Assume branches are resolved in the decode stage.

Sample Exam Questions

- For this question, you are given a 16-byte cache (initially empty) and the sequence of memory accesses (byte loads) shown in the table.
  - For each of the following cache configurations, explain whether it can produce this sequence.
  - If so, what is the result of the last access (shown as ???) for each of the matching sequences?

addr	Hit/miss
0	(miss)
12	(miss)
1	(hit)
17	(miss)
15	(hit)
3	(miss)
7	(???)

1. 4-byte blocks, 2-way set-associative (e.g. 2 sets of 2 blocks each)
2. 4-byte blocks, direct-mapped (4 blocks)
3. 8-byte blocks, direct-mapped (2 blocks)
4. 4-byte blocks, fully associative (4 blocks)

Acknowledgments

- These slides contain material developed and copyright by:
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