2)

a. Which existing blocks (if any) can be used for this instruction?
    i. Data Memory address and read
    ii. Register file
b. Which new functional blocks (if any) do we need for this instruction?
    i. An extra address and read port for the data memory
    ii. An extra wire from instruction to data memory
    iii. Wire from datamem output 2 into ALU input B
    iv. 2 extra muxes for ALU inputs
c. What new signals do we need (if any) from the control unit to support this instruction?
    i. Another 2 mux selection control signals to choose between the datamem inputs to the alu or the conventional inputs

3) Only listing largest delay per section, assuming mux delay is due to propagation.

a.
    i. I-Mem => Reg Read => Mux => ALU
    200 + 90 + 20 + 90 = 420 ps
    ii. I-Mem => Reg Read => Mux => ALU=> D-Mem => Mux
    200 + 90 + 20 + 90 + 250 + 20 = 690 ps
    iii. I-Mem => Reg Read => Mux => ALU => Mux
    200 + 90 + 20 + 90 + 20 = 440 ps

b.
    1. Change memory addressing mode - Skips use of the ALU and its prerequisite mux, cutting out that latency entirely.
    2. Extra fast Adder - Reduces ALU latency, used in each max-path. Would only shorten the ALU time, not remove it.
    3. Control Unit - Latency overshadowed by that of the other components, does not end up affecting the end result.