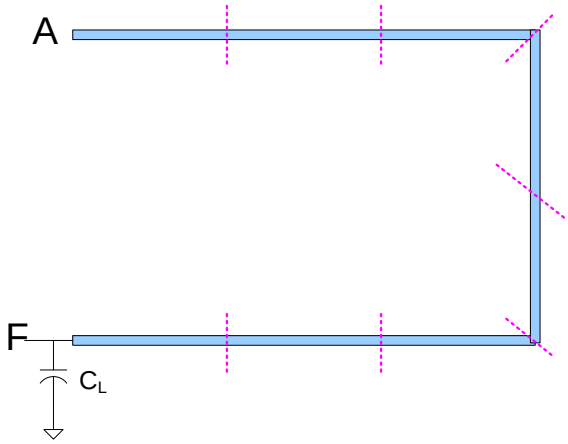
EE 330
Assignments 15
Spring 2018

This assignment will not be collected or graded. Even though the problems will not be collected, students are advised to work enough of them to have mastery of the material prior to looking at the posted solutions.

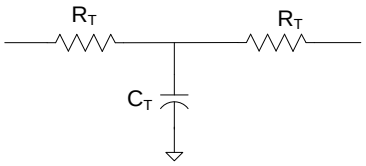
If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=350\mu A/v^2$,$\mu_p C_{OX}=70\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, $L_{MIN}=W_{MIN}=0.2\mu$, and $V_{DD}=2V$.

Problem 1 A poly interconnect that is 2u wide is used to connect a low impedance signal at node A to a 50fF load at node F as shown below. The distance between the dashed segments is 50u. Assume the capacitance density of this poly layer is .5fF/u^{2}and the sheet resistance of the poly is 20 ohms/square. Calculate the Elmore delay from A to F using a T-model for each of the 50u segments.



Problem 2 A poly interconnect that is 2u wide and 50u long is used to connect a low impedance signal to a 500fF load. Assume the capacitance density of this poly layer is .5fF/u^{2}and the sheet resistance of the poly is 20 ohms/square.

a) If this interconnect is modeled by the series connection of 4 T-connected segments shown, determine the value of the resistors R_T and the capacitor C_T in each of these segments.



b) Determine the Elmore delay associated with this interconnect model

c) Compare the Elmore delay with that obtained with a Spice simulation

Problem 3 A static CMOS implementation of an exclusive OR gate requires 29 transistors and requires 5 levels of logic.

a) How much can you reduce the number of transistors needed for a static CMOS implementation of the same function?

b) How much can you reduce the number of levels of logic needed for a static CMOS implementation?

Problem 4 A standard CMOS inverter with Wn=10u, Wp=40u, Ln=0.18u and Lp=0.18u is driving a 600fF capacitive load. Assume Cox for the process is $8fF/u^2$.

a) Determine the dynamic power dissipation in the inverter if the input to the inverter is a 10KHz square wave.
b) Repeat a) if Wn = Wp = 0.18u
c) How fast can the inverter be clocked if the original device sizes are used?

Problem 5 Determine the energy required to drive a minimum sized static CMOS inverter for a HL followed by a LH transition. From these results, make a prediction on the power level that would be expected in a system with 1million gates if half of the gates transitioned on each clock cycle and if all of the gates had an inupt capacitance equal to that of a minimum-sized inverter. Assume the clock of the system is 1.5GHz.

Problem 6 Determine the power that would be required in the final driver stage of a pad driver needed to drive a 25pF external load at 300MHz..

Problem 7 Assume a 32-bit data bus needs to go off-chip and that the average capacitance on each bit is 4pf. Determine the dynamic power dissipation in the last stage of a pad driver if the clock rate is 800MHz. Assume logic with V_H=2V, V_L=0V is being used and that, on the average, each bit changes once every other clock period.

Problem 8 Design a pad driver to drive a 32-bit data bus. Assume the load on the bus is 600fF and that the clock speed for data on the bus is 100MHz. The pad driver should be designed so to minimize the power dissipation in the pad driver while still meeting the 100MHz speed requirement.

Problem 9. What is the fastest clock that can be used in a 0.2u process if the clock must drive a 2pF load. Assume a standard pad driver structure is used to drive this load.

Problem 10 Consider the cascade of 3 inverters with a 50fF load on the last stage.

a) Determine the propagation delay if the devices are sized for equal rise/fall times.
b) Repeat part a) if all devices are minimum sized
c) Determine the total dynamic power dissipation if the input is a square wave of frequency 10MHz if the devices are sized for equal rise/fall times
d) Repeat part c) if all devices are minimum sized.

Problem 11 Compare the dynamic power required to drive a 6-input NOR gate using a standard equal rise/fall static CMOS design to that required if the 6-input NOR gate is realized with domino logic.

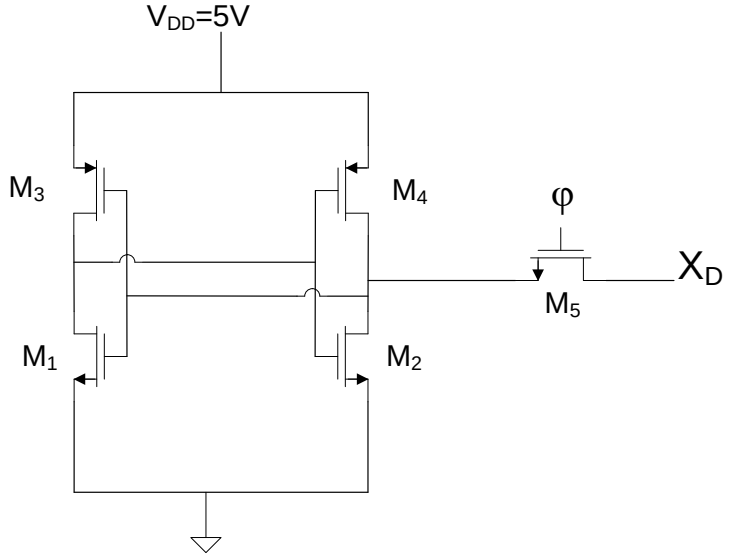
Problem 12 Implement the following Boolean circuit at the transistor level with dynamic zipper logic. Any gate can have at most 3 inputs.

$$F=(ABC+\bar{A}D)\cdot E$$

Problem 13 Design a ring oscillator that will oscillate at a frequency of 80MHz in the 0.18u CMOS process. Assume a supply voltage of 2V is to be used for the ring oscillator.

Problem 14 Describe the difference between a "footed" domino logic gate and an "unfooted" gate. Make a comparison between the advantages and the limitations of the two different types of domino gates.

Problem 15 A 5-transistor memory cell is loaded with X_D when φ is high and holds the value of X_D when φ is low. Assume M_1, M_2, M_3 and M_4 all have W=1μ and L=2μ and the length of M_5 is 1μ. If a high Boolean signal is 5V and a low Boolean signal is 0V, determine the minimum value of W_5 needed to guarantee that the value of X_D can be written into the memory cell.



Problem 16 A poly interconnect that is 2u wide is used to connect a low impedance signal at node A to a 50fF load at node F as shown below. The distance between the dashed segments is 50u. Assume the capacitance density of this poly layer is .5fF/$u^2$and the sheet resistance of the poly is 20 ohms/square. Calculate the Elmore delay from A to F using a T-model for each of the 50u segments.