EE 330
Lecture 9

IC Fabrication Technology

- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Resistance and Capacitance in Interconnect

Review from Last Time

IC Fabrication Technology

- Crystal Preparation
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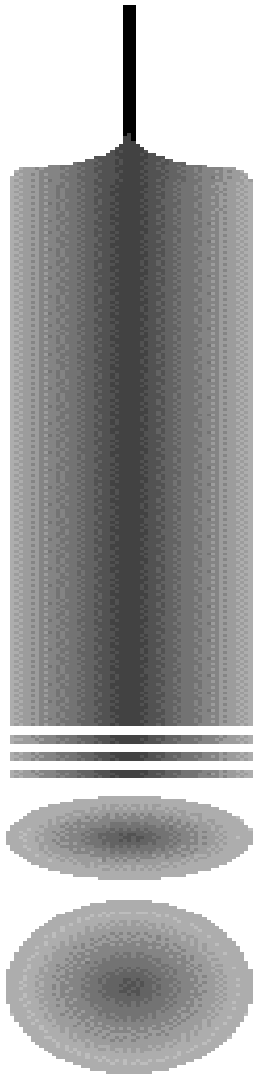
- Contacts, Interconnect and Metalization
- Planarization

Review from Last Time

Crystal Preparation



From www.infras.com

Crystal Preparation

Source: WEB

Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB

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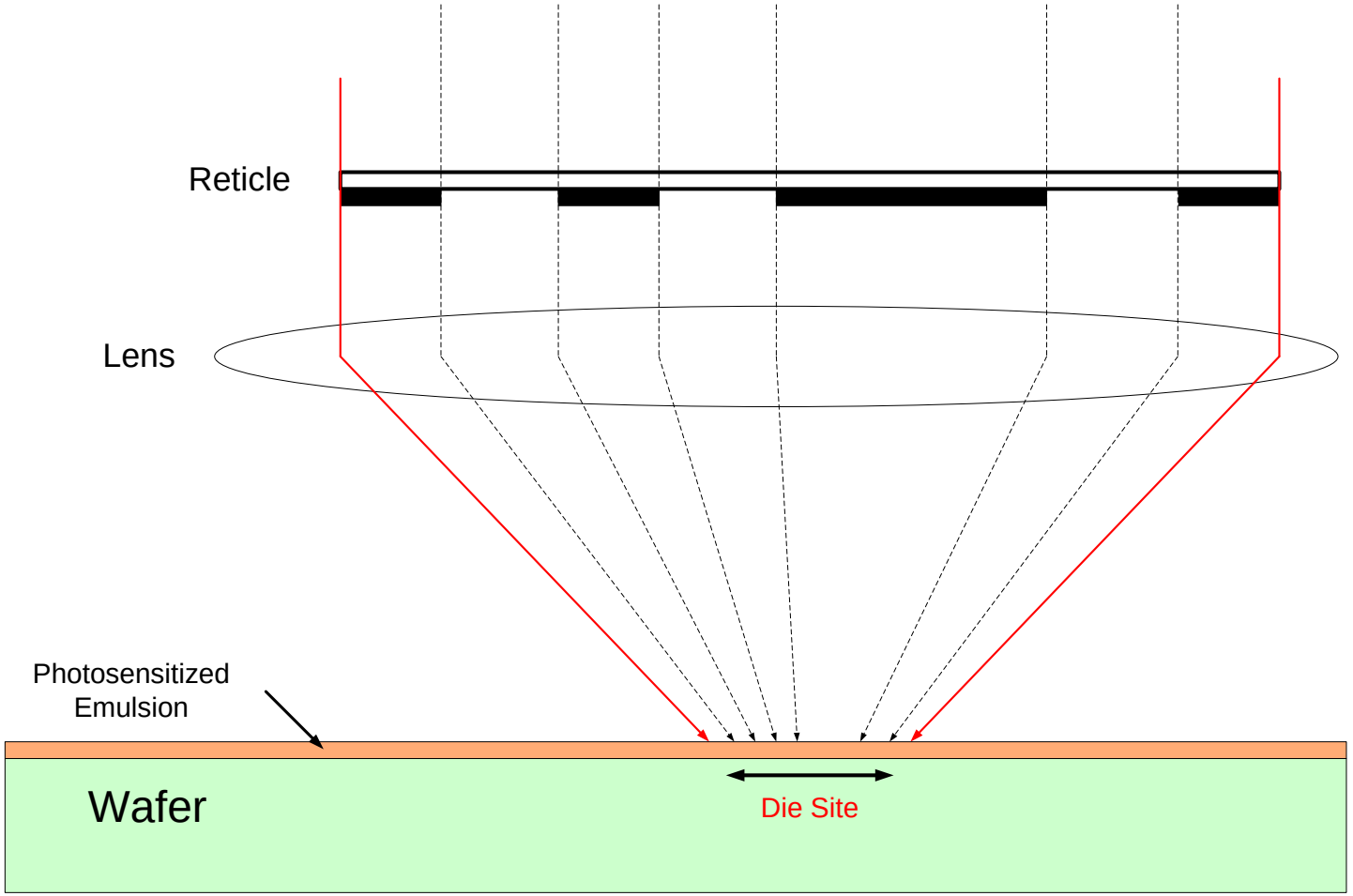
Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860mm^2
    (now through 2022 ITRS 2007 litho, Table LITH3a)

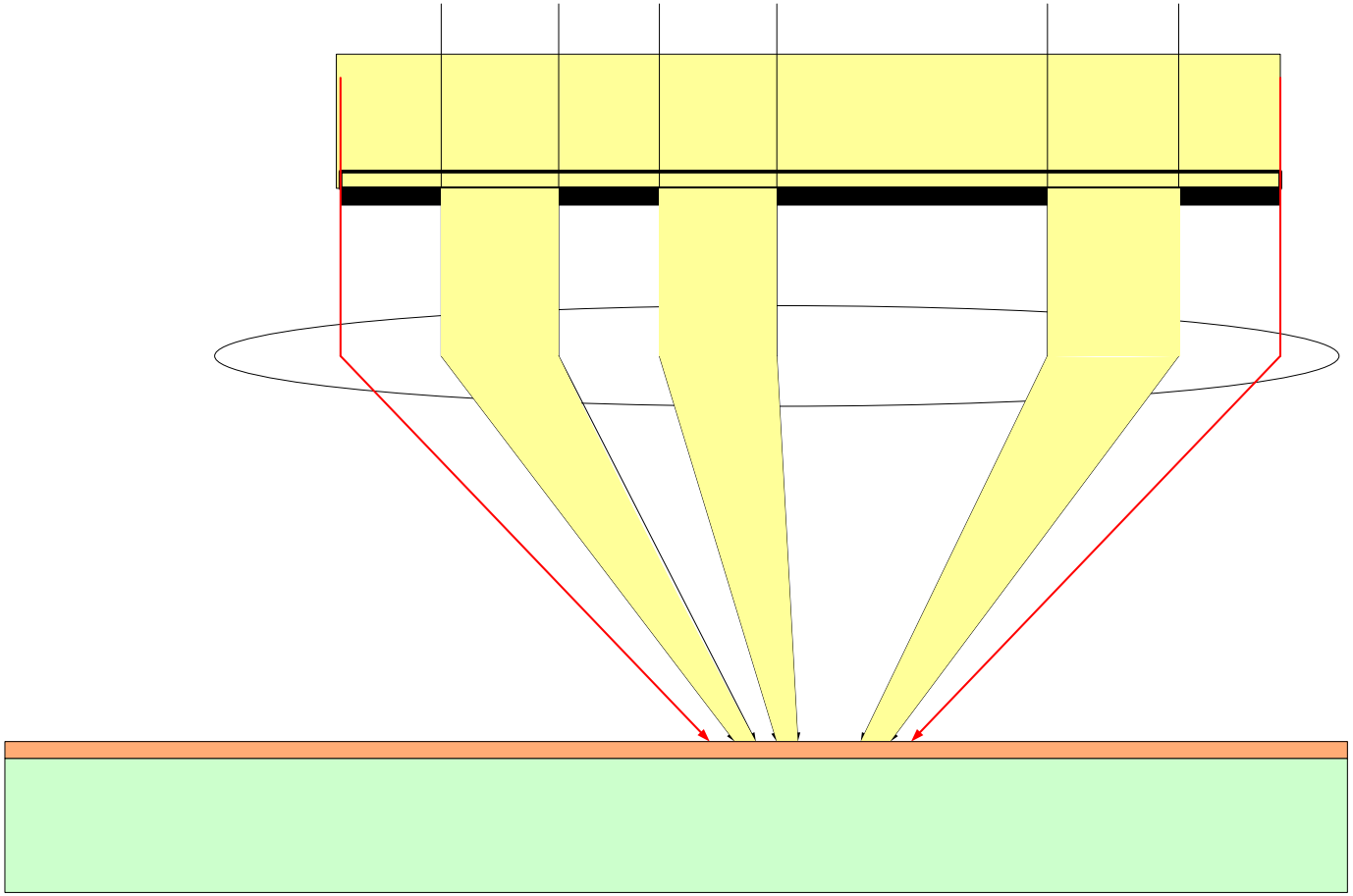
Masking



Step and Repeat (stepper) used to image across wafer

Masking

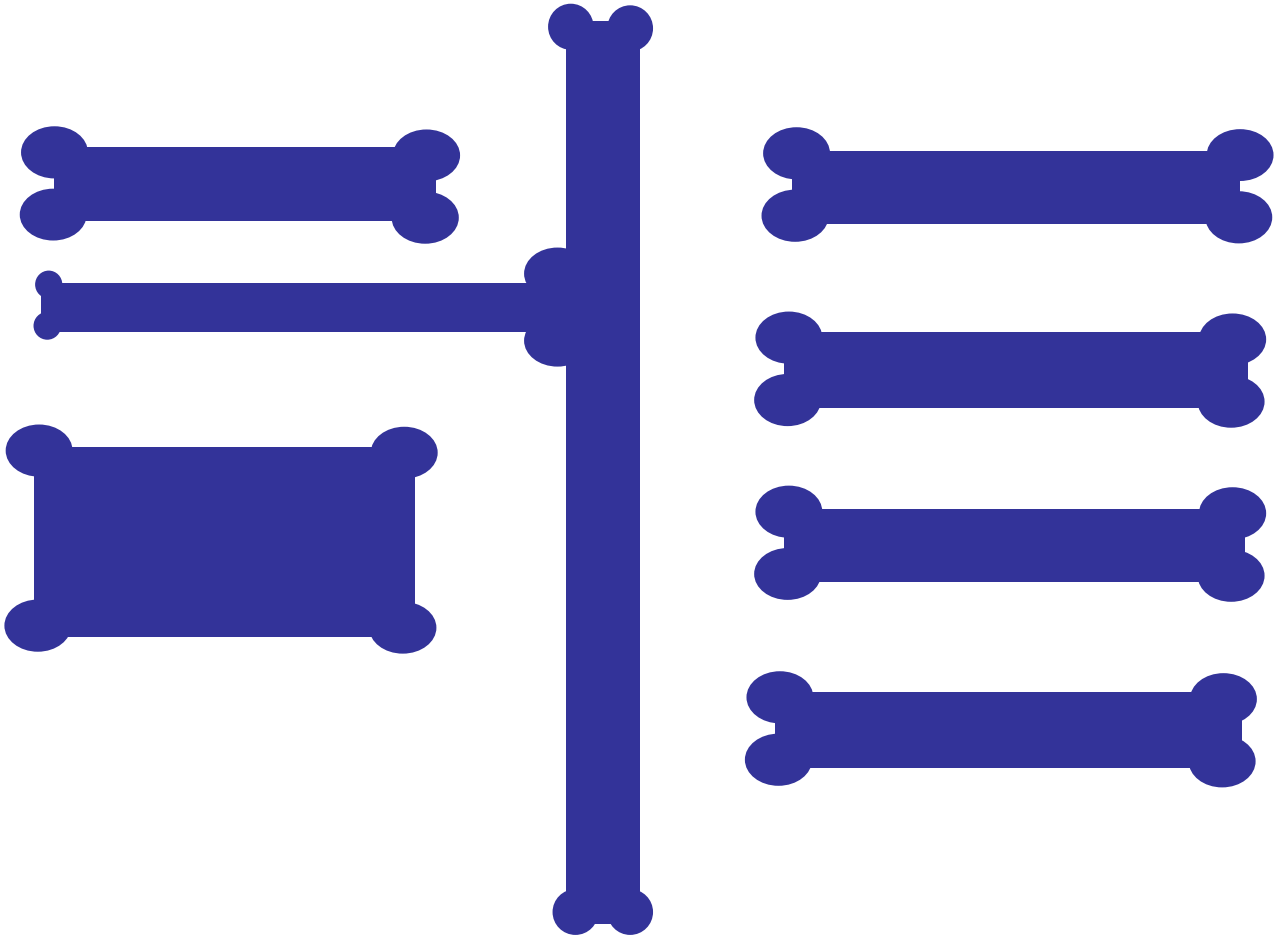
Exposure through reticle



Masking

Mask Features

Masking



Mask Features Intentionally Distorted to Compensated For Wavelength Limitations in Small Features

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Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size

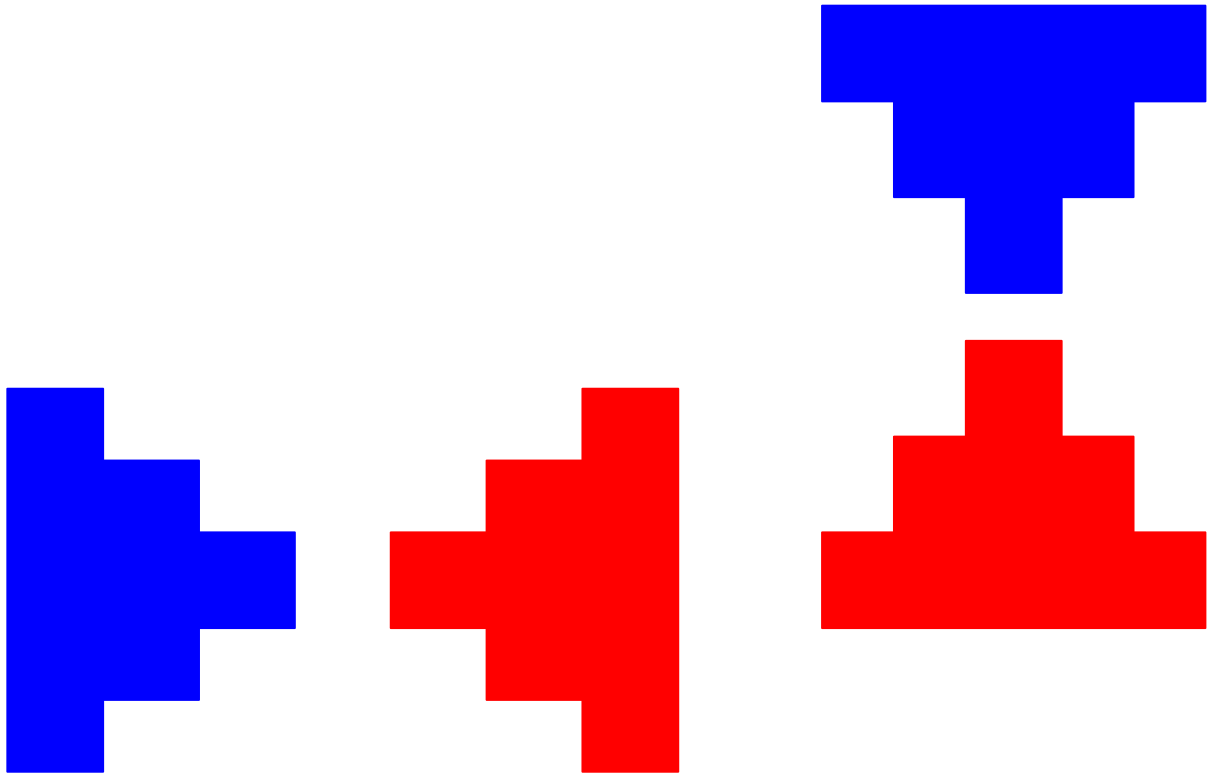
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour

Steppers

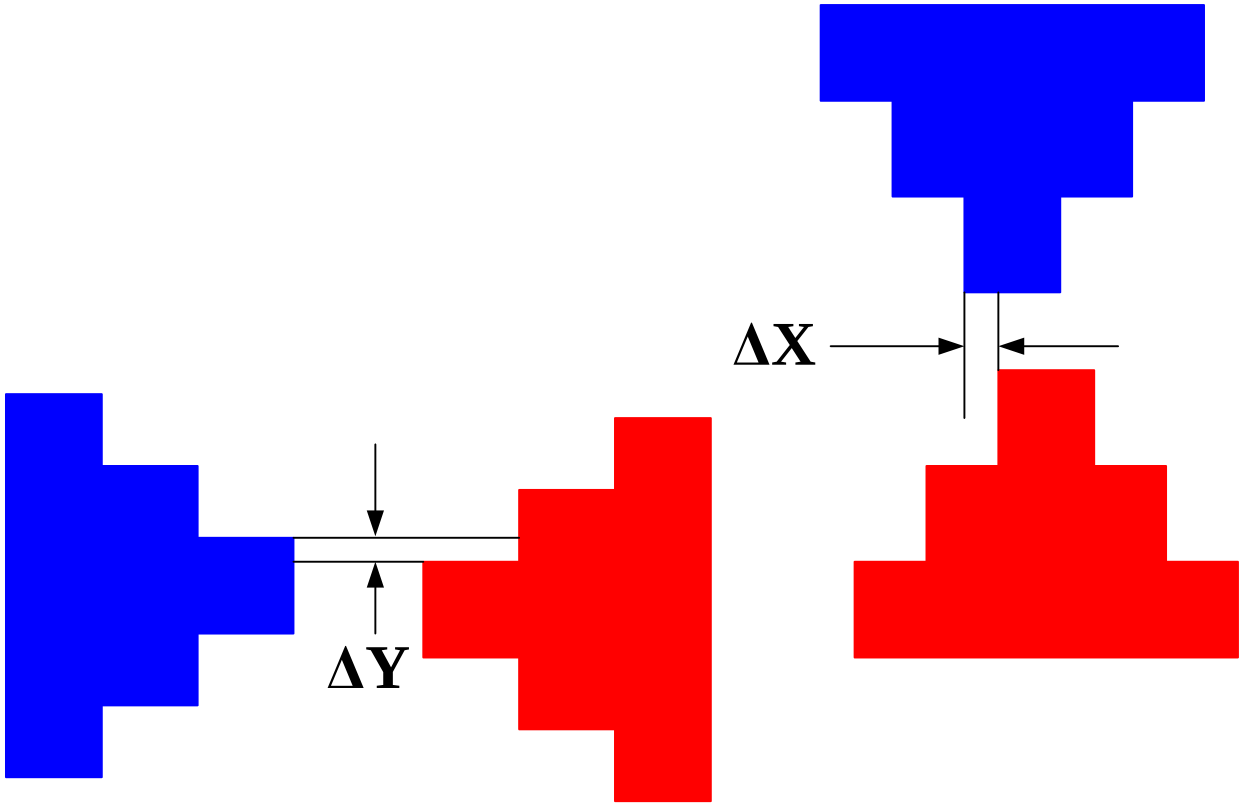
Mask Alignment

Correctly Aligned



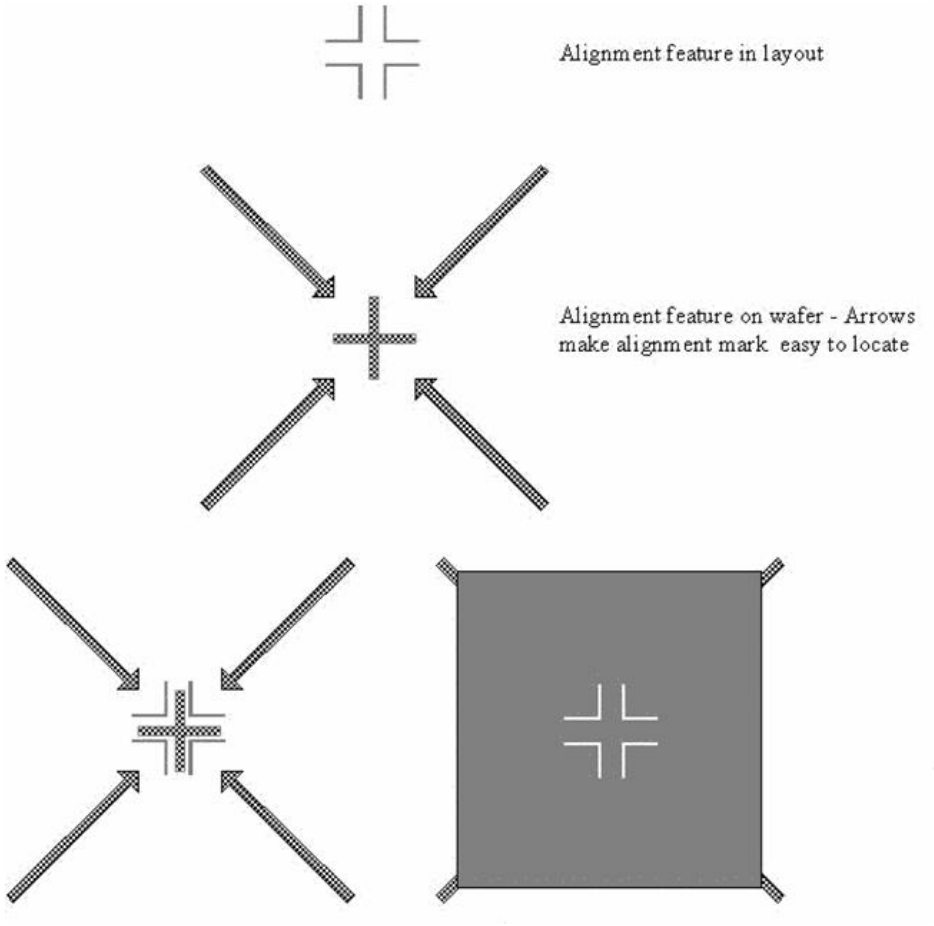
Mask Alignment

Alignment Errors



Mask Alignment

Other alignment marks (http://www.mems-exchange.org/users/masks/intro-equipment.html)



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Deposition

- Application of something to the surface of the silicon wafer or substrate
  - Layers 15A to 20u thick
- Methods
  - Physical Vapor Deposition (nonselective)
    - Evaporation/Condensation
    - Sputtering (better host integrity)
  - Chemical Vapor Deposition (nonselective)
    - Reaction of 2 or more gases with solid precipitate
    - Reduction by heating creates solid precipitate (pyrolytic)
  - Screening (selective)
    - For thick films
    - Low Tech, not widely used today

Deposition

Example: Chemical Vapor Deposition

Silane (SiH_4) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H_2 above 400^{o}C so can be used to deposit Si.

$$Si H_4 \rightarrow Si + 2H_2$$

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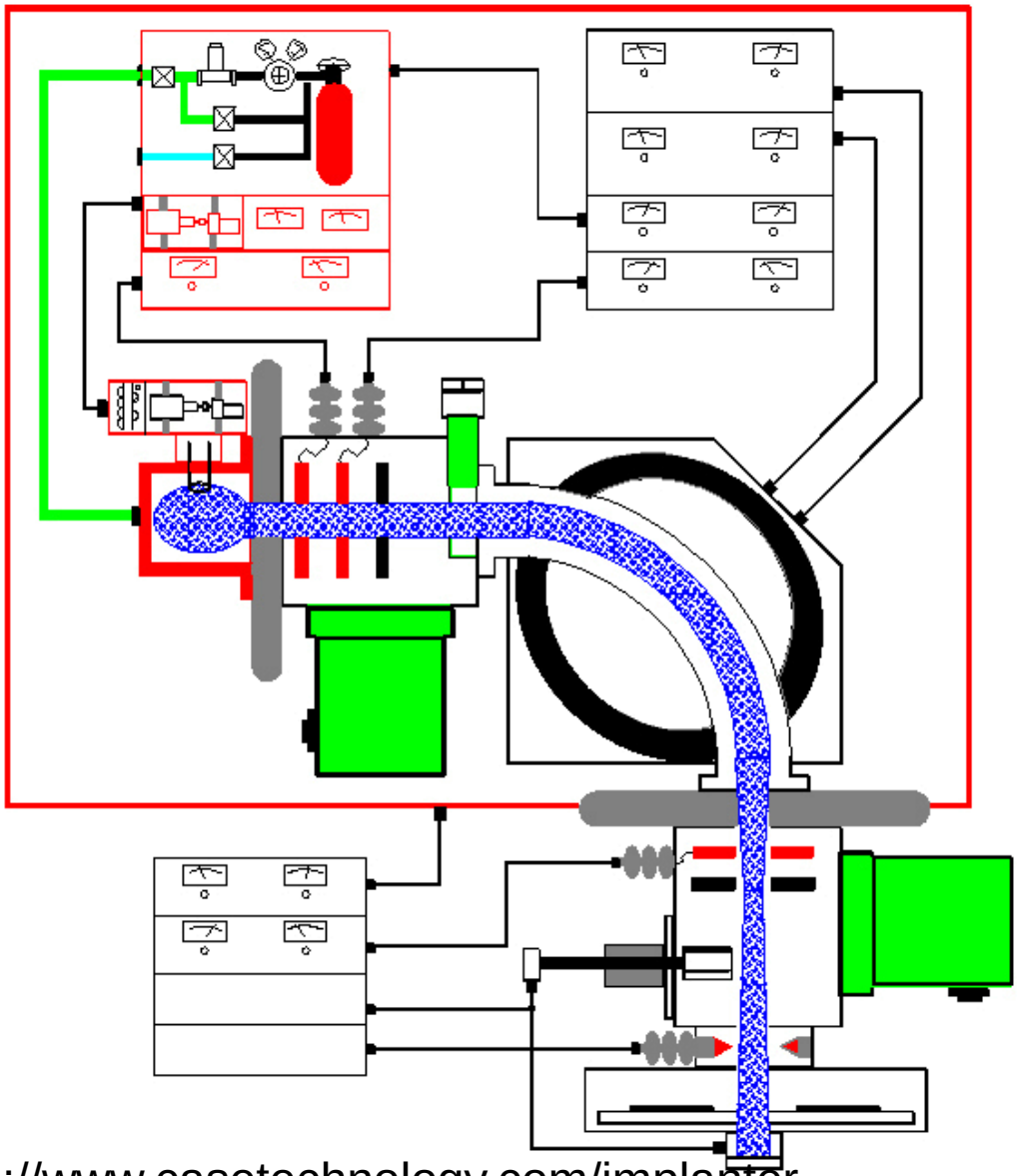
Implantation

Application of impurities into the surface of the silicon wafer or substrate

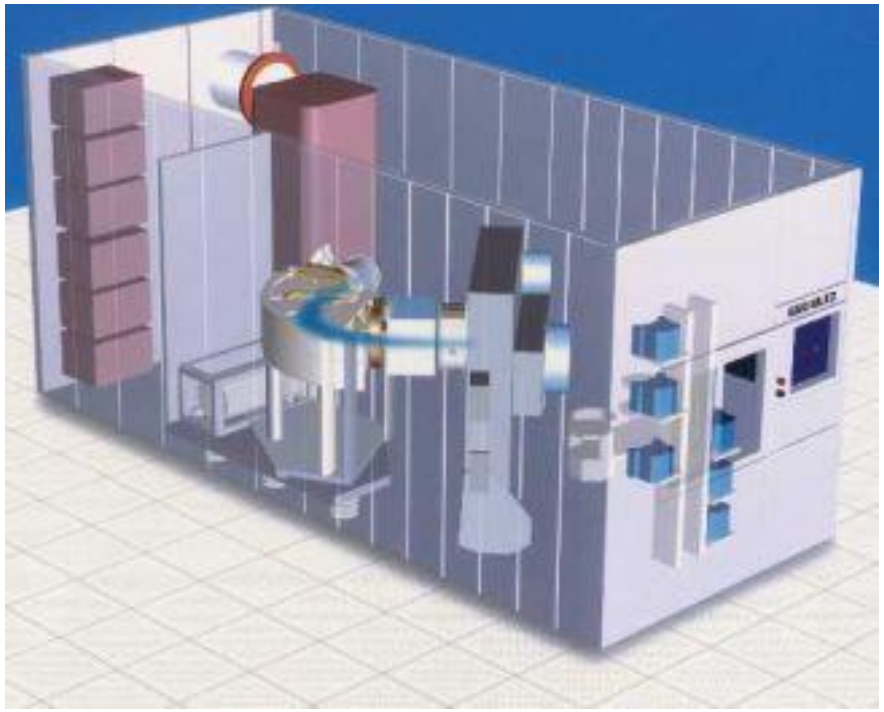
- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security

Ion Implantation Process



From http://www.casetechnology.com/implanter

Ion Implanter



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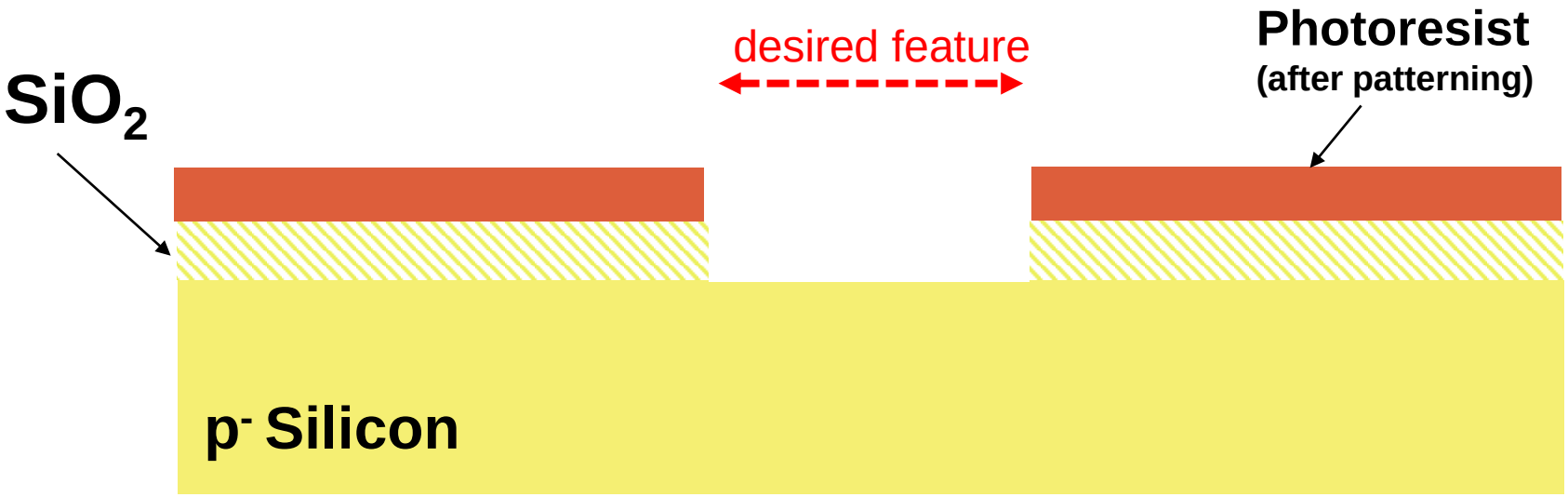
Etching

Selective Removal of Unwanted Materials

- Wet Etch
  - Inexpensive but under-cutting a problem
- Dry Etch
  - Often termed ion etch or plasma etch

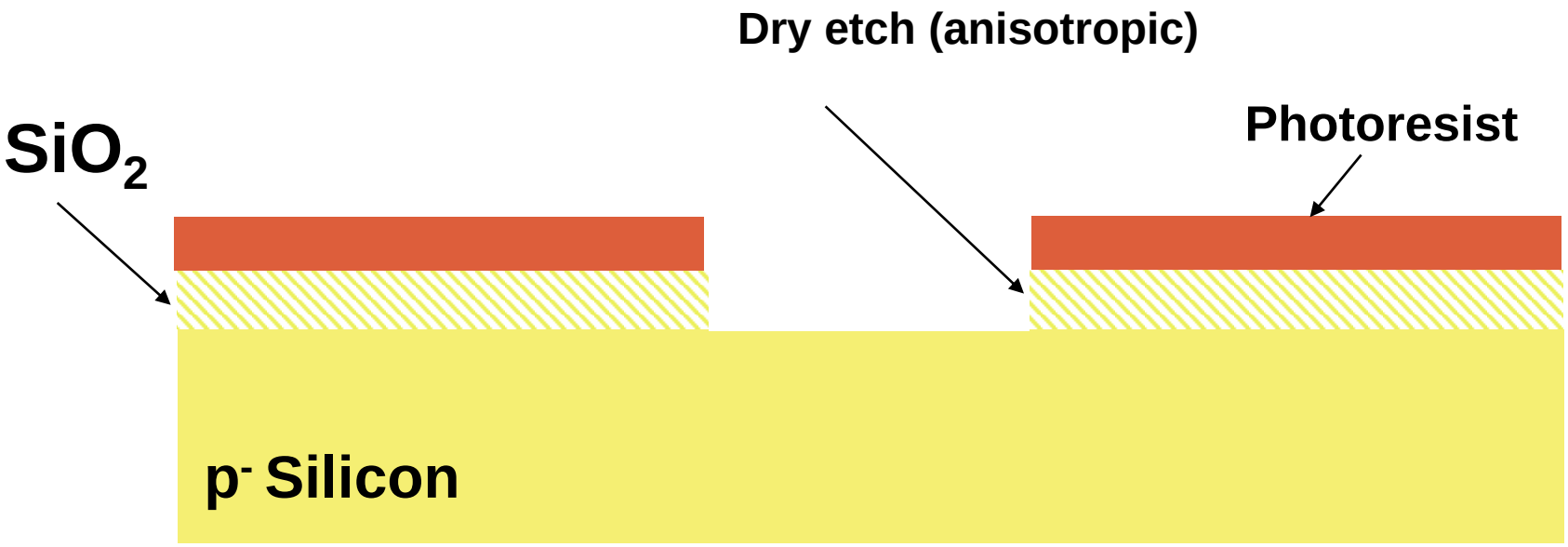
Etching



Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions

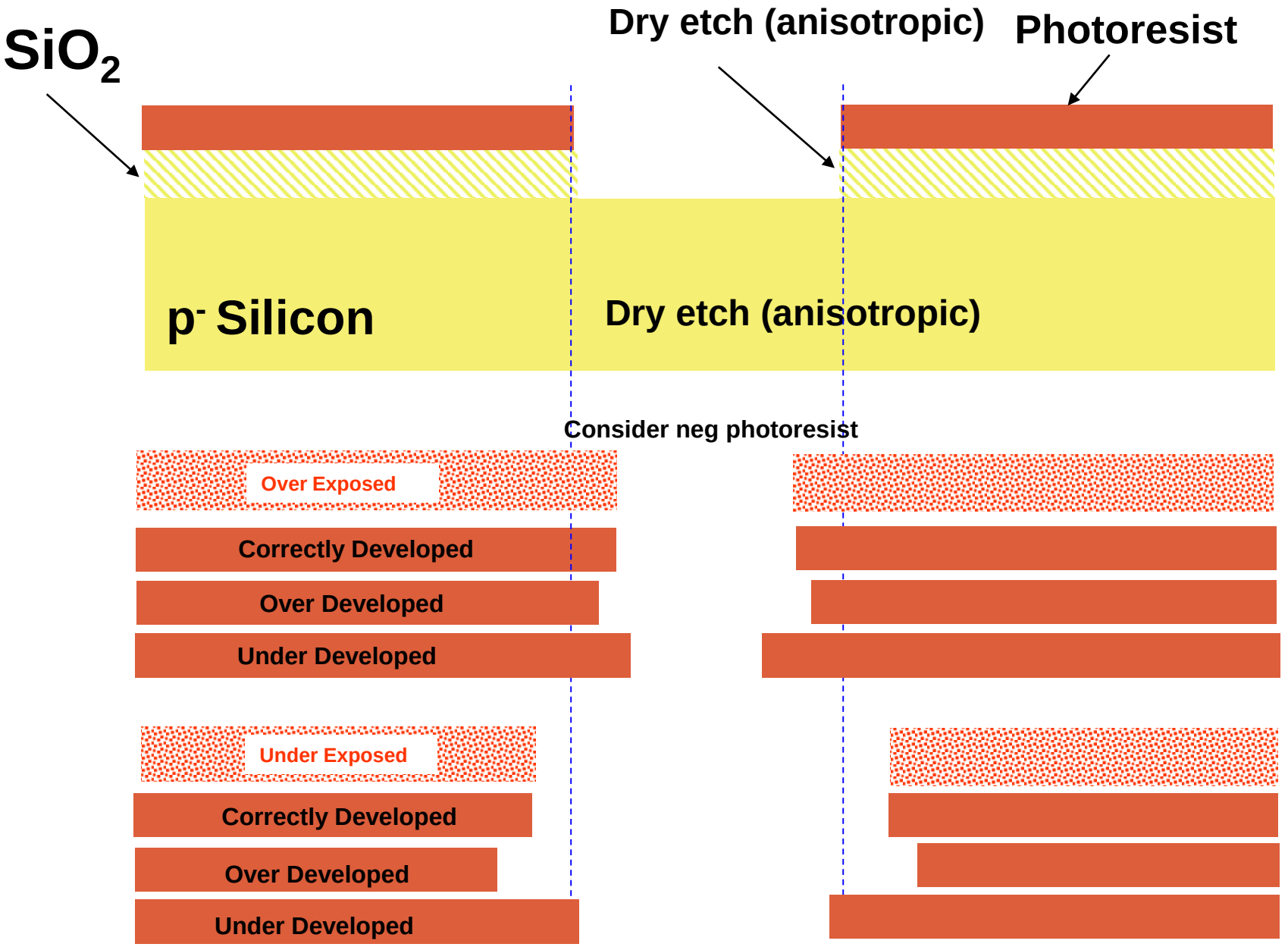
Etching



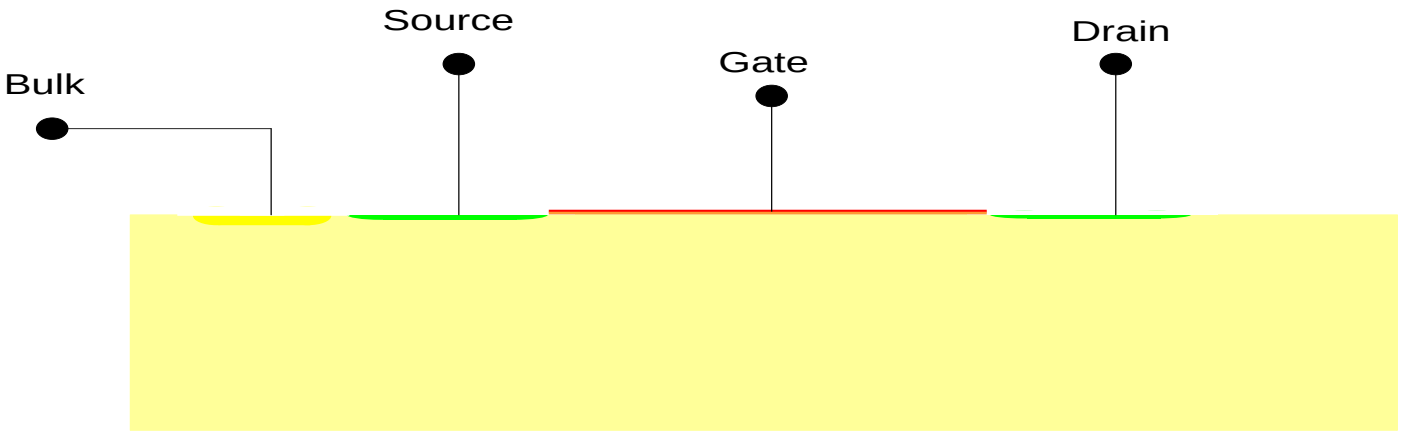
Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist paterning)

Etching (limited by photolitghographic process)



Lateral Relative to Vertical Dimensions

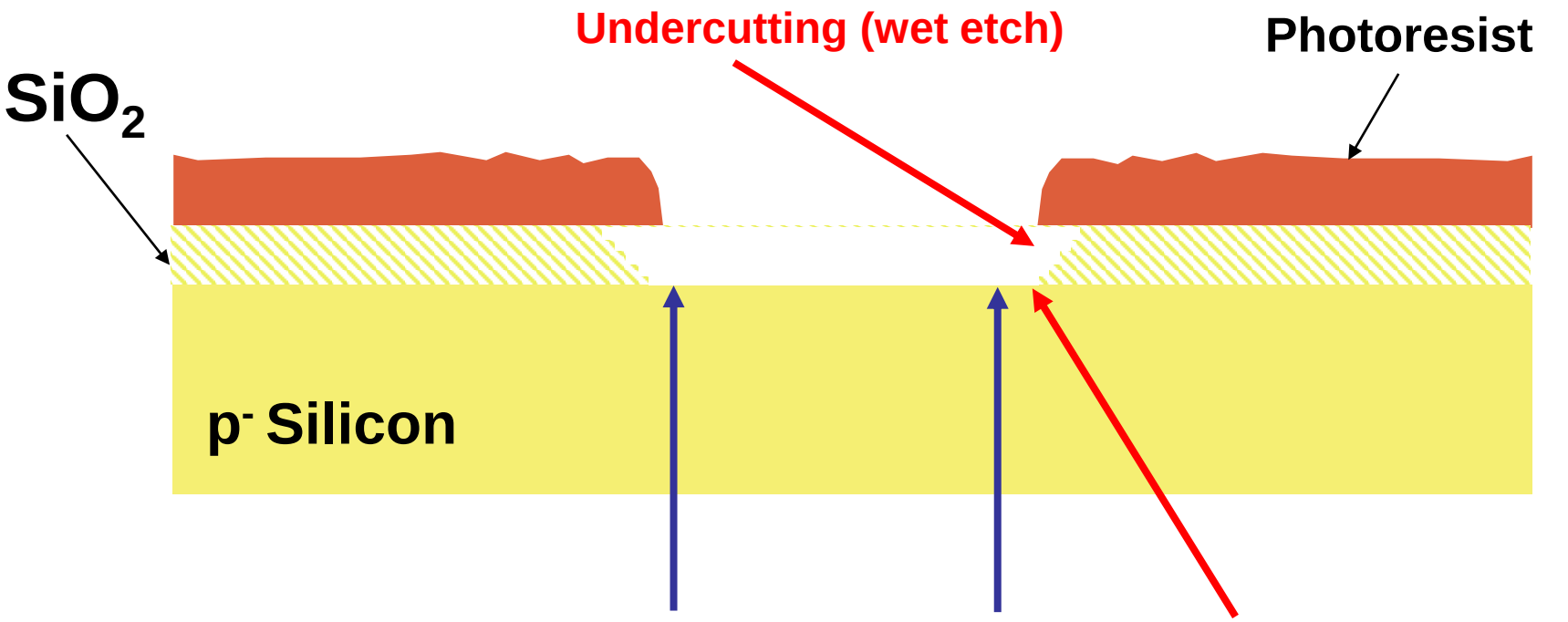


n-channel MOSFET

Still Not to Scale

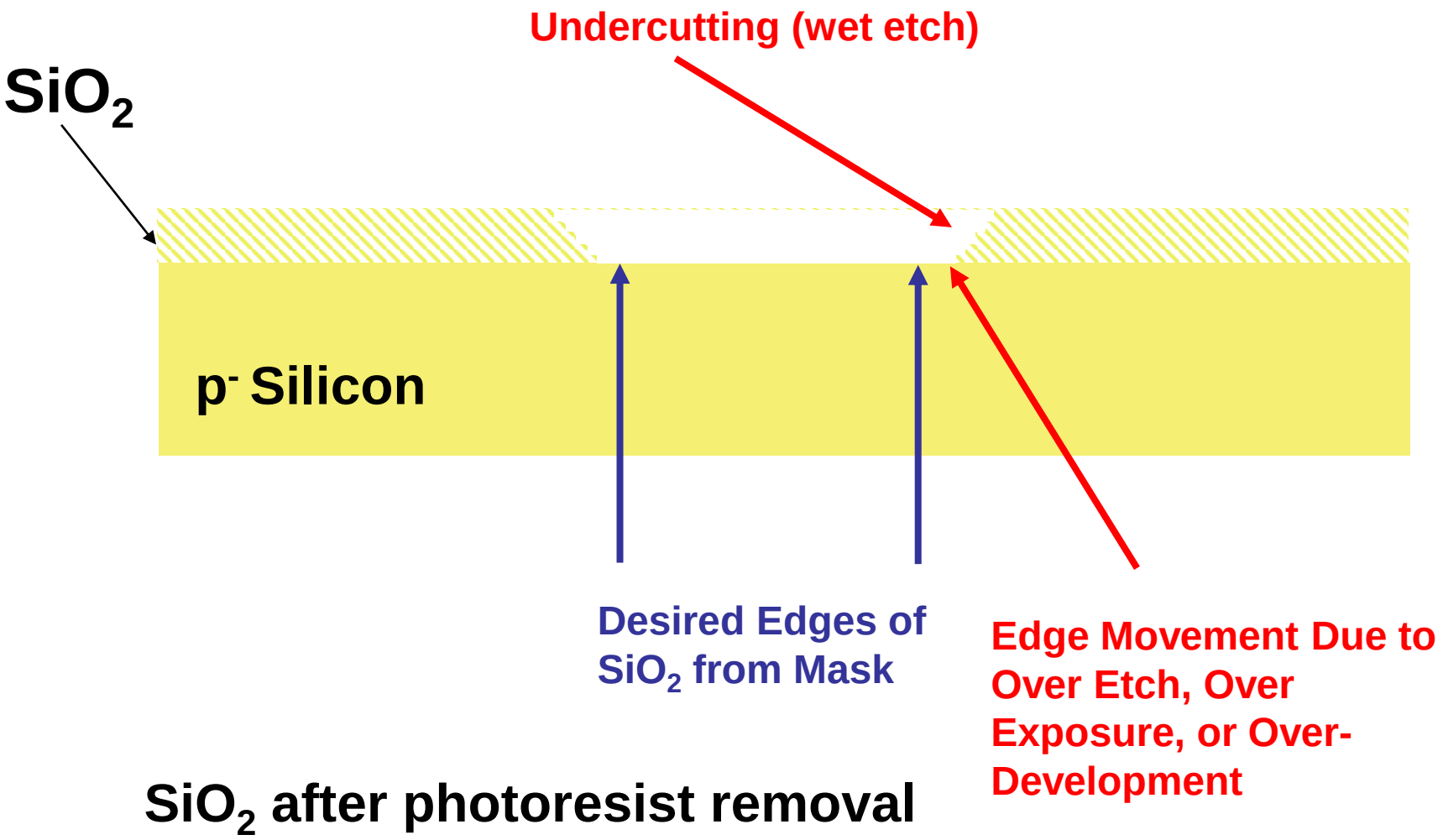
For Example, the wafer thickness is around 250u and the gate oxide is around 50A (5E-3u) and diffusion depths are around λ/5

Etching



Isotropic
Feature Degradation

Etching



SiO_2 after photoresist removal

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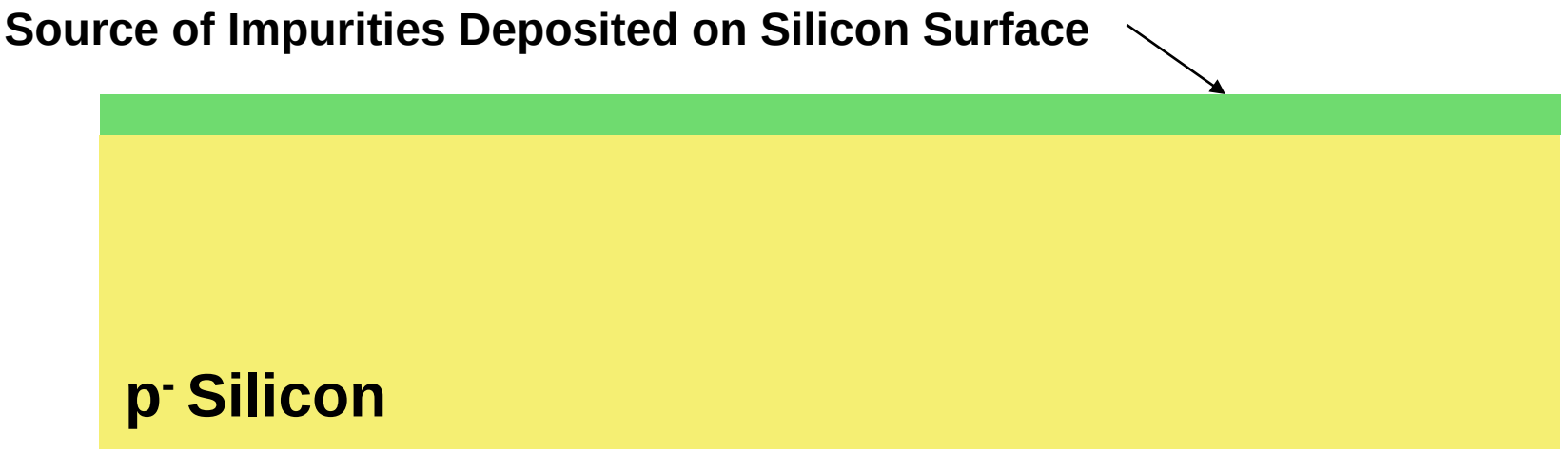
Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800^{o}C to 1200^{o}C
- Source of Impurities
  - Deposition
  - Ion Implantation
    - Depth depending on ion speed/enery
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion
- Types of Impurities
  - n-type Arsenic, Antimony, Phosphorous
  - p-type Gallium, Aluminum, Boron

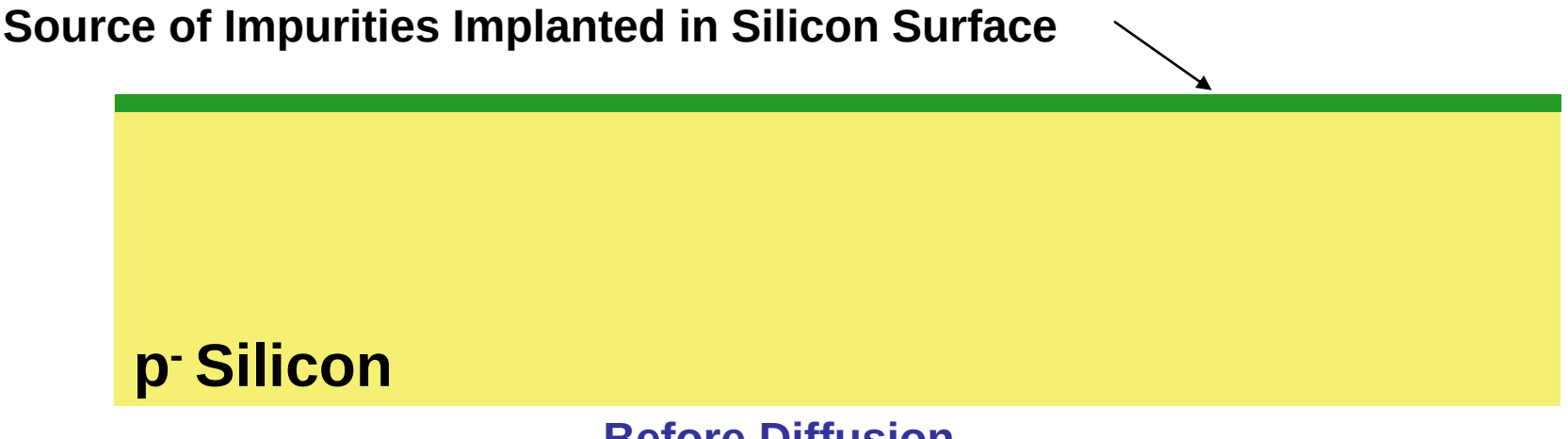
Diffusion



Before Diffusion

After Diffusion

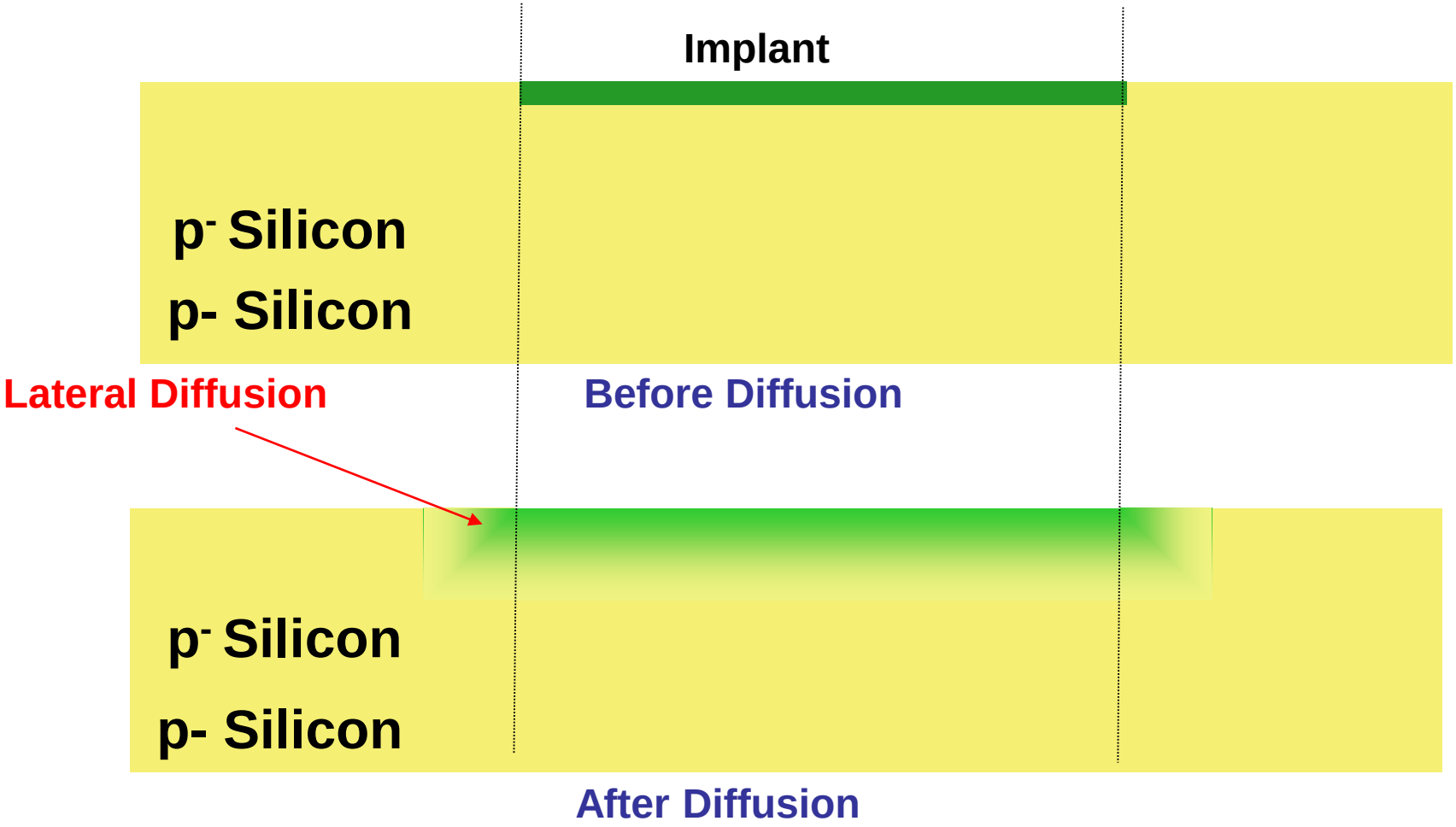
Diffusion



Before Diffusion

After Diffusion

Diffusion


Implant
p- Silicon
p- Silicon
Lateral Diffusion
Before Diffusion
p- Silicon
p- Silicon
After Diffusion

End of Lecture 9