EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Final Exam

Fall 2017

Tuesday Dec 12 12:00-2:00 p.m.

Instructions: Students may bring 3 pages of notes (3 front + 3 back) to this exam. There are 10 questions and 8 problems. There are two points allocated to each question. All problems are worth 10 points. Please solve problems in the space provided on this exam. Attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/V^2$, $\mu_p C_{OX}= \mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=4fF/\mu^2$, $\lambda = 0.01V^{-1}$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters for an npn transistor of $J_S=10^{-15}A/\mu^2$, $\beta_n=100$ and $V_{AFn} = \infty$ and those for a pnp transistor are $J_S=10^{-15}A/\mu^2$, $\beta_p=20$ and $V_{AFp} = \infty$. If any other process parameters are needed, use the process parameters associated with the process described in the attachments to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters. Several tables that may be of use are appended at the end of the exam.

1. (2pts) One of the sizing strategies used for determining dimensions of transistors in CMOS gates was termed "equal worst-case rise and fall times". What is the reason "worst-case" was included in this sizing strategy?

2. (2 pts) Simpler and less-expensive processes can be used to build ratio logic circuits but today most large digital circuits are fabricated in more expensive CMOS processes. What is the major reason for this?

3. (2 pts) What is the major use of large overdrive factors to size gates in a CMOS logic circuit?

4. (2pts) Elmore delay calculations are often used to predict the delay of Boolean signals that are propagating through an interconnect. Though not real accurate, Elmore delay calculations are generally said to be "faithful". What is the meaning conveyed by the word "faithful" in this context?

5. (2 pts) Dynamic logic is somewhat more complicated than static CMOS or ratio logic yet there can be a significant benefit from using dynamic logic in some applications. What is the major advantage dynamic logic offers in some applications?

6. Several contributors to power dissipation in a logic circuit were identified. These included dynamic power dissipation, pipe dissipation, leakage, and static power dissipation. Describe what "pipe" power dissipation is and what is naturally done to make the pipe power dissipation small.

7. Aside from the cost of die area which goes up linearly with area, there is a major reason that very large die are not practical. What is the major reason very large die are not practical?

8. (2 pts) Of the basic MOS amplifier structures, which is noted for having a large noninverting voltage gain?

9. (2pts) Why is C_{OX} for the n-channel transistors and the p-channel transistors nearly identical for the 0.5µm CMOS process we have discussed in class?

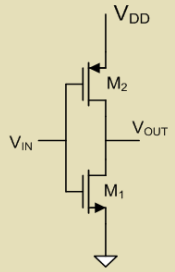
10. (2 pts) In the 90nm process node, the thickness of the SiO_2 gate is about 1.2nm. How many SiO_2 molecules stacked vertically on top of each other is required to make the 1.2nm gate oxide?

Problem 1 A polysilicon interconnect that is 1mm long and 1µm wide is driving an equal rise/fall inverter with an OD of 20 as shown in the figure. Assume this interconnect is in the process characterized by the description in the attachment at the end of this exam. A reference inverter in this process is shown below.

a) Using a three-segment Elmore delay model, calculate the delay of a Boolean low-to-high signal transition that propagates from point A to point B in this interconnect bus.

b) Calculate the propagation delay ($t_{HL}+t_{LH}$) from A to C. Assume V_{DD}=3.5V.

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

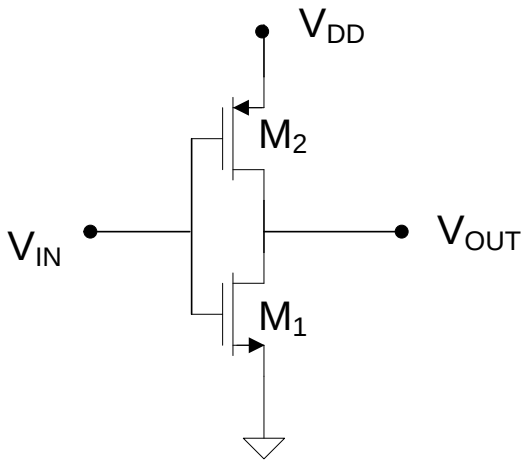
$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

Problem 2 The standard static CMOS inverter is shown below. The trip point for this inverter is given by the expression

$$V_{TRIP} = \frac{(V_{Tn})\sqrt{\frac{W_1}{L_1}} + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}$$

Mathematically derive this expression.

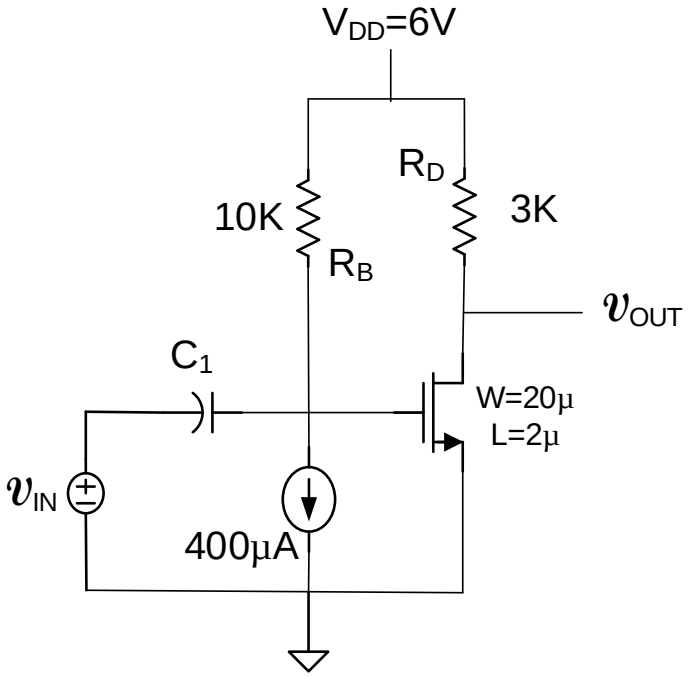


Problem 3 An amplifier circuit is shown below. Assume C_1 is large.

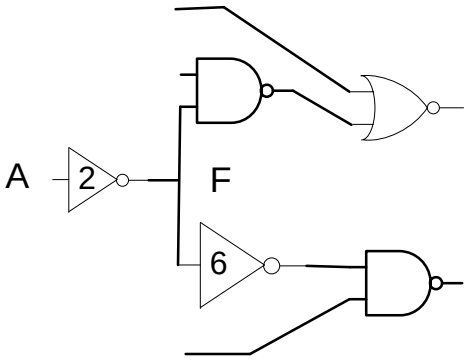
a) Determine the quiescent output voltage

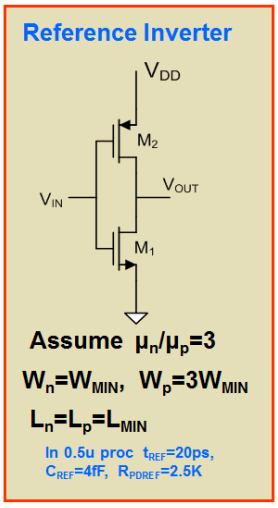
b) Determine the small-signal voltage gain in terms of the small-signal model parameters and the resistors in the circuit

c) Numerically determine the small-signal voltage gain.



Problem 4 A section of a logic block is shown below. Assume all devices are sized for equal worst-case rise and fall times and that the overdrives, if different than 1, are as indicated. If the input A is a 10MHz square wave, determine the dynamic power dissipation in the inverter with OD=2. Assume V_{DD}=3.5V. The characteristics of a reference inverter in the process used for the design of the logic block are shown below.

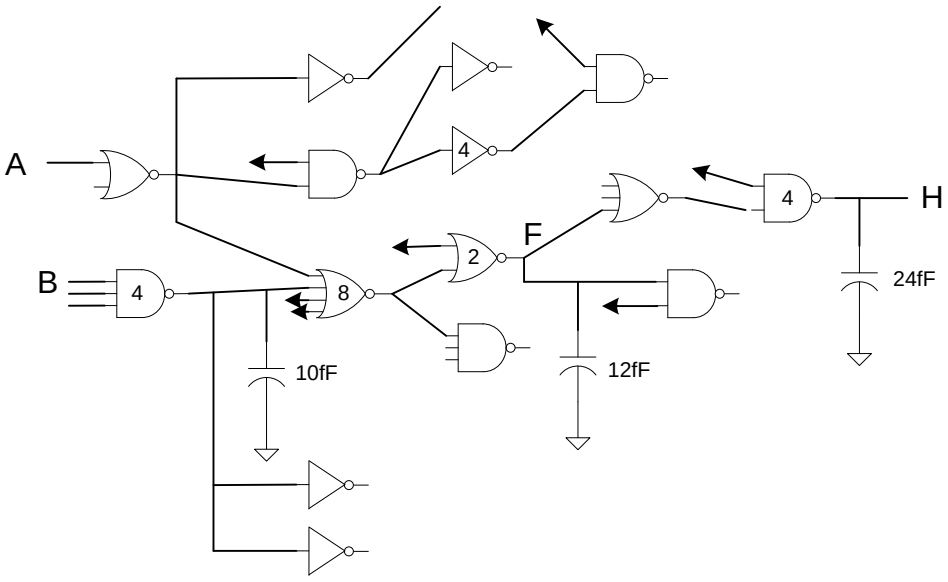




Problem 5 A segment of a logic block is shown below. Assume the lengths of all devices are L_{MIN}. Assume all gates are sized for equal worst-case rise and fall times. Gates with an overdrive factor that is different than 1 are as indicated by a number on the gate. Assume that the process in which these gates are fabricated is characterized by a minimum length reference inverter with

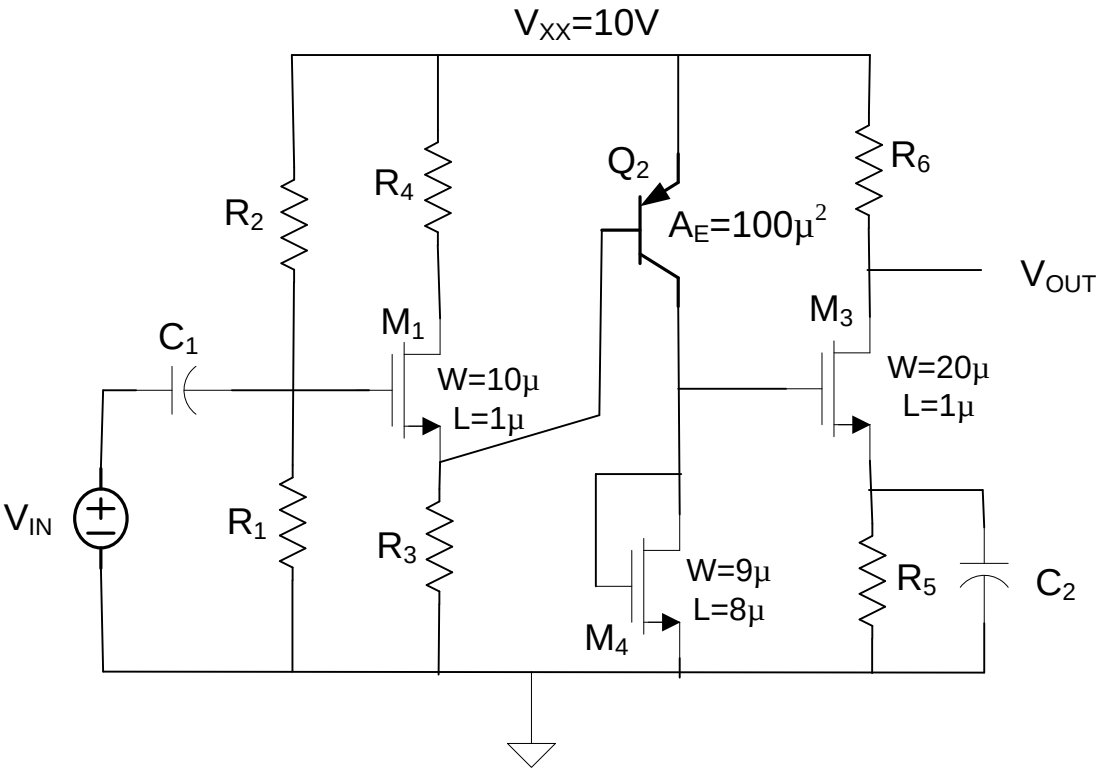
$$t_{REF}=20ps,\ C_{REF}=4fF,\ R_{PDREF}=2.5K$$

a) Determine the worst-case propagation delay from B to F
b) Repeat part a) if all gates are minimum sized.



Problem 6 Consider the amplifier block shown below. Assume all MOS transistors are operating in the saturation region and the BJT is operating in the forward active region. Assume the capacitors are all large.

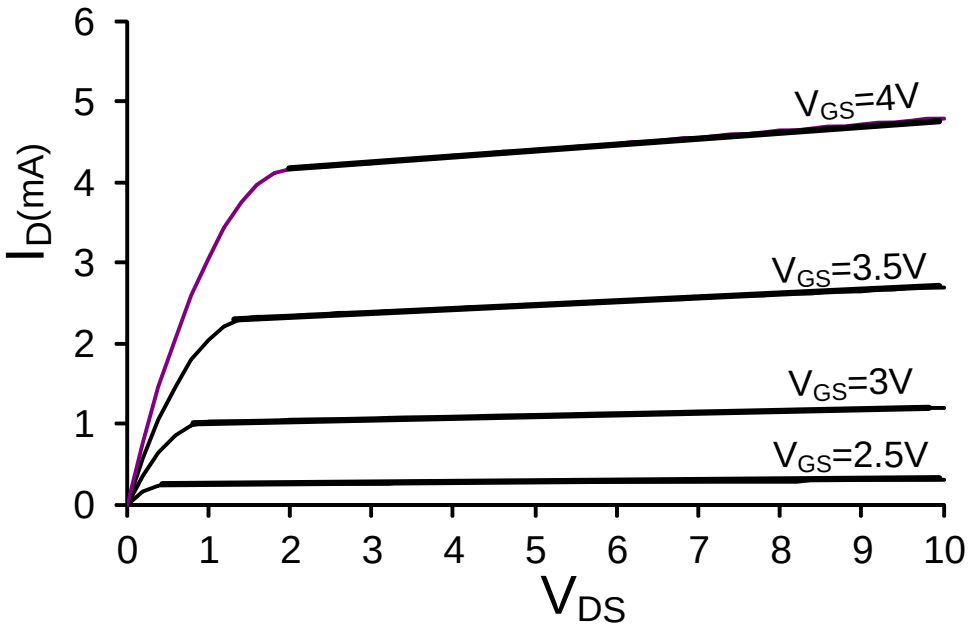
a) Draw the small-signal equivalent circuit of this amplifier
b) Determine the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the components in the circuit
c) Determine the input impedance in terms of the model parameters of the transistors and the components in the circuit



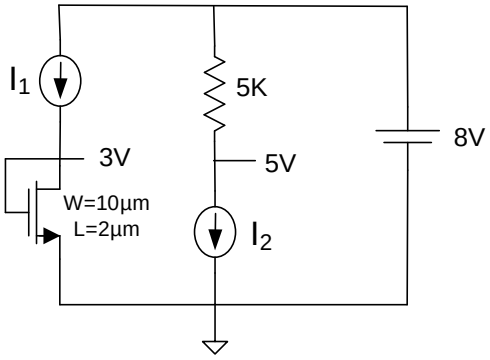
Problem 7 The I_D-V_{DS} characteristics for a MOSFET with different values of V_{GS} are shown below. The dimensions of the device are W=15µm and L=3µm.

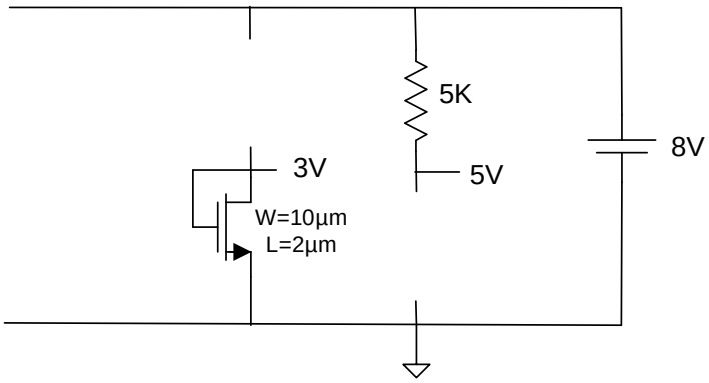
a) Determine V_{TH} for this transistor

b) Determine μC_{OX} for this transistor



Problem 8 Design the current sources I_1 and I_2 so that the node voltages are 3V and 5V as indicated. You may use any number of resistors, capacitors, MOS transistors, and BJT transistors as you choose in your design but your current generators should be powered by the 8V voltage source indicated. Sketch your design in the schematic given on the bottom of this page.





TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

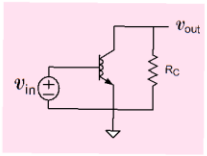
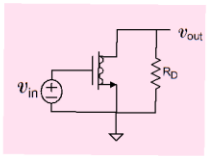
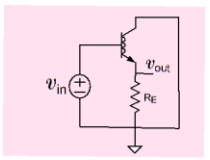
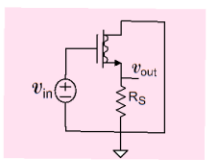
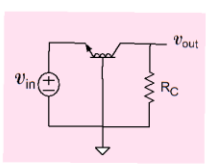
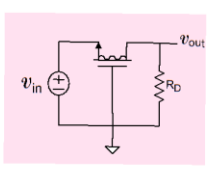
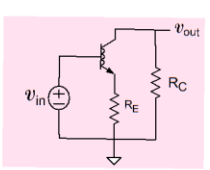
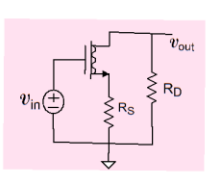
PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

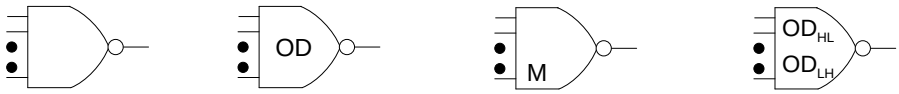
COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

Basic Amplifier Gain Table

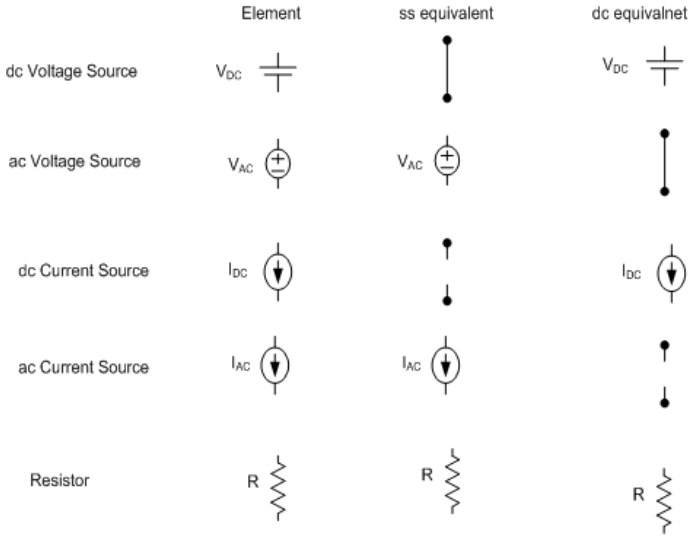
	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
								
A_V	$-g_mR_C$		$\frac{g_m}{g_m+g_E}$		g_mR_C		$-\frac{R_C}{R_E}$	
	$-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$	$\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	$\frac{I_{CQ}R_C}{V_t}$	$\frac{2I_{DQ}R_C}{V_{EB}}$		
R_{in}	r_π		$r_\pi+\beta R_E$		g_m^{-1}		$r_\pi+\beta R_E$	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞
R_{out}	R_C		g_m^{-1}		R_C		R_C	
			$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$				

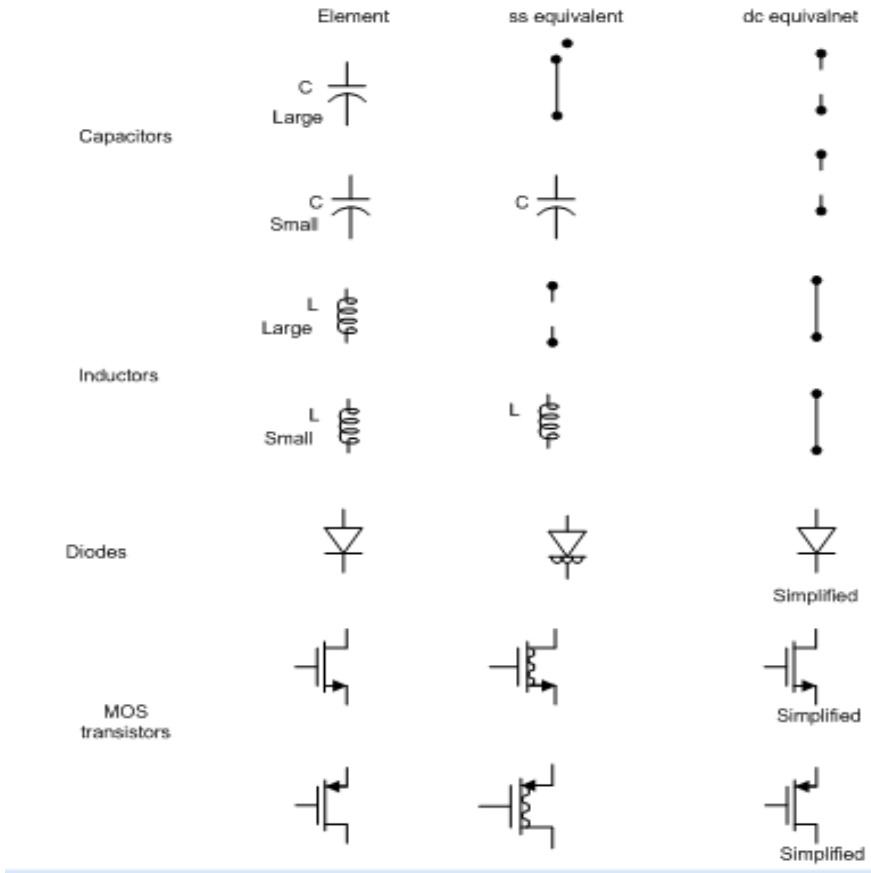
Propagation Delay in Logic Circuits with OD and Asymetry



	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{i(k+1)}$	$\sum_{k=1}^{n} \frac{F_{i(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{i(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{i(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Capacitors
C
Large
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Inductors
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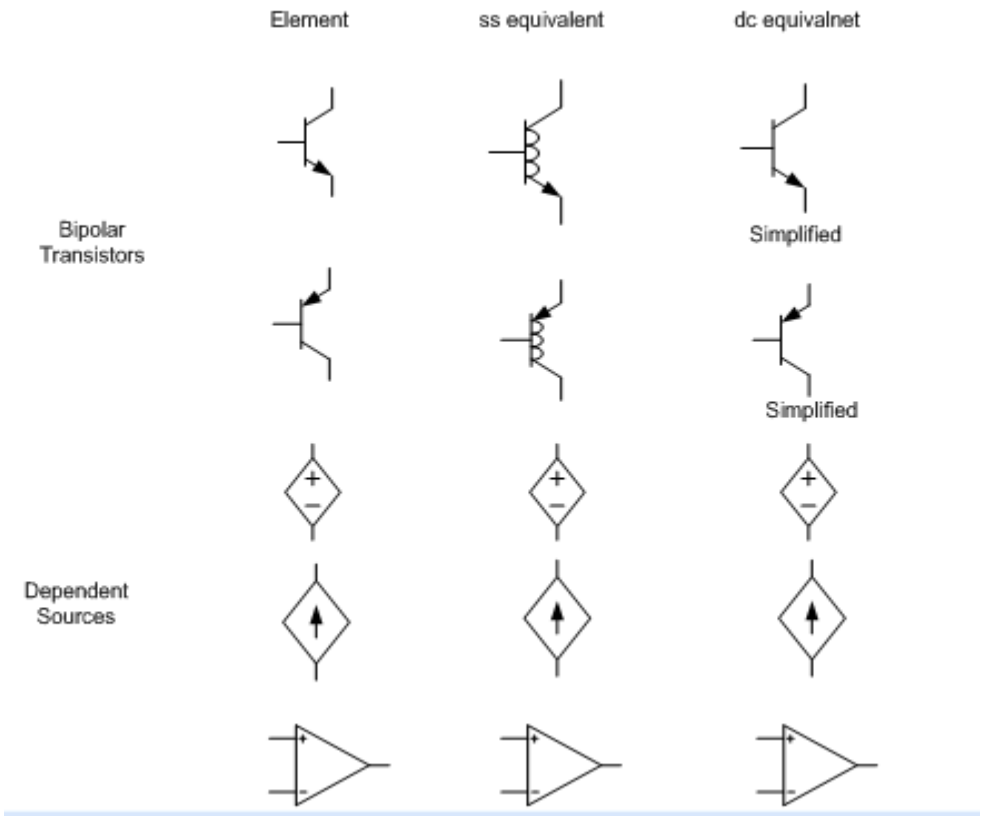
Diodes
Simplified
MOS
transistors
Simplified
Simplified


Element
ss equivalent
dc equivalnet
Bipolar
Transistors
Simplified
Simplified
Dependent
Sources