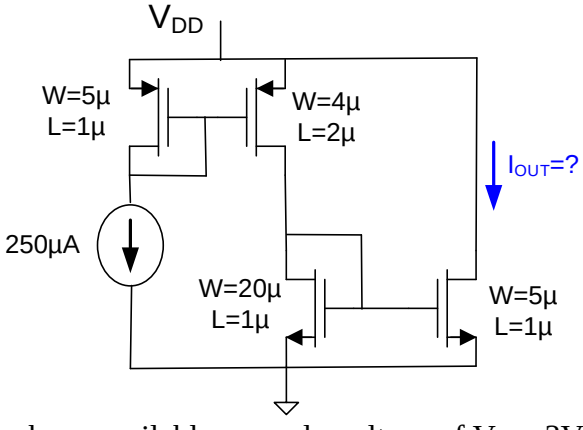
EE 330
Assignment 12
Fall 2019 Due Friday Nov 15

Solve Problems 1 – 13. The remaining problems are practice problems and will not be collected. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$, $V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$, $V_{Tp} = -0.5V$, and all JFET devices are from a process with $I_{DSSn0} = 100\mu A$, $I_{DSSp0} = 30\mu A$, $V_{Pp} = 1V$, $V_{Pn} = -1V$, and $\lambda = 0$. In this process, assume that for all MOS devices, $L_{MIN} = W_{MIN} = 0.18\mu$, and $V_{DD} = 2V$. Assume also that a bipolar process is available with parameters $J_S = 10^{-14} A/\mu^2$ and $\beta_n = 100$ and $\beta_p = 40$. Unless stated to the contrary, assume the output conductance of the BJT and the MOSFET are characterized, respectively, by $V_{AF} = 100V$ and $\lambda = .01V^{-1}$.

Problem 1 Determine I_{OUT}. Assume $V_{DD} = 2V$.



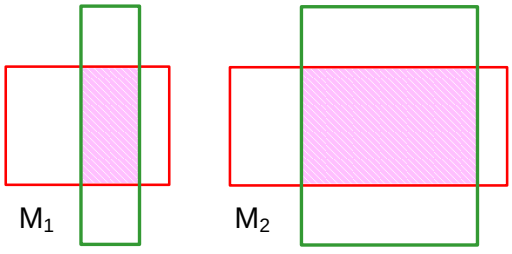
Problem 2 Assume you have available a supply voltage of $V_{DD} = 3V$ and a 10mA sourcing current (one end connected to V_{DD}).

a) Design a current mirror that provides two outputs, a sinking current of 100uA and a sourcing current of 10mA using MOS transistors.

b) What is the maximum voltage for the 10mA current source for your design if it is to work as a current mirror.

Problem 3 Design a noninverting amplifier with a nominal gain of +5 that has an input impedance that is between 100K and 200K that can drive a 2K resistive load using MOS transistors, resistors, capacitors, and one dc voltage source. Verify your design analytically and with SPICE.

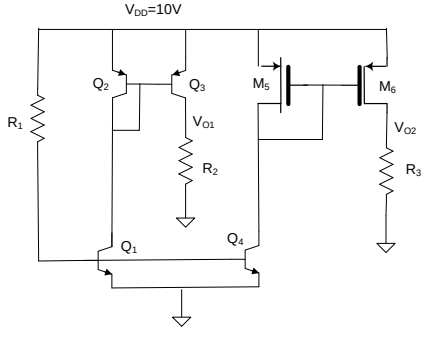
Problem 4 A potential layout strategy for a basic current mirror is shown below where the mirror gain is determined by the W/L ratio of the layout on the right to the W/L ratio of the layout on the left. If an n-channel current mirror is designed using this layout approach with an ideal mirror gain of $M = \dfrac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}$ and with nominal values of $L_1 = L_2 = 4u$ and $W_1 = 2u$, $W_2 = 10u$, determine the actual mirror gain if the field oxide encroachment into the active region results in an inward movement of the edges of 0.1u.



Problem 5 Assume the MOS transistors are all operating in the saturation region and the Bipolar transistors are all operating in the Forward Active region.

a) Determine the output voltages V_{01} and V_{02} in terms of the MOS device dimensions, W and L , the emitter areas, and the resistor variables R_1, R_2, and R_3.

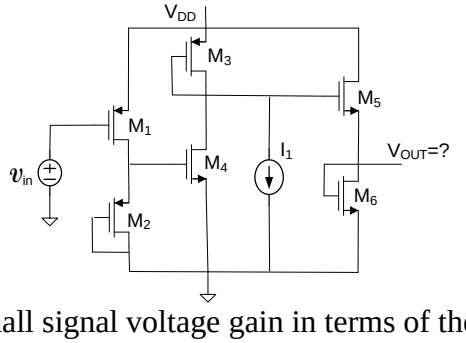
b) If R_1=60K, $A_{E1}=A_{E2}=100\mu^2$, $A_{E3}=25\ \mu^2$, $A_{E4}=300\ \mu^2$,W_5=10µ, L_5=1µ ,W_6=16µ, L_6=4µ, Determine R_2 and R_3 so that V_{01}=6V and V_{02}=3V.



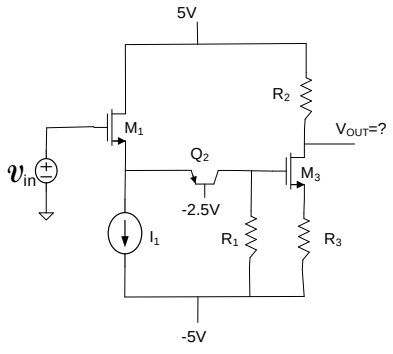
Problem 6 Consider the following amplifier structure where all devices are operating in the saturation region

a) Determine the small signal voltage gain in terms of the small-signal model parameters of the transistors.

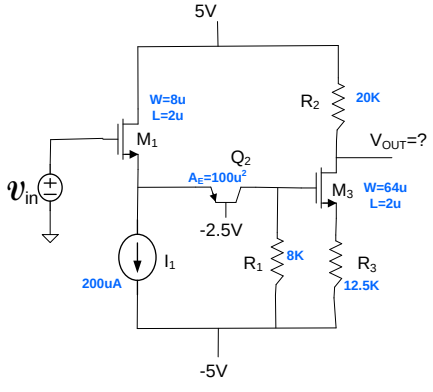
b) Assume V_{DD}=2V, I_1=500uA, and the quiescent current in transistors M_1,M_4, and M_5 is 500uA. Numerically determine the small signal voltage gain if the quiescent voltage on the gate of M_4 is 1V, the voltage on the gate of M_5 is 1.3V, and the quiescent output voltage is 0.7V. Be sure to use the model parameters given at the top of page 1 when solving this problem.



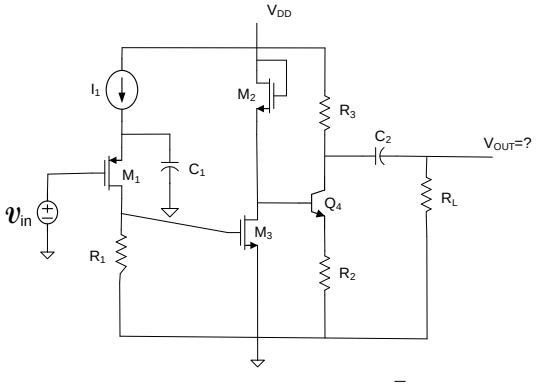
Problem 7 Determine the small signal voltage gain in terms of the small signal model parameters of the devices. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region. Assume the MOS transistors are in a 0.5u CMOS process with $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,V_{TNO}=0.5V, and V_{TP0}=-0.5V.



Problem 8 If the component values for the circuit in the previous problem are as shown below, numerically determine the small-signal voltage gain. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region. Assume the MOS transistors are in a 0.5u CMOS process with $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, and $V_{TP0}=-0.5V$.



Problem 9 Determine the small signal voltage gain in terms of the small signal model parameters of the devices. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region.

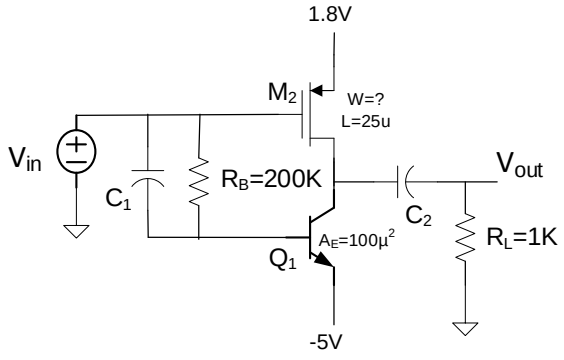


Problem 10 Design a noninverting amplifier using Bipolar transistors with a nominal voltage gain of 60 that has an input impedance larger than 100K and that can drive a 1K load resistor. Verify your design analytically and with SPICE.

Problem 11 Consider the circuit shown below. Assume the width of M_2 is selected so that the quiescent collector voltage of Q_1 is 0V and assume the capacitors C_1 and C_2 are large.

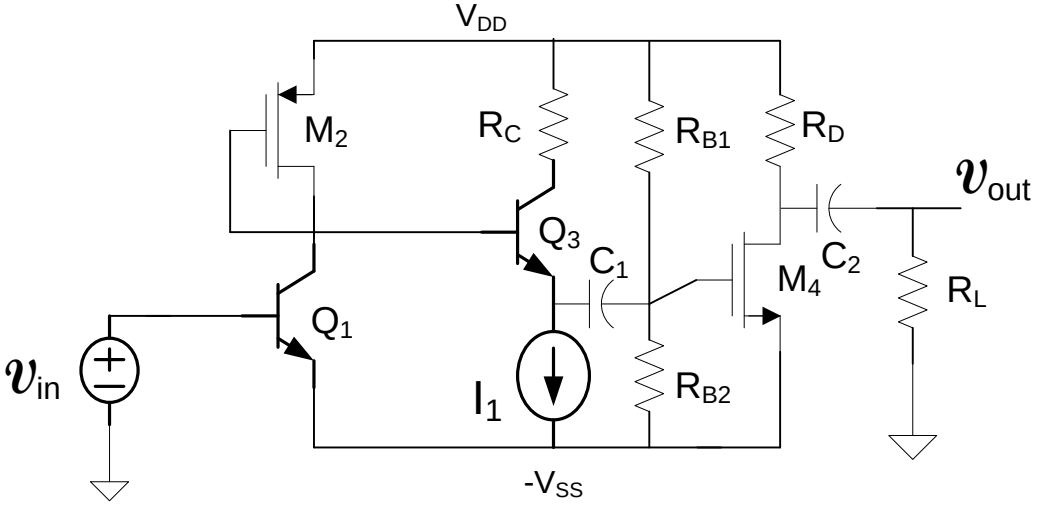
a) Determine the small signal voltage gain in terms of the small-signal model parameters and the resistor values in the circuit.

b) Determine the voltage v_{OUT} if v_{in}=0.01sin1000t.



Problem 12 Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

a) Draw the small signal equivalent circuit.
b) Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components



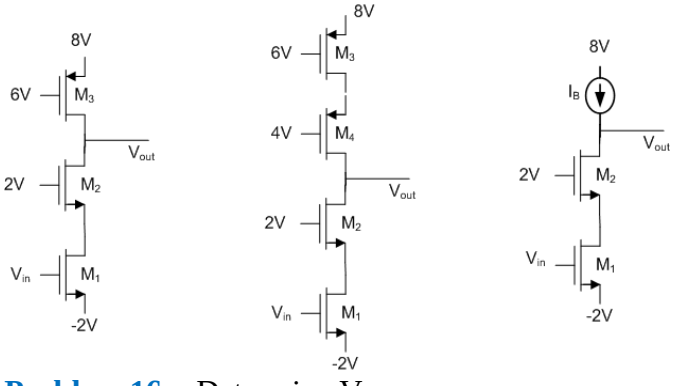
Problem 13 Use Modelsim to create a 4-bit shift register using the D flip-flops from the previous homework. The register should only change its value on a positive clock edge and include an enable bit. Create a test bench to test the correct operation of the shift register. Show multiple examples of loading and shifting. Include screenshots of your Verilog code, and simulation waveforms.

Problem 14 Assume you have available a 2mA sourcing current (one end connected to V_{DD}) and a single dc voltage source, V_{DD}.

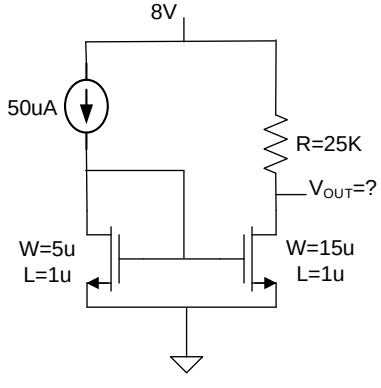
a) Design a current mirror that provides a sinking current of 200uA using MOS transistors.

b) What is the minimum voltage of the 200uA current source in your design for it to still work as a current mirror.

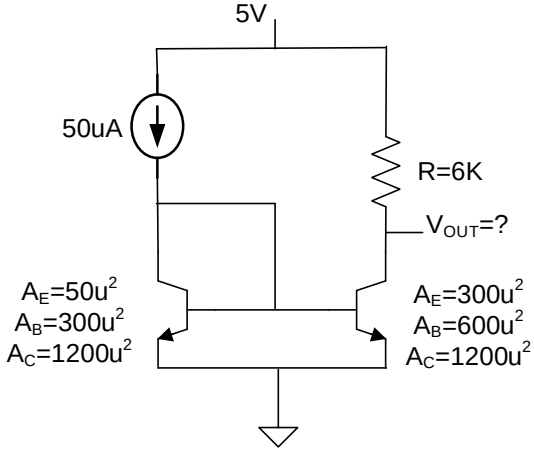
Problem 15 Assume the following circuits are all sized and biased so that all transistors are in the saturation region. Determine the small signal voltage gain in terms of the small signal device parameters and make a quantitative comparison of the relative gains of the three circuits



Problem 16 Determine V_{OUT}.



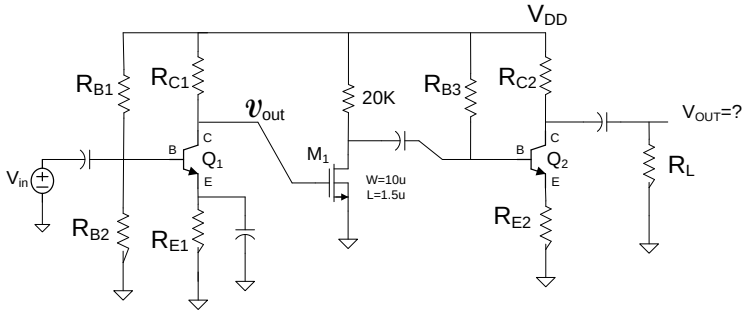
Problem 17 Determine V_{OUT}.



Problem 18 Design a current generator circuit that has output sinking currents of 10uA and 50uA. You have available MOS transistors, one resistor of value 200K, and a 5V dc voltage source.

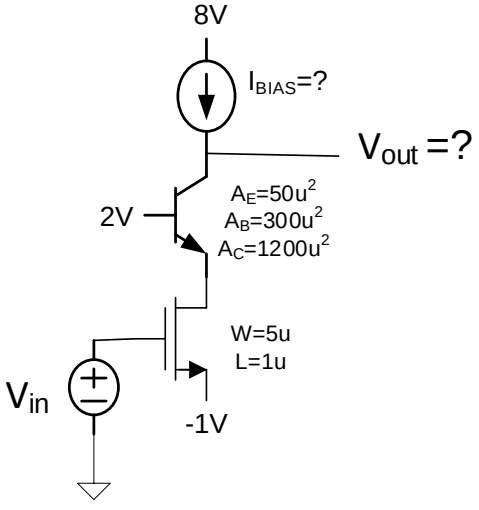
Problem 19 Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

a) Draw the small signal equivalent circuit.
b) Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components
c) Express the small signal voltage gain in terms of the quiescent values of I_{C1}, I_{D1}, I_{C2}, and the device model parameters (i.e. no small-signal parameters)



Problem 20

a) If the current I_{BIAS} is selected so that the quiescent output voltage is 4V, determine the small signal voltage gain of this circuit.
b) What is the approximate value of I_{BIAS} needed to establish V_{OUTQ}=4V?



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Problem 21 US Patent 5,952,884 describes a new current mirror. It is pictured on the first page of the patent.

a) What benefits do the inventors claim this current mirror has
b) Provide an analytical development that verifies the claims the inventors make

Problem 22 Identify one US patent that has been issued since 2002 that introduces a new current mirror. Give the current mirror schematic that is in the patent you identify and list the benefits the inventors claim this current mirror has.

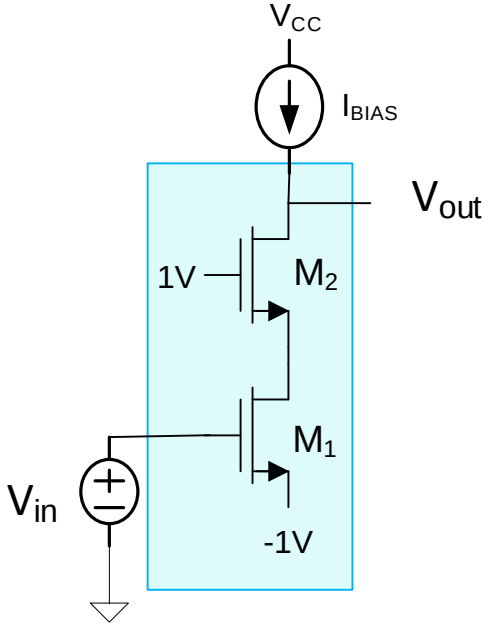
Problem 23 Consider the following circuit where M_1 and M_2 are matched with W=10u and L=2u.

a) Determine I_B so that the quiescent output voltage is 4V.

b) If the bias current obtained in Part a) were to change by .001%, how much change would occur in the quiescent output voltage?

c) Obtain an expression for the small-signal voltage gain in terms of the small-signal model parameters.

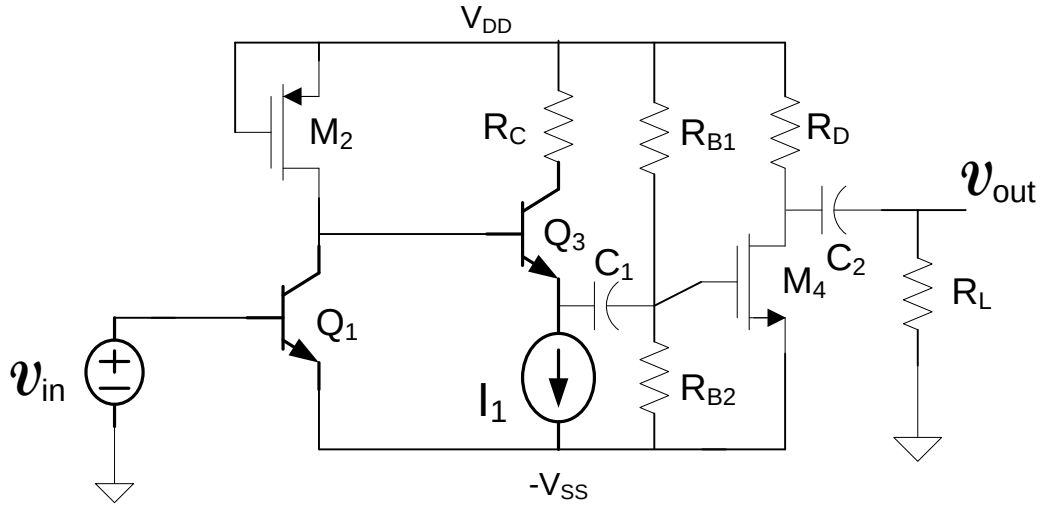
d) Determine a numerical value for the small-signal voltage gain.

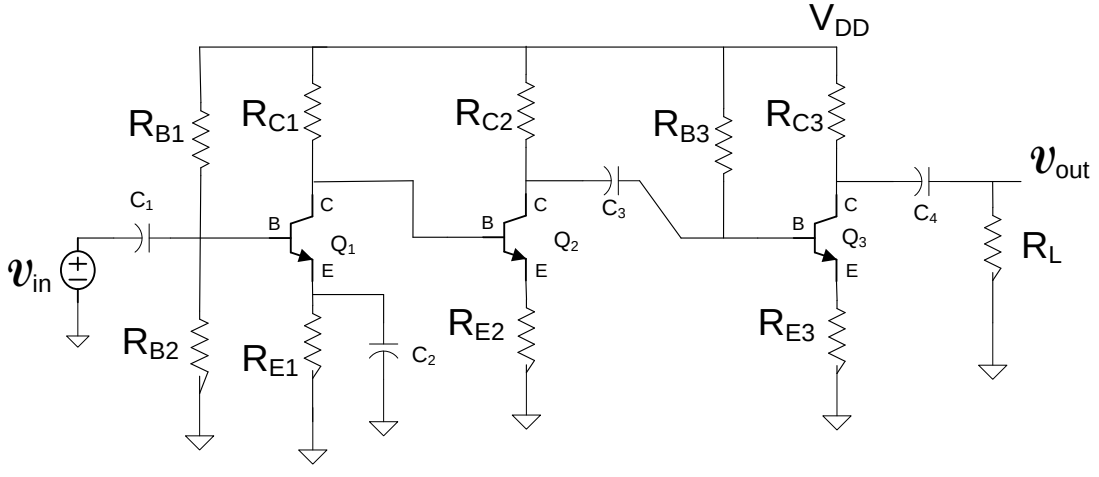


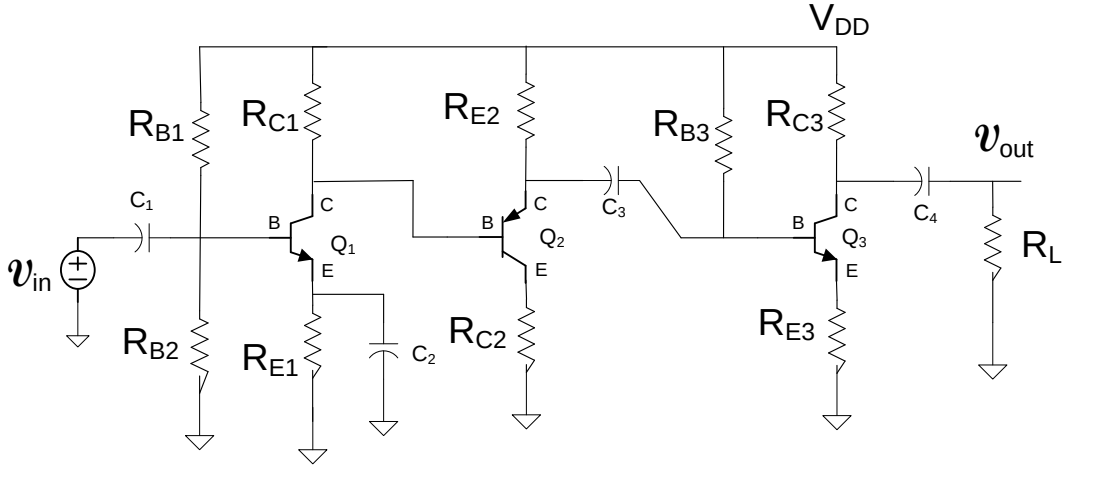
Problem 24-26 Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

c) Draw the small signal equivalent circuit.

d) Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components.


V_{DD}
M_2
R_C
R_{B1}
R_D
v_{out}
Q_3
C_1
C_2
M_4
R_L
Q_1
v_{in}
I_1
R_{B2}
$-V_{SS}$


V_{DD}
R_{B1}
R_{C1}
R_{C2}
R_{B3}
R_{C3}
v_{out}
C_1
C_3
C_4
B
C
E
Q_1
Q_2
Q_3
v_{in}
R_L
R_{B2}
R_{E1}
C_2
R_{E2}
R_{E3}


V_{DD}
R_{B1}
R_{C1}
R_{E2}
R_{B3}
R_{C3}
v_{out}
C_1
C_3
C_4
B
C
E
Q_1
Q_2
Q_3
v_{in}
R_L
R_{B2}
R_{E1}
C_2
R_{C2}
R_{E3}

Problem 27-30 Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

a) Draw the small signal equivalent circuit.

b) Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components. The last circuit has two outputs so there are two voltage gains for this circuit.