Problem 1:

Area of one transistor = $10\ nm * 10\ nm * 10 = 1000\ nm^2$

Diameter of wafer = $3.048 * 10^8\ nm$

Area of wafer = $(\frac{3.048*10^8}{2})^2 * \pi = 7.297 * 10^{16}\ nm$

Number of dies = $\frac{7.298*10^{16}\ nm^2}{2000*1000\ nm^2} = 3.649 * 10^{10}\ \frac{dies}{wafer}$

Problem 2:

The $\frac{cost}{die} = \frac{\$3500}{3.649*10^{10}} = \frac{\$9.592*10^{-8}}{die}$

Problem 3

Assuming that a circular ink drop diameter is 100 um:

$Area = (\frac{100*10^{-6}}{2})^2 * \pi = 7.854 * 10^9\ nm^2$

Number of transistors = $\frac{7.854*10^9\ nm\text{^}2}{1000\ nm^2} = 7.854 * 10^6$

Problem 4:

Some can be turned off when not needed. Lower frequency means less power consumed by parasitics.

Problem 5:

Feature size of 10 nm process = 10 nm

Diameter of a silicon atom = 210 pm = 0.210 nm

$\frac{10\ nm}{.210\ nm} = 47.62$ times larger.

Diameter of SiO_2 about 310 pm = .310 nm

$\frac{10\ nm}{.310\ nm} = 32.26$ times larger.

Diameter of a human hair = 100 um = 100,000 nm

$\frac{10\ nm}{100{,}000\ nm} = \frac{1}{1000}$ the diameter of a human hair.

Problem 6

Intel:	$59.38 Billion
Saudi Aramco:	$311 Billion
Nestle	$92.55 Billion

Problem 7:

a) Feature size = 14nm
b) Die area = 82 mm^2
c) Transistor area = $\frac{82\ mm^2}{1{,}400{,}000{,}000} = 58.572 * 10^3\ nm^2$
d) Active Area = $14\ nm * 14\ nm = 196\ nm^2$
   $\frac{Active\ Area}{Average\ Area} = \frac{196\ nm}{58{,}572\ nm} = 0.003345 = 0.335\%$ of the average area is active area
   This can also be read as the average area is 298.8 times the active area.

Problem 8:

a) For Core Intel i7 3930k P = 123.69W
   Current at 1.2V = $I = \frac{P}{V} = \frac{123.69W}{1.2V} = 103A$
b) For gold wire ρ = 1.16Ω/inch
   $R = \rho * L = 1.16\Omega * \frac{1}{2} = 0.58\Omega$
   $V = I * R = 59.78V$
c) Power Dissipated = $P = I^2 * R = 103^2 * 0.58 = 6153\ W$
d) Fusing Current = $0.6 \sim 0.7\ A$
   Actual Current = $0.06 \sim 0.07\ A$
   Number of wires = $\frac{103}{.06} \sim \frac{103}{.07} = 1471 \sim 1717$ gold wired

Problem 9:

Type	Storage Density (Bit/cm^2)	Cost of Storage ($/bit)	
CD	10^7	10^{-11}	
DVD	10^8	10^{-12}	Lowest
Blue Ray	10^9	10^{-12}	Lowest
Hard Disk	10^{10}	10^{-12}	Lowest
SRAM	10^7	10^{-6}	Highest
DRAM	10^9	10^{-9}	
FLASH	10^{10}	10^{-10}	

Ratio $= \frac{10^{-6}}{10^{-12}} = 10^6$

Problem 11:

Techcrunch and HIS Markit report approximately 6.1 billion smartphones will be in use by 2020.

Problem 12:

From Gartner.com

Android	81.7%
iOS	17.9%
Windows	0.3%
BlackBerry	0.0%
Other	0.1%

Problem 13:

From Gartner.com

Worldwide Smartphone sales in 2016 – 1,495,358,000

Worldwide Smartphone users in 2016 – 2,100,000,000

About 70% of smartphone users bought a new phone in 2016. This creates a large market potential each year and implies the useful life of a smartphone is about 1 – 2 years.

Problem 14:

Number of full time engineers = $\frac{\$500*.1*1495358000}{\$60000} = 1.25 * 10^6$ engineers

Problem 15:

Area of Skylane Chip = 82 mm^2

a) Number of Skylane Chips/wafer = $\frac{(\frac{450\ mm}{2})^2 * \pi}{82\ mm^2} = 1939$

b) Cost = $\frac{\$2500}{1940*0.9} = \frac{\$1.43}{chip}$

Problem 16:

/home/jaaymond/ee330/verilog/EE330Hom

```
Ln#
 1  `timescale 1ns/1ps
 2
 3  module HW1_2NOR(iA, iB, out);
 4    input iA, iB;
 5    output out;
 6    wire out;
 7
 8    assign out = ~(iA | iB);
 9  endmodule
10
11
12
```

/home/jaaymond/ee330/verilog/EE330Homework/

```
Ln#
 1  `timescale 1ns/1ps
 2
 3  module HW1_3AND(iA, iB, iC, out);
 4    input iA, iB, iC;
 5    output out;
 6    wire out;
 7
 8    assign out = iA*iB*iC;
 9  endmodule
10
11
```

/home/jaaymond/ee330/verilog/EE330Homework/HW1_tb.v (/HW1_tb) - Defau

```
Ln#
 1  `timescale 1ns/1ps
 2  module HW1_tb();
 3    reg a, b, c;
 4    wire oAnd, oNor;
 5    HW1_3AND myAnd( .iA(a), .iB(b), .iC(c), .out(oAnd) );
 6    HW1_2NOR myNor( .iA(a), .iB(b), .out(oNor) );
 7
 8    initial
 9    begin
10      a = 1'b0; b = 1'b0; c = 1'b0;
11      #20;
12      a = 1'b0; b = 1'b0; c = 1'b1;
13      #20;
14      a = 1'b0; b = 1'b1; c = 1'b0;
15      #20;
16      a = 1'b0; b = 1'b1; c = 1'b1;
17      #20;
18      a = 1'b1; b = 1'b0; c = 1'b0;
19      #20;
20      a = 1'b1; b = 1'b0; c = 1'b1;
21      #20;
22      a = 1'b1; b = 1'b1; c = 1'b0;
23      #20;
24      a = 1'b1; b = 1'b1; c = 1'b1;
25
26    end
27
28  endmodule
29
```