EE 330 Fall 2012
Homework 6

Due Friday September 28 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

If parameters are needed for process characterization beyond what is specified in a problem, use the measured parameters from the AMI 0.5µ (now ON) or the IBM 0.13µ process runs that are attached.

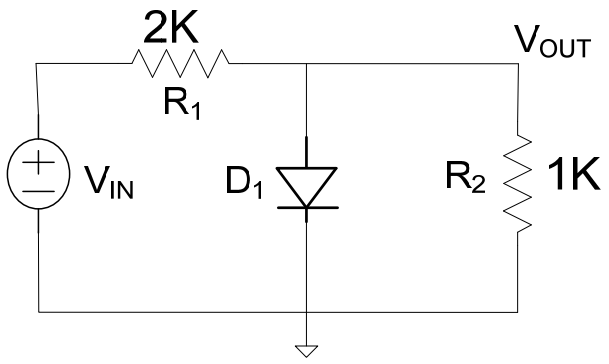
Problem 1 (10 points):
Size an n-channel transistor in the AMI 0.5u CMOS process so that the impedance in the switch-level model is 1000Ω when operating with a 3.5V power supply. Repeat for an n-channel transistor in the IBM 0.13u CMOS process when operating with a 1.5V supply.

Problem 2 (5 points):
If a minimum-sized inverter designed in the IBM 0.13u CMOS process could directly drive a minimum-sized inverter designed in the AMI 0.5u CMOS process, what would be t_{HL} and t_{LH}? Assume a supply voltage of 1.5V. Neglect any interconnect parasitics.

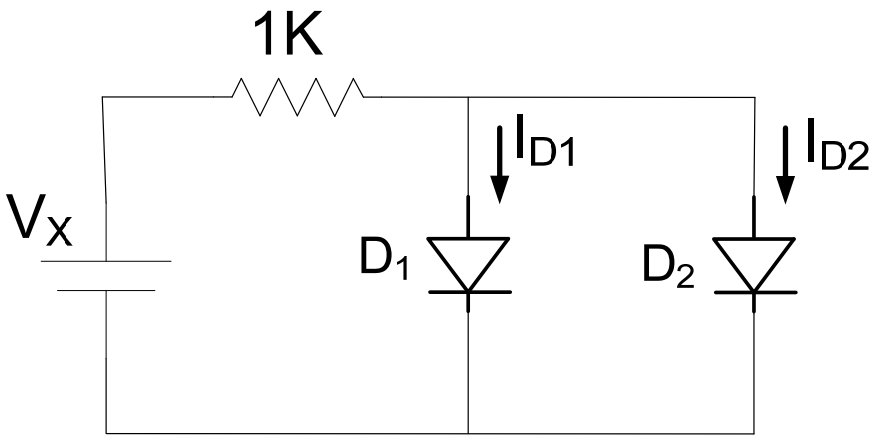
Problem 3 (5 points):
Using the short-channel α-law model, determine the impedance in the switch-level model of the MOSFET for a square (W=L) n-channel device if the short-channel device has the same μC_{OX} and V_T as in the IBM 0.13µ process but with short-channel parameters $\theta 1=\theta_2=1/2$ and $\alpha=1.25$. Comment on how the short-channel effect changes the switching performance of the MOSFET.

Problem 4 (10 points):
Consider the below circuit

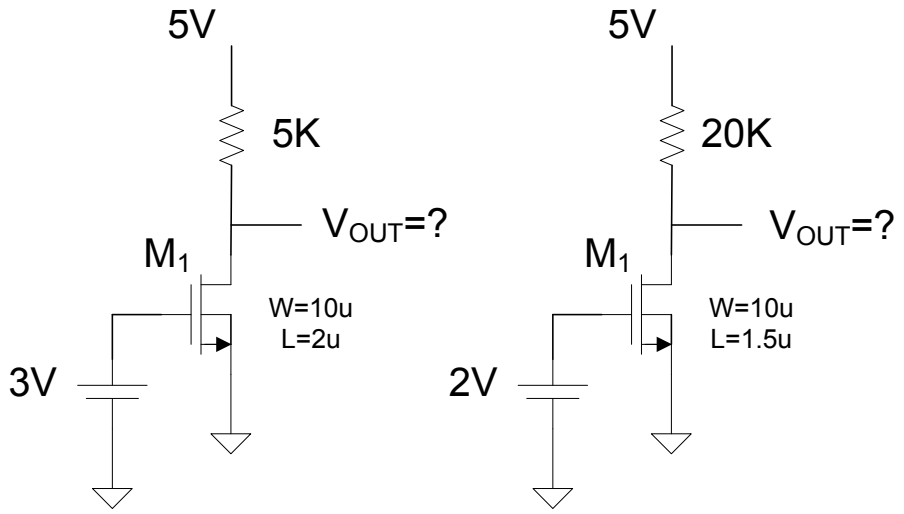
a) Obtain the voltage V_{OUT} if V_{IN}=-8V.
b) Obtain the current through R_2 if V_{IN}=5V
c) Obtain an expression for V_{OUT} and plot it for one period of the input is V_{IN} = 5sin1000t



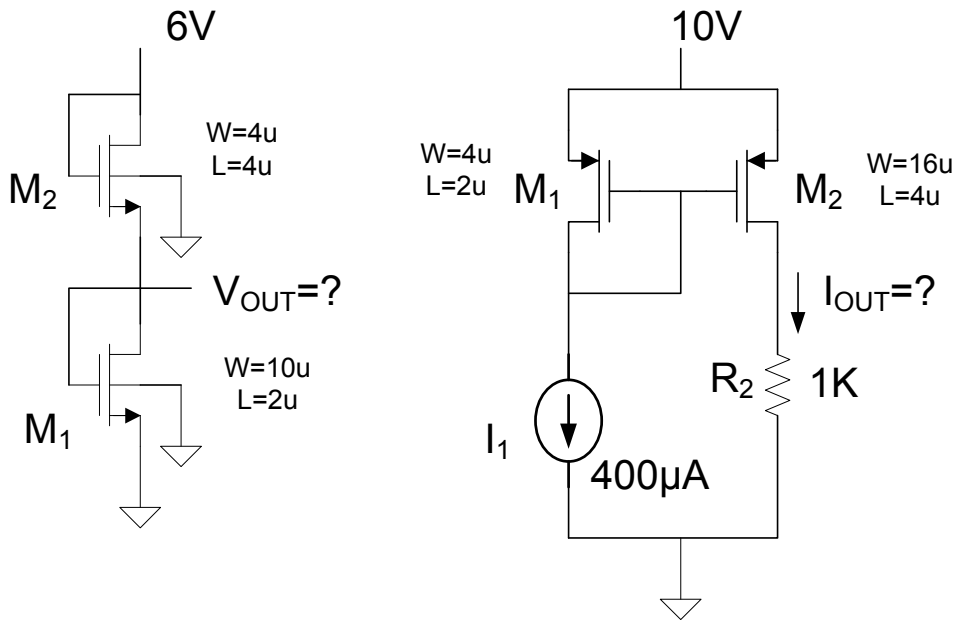
Problem 5 (10 points):
Assume the junction area of D_1 is $100\mu^2$ and that of D_2 is 4 times as large. Determine the current I_{D1} if V_X=1.5V. Assume J_S to be $5fA/\mu^2$.



Problem 6 (10 points):
Analytically determine the variable indicated by a "?" in the below circuits. Assume the devices are in a process with V_{TN}=1V, and $\mu_n C_{OX}=100\mu AV^{-2}$



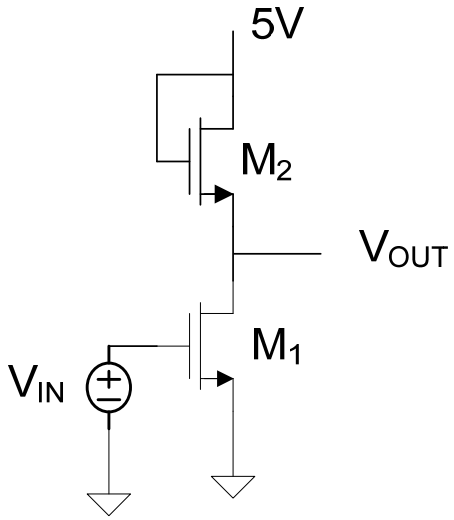
Problem 7 (10 points):
Analytically determine the variable indicated by a "?" in the below circuits. Assume the devices are in a process with V_{TN}=1V, V_{TP}=-1V, $\mu_n C_{OX}$=100μAV^{-2} and $\mu_p C_{OX}$=33μAV^{-2}.



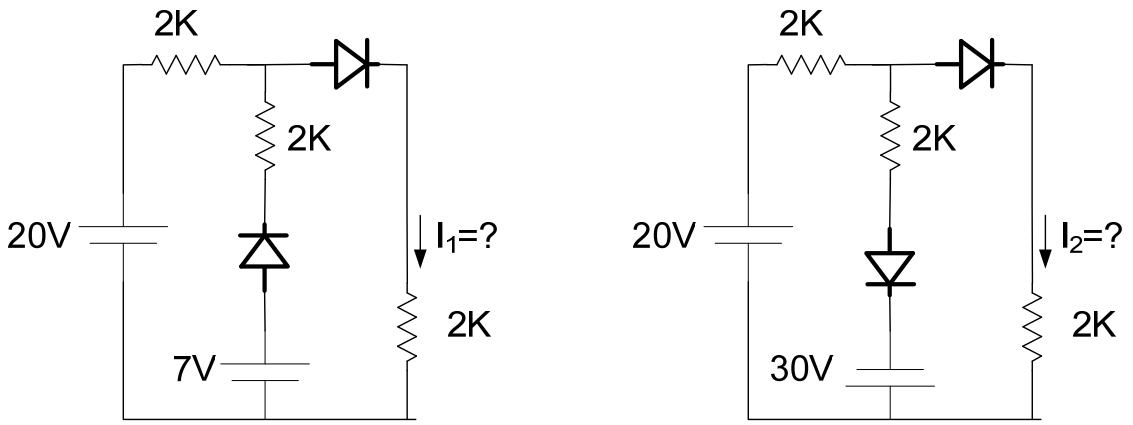
Problem 8 (15 points):
Consider the below circuit.

a) If V_{IN}=3V, determine the dimensions of M_1 that will result in an output voltage of 2V. Assume that the dimensions of M_2 are W_2=10u and L_2=1u. The model parameters of the devices are V_{TN}=1V, V_{TP}=-1V, $\mu_n C_{OX}$=100μAV^{-2} and $\mu_p C_{OX}$=33μAV^{-2}.

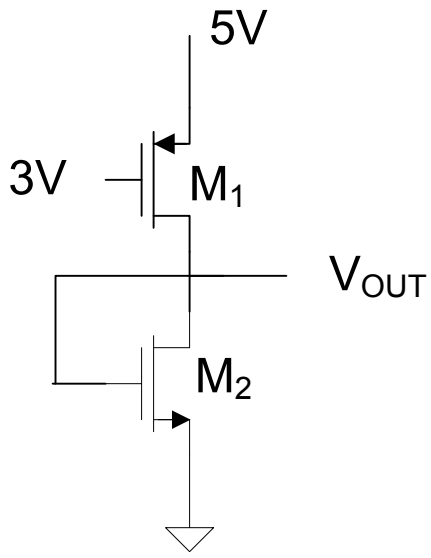
b) Repeat part a) if the goal is to have an output voltage of 0.5V.



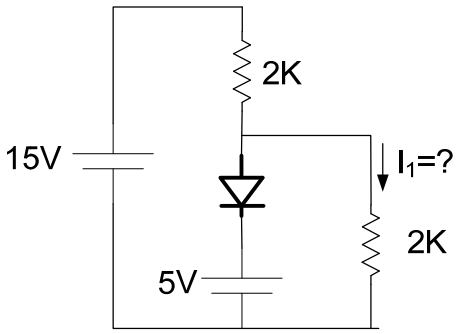
Problem 9 (10 points):
Determine the currents indicated with a "?" in the below circuits. Assume the diodes are ideal.

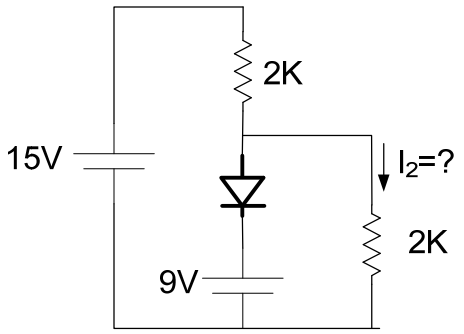


Problem 10 (10 points):
Determine V_{OUT} for the below circuit. Assume the devices M_1 and M_2 are identically sized with W=L=5u. The model parameters of the devices are VTN=1V, V_{TP}=-1V, $\mu_n C_{OX}$=100μAV^{-2} and $\mu_p C_{OX}$=33μAV^{-2}.



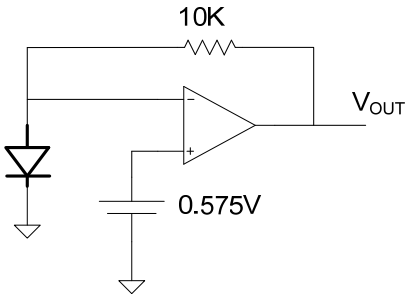
Problem 11 (Extra Credit of 10 points):
Determine the currents indicated with a "?" in the below circuits. Assume the diodes are ideal.





Problem 12 (Extra Credit of 10 points):
Assume the op amp is ideal and biased with V_{DD}=20Vand V_{SS}=-20V and the diode is characterized by model parameters: J_{SX}=0.5A/μ^2, V_{G0}=1.17V, m=2.3. Assume the area of the junction is 100u^2.

a) Determine V_{OUT} if T= -20°C
b) Repeat part a) if T= 40°C.
c) Repeat part a) if T=120°C



Problem 13 (Extra Credit of 20 points):
Using Verilog, build a counter that outputs to a seven segment display. Whenever the INPUT makes a low to high transition, the counter should increase by one. This should be reflected by the seven segment display. Each bit of the seven segment display is controlled by an individual output. A high output corresponds to a lit segment while a low output causes an unlit segment. The counter should go back to zero upon passing 9. Label your outputs clearly and prove your design with sufficient testing.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T86S VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		463	-248	uA/um
Vth		0.67	-0.91	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.8	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.49	0.57	V^0.5
K' (Uo*Cox/2)		57.8	-19.1	uA/V^2
Low-field Mobility		475.38	157.09	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	84.4	109.2	22.9	1102	41.9	0.09	0.09	ohms/sq
Contact Resistance	60.9	150.6	15.8		26.8		0.81	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	818	808	ohms/sq
Contact Resistance	0.81			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	426	724	85		30	15	9	37	aF/um^2
Area (N+active)			2434		34	17	12		aF/um^2
Area (P+active)			2351						aF/um^2
Area (poly)				899	56	16	9		aF/um^2
Area (poly2)					46				aF/um^2
Area (metal1)						33	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	361	241			71	49	33		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						46	34		aF/um
Fringe (metal2)							54		aF/um
Overlap (N+active)			292						aF/um
Overlap (P+active)			387						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.04	volts
Vinv	1.5	2.29	volts
Vol (100 uA)	2.0	0.12	volts
Voh (100 uA)	2.0	4.86	volts
Vinv	2.0	2.47	volts
Gain	2.0	-18.26	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		98.75	MHz
D256_WIDE (31-stg,5.0V)		153.47	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.00	uW/MHz/gate

COMMENTS: SUBMICRON

MOSIS WAFER ACCEPTANCE TESTS

RUN: T85X (8WL_8LM_OL) VENDOR: IBM-BURLINGTON
TECHNOLOGY: SIGE013 FEATURE SIZE: 0.13 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SIGE8WL_IBM-BU

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.16/0.12			
Vth		0.41	-0.42	volts
SHORT	20.0/0.12			
Idss		406	-178	uA/um
Vth		0.43	-0.42	volts
Vpt		3.6	-3.6	volts
WIDE	20.0/0.12			
Ids0		155.2	-127.9	pA/um
LARGE	20.0/20.0			
Vth		0.12	-0.23	volts
Vjbkd		2.7	-3.2	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.28	0.23	V^0.5
K' (Uo*Cox/2)		308.0	-48.8	uA/V^2
Low-field Mobility		553.02	87.62	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	UNITS
Sheet Resistance	6.7	6.3	6.6					ohms/sq
Sheet Resistance				78	51	50	50	mohms/sq
Contact Resistance	9.4	9.2	8.3		0.68	1.37	2.00	ohms
Gate Oxide Thickness	31							angstrom

PROCESS PARAMETERS	M5	M6	M7	M8	N_W	PPLY+BLK	N+BLK	POLY_NON	POLY_NON TaN	UNITS
Sheet Resistance	41	44	7	7.4						mohms/sq
Sheet Resistance					327	321.2	73.4	231.6	1547.4 58.9	ohms/sq
Contact Resistance	2.19	2.51	2.51	2.53						ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	M7	M8	TaN	MiM	UNITS
Area (substrate)	973	1203	109	57	41	32	27	23	20	17	14	24		aF/um^2
Area (N+active)		11176												aF/um^2
Area (P+active)		10496												aF/um^2
Area (r well)	605													aF/um^2
Area (N+ HA varactor)		2390												aF/um^2
Area (M1)			128											aF/um^2
Area (M2)				171										aF/um^2
Area (M3)					182									aF/um^2
Area (M4)						176								aF/um^2
Area (M5)							82							aF/um^2
Area (M6)								81						aF/um^2
Area (M7)									45					aF/um^2
Area (M8)										85				aF/um^2
Area (MiM)													4100	aF/um^2
Fringe (substrate)	60	68												aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.50	volts
Vinv	1.5	0.52	volts
Vol (100 uA)	2.0	0.01	volts
Voh (100 uA)	2.0	1.18	volts
Vinv	2.0	0.53	volts
Gain	2.0	-18.48	
Ring Oscillator Freq.			
DIV1024 (31-stg,1.2V)		376.81	MHz
D1024_THK (31-stg,2.5V)		279.93	MHz
Ring Oscillator Power			
DIV1024 (31-stg,1.2V)		5.13	nW/MHz/gate
D1024_THK (31-stg,2.5V)		26.50	nW/MHz/gate
Operational Amplifier			
Gain		10	

COMMENTS: DEEP_SUBMICRON