

EE 330

Homework 5

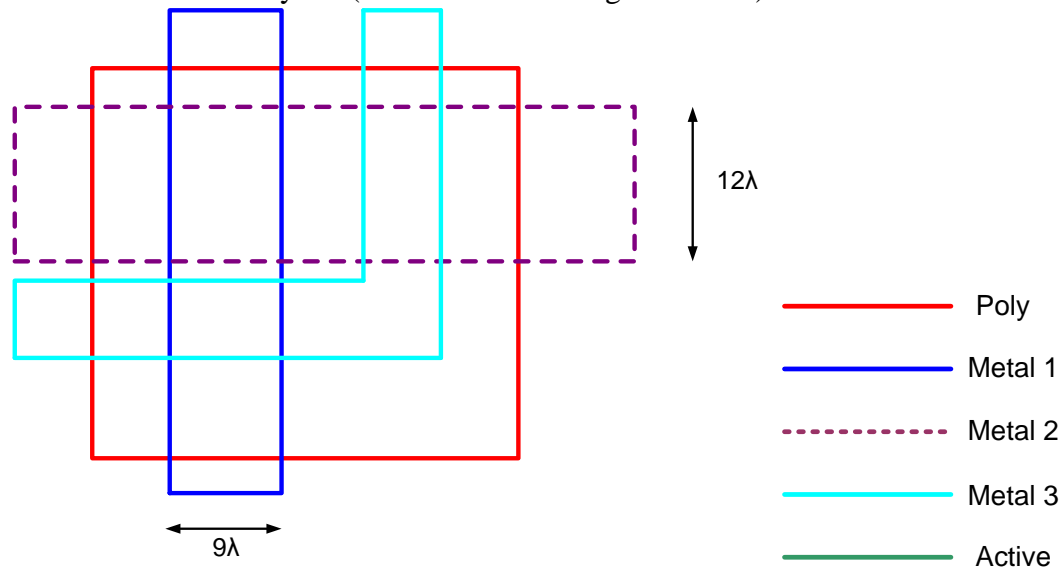
Spring 2018 (This assignment is due Friday Feb. 9)

Assume the CMOS process is characterized by model parameters $V_{TH}=1V$ and $\mu C_{OX}=100\mu A/V^2$. If any other model parameters are needed, use the measured parameters from the ON T6AU process run that are attached. On those problems that involve the design of passive components, a sketch of the design is sufficient provided you indicate dimensions (i.e. it need not be done in Cadence).

Problem 1 Design a 3K resistor in the ON 0.5 μ CMOS process. Use Poly 1 for the resistor. The width-length ratio of an imaginary box enclosing the resistor should have a W/L ratio of between 1:2 and 2:1. The layout of the resistor can be either sketched or come from a Cadence layout.

Problem 2 Design a 500fF capacitor in the ON 0.5 μ CMOS process. Clearly specify which layers you are using for this capacitor. The layout of the capacitor can be either sketched or come from a Cadence layout.

Problem 3 Four non-contacting regions are shown. Identify the parasitic capacitances and their size if this is fabricated in the 0.5 μ CMOS process. Don't forget that there is substrate below all layers. (assume this drawing is to scale)



Problem 4 Assume a resistor has a resistance of 4.534K Ω at $T=250^\circ K$. If the TCR of this resistor is constant of value 1200 ppm/ $^\circ C$, what will be the resistance at $T=320^\circ K$?

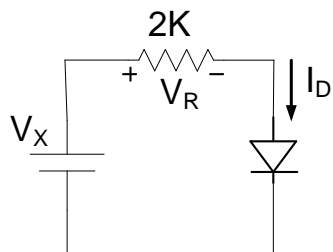
Problem 5 Consider an n+ diffused resistor that is 50 μ long and 2 μ wide. What is the nominal value of the resistance if it is doped with Arsenic and the doping density is $2E14/cm^3$.

Problem 6 Consider a 15K resistor that is made by the series connection of two resistors. One of the resistors is a n+ doped 5K polysilicon resistor with a TCR of -1400 ppm/°C and the other is a p+ diffused silicon 10K resistor with a TCR of 900 ppm/°C. What is the TCR of the series combination? How does this compare to the TCR that would be achieved if the 15K resistor were made entirely with n+ doped polysilicon?

Problem 7 Consider a Poly 1 interconnect in the 0.5μ CMOS process that is 1μ wide and 100μ long. What is the resistance of this interconnect? What is the capacitance from this interconnect to the substrate? If Metal 1 is above this interconnect, what is the capacitance between this interconnect and Metal 1?

Problem 8 If the voltage of a forward-biased pn junction is varied between 0.5V and 0.6V, what is the range in the diode current. Assume the junction area of the diode is $50\mu^2$ and $J_S=10^{-15}\text{A}/\mu^2$.

Problem 9 Determine the current I_D (within $\pm 5\%$) if $V_X=10\text{V}$ for the following circuit. Assume the area of the diode is $200\mu^2$ and $J_S=10^{-15}\text{A}/\mu^2$.



Problem 10 Repeat Problem 5 if $V_X=520\text{mV}$.

Problem 11 and 12 Use Modelsim to create a 3-8 decoder. The truth table for the decoder is attached for reference. Include screenshots of your Verilog code, and simulation waveforms.

Inputs			Outputs							
A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU
TECHNOLOGY: SCN05
microns

VENDOR: AMIS
FEATURE SIZE: 0.5

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS

from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
	M3	N\PLY	N_W					UNITS
Sheet Resistance	0.05	824	816					ohms/sq
Contact Resistance	0.79							ohms

Gate Oxide Thickness 142

angstrom

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg, 5.0V)		95.31	MHz
D256_WIDE (31-stg, 5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg, 5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg, 5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON
T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 11/07
* LOT: T6AU WAF: 7101
* Temperature_parameters=Default

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ = 1.5E-7           NCH = 1.7E17       TOX = 1.42E-8
+K1 = 0.8976376        K2 = -0.09255      VTH0 = 0.629035
+K3B = -8.2369696      W0 = 1.041146E-8    K3 = 24.0984767
+DVT0W = 0             DVT1W = 0          NLX = 1E-9
+DVT0 = 2.7123969      DVT1 = 0.4232931   DVT2W = 0
+U0 = 451.2322004      UA = 3.091785E-13  DVT2 = -0.1403765
+UC = 1.22401E-11      VSAT = 1.715884E5  UB = 1.702517E-18
+AGS = 0.130484        B0 = 2.446405E-6    A0 = 0.6580918
+KETA = -3.043349E-3   A1 = 8.18159E-7      B1 = 5E-6
+RDSW = 1.367055E3     PRWG = 0.0328586     A2 = 0.3363058
+WR = 1                WINT = 2.443677E-7  PRWB = 0.0104806
+XL = 1E-7             XW = 0             LINT = 6.999776E-8
+DWB = 3.676235E-8     VOFF = -1.493503E-4    DWG = -1.256454E-8
+CIT = 0               CDSC = 2.4E-4       NFACTOR = 1.0354201
+CDSCB = 0             ETA0 = 2.342963E-3  CDSCD = 0
+DSUB = 0.0764123      PCLM = 2.5941582     ETAB = -1.5324E-4
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505  PDIBLC1 = 0.8187825
+PSCBE1 = 6.611774E8   PSCBE2 = 3.238266E-4  DROUT = 0.9919348
+DELTA = 0.01          RSH = 83.5         PVAG = 0
+PRT = 0               UTE = -1.5         MOBMOD = 1
+KT1L = 0              KT2 = 0.022         KT1 = -0.11
+UB1 = -7.61E-18       UC1 = -5.6E-11      UA1 = 4.31E-9
+WL = 0                WLN = 1           AT = 3.3E4
+WWN = 1               WWL = 0           WW = 0
+LLN = 1               LW = 0            LL = 0
+LWL = 0               CAPMOD = 2         LWN = 1
+CGDO = 2.32E-10       CGSO = 2.32E-10      XPART = 0.5
+CJ = 4.282017E-4      PB = 0.9317787     CGBO = 1E-9
+CJSW = 3.034055E-10   PBSW = 0.8           MJ = 0.4495867
+CJSWG = 1.64E-10      PBSWG = 0.8          MJSW = 0.1713852
+CF = 0                PVTH0 = 0.0520855  MJSWG = 0.1713852
+PK2 = -0.0289036      WKETA = -0.0237483  PRDSW = 112.8875816
                        LKETA = 1.728324E-3
*)
*
```

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.MODEL CMOSF PMOS (
+VERSION = 3.1
+XJ      = 1.5E-7
+K1      = 0.5464347
+K3B     = -0.8373484
+DVT0W   = 0
+DVT0    = 2.0973823
+U0      = 220.5922586
+UC      = -6.19354E-11
+AGS     = 0.1447245
+KETA    = -1.093365E-3
+RDSW    = 3E3
+WR      = 1
+XL      = 1E-7
+DWB     = 1.706031E-8
+CIT      = 0
+CDSCB   = 0
+DSUB    = 1
+PDIBLC2 = 3.201161E-3
+PSCBE1  = 4.876974E9
+DELTA   = 0.01
+PRT     = 0
+KT1L    = 0
+UB1     = -7.61E-18
+WL      = 0
+WWN     = 1
+LLN     = 1
+LWL     = 0
+CGDO    = 3.12E-10
+CJ      = 7.254264E-4
+CJSW    = 2.496599E-10
+CJSWG   = 6.4E-11
+CF      = 0
+PK2     = 3.73981E-3
)
*
TNOM     = 27
NCH      = 1.7E17
K2       = 8.119291E-3
W0       = 1.30945E-8
DVT1W   = 0
DVT1     = 0.5356454
UA       = 3.144939E-9
VSAT     = 1.176415E5
B0       = 1.149181E-6
A1       = 3.467482E-4
PRWG     = -0.0418549
WINT     = 3.007497E-7
XW       = 0
VOFF     = -0.0801591
CDSC     = 2.4E-4
ETA0     = 0.4060383
PCLM     = 2.2703293
PDIBLCB  = -0.057478
PSCBE2   = 5E-10
RSH      = 105.3
UTE      = -1.5
KT2      = 0.022
UC1      = -5.6E-11
WLN      = 1
WWL      = 0
LW       = 0
CAPMOD   = 2
CGSO     = 3.12E-10
PB       = 0.9682229
PBSW     = 0.99
PBSWG    = 0.99
PVTH0    = 5.98016E-3
WKETA    = 7.286716E-4
LEVEL    = 49
TOX      = 1.42E-8
VTH0     = -0.9232867
K3       = 5.1623206
NLX      = 5.772187E-8
DVT2W   = 0
DVT2     = -0.1185455
UB       = 1E-21
A0       = 0.8441929
B1       = 5E-6
A2       = 0.4667486
PRWB     = -0.0212201
LINT     = 1.040439E-7
DWG      = -2.133809E-8
NFACTOR  = 0.9468597
CDSCD    = 0
ETAB     = -0.0633609
PDIBLC1  = 0.0279014
DROUT    = 0.1718548
PVAG     = 0
MOBMOD   = 1
KT1      = -0.11
UA1      = 4.31E-9
AT       = 3.3E4
WW       = 0
LL       = 0
LWN      = 1
XPART    = 0.5
CGBO     = 1E-9
MJ       = 0.4969013
MJSW     = 0.386204
MJSWG    = 0.386204
PRDSW    = 14.8598424
LKETA    = -4.768569E-3

```