Project 8 Transceiver Block

This project is for the design of a transceiver integrated circuit. The design should be in a 0.5u CMOS process and include layout and post-layout simulation results.

Serial channels are widely used for communicating between computers that may be a few feet apart of on the other side of the world. The data that is to be transmitted is parallel data so a parallel to serial conversion is needed to get the data ready for transmission and a serial to parallel conversion is needed to convert the data from serial data to parallel data at the receiver. The data is transmitted from a synchronous system on transitions of a clock and the data at the received is synchronized relative to a clock at the receiver. The two clock frequencies may not be exactly the same and it is generally considered impractical to transmit the clock signal to the output so the clock must be recovered from the serial data stream itself. This is often done with a phase-locked loop (PLL) at the receiver which contains an internal voltage controlled oscillator (VCO) that must be "locked" to the input data sequence. The "recovered" clock is simply the output of the VCO in the PLL. The PLL must obtain regular measurements of the phase difference between the VCO output and the data input to maintain lock.

It is common in many applications to have periods of time where no data is available and during these intervals, long strings long serial strings of 0's or 1's must be transmitted. Unfortunately, it is difficult (actually impossible) for the PLL to maintain lock in the absence of transitions on the incoming data stream. To circumvent this problem, the parallel data is often coded prior to serial transmission to guarantee that there will be ample transitions in the transmitted data to recover the clock. Of course, the received data must be decoded at the output to recover the intended data sequence. 8B: 10B and 4B:5B coders are often used for this purpose. In an nB: (n+1)B coder, an n-bit word is converted to an n+1 bit word with a fixed mapping that will guarantee that the maximum number of consecutive 0's and 1's in the transmitted data stream is small (like 3 or 4) irrespective of the nature of the input data.

In many communication channels, data itself is arranged in packets in which a fixed number of bytes are put together sequentially to form a packet. A header is generally placed at the front of each packet. This header serves two purposes. One is to give information about where the packet is to go or where it comes from. The second is to allow for synchronization of the packet so that the bytes within the packet can be appropriately framed.

The design of transceivers which perform these functions is widely undertaken in industry but it is beyond the scope of this course. This project will focus on a part of a transceiver block associated with the encoder and decoder. The PLL that is usually used for clock and data recovery is not a part of this project. Details follow.

a) Devise a 4B-5B coding scheme that will guarantee at most 3 consecutive 0's or 1's for any input data sequence.

b) Design a circuit that will take an 8-bit wide parallel data sequence at 10K bytes/sec and serialize it using the 4B-5B coding scheme you devised in part a). You may assume that a 10KHz clock is present that is synchronous with the input data.

c) Design a receiver that will take the serial data string, decode it, and recreate an 8-bit wide data sequence at the output.

d) Design a "comma detect" circuit that will allow for proper framing of the received data. The "comma" should be a 10-bit code that cannot represent any data sequence. The "comma" would be inserted in place of a byte in the transmitted data stream for synchronization and the receiver should frame the received data relative to the detected "comma" whenever a comma is detected. After the "comma" is detected, the received should be in synch with the input data sequence.