EE330
Homework 8
Fall 2017
Solutions – TA: Joseph Aymond

Problem 1

Assume BJT works in forward active region

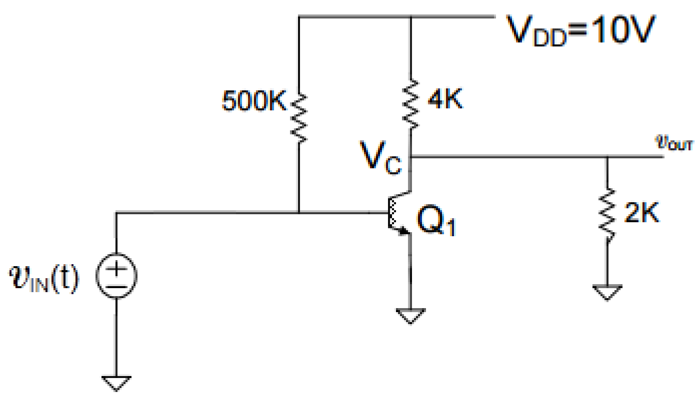
$I_B = \left(\frac{10 - 0.6}{500k}\right) = 18.8\mu A$

$I_C = \beta I_B = 100 * 18.8\mu A = 1.88mA$

$V_C = 10 - 4000 * 0.00188 = 2.48V$

$V_{out} = 0V$ (there is a capacitor creating an open circuit in DC.)

Small signal equivalent circuit:



Problem 2

For the MOSFET to be in saturation $V_{DS} \geq V_{GS} - V_T$

$V_{out} + 2 \geq 2 - 0.5 \rightarrow V_{out} \geq -0.5$

$I_D = \frac{\mu_n C_{OX} W}{2L}(V_{GS} - V_T)^2 = \frac{4 - V_{out}}{R_1} \rightarrow V_{out} = 4 - 337.5 * 10^{-6} * R_1 \geq -0.5V$

$\rightarrow R_1 \leq 13.3k\Omega$

Problem 3

$\frac{R_1}{2} = 6.666k\Omega$

$A_V = \frac{2I_{DQ}R}{V_{SS} + V_T} = \frac{4.5\ V}{-1.5\ V} = -3$

Problem 4

Assuming that M_1 and M_2 are in saturation

$$I_{D_1} = I_{D_2} \rightarrow \frac{\mu_n C_{OX} W_n}{2L_n}(V_{GS} - V_T)^2 = \frac{\mu_p C_{OX} W_p}{2L_p}(V_{GS} - V_T)^2$$

$$\rightarrow \frac{100 * 10^{-6} * 10}{2 * 2}(0 - (-2) - 0.5)^2 = \frac{30 * 10^{-6} * 3}{2 * 1}\left(V_{out} - 5 - (-0.5)\right)^2$$

$$\rightarrow V_{out} = 0.96447V$$

Problem 5

For quiescent values that capacitors act as open circuits, so the voltage is simply,

$$I_B = \frac{32 - V_B}{90\text{K}} - \frac{V_B}{10\text{K}} = \frac{32 - 10 * V_B}{90\text{K}}$$

$$I_E = (\beta + 1)I_B = (101) * \frac{32 - 10 * (V_E + 0.6)}{90\text{K}} = \frac{V_E}{1.5\text{K}} \rightarrow V_E = 2.454\text{ V} \rightarrow V_B = 3.054\text{ V}$$

$$I_C = 101 * 16.222\ \mu\text{A} \rightarrow V_C = 32 - 3000 * I_C = 27.085\text{ V}$$

$$V_{out} = 0V$$

Problem 6

$$V_{out} = 12 - (12000 * i_{DQ})$$

$$I_{DQ} = 100 * 10^{-6} * \left(\frac{6}{2 * 4}\right) * (0 - (-2) - 1)^2$$

$$I_{DQ} = 75\mu A$$

$$V_{out} = 11.1V$$

Problem 7

a)

$$I_{DQ} = 100 * 10^{-6} * \left(\frac{6}{2 * 3}\right)(2 - 1)^2$$

$$I_{DQ} = 100\ \mu A$$

$$V_{outq} = 4 + 100\ \mu * 20k = 6V$$

b)

When $V_{in} = 0V, V_{out1} = V_{outQ} = 6V$

When $V_{in} = 25mV, V_{out2} = V_{outQ} + \Delta\text{V}$

$$g_m = 100 * 10^{-6}\left(\frac{6}{3}\right)(1) = 200\frac{\mu A}{V}$$

$$\Delta V = (g_m * \Delta V_{in}) * 20k = 0.1V$$

$$V_{out2} = 6.1V$$

Problem 8

$$R_{FET} = \frac{1}{\mu_n C_{OX}}\left(\frac{L}{W}\right)(2-1)$$
$$\frac{V_{out} - V_{in}}{R_F} = \frac{V_{in}}{R_{FET}}$$
$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_F}{R_{FET}}$$
$$\rightarrow \frac{V_{out}}{V_{in}} = 1 + \mu_n C_{OX} * \left(\frac{W}{L}\right) * R_F = 1 + \frac{R_F}{2500}$$

Problem 9

a) $\frac{I_{B1}}{I_{B2}} = \frac{A_{E1}}{A_{E2}} = \frac{1}{4}$

$I_B = I_{B1} + I_{B2} = 5\, I_{B1}$

$I_{IN} = I_{C1} + \beta I_B = \beta I_{B1} + 5 I_{B1}$

$$I_{B1} = I_{in}\left(\frac{1}{\beta + 5}\right) -> I_{out} = \beta I_{B2} = \beta * 4 I_{B1} = I_{in}\left(\frac{4}{1 + \frac{5}{\beta}}\right)$$

Assuming that β is large $\rightarrow I_{out} = 4 * I_{in} = 4\ mA$

b)

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = \frac{10}{20} = \frac{1}{2}$$

$I_{out} = 2 I_{in} = 2\ mA$

Problem 10

$$BJT: I_{out} = \frac{A_{E2}}{A_{E1}} I_{in}$$

$$MOSFET: I_{out} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} I_{in}$$

Problem 11

At the basics, $I_d = \mu C_{ox}\left(\frac{w}{2L}\right)\left(V_{gs} - V_T\right)^2$, and all three have the same total length and width. Becuase the length/width is the one degree of freedom we have to modify the MOSFET, they should behave the same.

Problem 12

Yes, this does behave as a rectifier, but it does not work particularly well. It is “Diode Connected” and behaves as a diode, but it’s I-V curve is not as good as the standard diodes used in class, but may be better than some LEDs.

Problem 13

As always, we will assume we are operating in saturation region,

$$I_D = \mu_n C_{ox}\left(\frac{W}{2L}\right)\left(V_{gs} - V_T\right)^2 = \frac{V_{dd} - V_{out1}}{R_1}$$

$$I_D = \frac{(4-3)}{10k} = 0.1mA$$

$$100 * 10^{-6} * \left(\frac{W}{2L}\right)(2-1)^2 = 0.0001$$

$$\frac{W}{2L} = 1 \rightarrow W = 2L$$

$$W = 0.6\mu, L = 0.3\mu$$

Problem 14

Code:

```
module DFF(D, Q, notQ, clk);
  input D, clk;
  output Q, notQ;
  reg Q, notQ;

  always@(posedge clk) begin
      Q <= D;
      notQ <= ~D;
  end

endmodule
```

Testbench:

```
module DFF(D, Q, notQ, clk);
  input D, clk;
  output Q, notQ;
  reg Q, notQ;

  always@(posedge clk) begin
      Q <= D;
      notQ <= ~D;
  end

endmodule
```

Output: