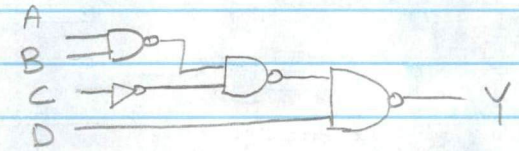
EE 330 F12
HW 3 - solution
Due 9/7/2012

1 Problem 1.6 of WH

b) $Y = \overline{(AB + C) \cdot D}$

logic level

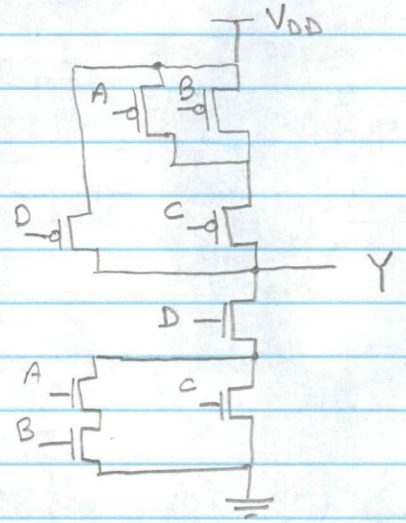


3 logic levels
14 transistors

Transistor level

$Y_{PDN} = \bar{Y} = (AB + C) \cdot D$

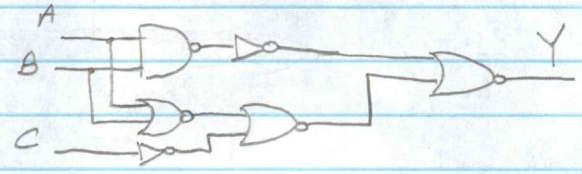
$Y_{PUN} = Y_{PDN}' = (A + B) \cdot C + D$



8 transistors

c) $Y = \overline{A \cdot B + C \cdot (A + B)}$

logic level

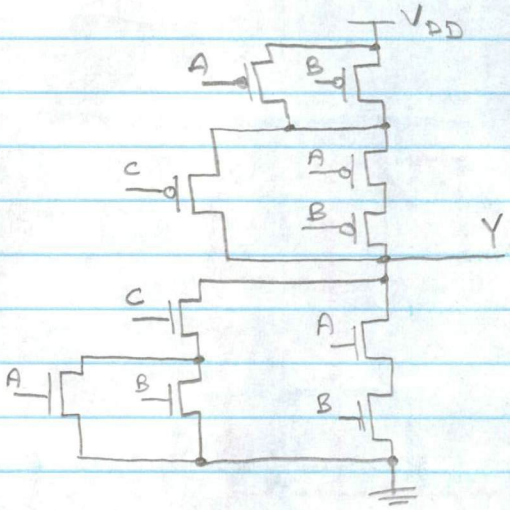


3 logic levels
20 transistors

Transistor level

$Y_{PDN} = \bar{Y} = A \cdot B + C \cdot (A + B)$

$Y_{PUN} = Y_{PDN}' = (A + B) \cdot (C + A \cdot B)$



10 transistors

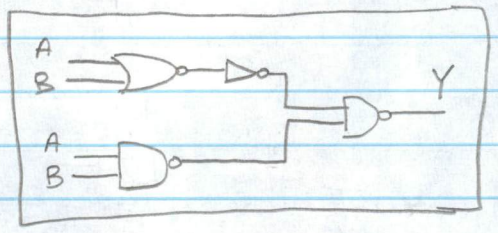
2 Problem 1.7 of WH

c) $Y = \bar{A}\cdot\bar{B} + A\cdot B$

$= \overline{\overline{\bar{A}\cdot\bar{B}} + \overline{A\cdot B}}$

$= \overline{\overline{A+B} + \overline{\bar{A}+\bar{B}}}$

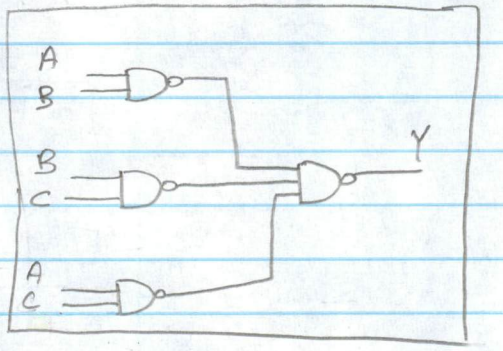
$= \overline{(A+B)\cdot\overline{(\bar{A}+\bar{B})}}$



d) $Y = A\cdot B + B\cdot C + A\cdot C$

$= \overline{\overline{A\cdot B} + \overline{B\cdot C} + \overline{A\cdot C}}$

$= \overline{(\overline{A\cdot B})\cdot(\overline{B\cdot C})\cdot(\overline{A\cdot C})}$

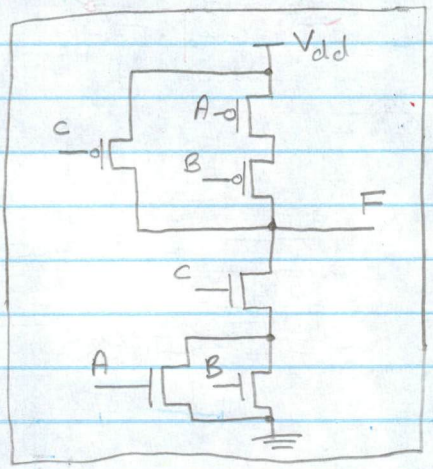


3 Problem 1.16 of WH

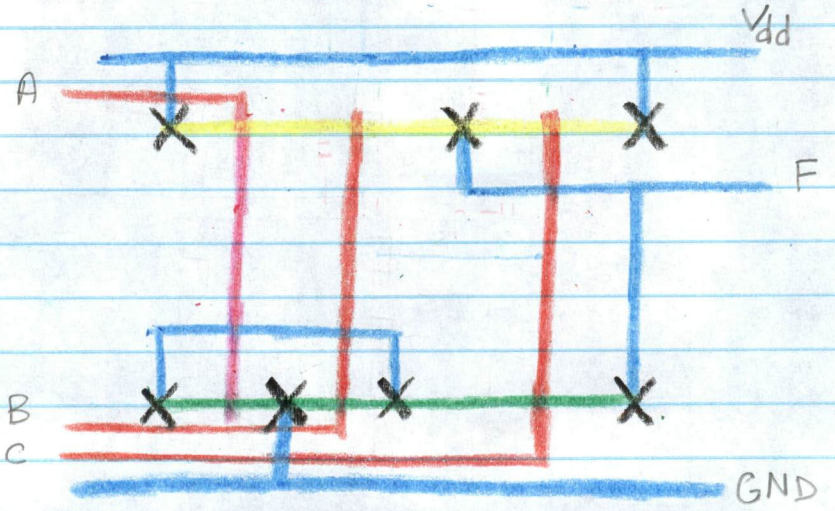
a) $F = \overline{(A+B)\cdot C}$

$F_{PDN} = \bar{F} = (A+B)\cdot C$

$P_{PUN} = F_{PDN}' = A\cdot B + C$



b)

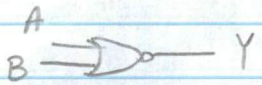


4

$Y_{PDN} = A + B$

$Y_{PUN} = A \cdot B$

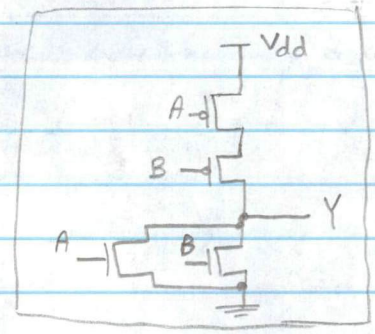
logic



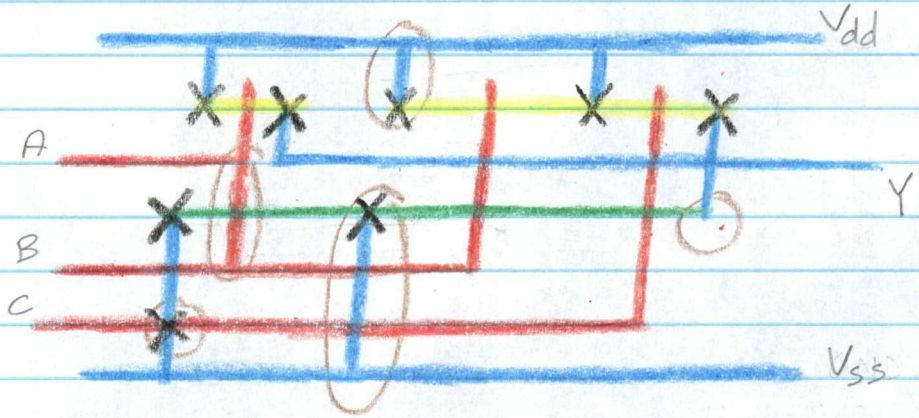
$Y = \overline{A + B}$

2 input NOR gate

transistor

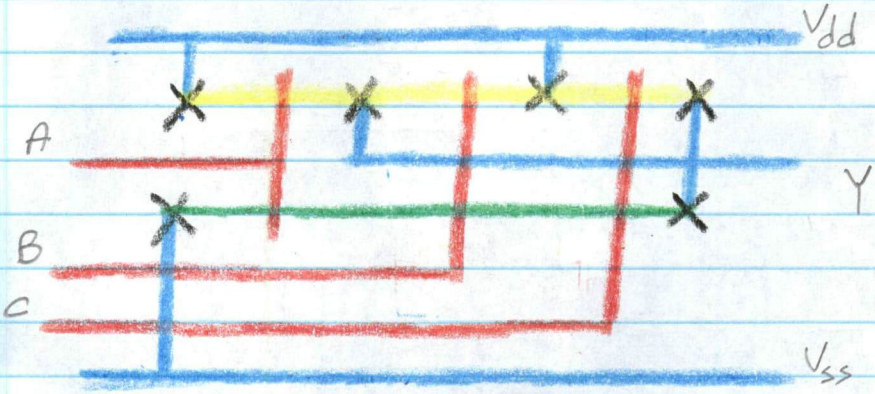


5 Original w/ errors



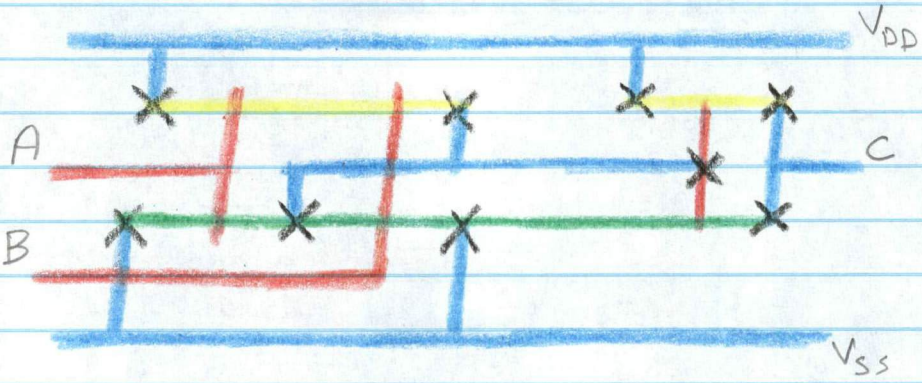
5 errors

Corrected design



6 2 input NOR + inverter

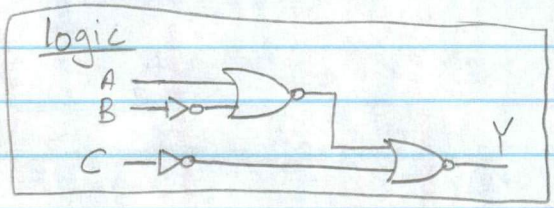
$C = A \cdot B$



7 $Y = (A + \bar{B}) \cdot C$

$= \overline{(A + \bar{B}) \cdot C}$

$Y = \overline{(A + \bar{B})} + \bar{C}$



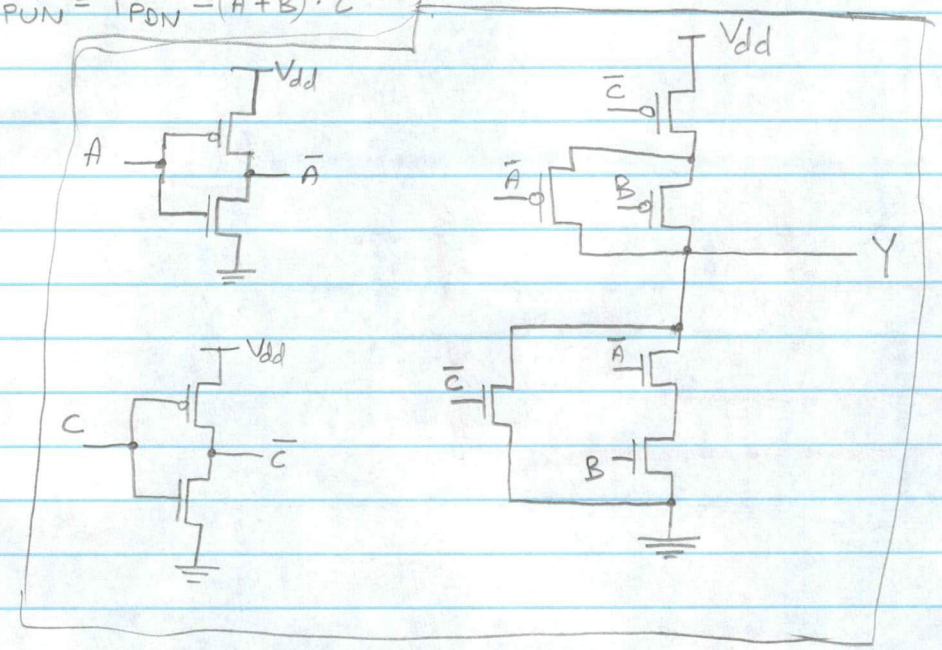
3 logic level
12 transistors

$Y_{PDN} = \bar{Y} = \overline{(A + \bar{B})} + \bar{C}$

$= \bar{A} \cdot B + \bar{C}$

$Y_{PUN} = Y'_{PDN} = (\bar{A} + B) \cdot \bar{C}$

transistor



2 logic levels
10 transistors

8 for the ON 0.5μ process $C_{GS} = 1.5fF$

$C_L = (1.5fF) * (2) * (8) = 24fF$ $R_{sw} = 2k\Omega$ n-channel

$= 6k\Omega$ p-channel

$t_{HL} = (R_{sw_n}) * (C_L) = 24fF \cdot 2k\Omega$

$\boxed{t_{HL} = 48_{ps}}$

9 attached

EE 330 F 12
HW 3 –solution
Problem 9

A) With if-else statement

```
1   module SecurityCamera_A(SWITCH, JEWELS, ARTIFACTS, look_at);
2     input SWITCH, JEWELS, ARTIFACTS;
3     output reg look_at;
4
5     always @(SWITCH or JEWELS or ARTIFACTS)
6       if(SWITCH)
7         look_at = JEWELS;
8       else
9         look_at = ARTIFACTS;
10
11  endmodule
```

B) Without if-else statement

```
1   module SecurityCamera_B(SWITCH, JEWELS, ARTIFACTS, look_at);
2     input SWITCH, JEWELS, ARTIFACTS;
3     output look_at;
4
5     assign look_at = JEWELS & SWITCH | ARTIFACTS & ~SWITCH;
6
7   endmodule
```

Testbench

```
1   `timescale 1ns / 1ps
2
3   module SecurityCamera_tb();
4     reg SWITCH_t, JEWELS_t, ARTIFACTS_t;
5     wire look_at_t, look_at_2_t;
6
7     //Security Camera A -> using if-else statements
8     SecurityCamera_A SecCam_A_1(SWITCH_t, JEWELS_t, ARTIFACTS_t, look_at_t);
9
10    //Security Camera B -> without using if-else statements
11    SecurityCamera_B SecCam_B_1(SWITCH_t, JEWELS_t, ARTIFACTS_t, look_at_2_t);
12
13    initial
14    begin
15      #0 SWITCH_t<=0; JEWELS_t<=0; ARTIFACTS_t<=0;     // case 0
16      #1 SWITCH_t<=0; JEWELS_t<=0; ARTIFACTS_t<=1;     // case 1
17      #1 SWITCH_t<=0; JEWELS_t<=1; ARTIFACTS_t<=0;     // case 2
18      #1 SWITCH_t<=0; JEWELS_t<=1; ARTIFACTS_t<=1;     // case 3
19      #1 SWITCH_t<=1; JEWELS_t<=0; ARTIFACTS_t<=0;     // case 4
20      #1 SWITCH_t<=1; JEWELS_t<=0; ARTIFACTS_t<=1;     // case 5
21      #1 SWITCH_t<=1; JEWELS_t<=1; ARTIFACTS_t<=0;     // case 6
22      #1 SWITCH_t<=1; JEWELS_t<=1; ARTIFACTS_t<=1;     // case 7
23    end
24  endmodule
```

Waveform