# EE 330
# Lecture 12

## Back-End Processing

## Semiconductor Processes

## Devices in Semiconductor Processes

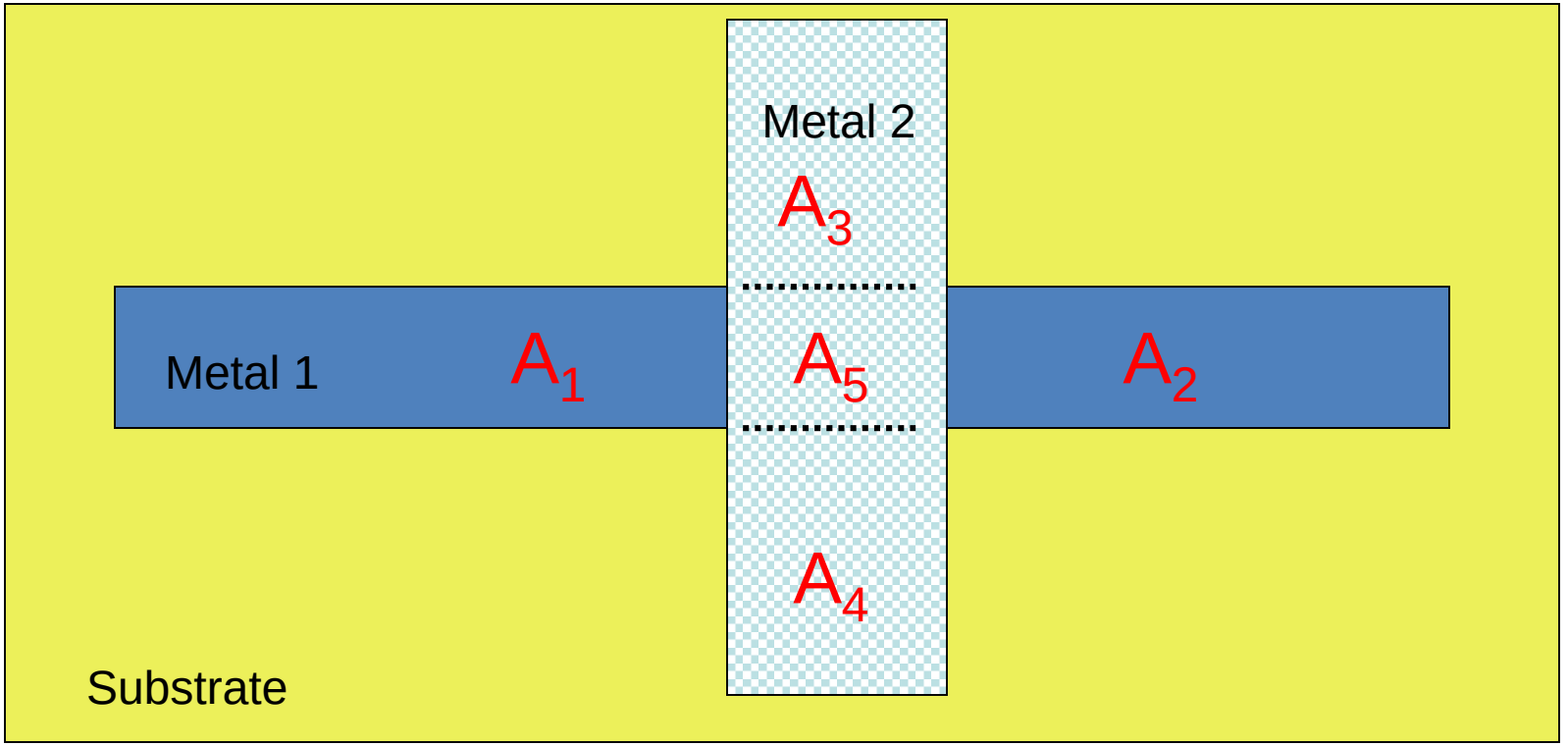
- Resistors
- Diodes
- Capacitors
- MOSFET
- BJT

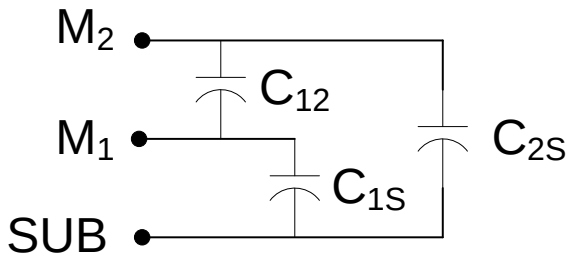
# Exam 1  Friday Sept 27

- Students may bring 1 page of notes
- HW assignment  for week of Sept  23 due on Wed Sept 25 at beginning of class
- No 5:00 p.m extension so solutions can be posted
- Scientific calculators will be provided – no use of any personal electronic devices of any kind
- Those with special accommodation needs, please send me an email message or contact me so arrangements can be made
- Review session – to be determined

Review from Last Lecture

# Capacitance in Interconnects




**Equivalent Circuit**

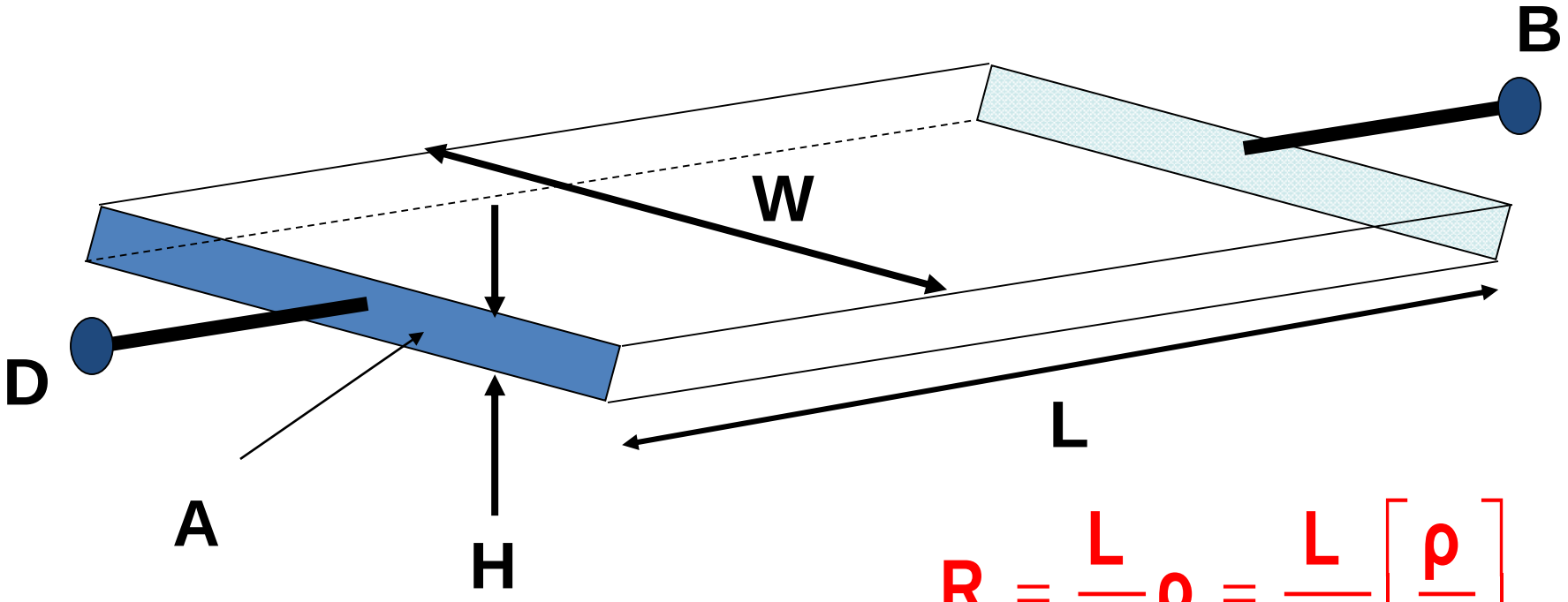
$$C_{12}=CD_{12}\,A_5$$

$$C_{1S}=CD_{1S}\,(A_1+A_2+A_5)$$

$$C_{2S}=CD_{2S}\,(A_3+A_4)$$

Review from Last Lecture

# Resistance in Interconnects




$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

$R_{\square}=\rho/H$ $R=R_{\square}[L / W]$

# Review from Last Lecture

| | | |
|---|---|---|
| SCMOS_SUBM (lambda=0.30) | 0.10 | 0.00 |
| SCMOS (lambda=0.35) | 0.00 | 0.20 |

| FOX TRANSISTORS | GATE | N+ACTIVE | P+ACTIVE | UNITS |
|---|---|---|---|---|
| Vth | Poly | >15.0 | <-15.0 | volts |

| PROCESS PARAMETERS | N+ | P+ | POLY | PLY2_HR | POLY2 | M1 | M2 | UNITS |
|---|---|---|---|---|---|---|---|---|
| Sheet Resistance | 83.5 | 105.3 | 23.5 | 999 | 44.2 | 0.09 | 0.10 | ohms/sq |
| Contact Resistance | 64.9 | 149.7 | 17.3 | | 29.2 | | 0.97 | ohms |
| Gate Oxide Thickness | 142 | | | | | | | angstrom |

| PROCESS PARAMETERS | M3 | N\PLY | N_W | UNITS |
|---|---|---|---|---|
| Sheet Resistance | 0.05 | 824 | 816 | ohms/sq |
| Contact Resistance | 0.79 | | | ohms |

COMMENTS: N\POLY is N-well under polysilicon.

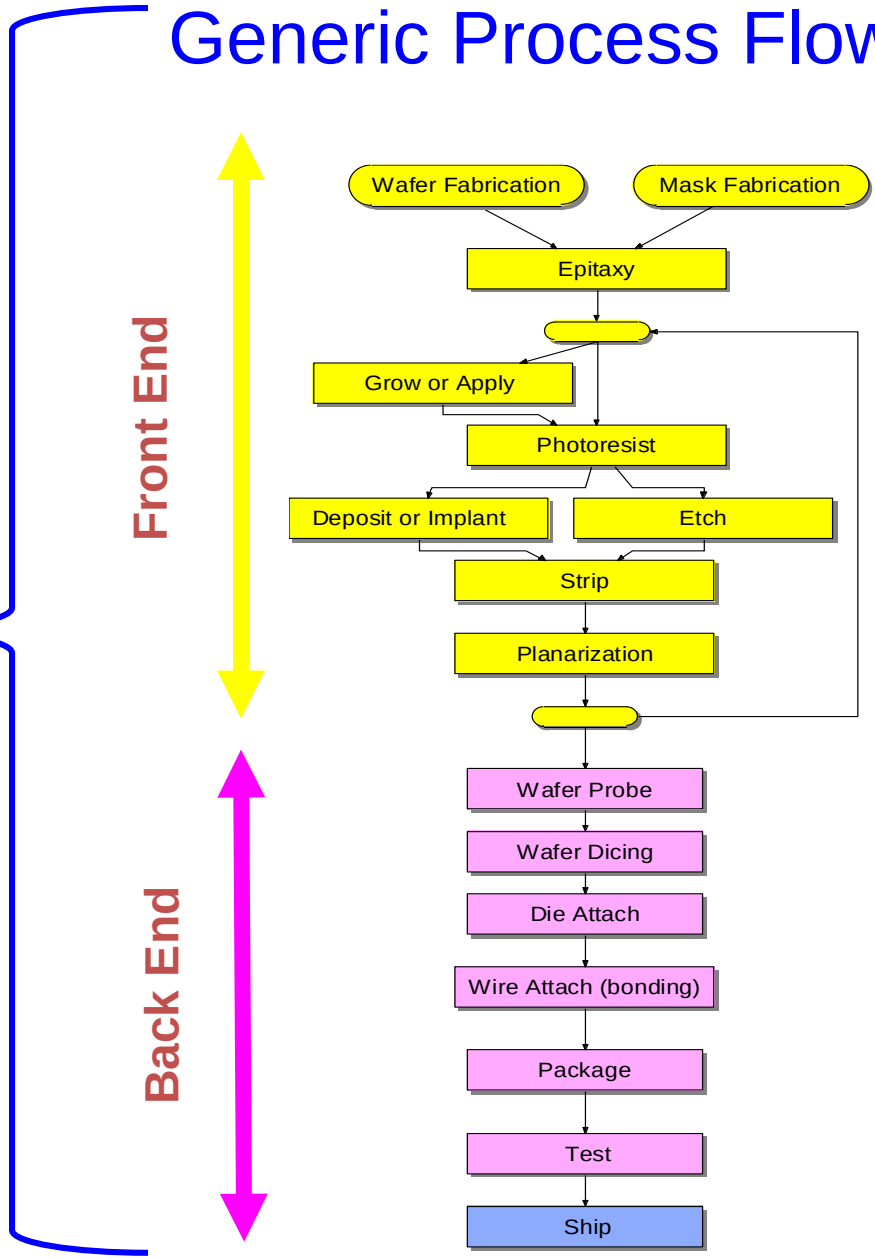
| CAPACITANCE PARAMETERS | N+ | P+ | POLY | POLY2 | M1 | M2 | M3 | N_W | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Area (substrate) | 425 | 731 | 84 | | 27 | 12 | 7 | 37 | aF/um^2 |
| Area (N+active) | | | 2434 | | 35 | 16 | 11 | | aF/um^2 |
| Area (P+active) | | | 2335 | | | | | | aF/um^2 |
| Area (poly) | | | | 938 | 56 | 15 | 9 | | aF/um^2 |
| Area (poly2) | | | | | 49 | | | | aF/um^2 |
| Area (metal1) | | | | | | 31 | 13 | | aF/um^2 |
| Area (metal2) | | | | | | | 35 | | aF/um^2 |
| Fringe (substrate) | 344 | 238 | | | 49 | 33 | 23 | | aF/um |
| Fringe (poly) | | | | | 59 | 38 | 28 | | aF/um |
| Fringe (metal1) | | | | | | 51 | 34 | | aF/um |
| Fringe (metal2) | | | | | | | 52 | | aF/um |
| Overlap (N+active) | | | 232 | | | | | | aF/um |
| Overlap (P+active) | | | 312 | | | | | | aF/um |

| CIRCUIT PARAMETERS | | | UNITS |
|---|---|---|---|
| Inverters | K | | |
| Vinv | 1.0 | 2.02 | volts |
| Vinv | 1.5 | 2.28 | volts |
| Vol (100 uA) | 2.0 | 0.13 | volts |

# Back End Processing

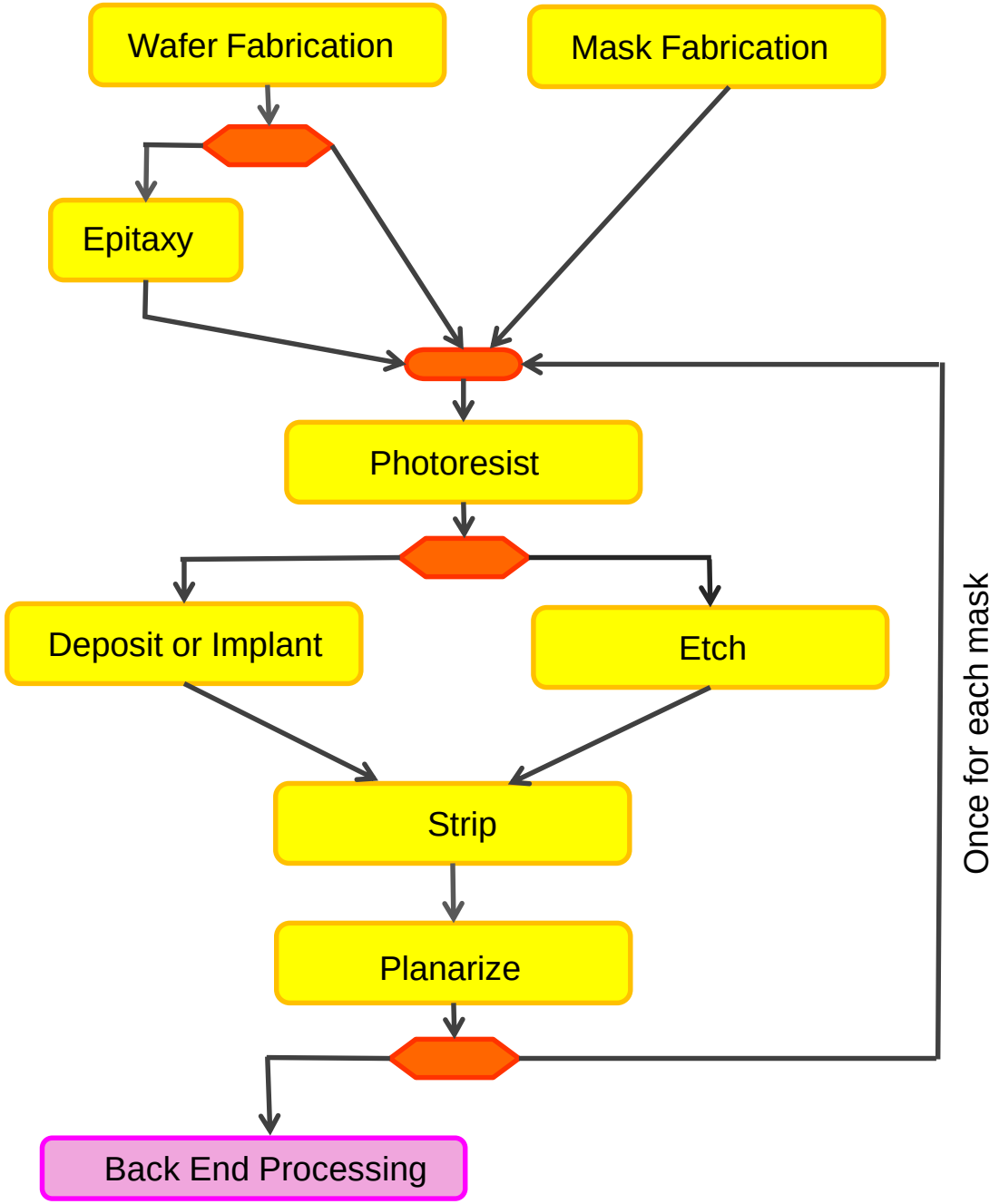
Recall:

## Generic Process Flow



# Front End Process Integration for Fabrication of ICs

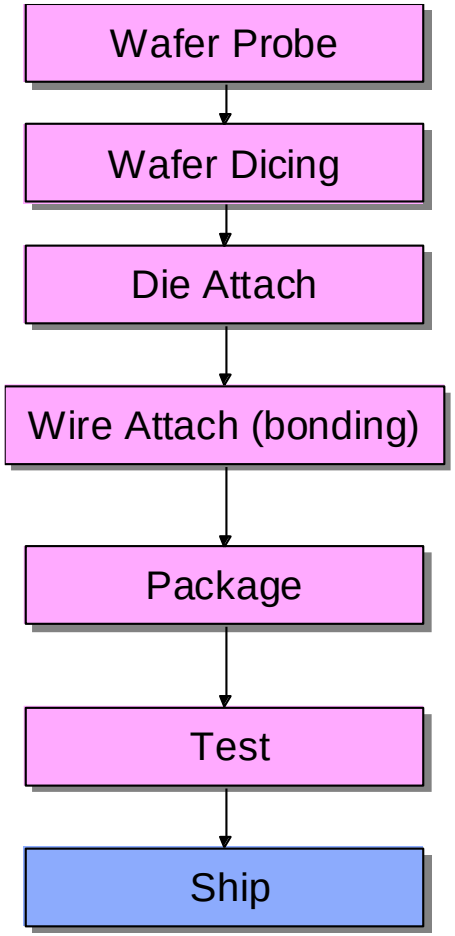
Recall:



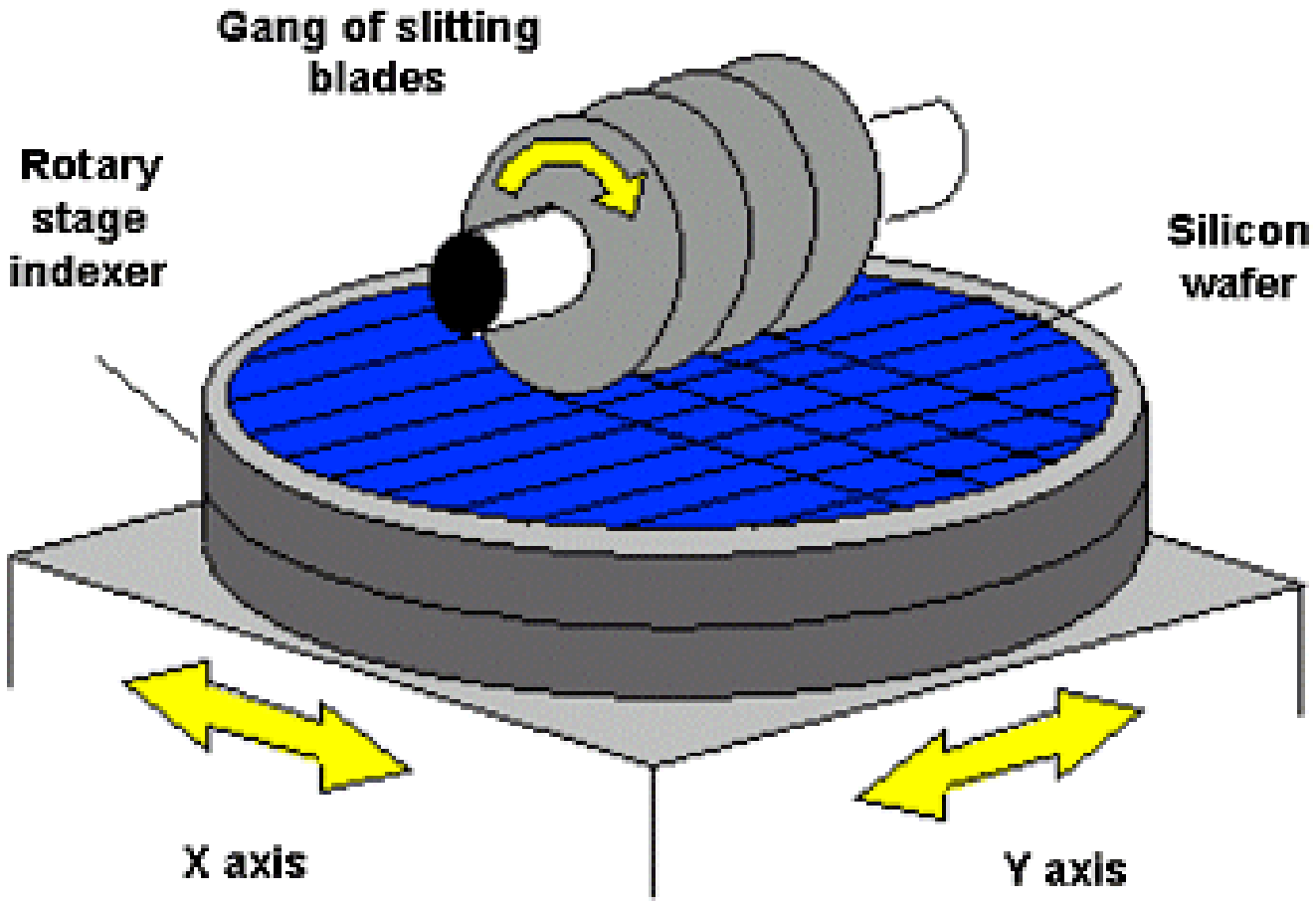
# Front-End Process Flow

- Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary

# Back-End Process Flow



# Wafer Dicing




www.renishaw.com

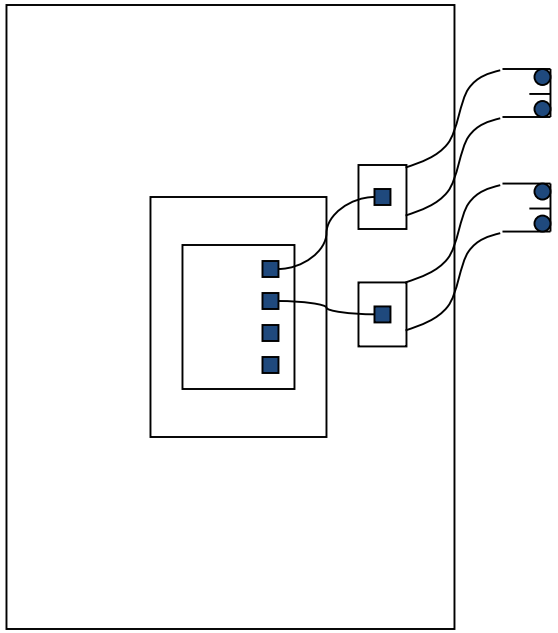
# Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy

# Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding

# Wire Bonding



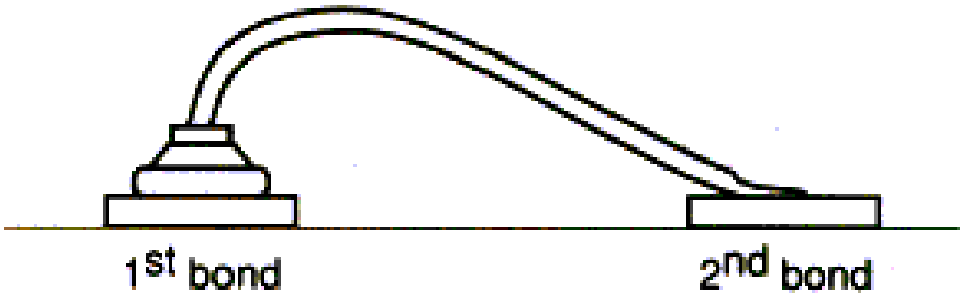
Wire – gold or aluminum
25 μ in diameter

# Wire Bonding

Excellent Annimation showing process at :

http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf

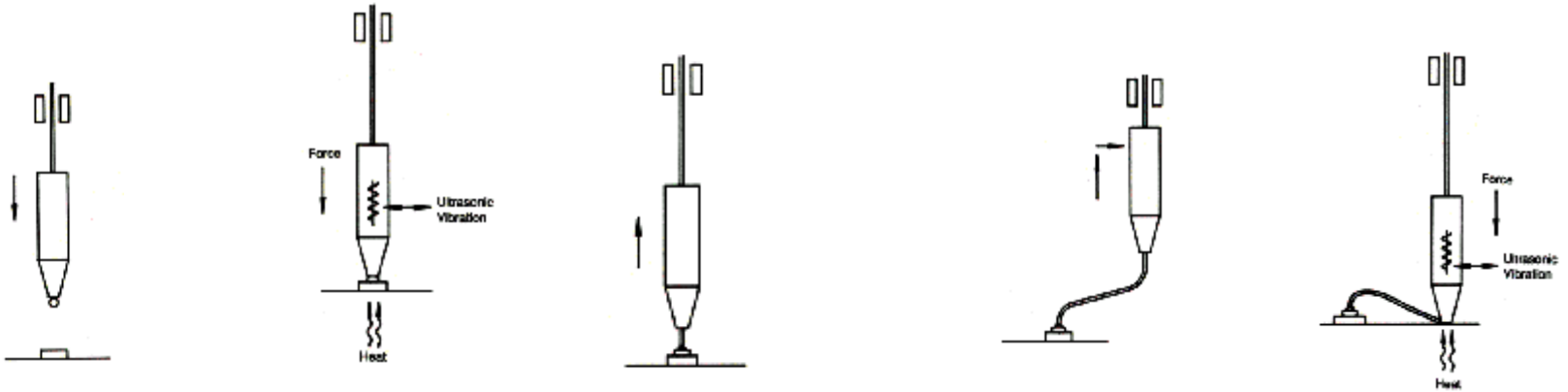
# Wire Bonding



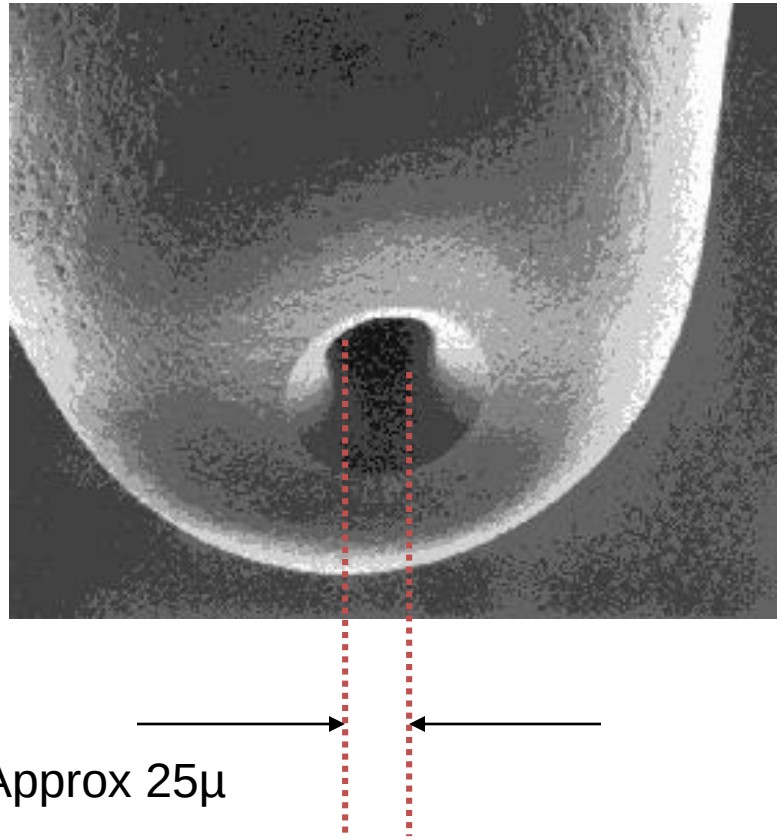

Ball Bond


Wedge Bond

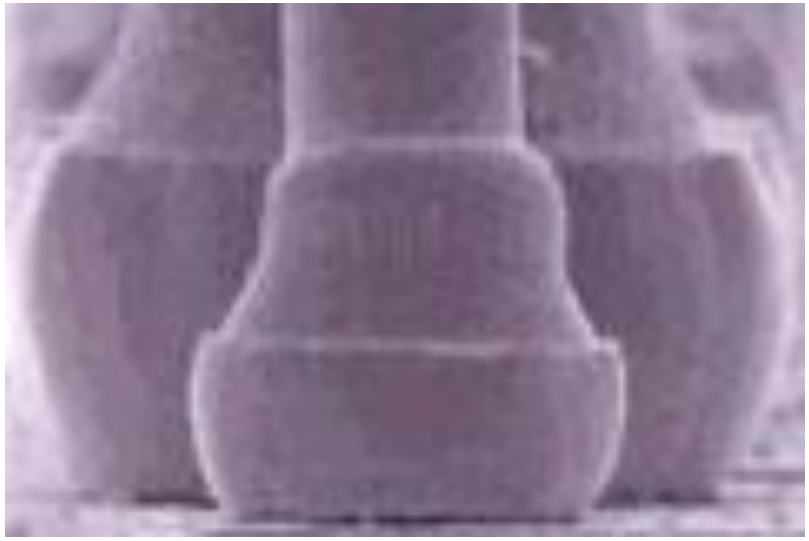
# Ball Bonding Steps

# Ball Bonding Tip

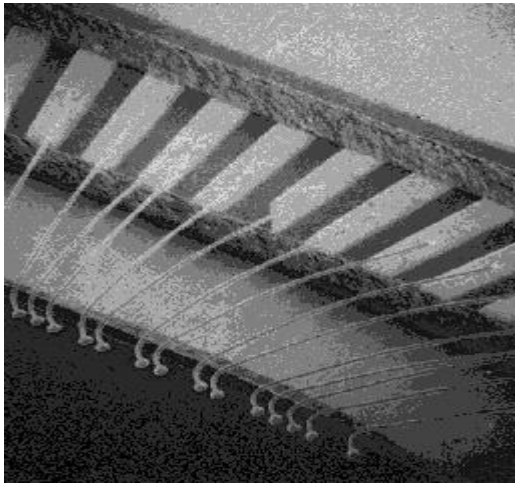


# Wire Bonding



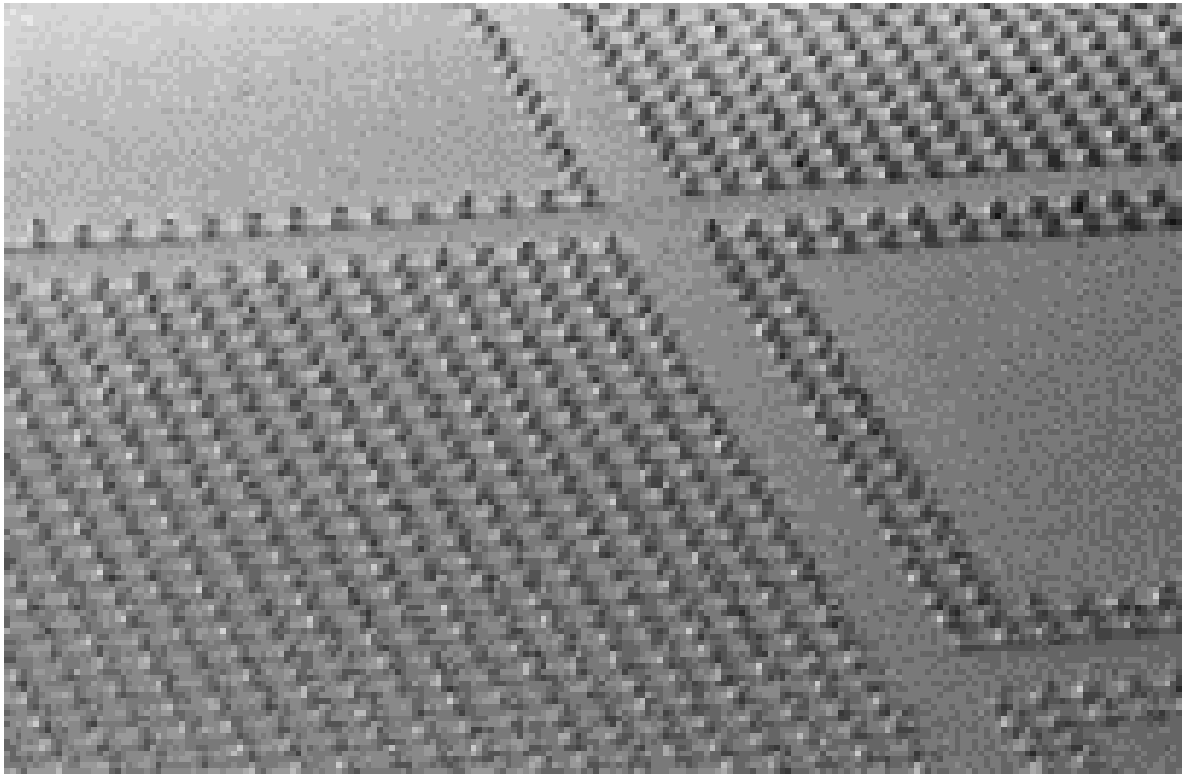
Ball Bond

Termination Bond



Ball Bond Photograph

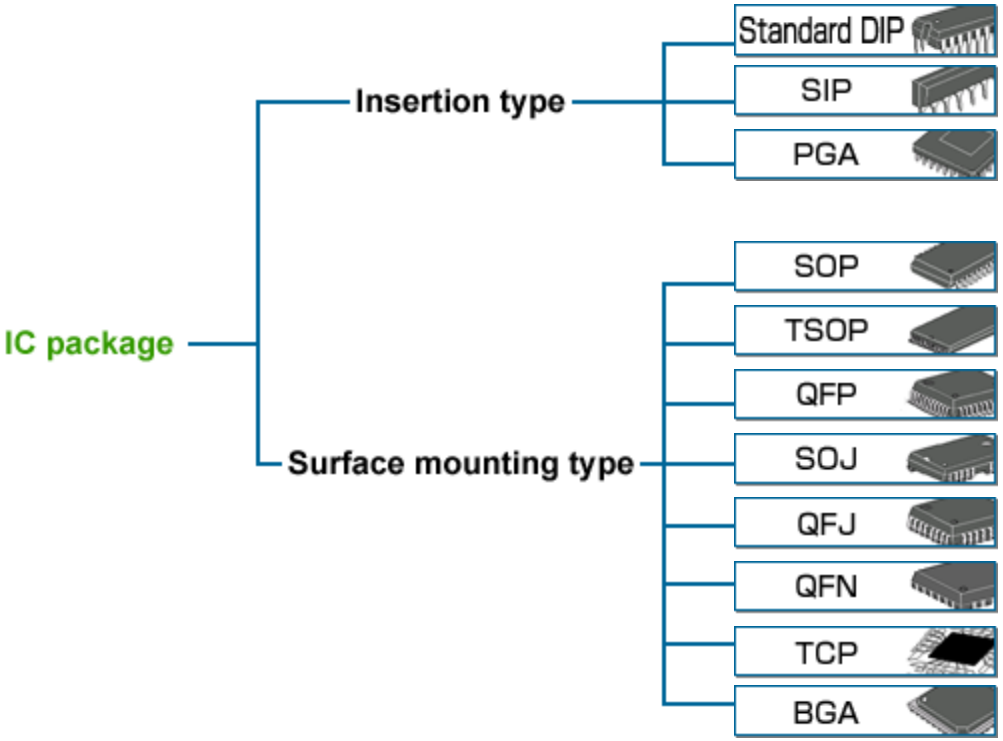
# Bump Bonding



# Packaging

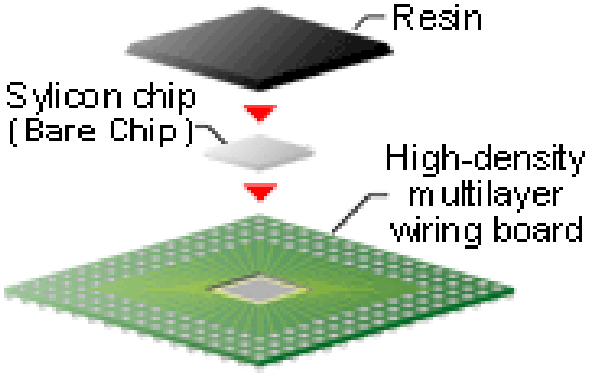
1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models

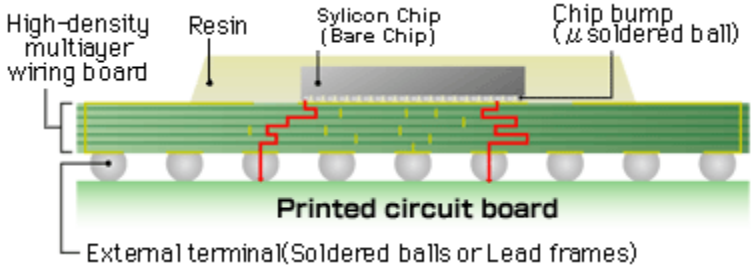
# Packaging




www.necel.com

# Packaging



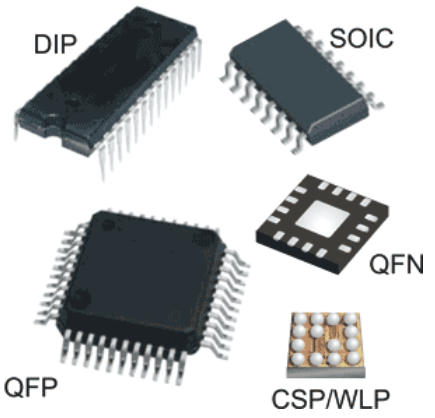




www.necel.com

# Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

| Name | Pin pitch | Size | Height |
|---|---|---|---|
| DIP or DIL | 2.54 | | |
| SOIC-16 | 1.27 | 3.9 x 10 | 1.72 |
| SSOP | 0.635 | | |
| TSSOP54-II | 0.8 | 12.7 x 22.22 | ~1 |
| PLCC44 | 1.27 | | |
| PQ208[1] | 0.50 | 28 x 28 | 3.4 |
| TQFP64 | 0.40 | 7 x 7 | 1.0 |
| TQFP144[2] | 0.50 | 20 x 20 | 1.0 |
| 128PQFP | 0.50 | 23.23 x 14.0 | 3.15 |




http://www.electroiq.com/index/display/packaging-article-display/234467/articles/advanced-packaging/volume-14/issue-8/features/the-back-end-process/materials-and-methods-for-ic-package-assemblies.htm

From Wikipedia, Sept 20, 2010

http://en.wikipedia.org/wiki/List_of_chip_carriers

# Many standard packages available today:

http://www.interfacebus.com/Design_Pack_types.html

**BCC**: Bump Chip Carrier
**BGA**: Ball Grid Array; BGA graphic
**BQFP**: Bumpered Quad Flat Pack
**CABGA/SSBGA**: Chip Array/Small Scale Ball Grid Array
**CBGA**: Ceramic Ball Grid Array
**CFP**: Ceramic Flat Pack
**CPGA**: Ceramic Pin Grid Array, **CPGA Graphic**
**CQFP**: Ceramic Quad Flat Pack, **CQFP Graphic**
**TBD**: Ceramic Lead-Less Chip Carrier
**DFN**: Dual Flat Pack, No Lead
**DLCC**: Dual Lead-Less Chip Carrier (Ceramic)
**ETQFP**: Extra Thin Quad Flat Package
**FBGA**: Fine-pitch Ball Grid Array
**fpBGA**: Fine Pitch Ball Grid Array
**HSBGA**: Heat Slug Ball Grid Array
**JLCC**: J-Leaded Chip Carrier (Ceramic) **J-Lead Picture**
**LBGA**: Low-Profile Ball Grid Array
**LCC**: Leaded Chip Carrier **LCC Graphic**
**LCC**: Leaded Chip Carrier **Un-formed LCC Graphic**
**LCCC**: Leaded Ceramic Chip Carrier;
**LFBGA**: Low-Profile, Fine-Pitch Ball Grid Array
**LGA**: Land Grid Array, **LGA uP** [Pins are on the Motherboard, not the socket]
**LLCC**: Leadless Leaded Chip Carrier **LLCC Graphic**
**LQFP**: Low Profile Quad Flat Package
**MCMBGA**: Multi Chip Module Ball Grid Array
**MCMCABGA**: Multi Chip Module-Chip Array Ball Grid Array
**MLCC**: Micro Lead-frame Chip Carrier

**PBGA**: Plastic Ball Grid Array
**PLCC**: Plastic Leaded Chip Carrier
**PQFD**: Plastic Quad Flat Pack
**PQFP**: Plastic Quad Flat Pack
**PSOP**: Plastic Small-Outline Package PSOP graphic
**QFP**: Quad Flatpack **QFP Graphics**
**QSOP**: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
**SBGA**: Super BGA - above 500 Pin count
**SOIC**: Small Outline IC
**SO Flat Pack**: Small Outline Flat Pack IC
**SOJ**: Small-Outline Package [J-Lead]; **J-Lead Picture**
**SOP**: Small-Outline Package; SOP IC, Socket
**SSOP**: Shrink Small-Outline Package
**TBGA**: Thin Ball Grid Array
**TQFP**: Thin Quad Flat Pack TQFP Graphic
**TSOP**: Thin Small-Outline Package
**TSSOP**: Thin Shrink Small-Outline Package
**TVSOP**: Thin Very Small-Outline Package
**VQFB**: Very-thin Quad Flat Pack

# Considerable activity today and for years to come on improving packaging technology

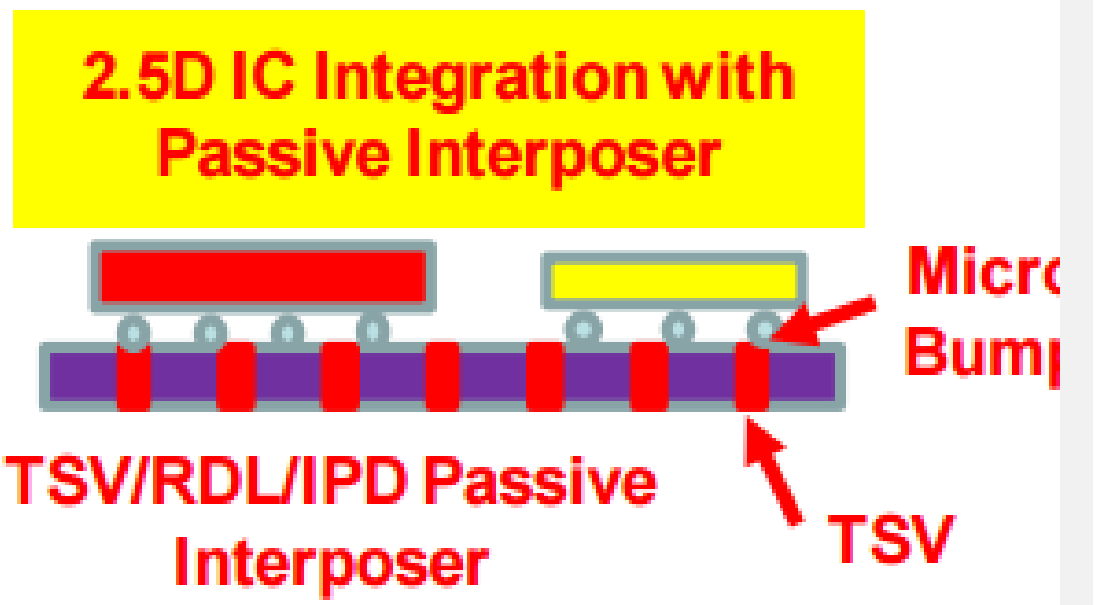
- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained

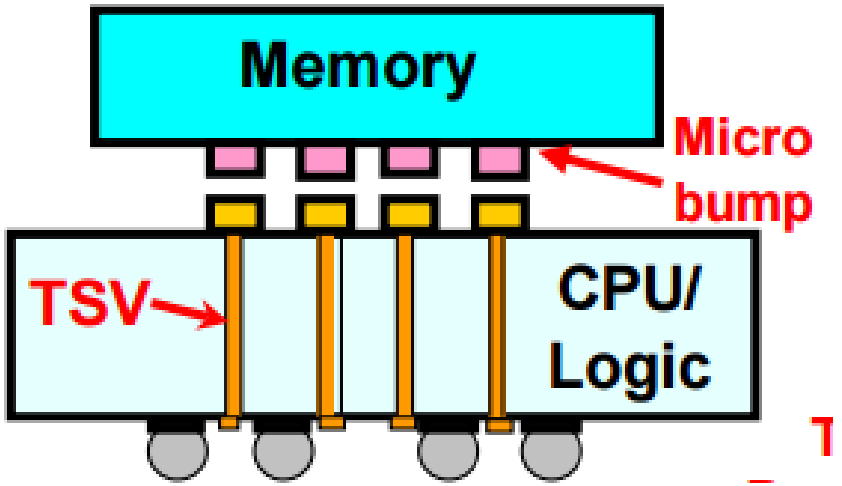
The following few slides come from a John Lau presentation

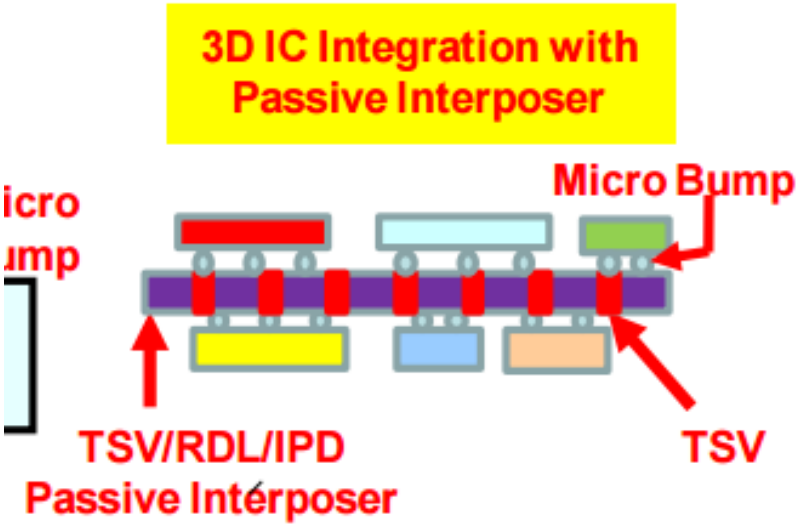
www.sematech.org/meetings/archives/symposia/10187/Session2/04_Lau.pdf

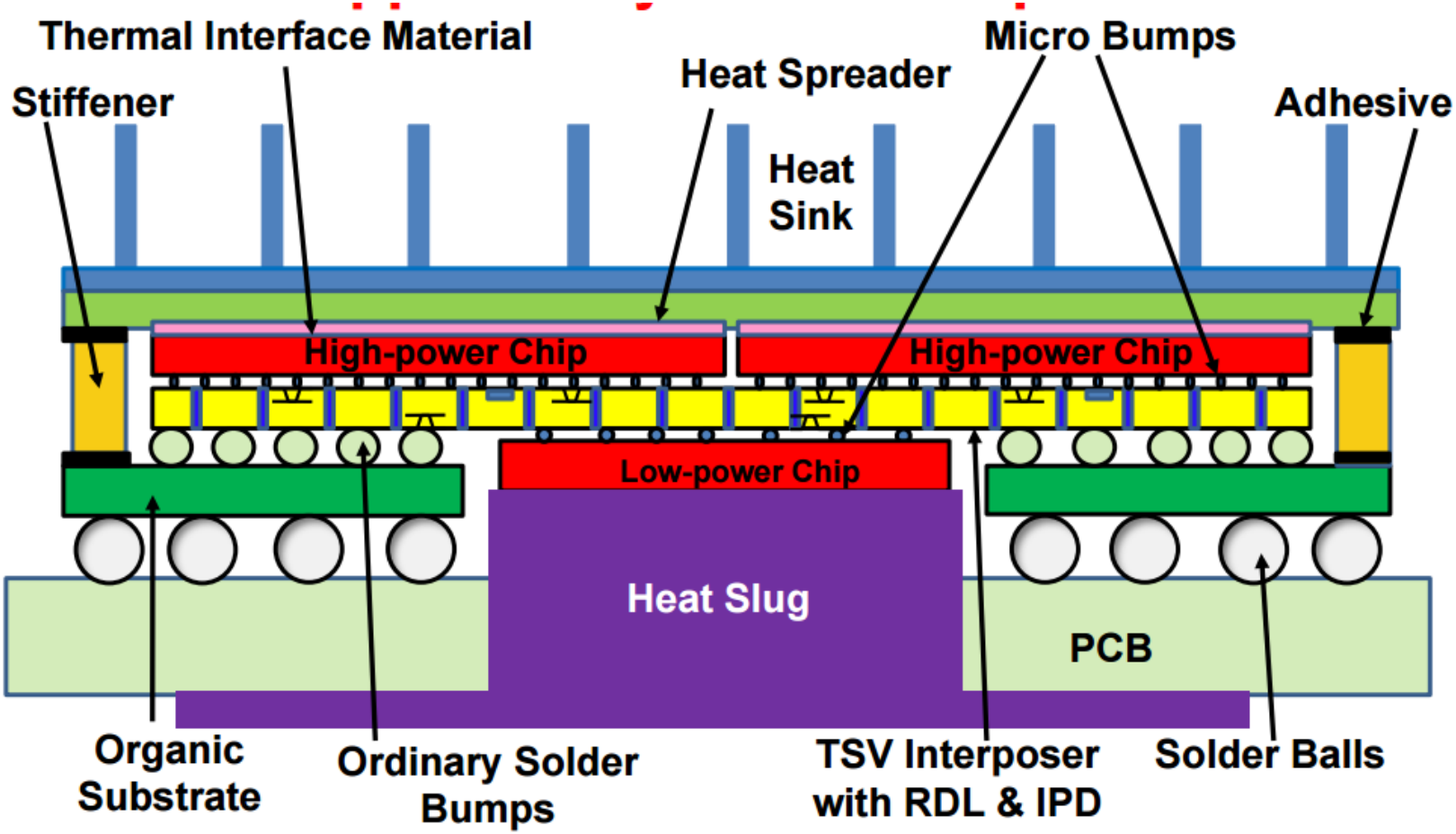
# TSV Interposer: The Most Cost-Effective Integrator for 3D IC Integration

**John H. Lau**
**Electronics & Optoelectronics Research Laboratories**
**Industrial Technology Research Institute (ITRI)**
**Chutung, Hsinchu, Taiwan 310, R.O.C.**
**886-3591-3390, johnlau@itri.org.tw**

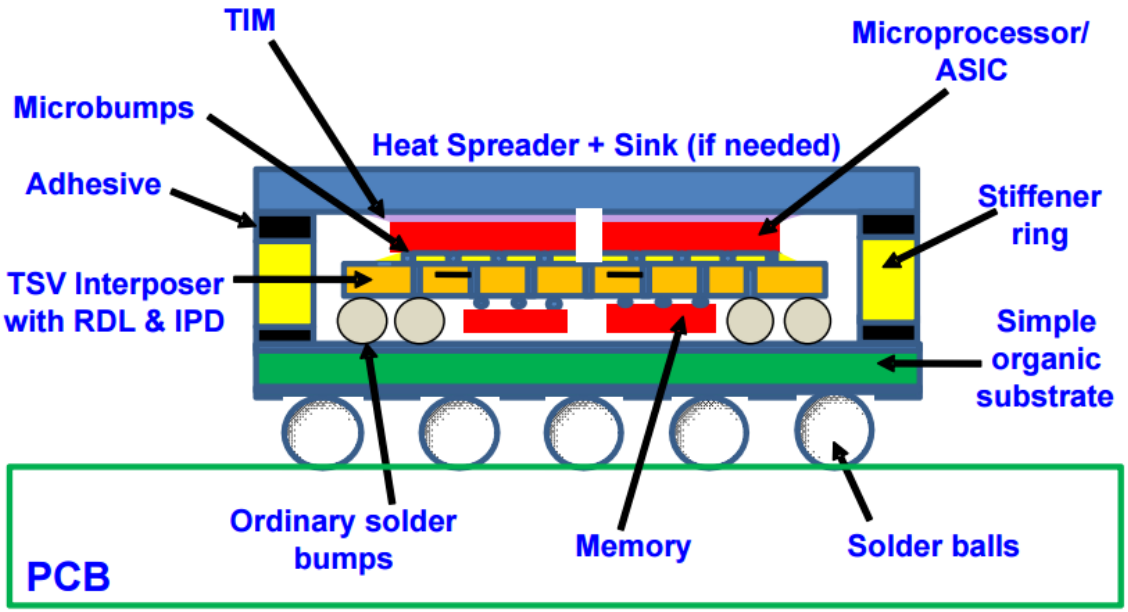

2.5D IC Integration with Passive Interposer
Micro Bump
TSV/RDL/IPD Passive Interposer
TSV


Memory
Micro
bump
TSV
CPU/
Logic


3D IC Integration with
Passive Interposer
Micro Bump
TSV/RDL/IPD
Passive Intérposer
TSV

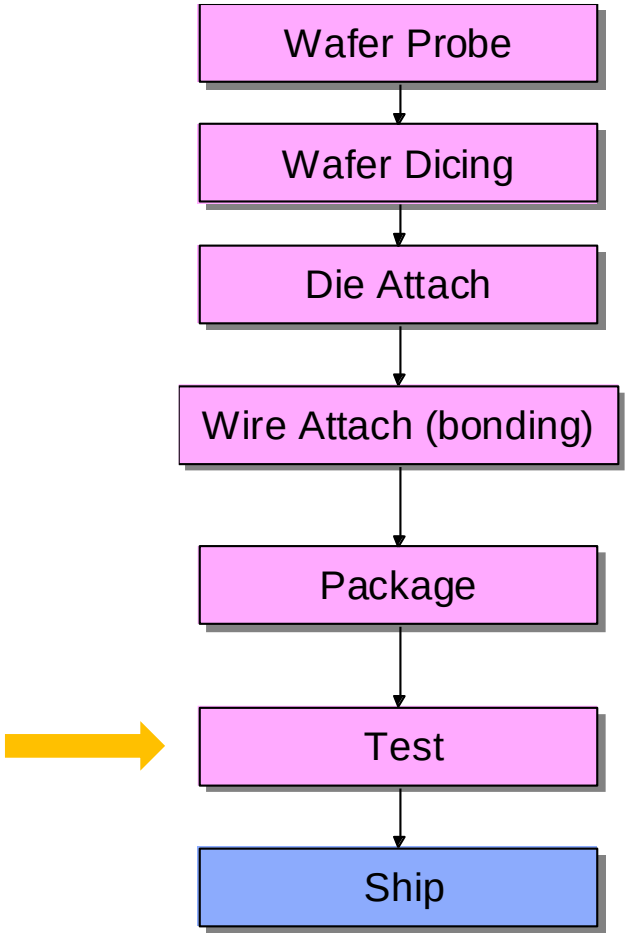

Thermal Interface Material
Stiffener
Heat Spreader
Micro Bumps
Adhesive
Heat
Sink
High-power Chip
High-power Chip
Low-power Chip
Heat Slug
PCB
Organic
Substrate
Ordinary Solder
Bumps
TSV Interposer
with RDL & IPD
Solder Balls

# TSV passive interposer supporting high-power chips (e.g., microprocessor and logic) on its top side and low-power chips (e.g., memory) on its bottom side




Special underfills are needed between the Cu -filled interposer and all the chips. Ordinary underfills are needed between the interposer and the organic substrate.

# Back-End Process Flow



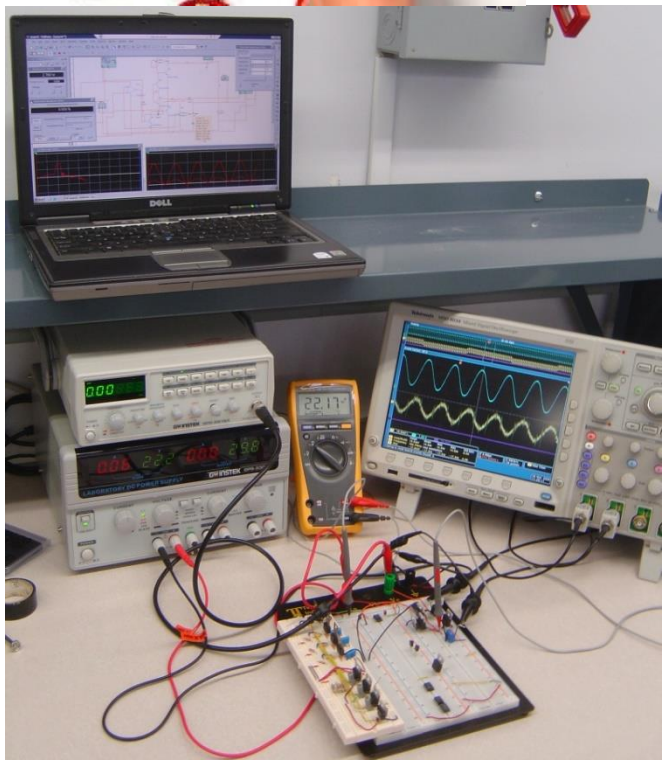
# Testing of Integrated Circuits

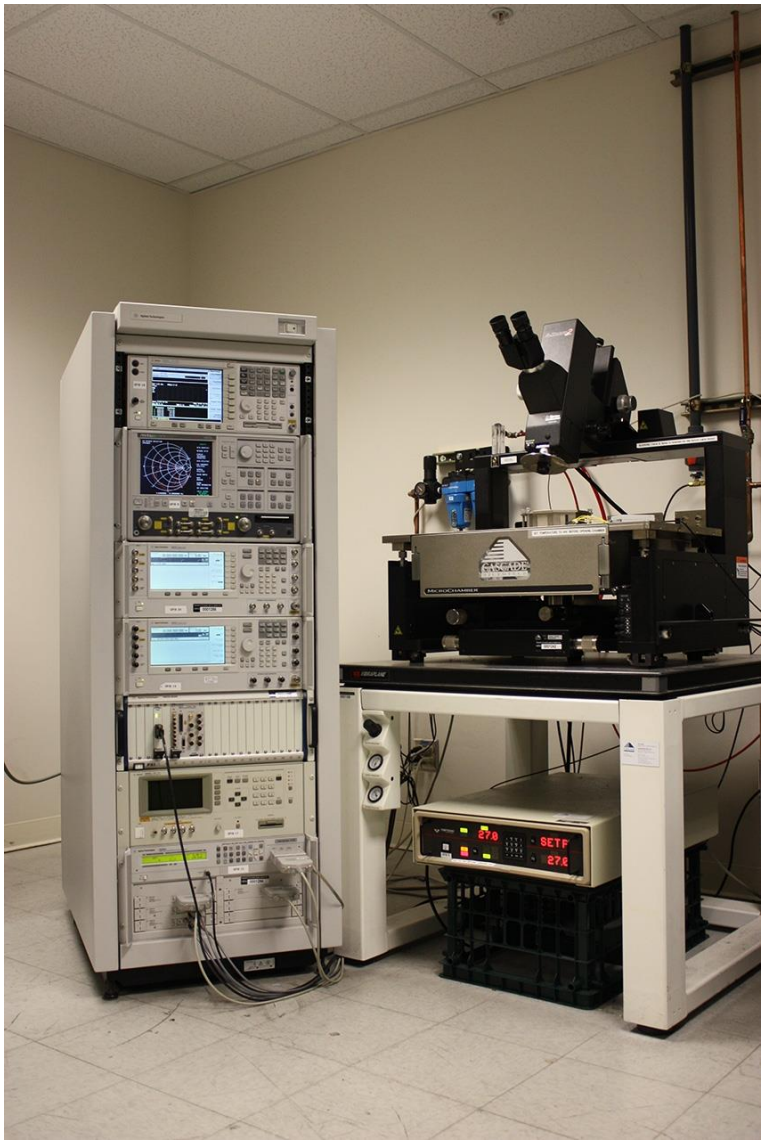
Bench testing used to qualify parts for production

Most integrated circuits are tested twice during production

- Wafer Probe Testing
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts
- Packaged Part Testing
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts

# Bench Test Environment



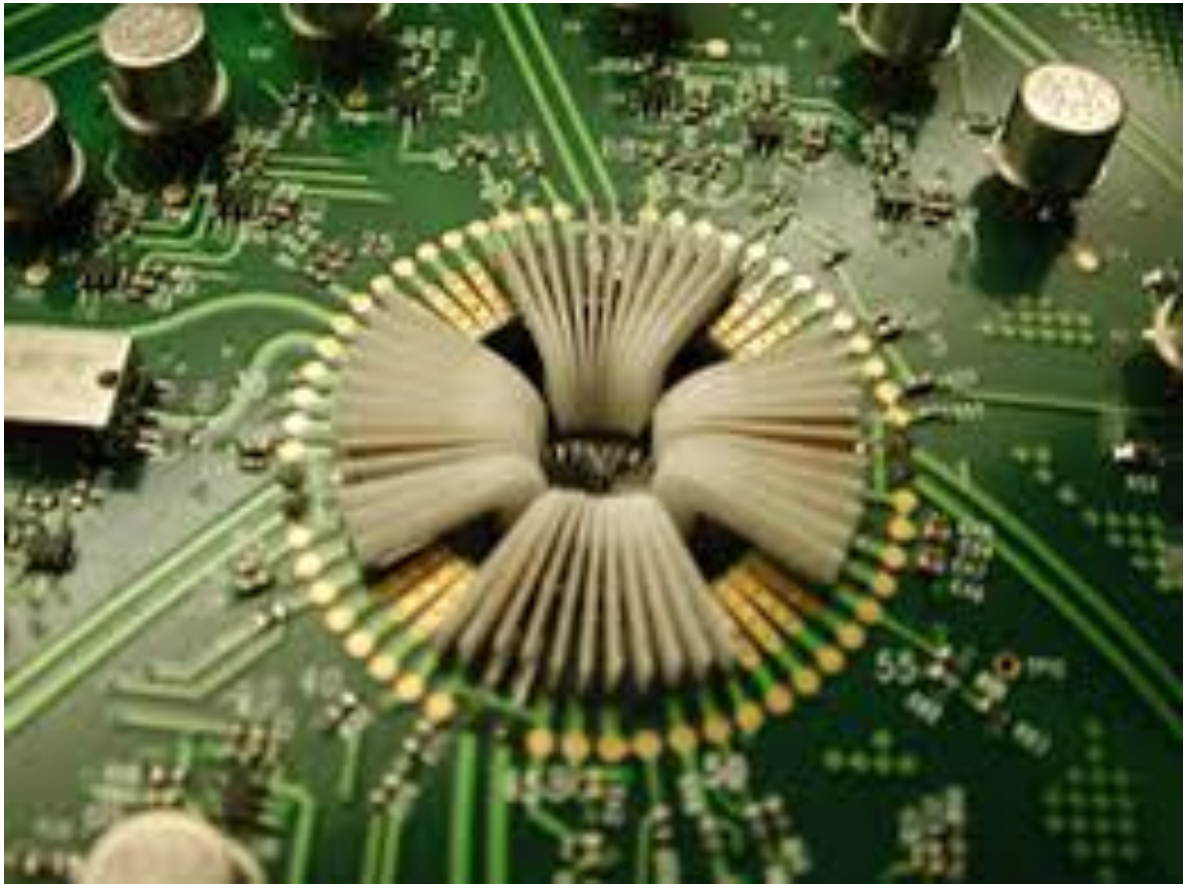


Photos from www postings and Google image search

# Bench Test Environment


Photo courtesy of Texas Instruments

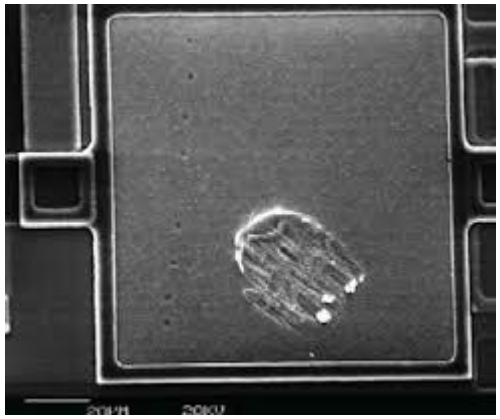
# Probe Test



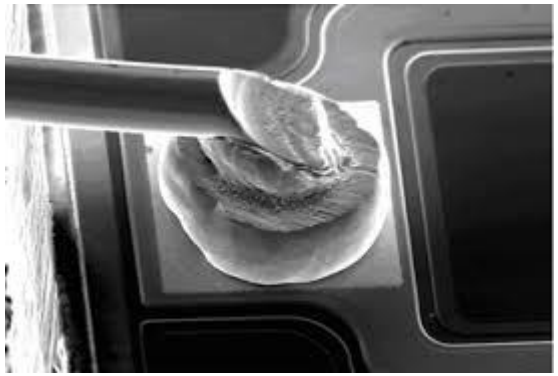
Probes on section of probe card

Photos from www postings and Google image search

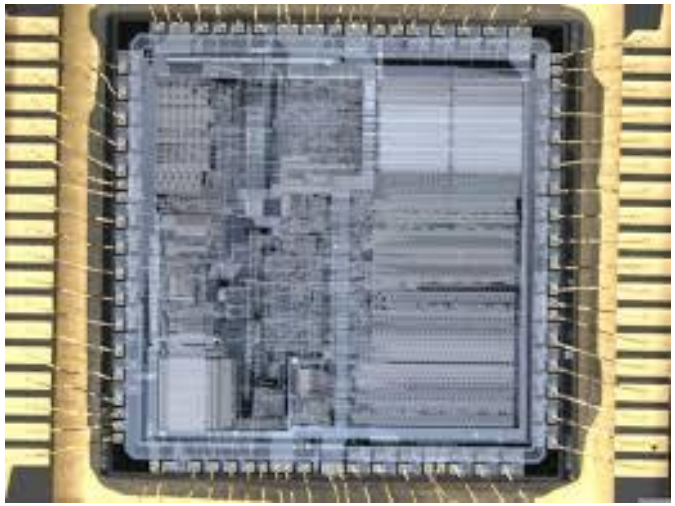
# Probe Test



Pad showing probe marks



Pad showing bonding wire



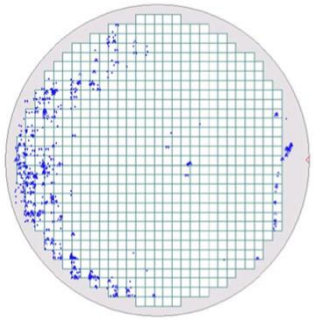
Die showing wire bonds to package cavity

Photos from www postings and Google image search

# Probe Test


Production probe test facility

Goal to Identify
defective die on wafer

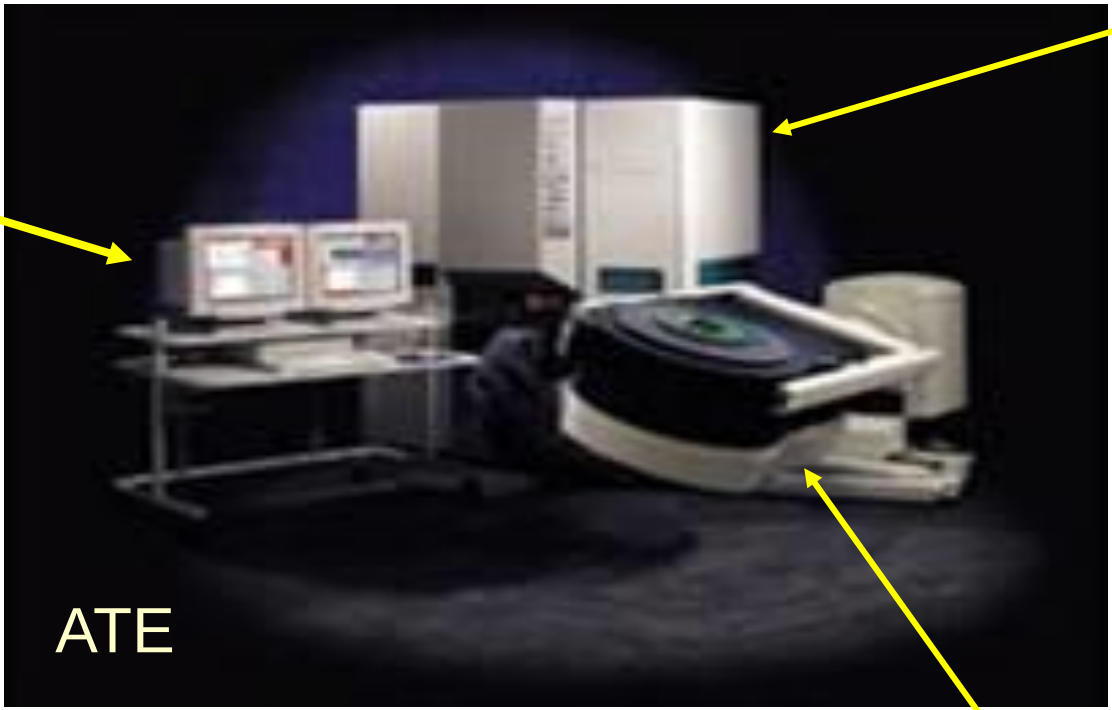




Photos from www postings and Google image search

# Final Test

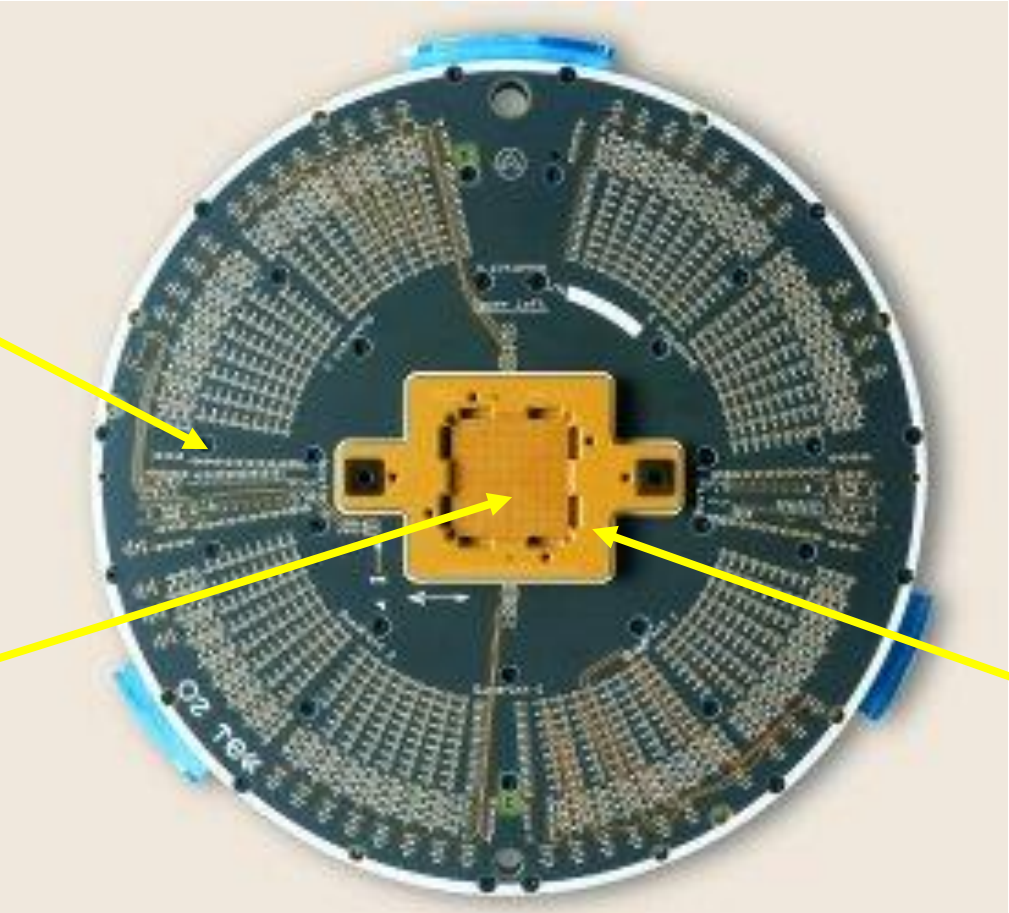
Typical ATE System (less handler)




Automated Test Equipment (ATE)

# Device Interface Board - DIB

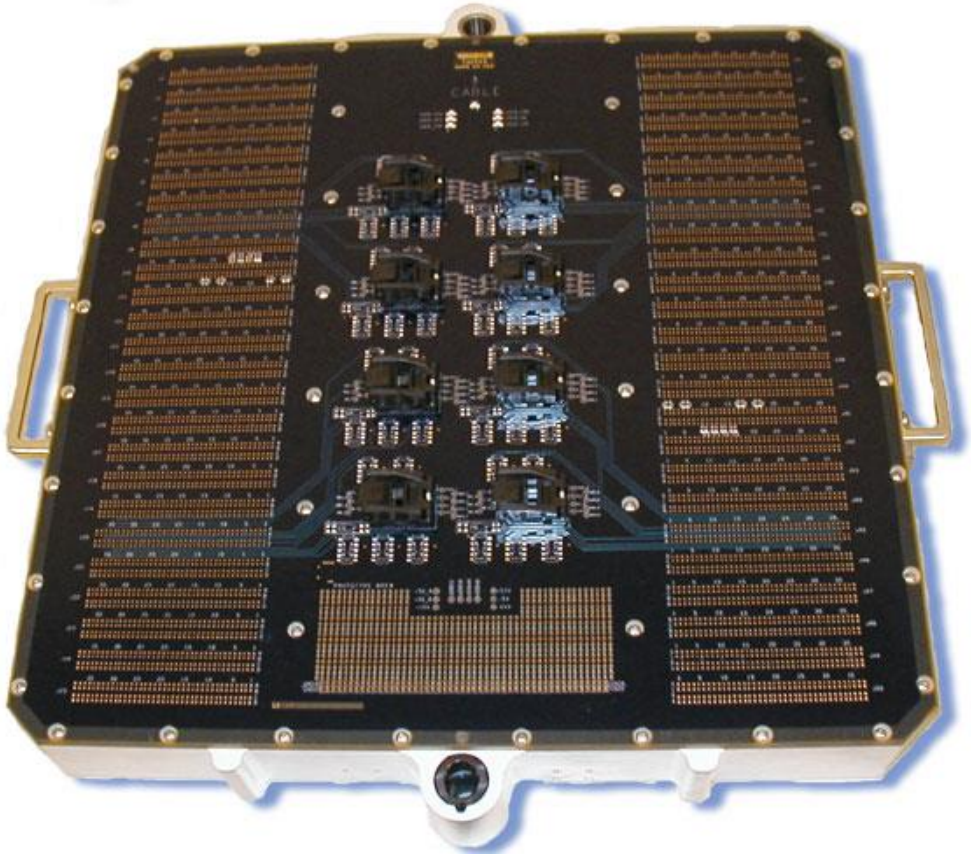
## (Load Board)



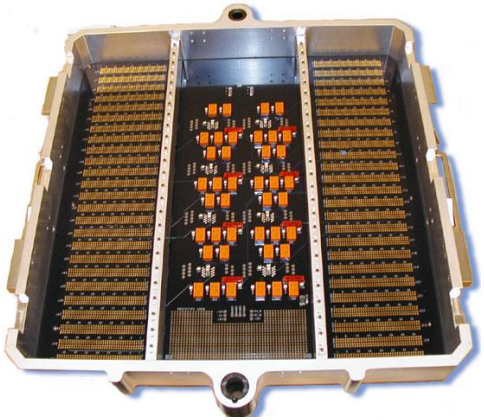

**DIBs Vary Considerably from one ATE Platform to another and are often personalized for a particular DUT**

# Octal Site DIB

Flex Octal (Teradyne)



Top



Bottom

# Final Test

Typical ATE Configuration

Handler

Tester

Test Head


Atlas (SSI Robotics)

# Basic Semiconductor Processes

## MOS (Metal Oxide Semiconductor)

1. NMOS — n-ch
2. PMOS — p-ch
3. CMOS — n-ch & p-ch
   - Basic Device: MOSFET
   - Niche Device: MESFET
   - Other Devices: Diode
     BJT
     Resistors
     Capacitors
     Schottky Diode

# Basic Semiconductor Processes

## Bipolar

1. $T^2L$
2. ECL
3. $I^2L$
4. Linear ICs
   - Basic Device: BJT (Bipolar Junction Transistor)
   - Niche Devices: HBJT (Heterojunction Bipolar Transistor)
     HBT
   - Other Devices: Diode
     Resistor
     Capacitor
     Schottky Diode
     JFET (Junction Field Effect Transistor)

# Basic Semiconductor Processes

## Other Processes

- Thin and Thick Film Processes
  - Basic Device:  Resistor
- BiMOS or BiCMOS
  - Combines both MOS & Bipolar Processes
  - Basic Devices:  MOSFET & BJT
- SiGe
  - BJT with HBT implementation
- SiGe / MOS
  - Combines HBT & MOSFET technology
- SOI / SOS (Silicon on Insulator / Silicon on Sapphire)
- Twin-Well & Twin Tub CMOS
  - Very similar to basic CMOS but more optimal transistor char.

# Devices in Semiconductor Processes

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT ( decent in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel
- Standard Bipolar Process
  - BJT
    - npn
    - pnp
  - JFET
    - n-channel
    - p-channel
  - Diodes
  - Resistors
  - Capacitors

- Niche Devices
  - Photodetectors (photodiodes, phototransistors, photoresistors)
  - MESFET
  - HBT
  - Schottky Diode (not Shockley)
  - MEM Devices
  - TRIAC/SCR
  - ….

# Basic Devices

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel
- Niche Devices
  - Photodetectors
  - MESFET
  - Schottky Diode (not Shockley)
  - MEM Devices
  - Triac/SCR
  - ….

**Primary Consideration in This Course**

**Some Consideration in This Course**

# Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

# Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

Resistors were discussed when considering interconnects so will only be briefly reviewed here

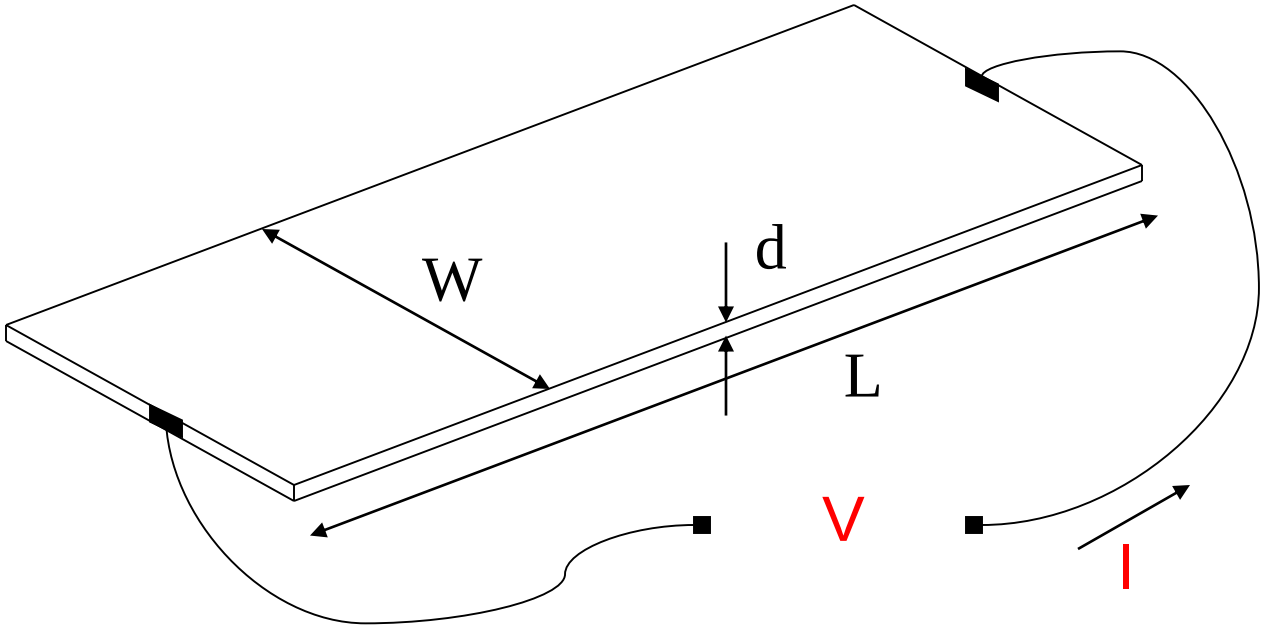
# Resistors

- Generally thin-film devices
- Almost any thin-film layer can be used as a resistor
  - Diffused resistors
  - Poly Resistors
  - Metal Resistors
  - “Thin-film” adders (SiCr or NiCr)
- Subject to process variations, gradient effects and local random variations
- Often temperature and voltage dependent
  - Ambient temperature
  - Local Heating
- Nonlinearities often a cause of distortion when used in circuits
- Trimming possible resistors
  - Laser,links,switches

Have already modeled resistance as an interconnect

Modeling is the same as for a resistor so will briefly review

# Resistor Model

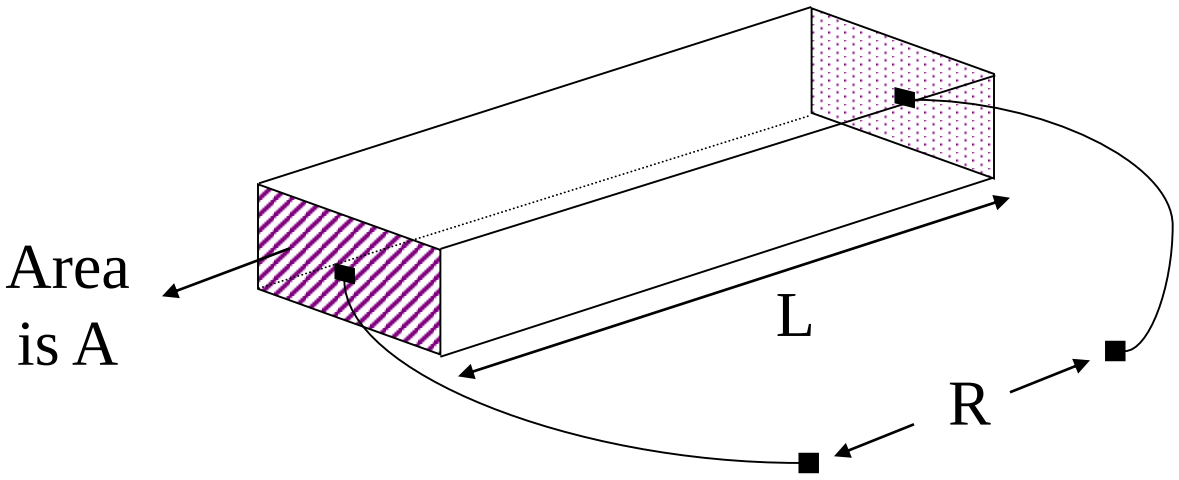



Model:

$$R = \frac{V}{I}$$

# Resistivity

- Volumetric measure of conduction capability of a material

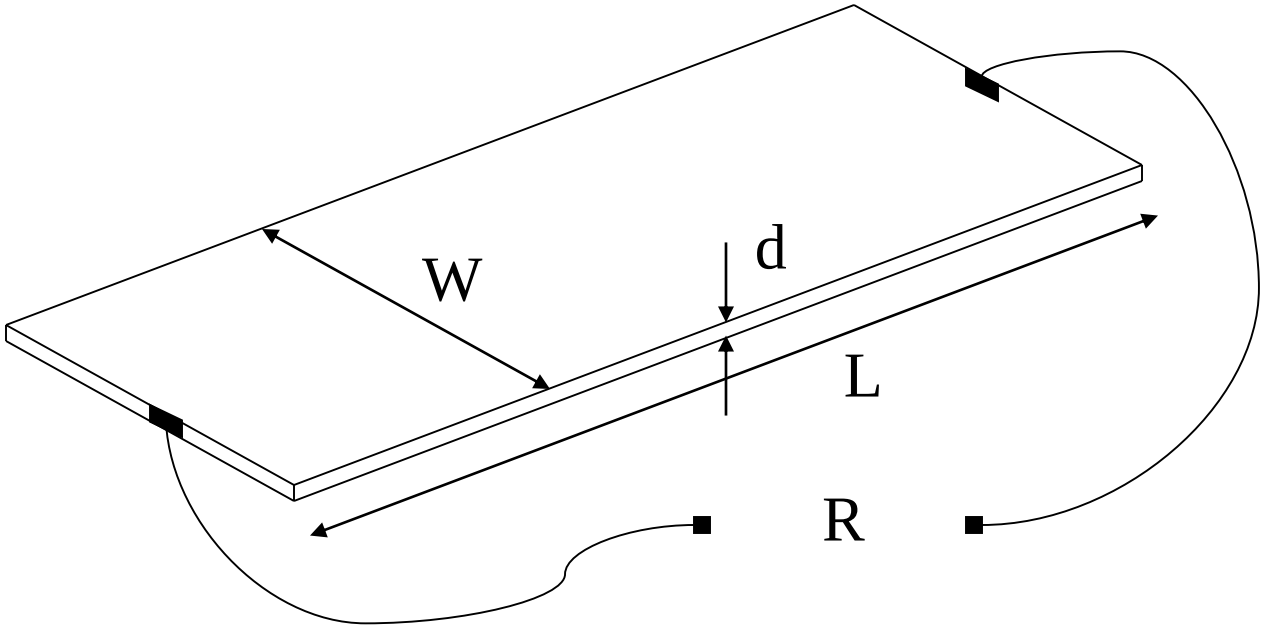



$$\rho = \frac{AR}{L}$$

for homogeneous material,
$\rho \perp A, R, L$

units : ohm cm

# Sheet Resistance




$$R_{\square} = \frac{RW}{L} \quad (\text{ for } d << w,\ d << L\ ) \qquad \text{units : ohms /•}$$

for homogeneous materials, R□ is independent of W, L, R

# Relationship between ρ and $R_{□}$

$$R_{□} = \frac{RW}{L} \qquad \rho = \frac{AR}{L}$$

$$\rho = \frac{A}{W} R_{□}$$

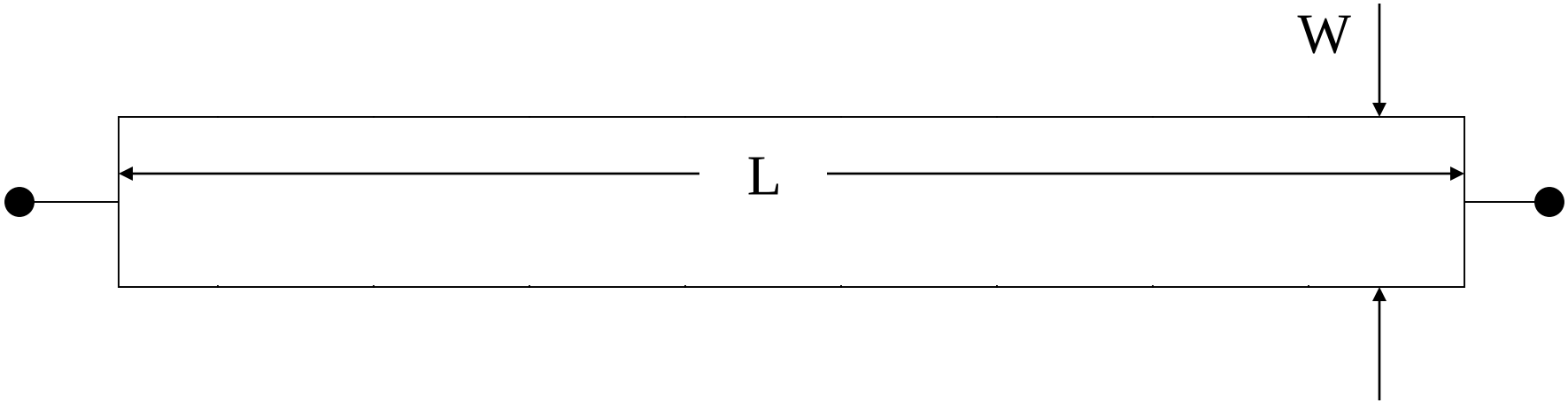
$$A = W \times d$$

$$\rho = \frac{A}{W} R_{□} = \frac{W\,d}{W} R_{□} = d \times R_{□}$$

Number of squares, $N_S$, often used instead of L / W in determining resistance of film resistors

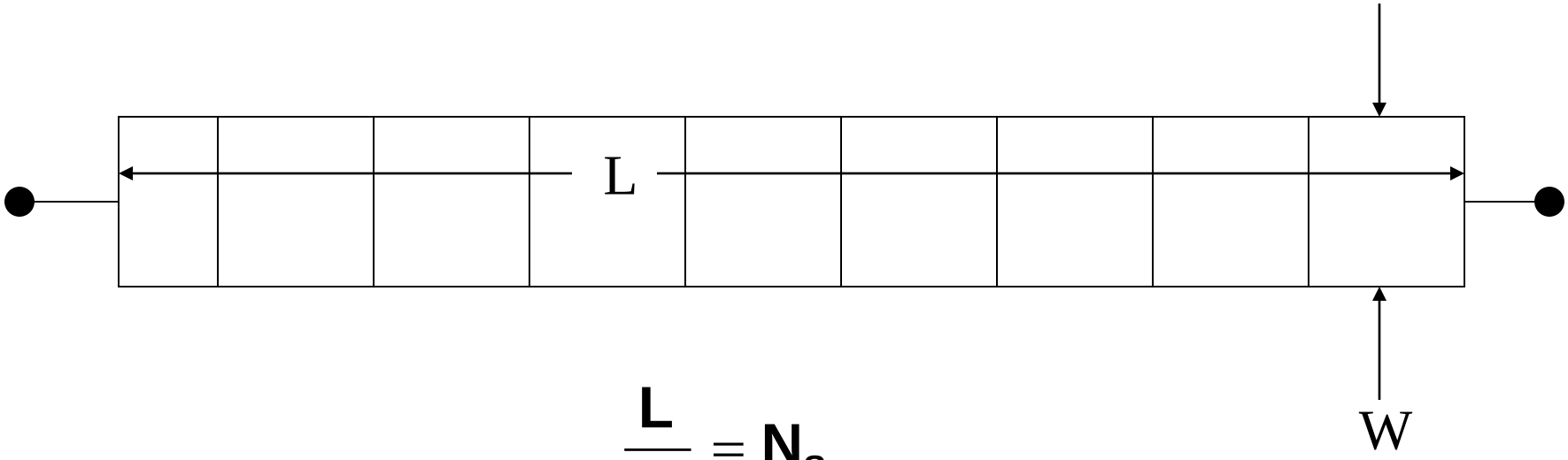
$$R = R_{□} N_S$$

# Example 1



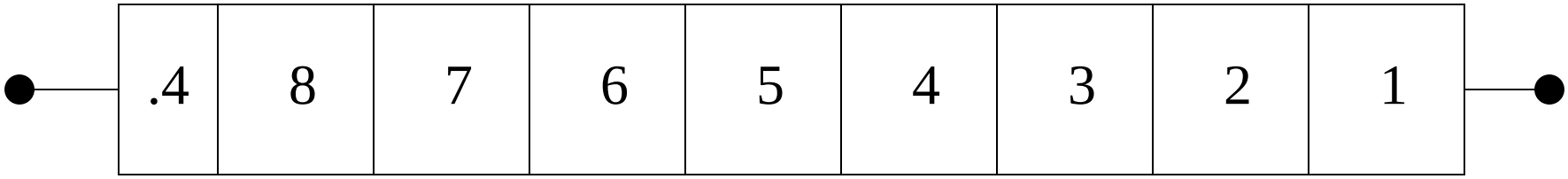

R = ?

# Example 1



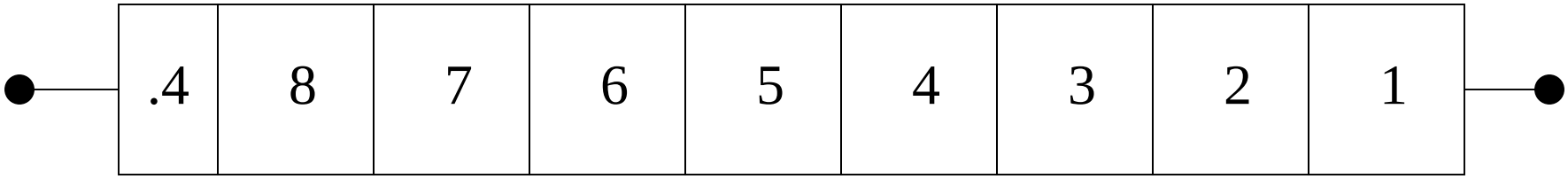

$$\frac{\mathbf{L}}{\mathbf{W}} = \mathbf{N_S}$$

# Example 1




R = ?

# Example 1

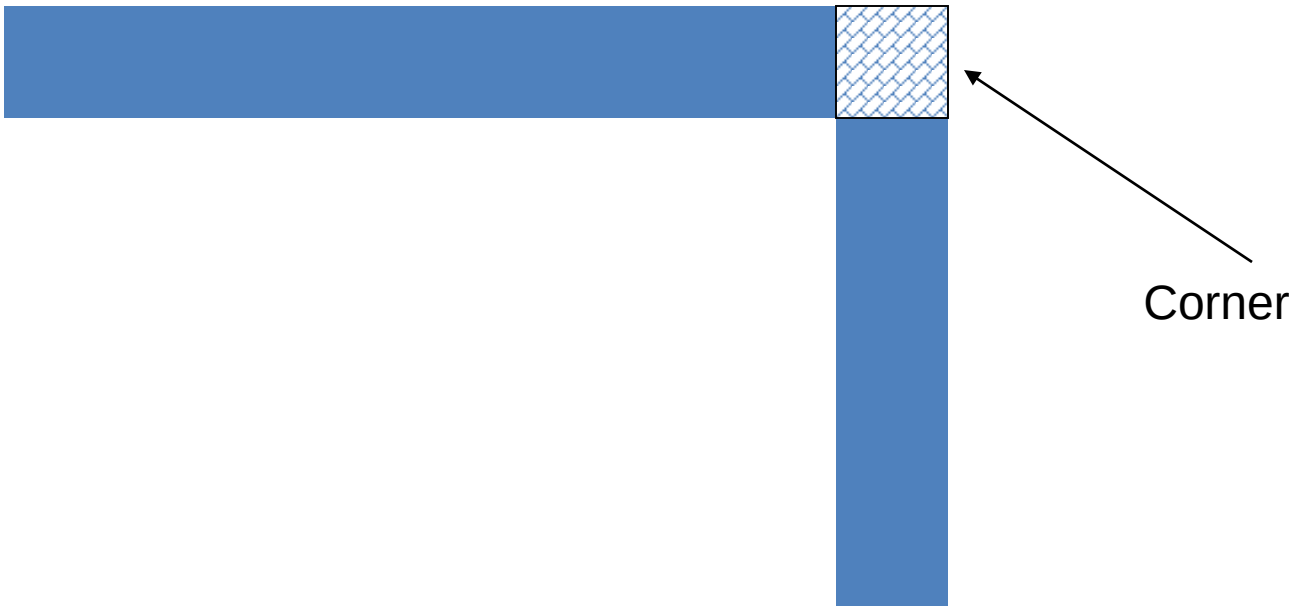



$R = ?$

$N_S = 8.4$

**$R = R_{8.4}$**

# Corners in Film Resistors

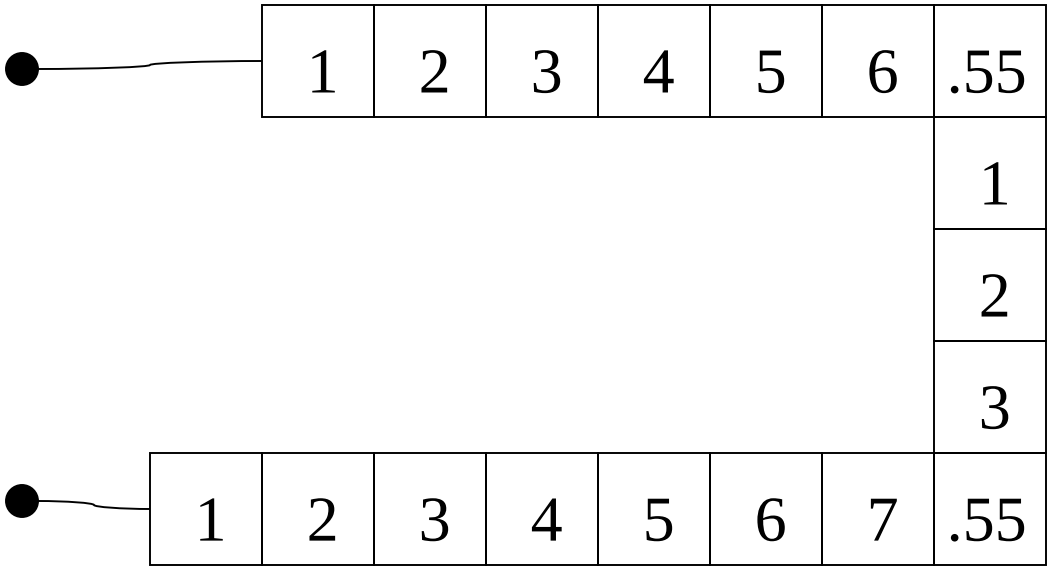



Rule of Thumb: .55 squares for each corner

# Example 2

Determine R if $R_s = 100\ \Omega/\bullet$

# Example 2




$N_S$=17.1

R = (17.1) R

R = 1710 Ω

# Resistivity of Materials used in Semiconductor Processing

- Cu: 1.7*E*-6 Ωcm
- Al: 2.7*E*-4 Ωcm
- Gold: 2.4*E*-6 Ωcm
- Platinum: 3.0*E*-6 Ωcm
- Polysilicon: 1E-2 to 1E4 Ωcm*
- n-Si: typically .25 to 5 Ωcm* (but larger range possible)
- intrinsic Si: 2.5*E5* Ωcm
- $SiO_2$: *E*14 Ωcm

* But fixed in a given process

http://www.cleanroom.byu.edu/ResistivityCal.phtml

**Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon**

Dopant: (•) Arsenic ( ) Boron ( ) Phosphorus

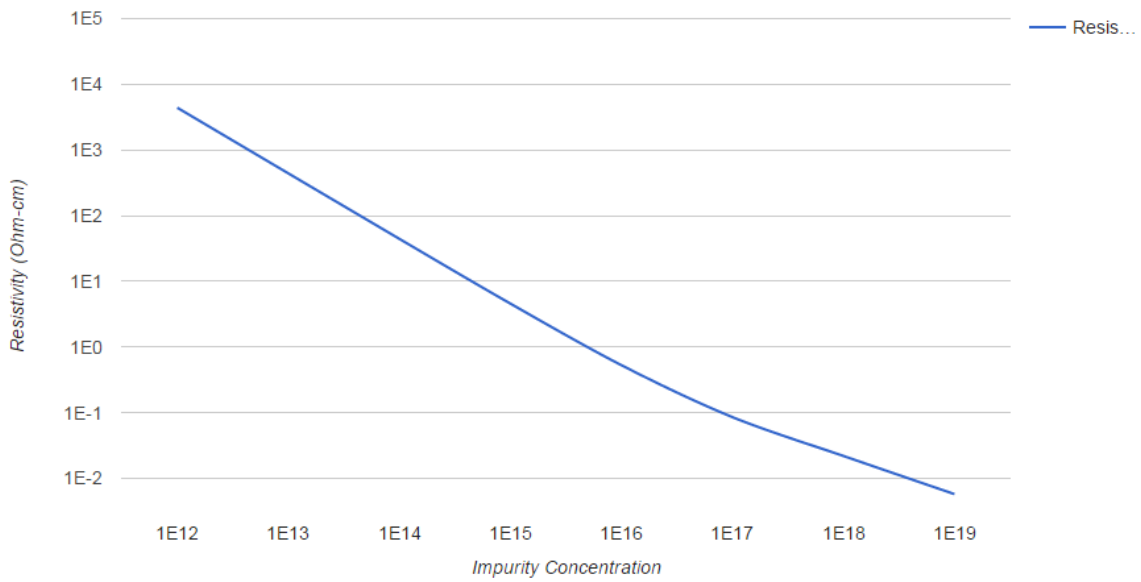
Impurity Concentration: 1e15 ($cm^{-3}$)

Calculate | Export to CSV

Mobility: 1358.6941377290254 [$cm^2/V\text{-}s$]

Resistivity: 4.593746148183427 [$\Omega\text{-}cm$]

Calculations are for a silicon substrate.



http://www.cleanroom.byu.edu/ResistivityCal.phtml

## Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- ○ Arsenic
- ◉ Boron
- ○ Phosphorus

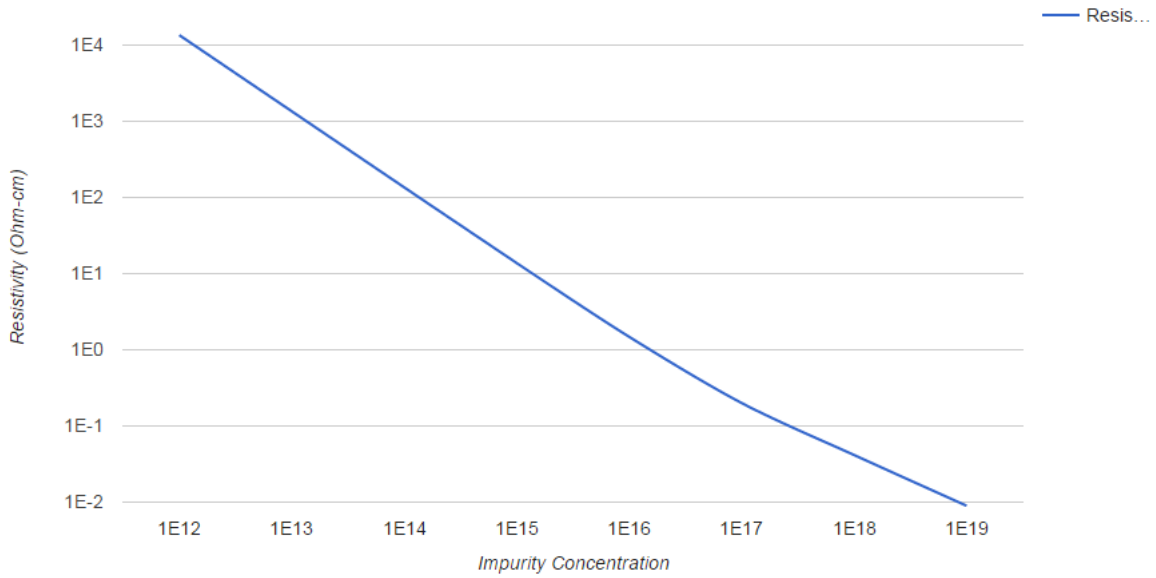
Impurity Concentration: 1e15 ($cm^{-3}$)

Calculate | Export to CSV

Mobility: 461.9540345952693 [$cm^2/V\text{-}s$]

Resistivity: 13.511075765839905 [Ω-cm]

Calculations are for a silicon substrate.



http://www.cleanroom.byu.edu/ResistivityCal.phtml

## Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- ○ Arsenic
- ○ Boron
- ◉ Phosphorus

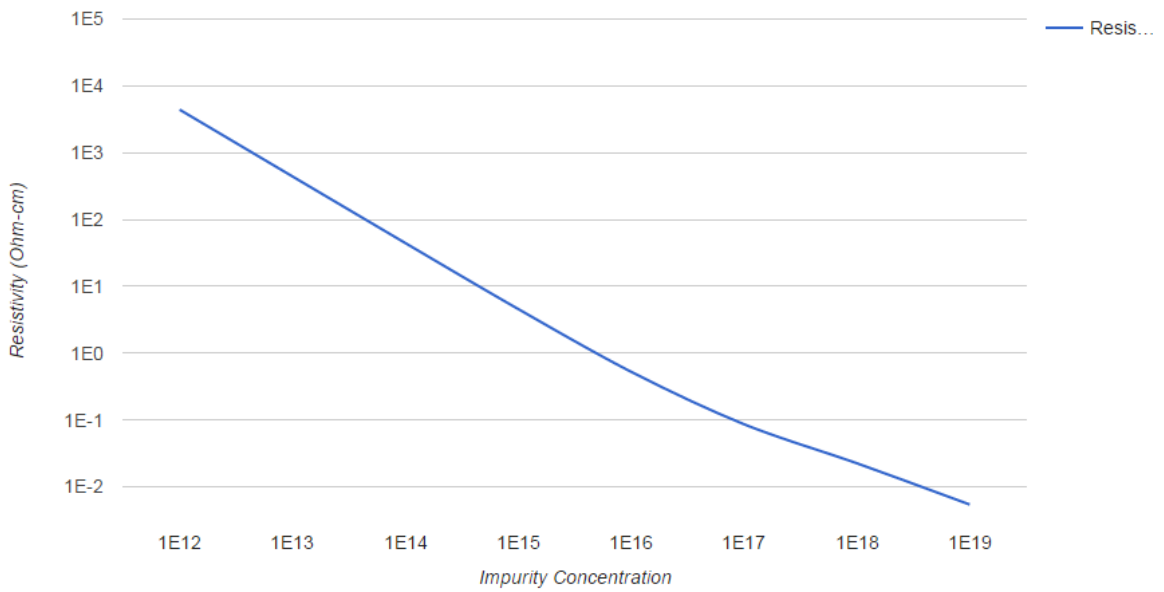
Impurity Concentration: 1e15 ($cm^{-3}$)

Calculate | Export to CSV

Mobility: 1362.0563795030084 [$cm^2/V\text{-}s$]

Resistivity: 4.582406466925789 [$\Omega$-cm]

Calculations are for a silicon substrate.



# Temperature Coefficients

Used for indicating temperature sensitivity of resistors & capacitors

**For a resistor:**

$$\mathbf{TCR} = \left( \frac{\mathbf{1}}{\mathbf{R}} \frac{\mathbf{dR}}{\mathbf{dT}} \right)\Bigg|_{\mathbf{op.\ temp}} \bullet \mathbf{10^6\ ppm/^\circ C}$$

This diff eqn can easily be solved if TCR is a constant

$$R(T_2) = R(T_1) e^{\frac{T_2 - T_1}{10^6} TCR}$$

$$R(T_2) \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right]$$

Identical Expressions for Capacitors

End of Lecture 12