EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 2
Fall 2017

Instructions: This is a 50-minute exam. Students may bring 2 pages of notes (front and back) to this exam. Each short question is worth 2 points and each problem is worth 16 points. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=1V$,$V_{TPO}= - 1V$, $\gamma =0.4V^{-1/2,}$, $\phi=0.6V$, $C_{OX}=2fF/\mu^2$, and $\lambda = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta_n=100$, $\beta_p=10$, and $V_{AF} = \infty$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters are needed, use the process parameters associated with the process described on the attachments to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters. Also attached to this exam is a table that has information about large and small signal models of devices.

1. (2 pts) What is the major reason that the small-signal model of the BJT was developed for operation in the Forward Active region?

2. (2 pts) The diode equation is much more difficult to work with than the simpler piecewise-linear diode model (open circuit when not conducting and a dc voltage source of 0.6V when conducting). What is a quick way to check and see if the simpler piecewise-linear model can be used when analyzing a diode circuit?

3. (2 pts) What is the approximate number of parameters in the BSIM model of a MOSFET?

4. (2 pts) In the CMOS process flow discussed in class, does the n+ source/drain diffusion come before or after the n-well diffusion?

5. (2pts) Placing the n+ buried collector under the p-base diffusion is used to reduce the resistance in the collector lead of a vertical npn transistor. The same n+ diffusion is also placed under the lateral pnp transistors. What is the major benefit of placing the n+ diffusion under the lateral pnp transistors?

6. (2pts) With similar minimum feature sizes, the area required for a minimum-sized vertical npn transistor in a bipolar process is much larger than the area required for a minimum-sized NMOS transistor in a bulk CMOS process. What processing step in a bipolar process is the major contributor to the large size of the vertical npn bipolar transistor?

7. (2pts) What is the major reason the g_m of a BJT is much larger than that of a MOSFET if they are biased at the same current level?

8. (2pts) What parameter in the JFET model corresponds to the threshold voltage in a MOSFET?

9 (2pts) How many small-signal parameters are required for the small-signal model of a nonlinear one-port circuit?

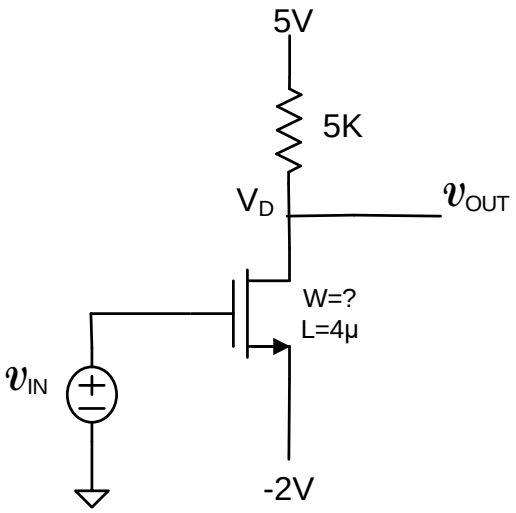
10 (2pts) There is a term that is widely used for a two-port circuit in which the signal propagates in only one direction. What is the special term that indicates a signal propagates in only one direction?

Problem 1 (16 pt) Consider the following circuit.

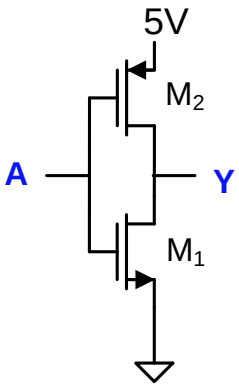
a) Draw the small signal equivalent circuit assuming the MOS transistor is operating in the saturation region

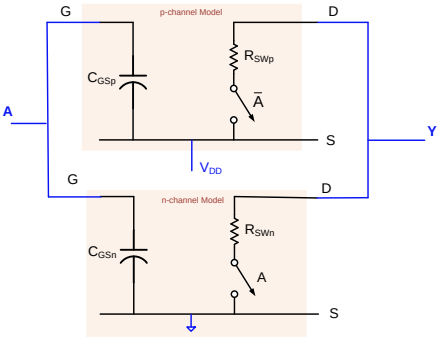
b) Give the small-signal voltage gain in terms of the small-signal model parameters assuming the MOS transistor is operating in the saturation region

c) Determine W so that the small-signal voltage gain is -5



Problem 2 (16 pts) A standard CMOS inverter is shown below along with a switch-level model for the inverter. If this inverter is designed in the process characterized by the model parameters given in the instructions for this exam, determine the switch-level model parameters R_{SWp}, R_{SWn},C_{GSn}, and C_{GSp}. Assume the dimensions of the transistors are W_1=5µ, L_1=5µ, W_2=20µ and L_2=5µ.

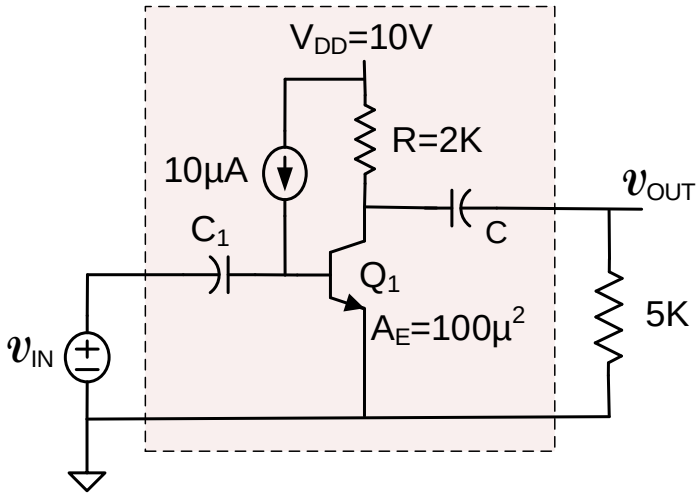




Problem 3 (16 pts) Consider the following circuit.

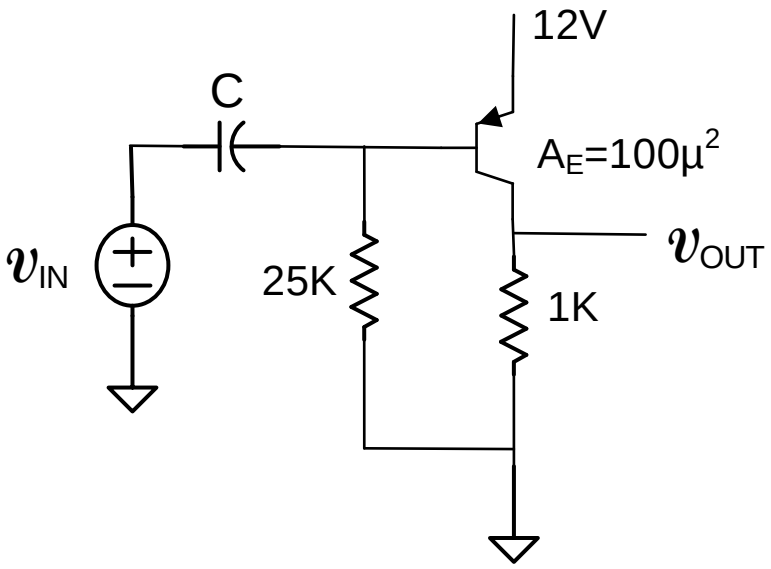
a) Give the two-port model for the portion of the circuit that is in the shaded region in terms of the small-signal amplifier model parameters. Assume the capacitors are large.

b) Repeat part a) but with the numerical values for the small-signal amplifier model parameters.

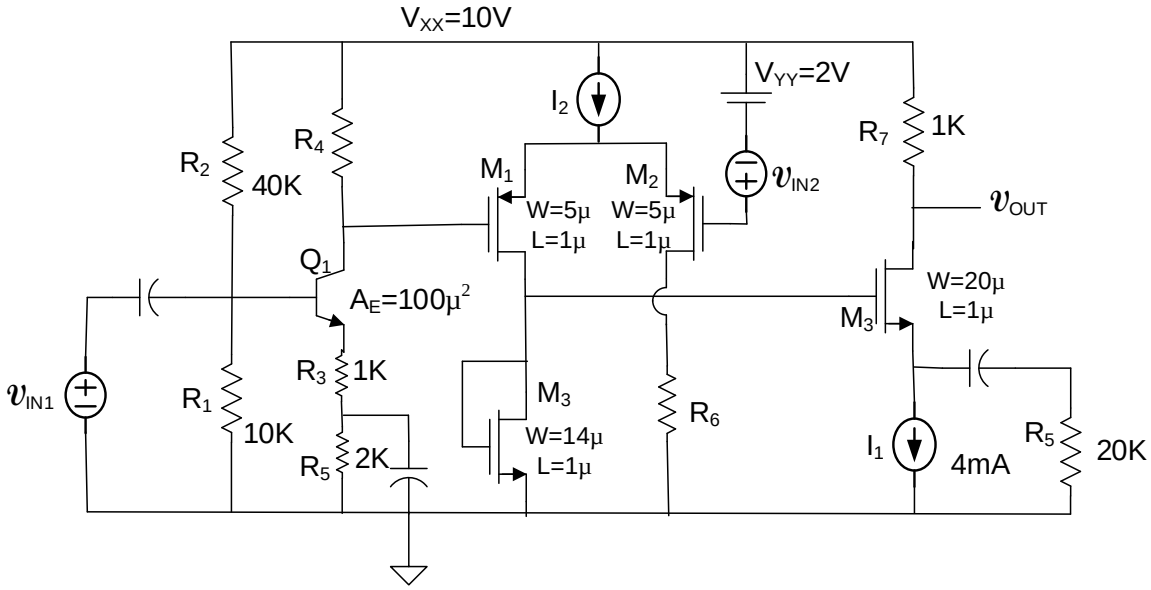


Problem 4 (16 pts) Consider the following circuit. Assume the β of the pnp transistor is 10.

a) Determine the quiescent output voltage
b) Determine the small-signal voltage gain. Assume C is large.
c) The β of a transistor is quite process and temperature dependent. If the β of the transistor varies between 8 and 12, what will be the variation in the small signal voltage gain?.



Problem 5 (16 pts) Draw the small-signal equivalent circuit for the following amplifier structure. Assume the capacitor is large, all MOS transistors are operating in the Saturation region, and all bipolar transistors are operating in the Forward Active region. Do not solve.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

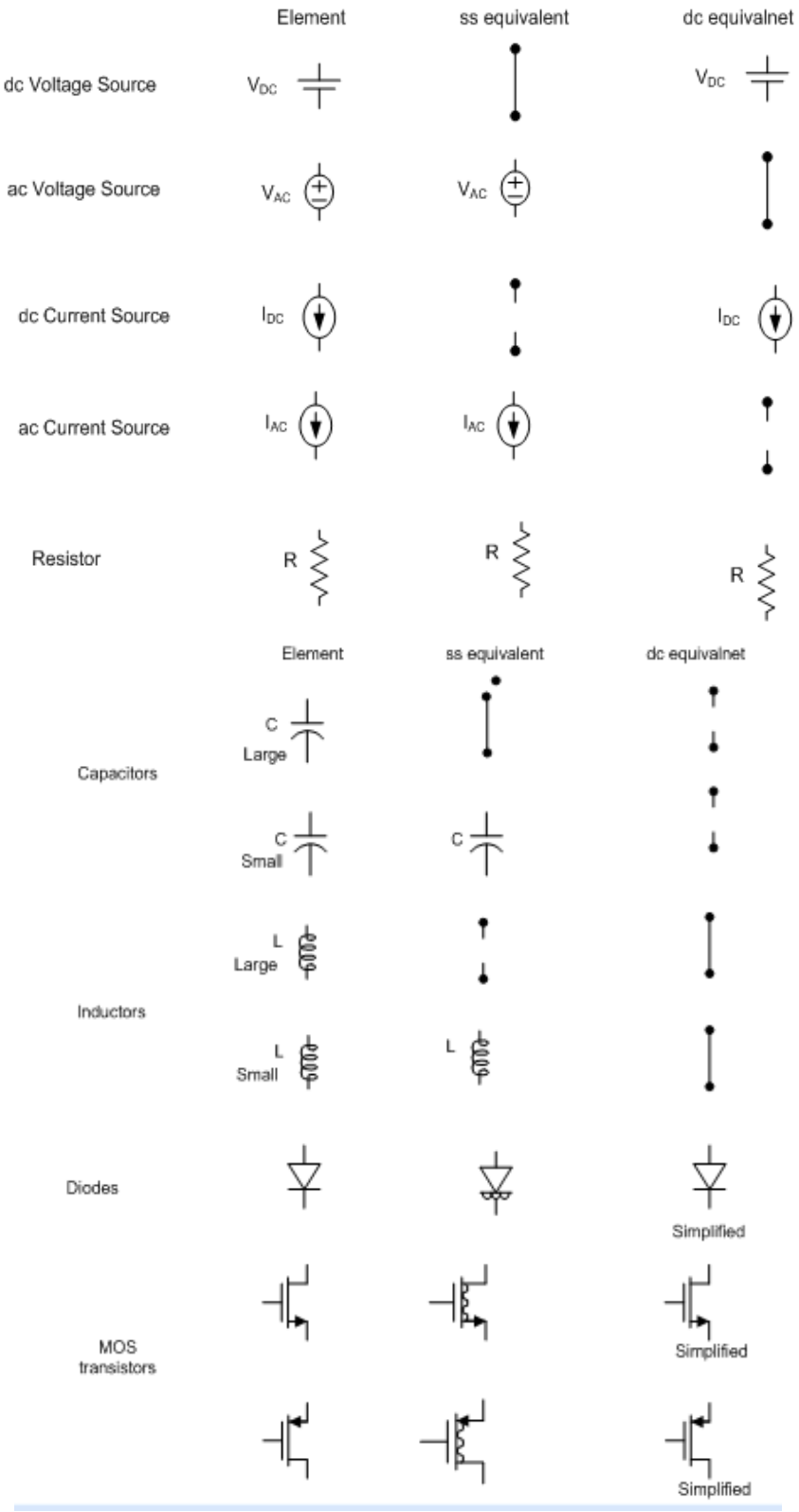
PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

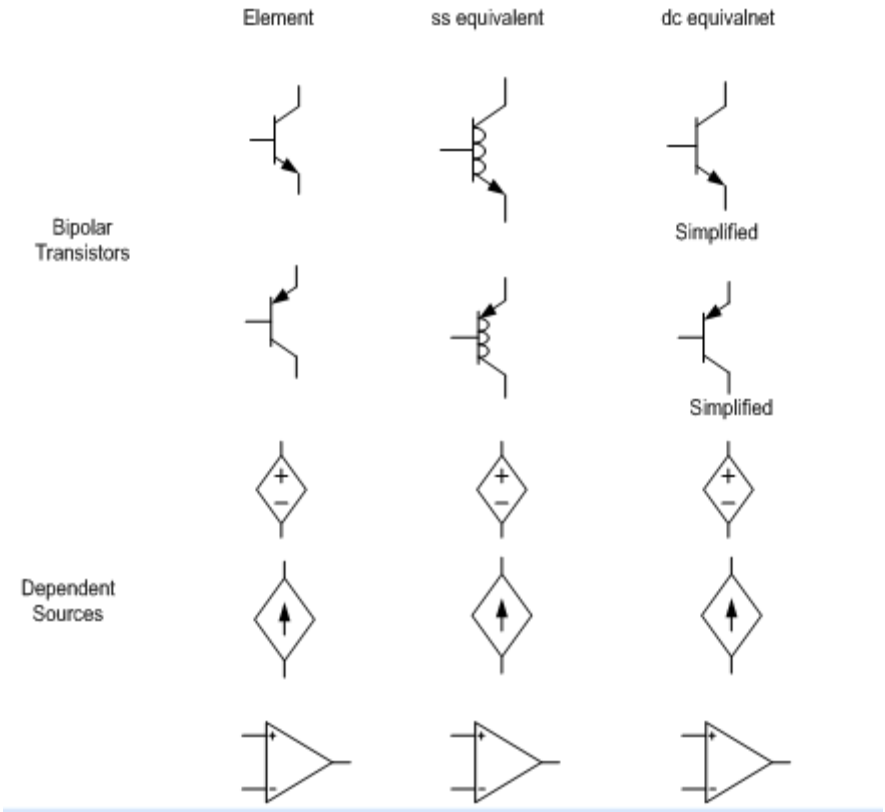
PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Bipolar Transistors
Simplified
Simplified
Dependent Sources