EE 330

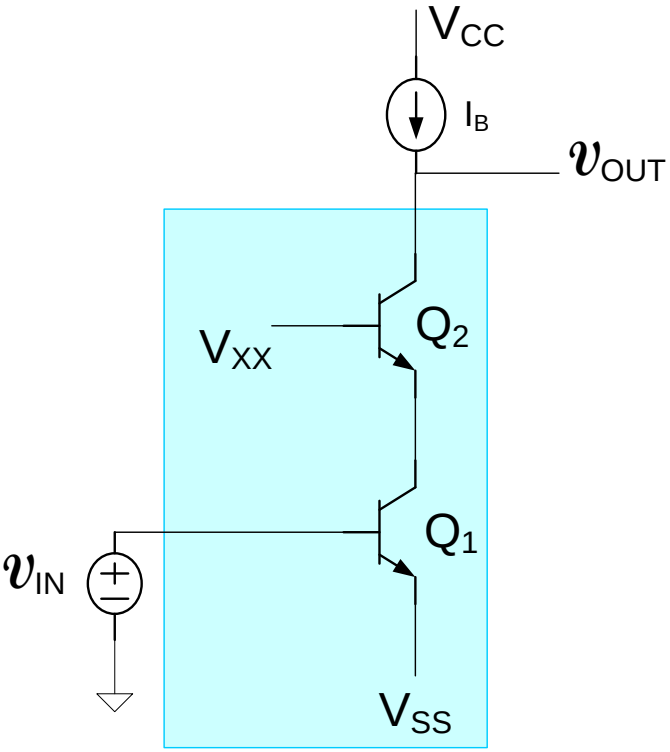
Lecture 36

- Parasitic Capacitances in MOS Devices
- Digital Systems

Review from Last Lecture

Cascode Configuration

Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{02}}\beta\right] \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

$$g_{0CC} \cong \frac{g_{02}}{\beta}$$

$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta = \left[\frac{2V_{AF}}{V_t}\right]\beta = [-8000]100$$

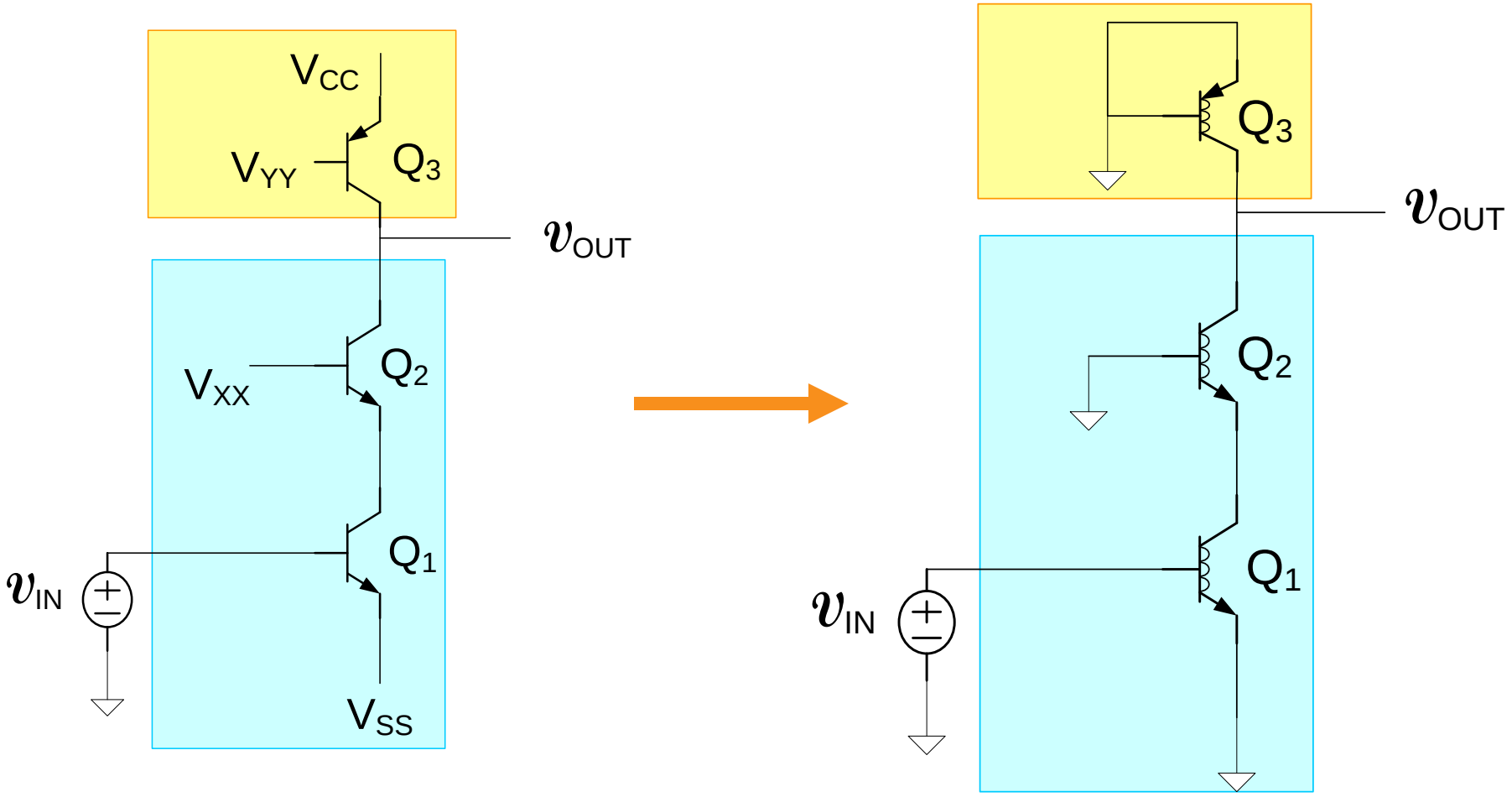
$$A_{VCC} \cong -800{,}000$$

This gain is very large and only requires two transistors!

What happens to the gain if a transistor-level current source is used for I_B?

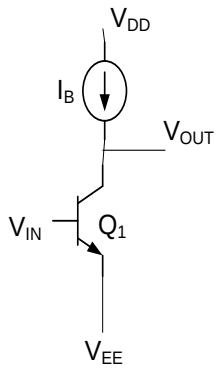
Review from Last Lecture

Cascode Configuration

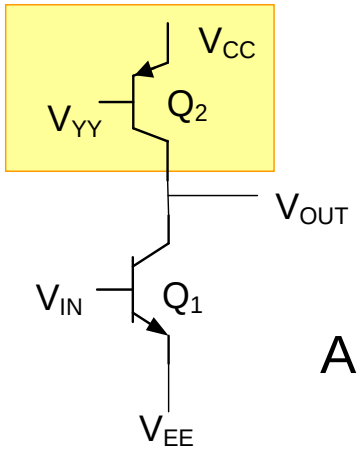


Review from Last Lecture

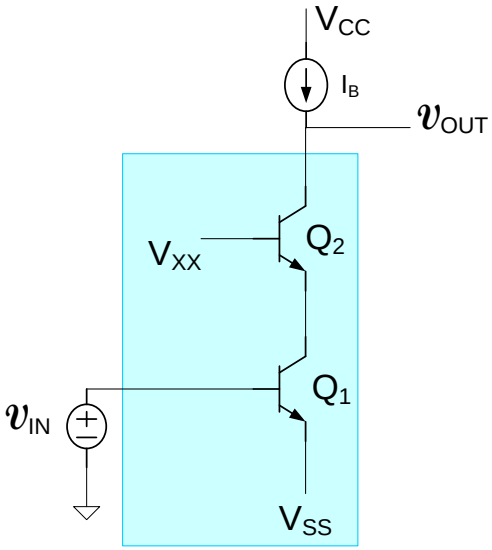
Cascode Configuration Comparisons



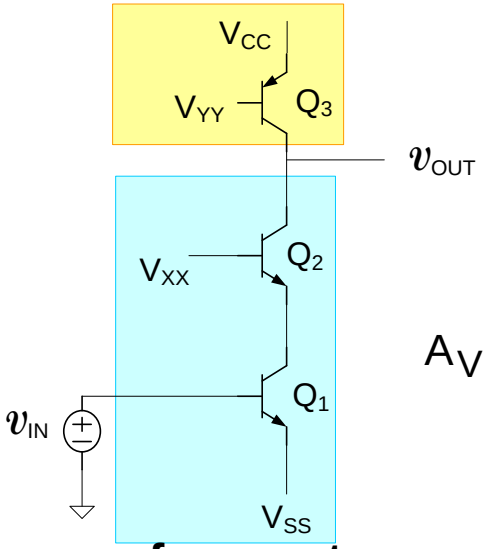
$$A_V = \frac{-g_m}{g_0}$$



$$A_V \cong \frac{-g_{m1}}{g_{01}+g_{02}} = \frac{-g_{m1}}{2g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



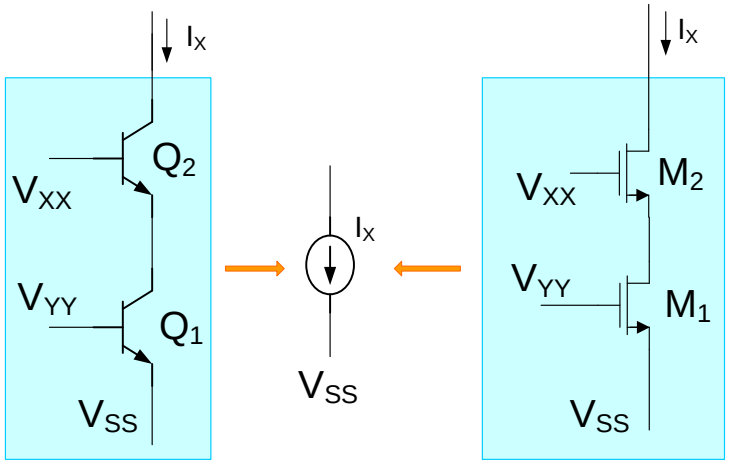
$$A_V \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta}+g_{03}}\right] \cong -\left[\frac{g_{m1}}{g_{03}}\right]$$

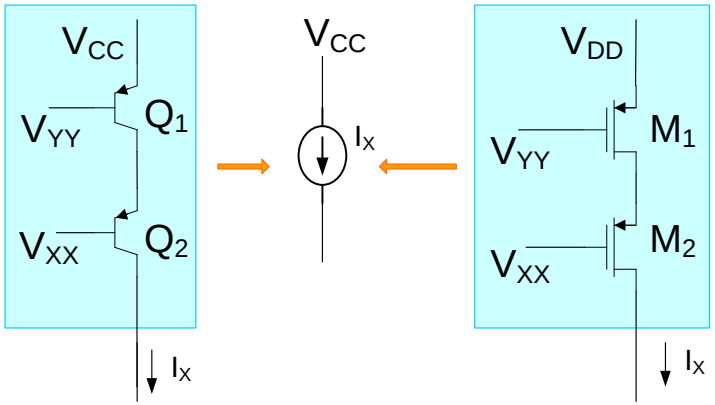
Gain limited by output impedance of current scource !!

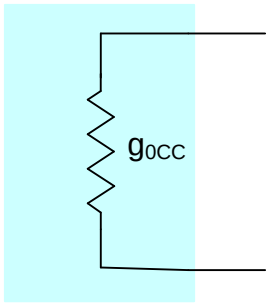
Can we design a better current source?

In particular, one with a higher output impedance?

Cascode current sources







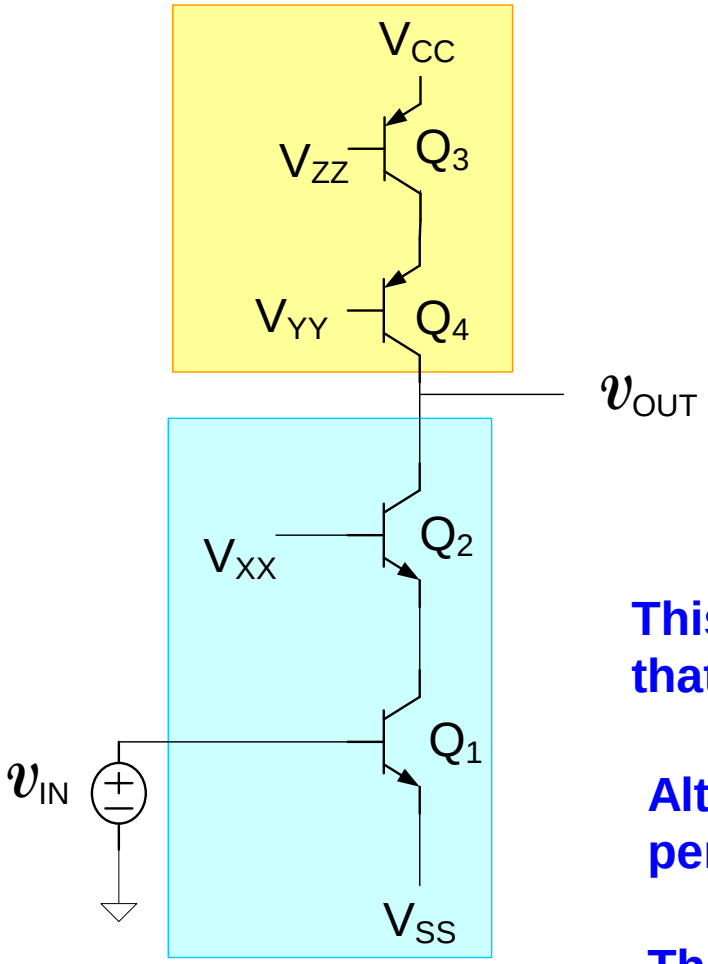
All have the same small-signal model

$$g_{0CC} = \left[\frac{g_{02}\left(g_{01}+g_{\pi 2}\right)}{g_{01}+g_{02}+g_{\pi 2}+g_{m2}} \right]$$

Review from Last Lecture

Cascode Configuration

Discuss



$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

$$A_V = -[8000]\frac{100}{2} \cong -400{,}000$$

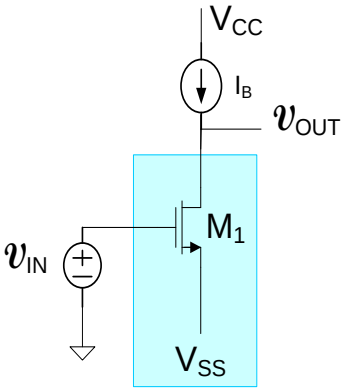
This gain is very large and is a factor of 2 below that obtained with an ideal current source biasing

Although the factor of 2 is not desired, the performance of this circuit is still very good

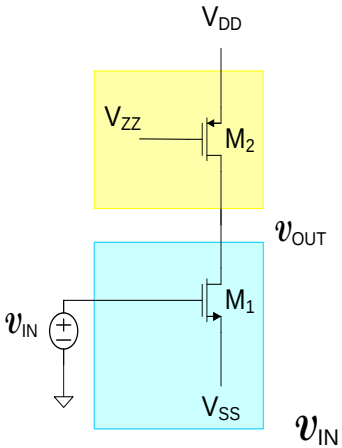
This factor of 2 gain reduction is that same as was observed for the CE amplifier when a transistor-level current source was used

Review from Last Lecture

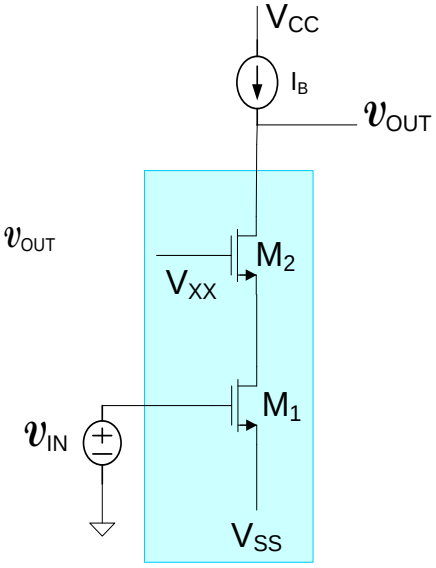
High Gain Amplifier Comparisons (n-ch MOS)



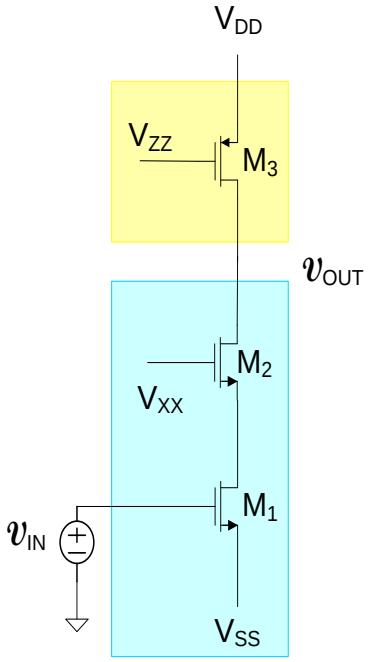
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



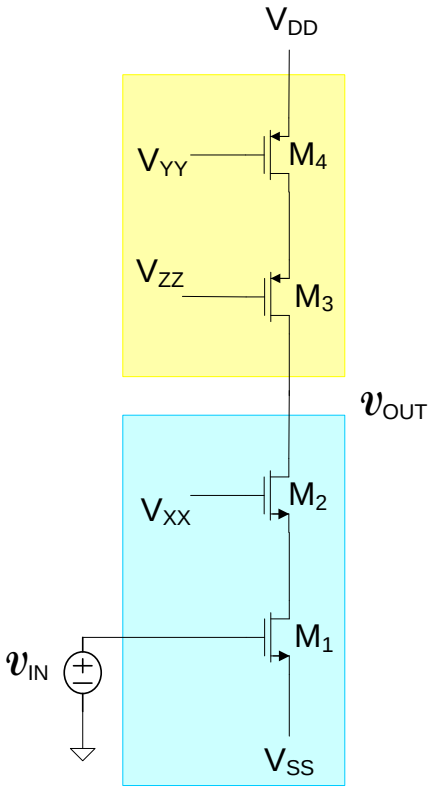
$$A_V \cong -\frac{1}{2}\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_{VCC} \cong -\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$



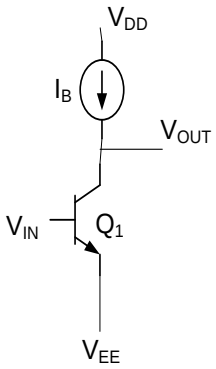
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



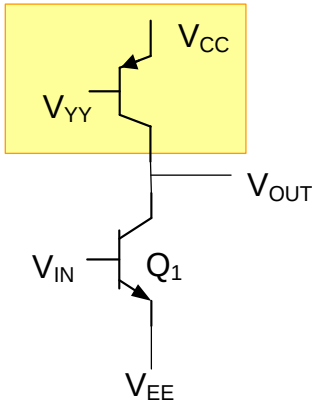
$$A_{VCC} \cong -\frac{1}{2}\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

Review from Last Lecture

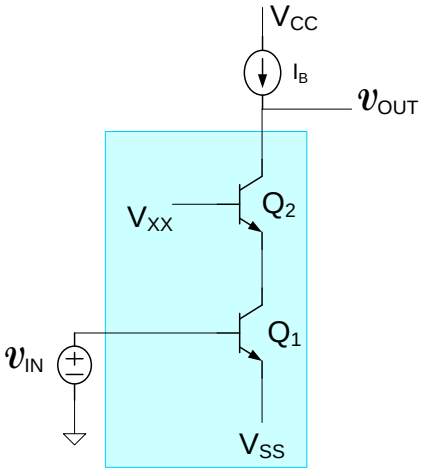
High Gain Amplifier Comparisons (BJT)



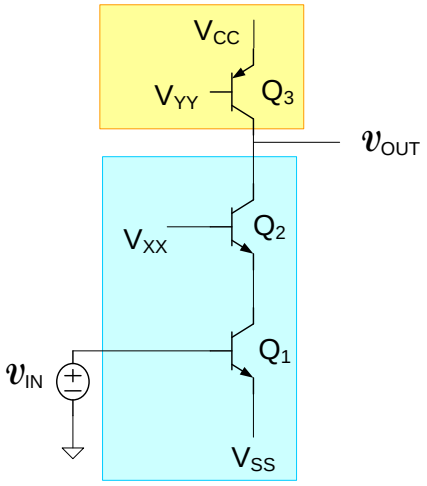
$$A_V = \frac{-g_m}{g_0}$$



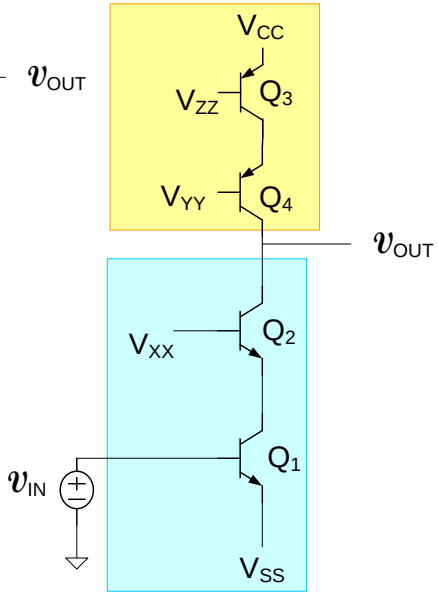
$$A_V \cong -\frac{1}{2}\frac{g_{m1}}{g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



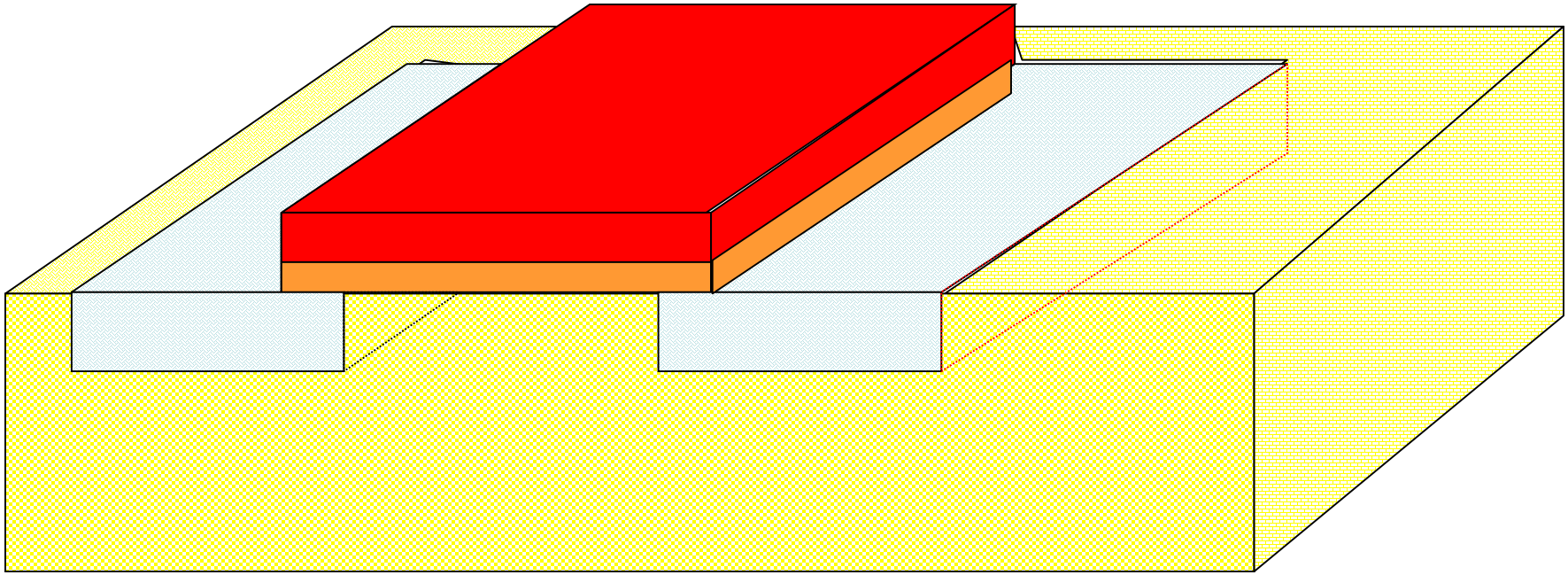
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



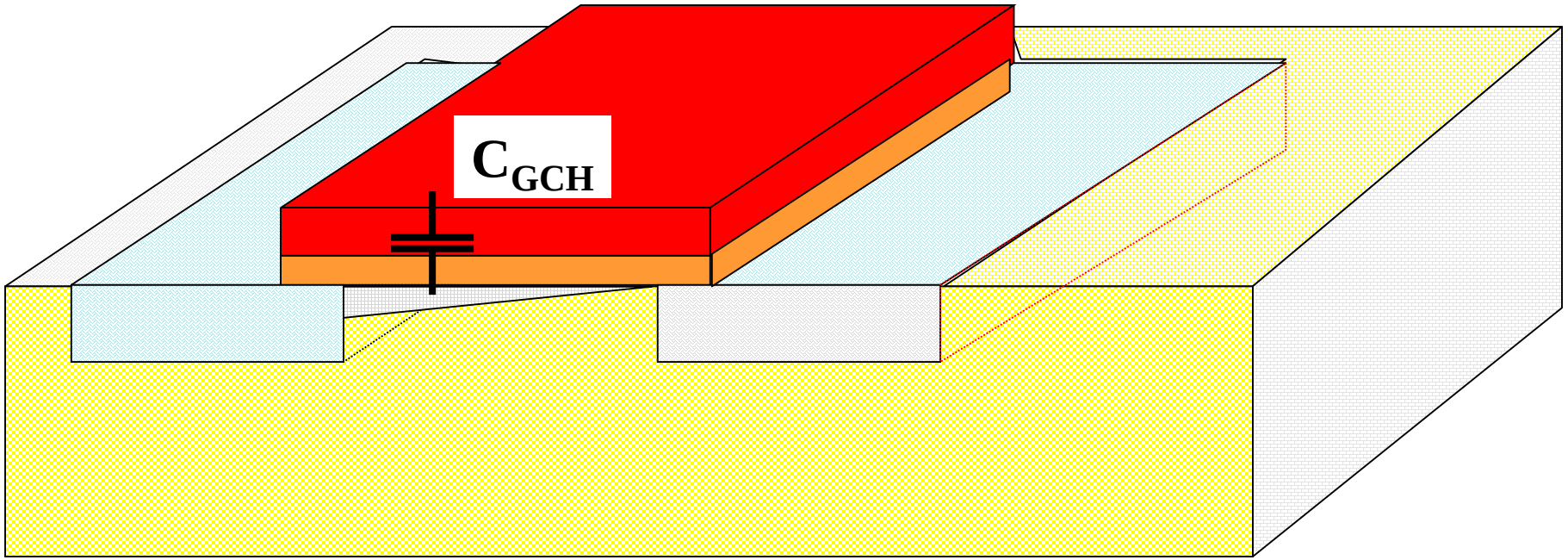
$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

- Single-ended high-gain amplifiers inherently difficult to bias (because of the high gain)
- Biasing becomes practical when used in differential applications
- These structures are widely used but usually with differential inputs

Parasitic Capacitors in MOSFET

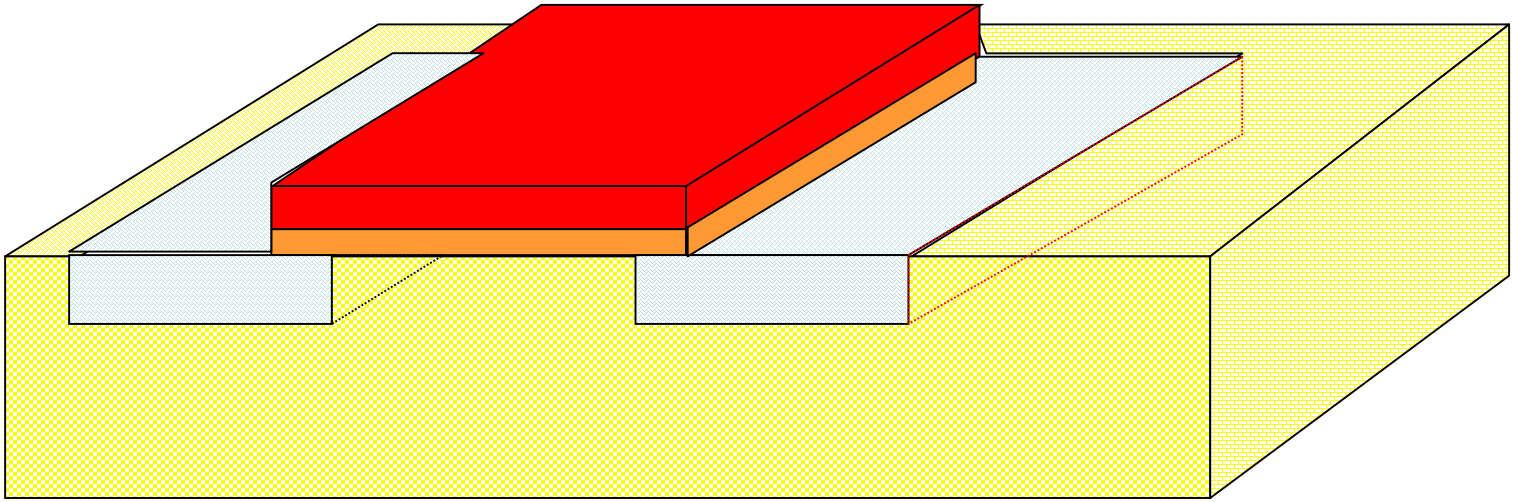


Parasitic Capacitors in MOSFET

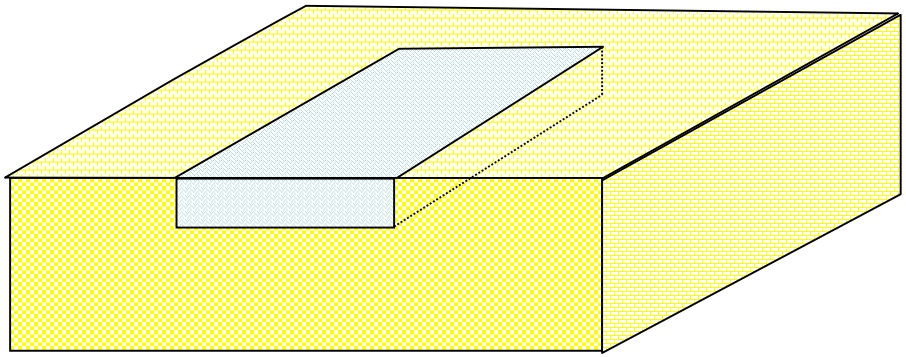


- This capacitance was modeled previously and exists when the transistor is operating in triode or saturation
- But there are others that also affect high-frequency or high-speed operation

Parasitic Capacitors in MOSFET

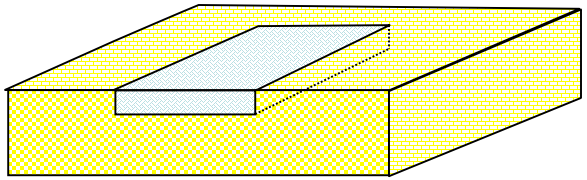


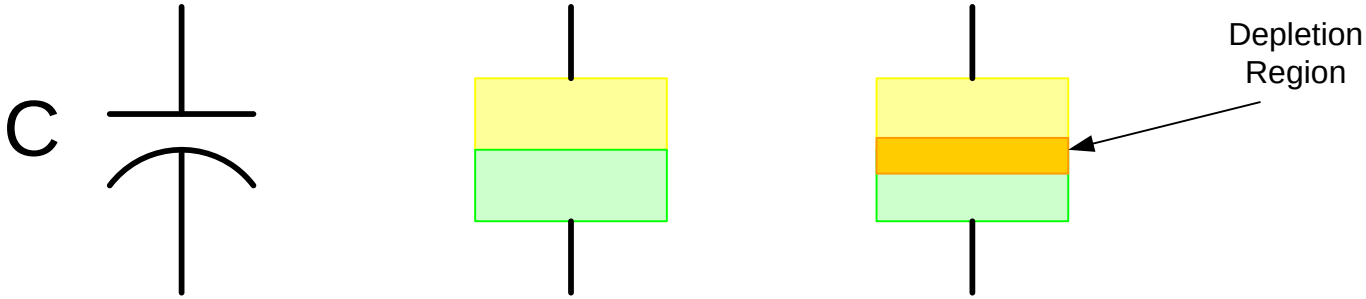
Recall that pn junctions have a depletion region!



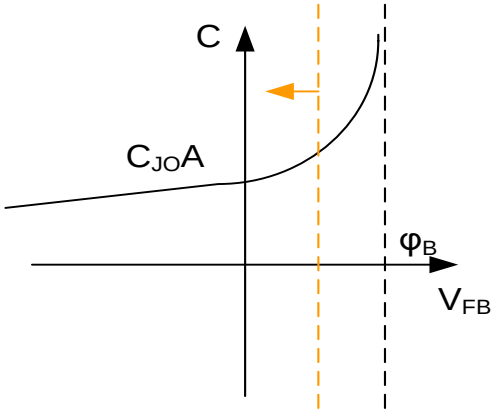
Parasitic Capacitors in MOSFET

pn junction capacitance





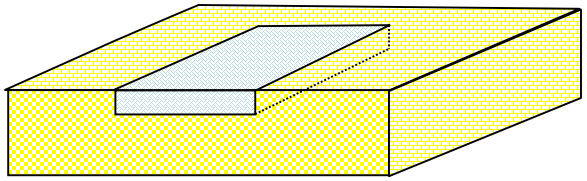
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

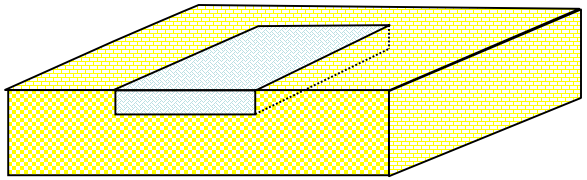
pn junction capacitance

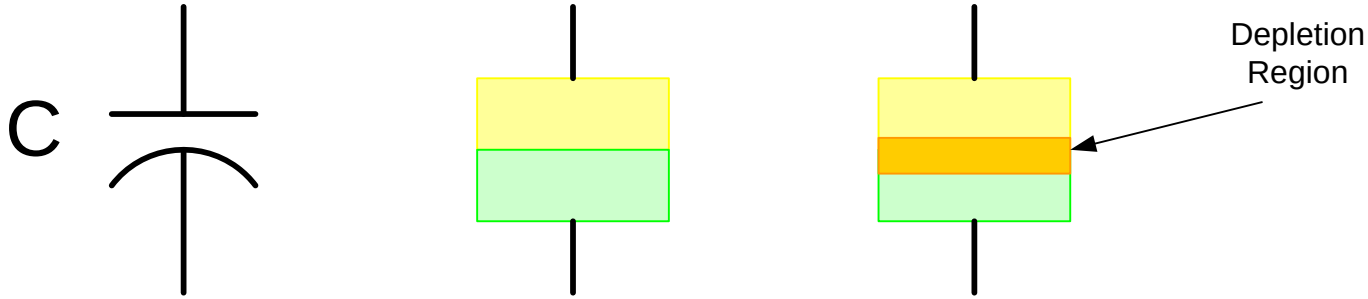


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

$$C_J = C_{BOT} A + C_{SW} P$$

$$C_{BOT} = \frac{C_{BOT} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

$$C_{SW} = \frac{C_{SW} P}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

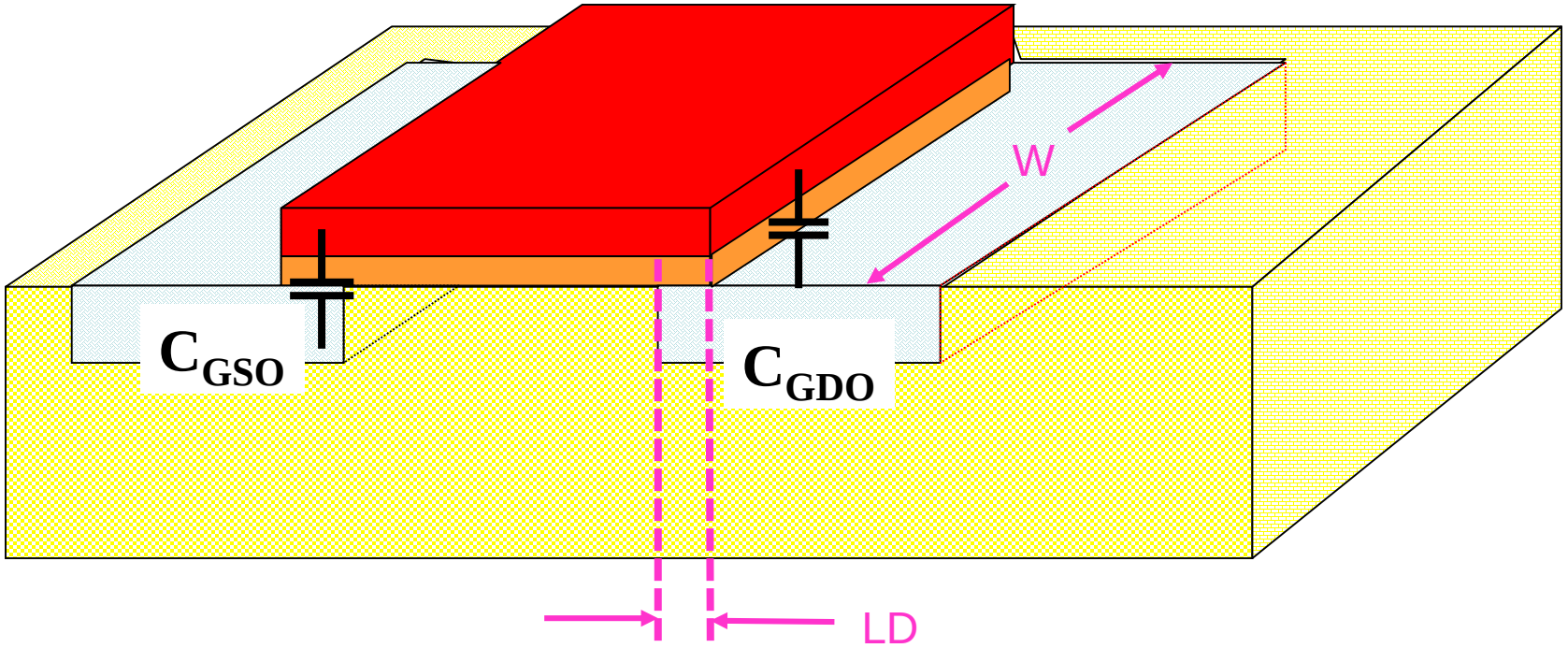
Types of Capacitors in MOSFETs

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent

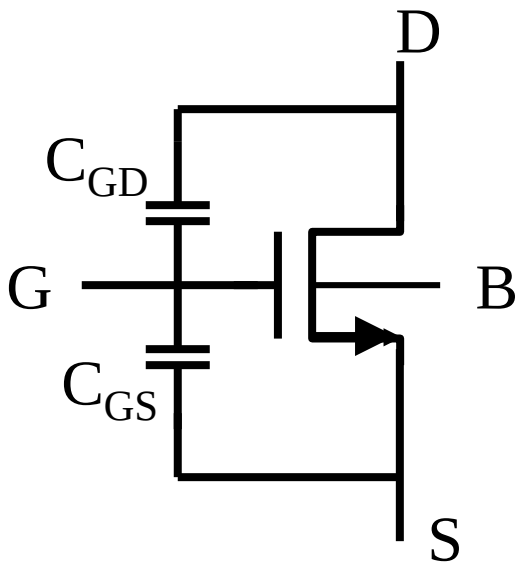
Parasitic Capacitors in MOSFET

Fixed Capacitors – Fixed Geometry



Overlap Capacitors: C_{GDO}, C_{GSO}

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$

L_D is a model parameter

Overlap Capacitance Model Parameters

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34				984	aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235		41	35	29	21	14						aF/um
Fringe (poly)				70	39	29	23	20	17					aF/um
Fringe (metal1)					52	34		22	19					aF/um
Fringe (metal2)						48	35	27	22					aF/um
Fringe (metal3)							53	34	27					aF/um
Fringe (metal4)								58	35					aF/um
Fringe (metal5)									55					aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

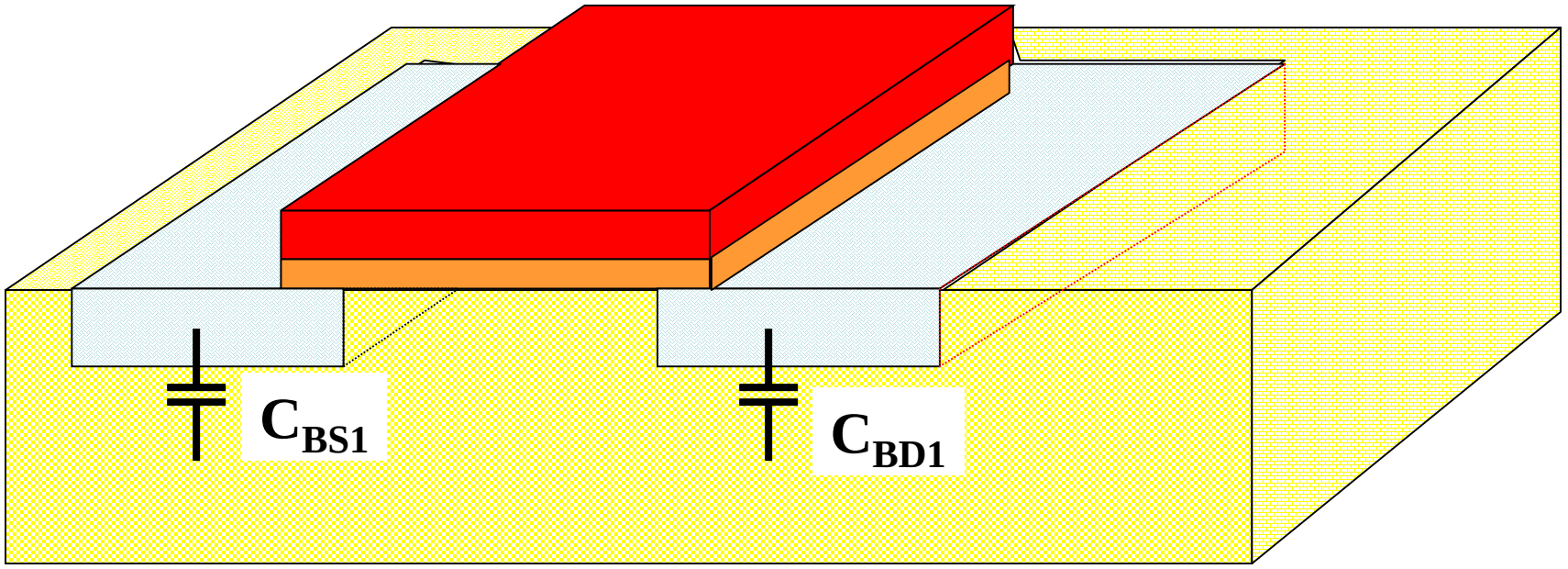
Types of Capacitors in MOSFETs

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent

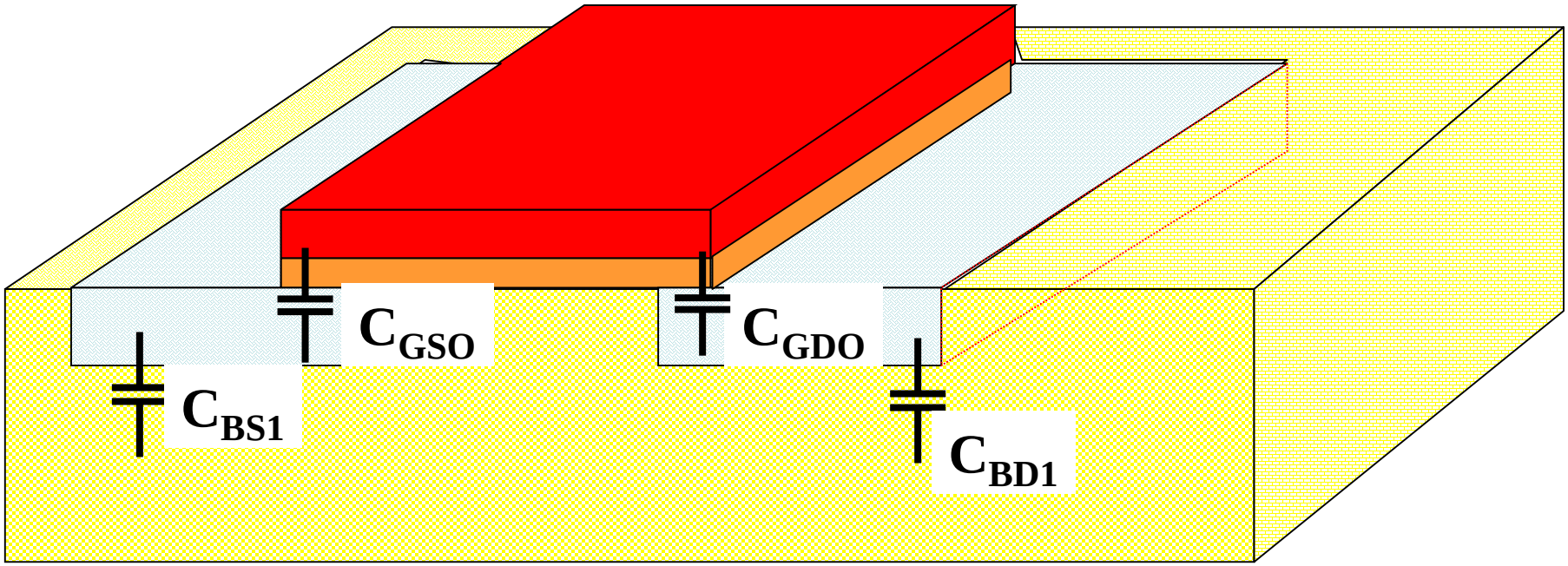
Parasitic Capacitors in MOSFET

Fixed Capacitors- Junction



Junction Capacitors: C_{BS1}, C_{BD1}

Parasitic Capacitors in MOSFET
Fixed Capacitors



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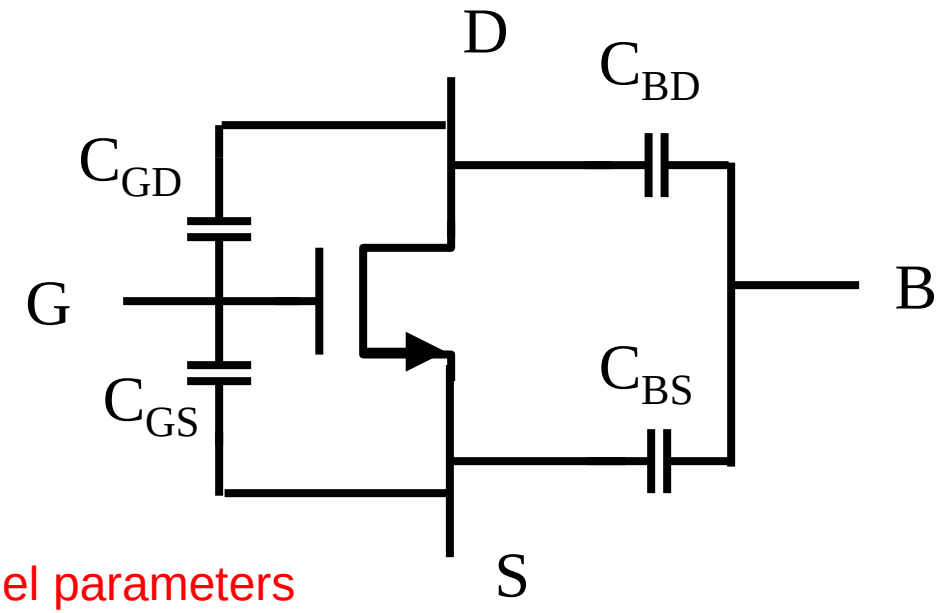
Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}			
C_{BS}	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

C_{BOT} and C_{SW} model parameters

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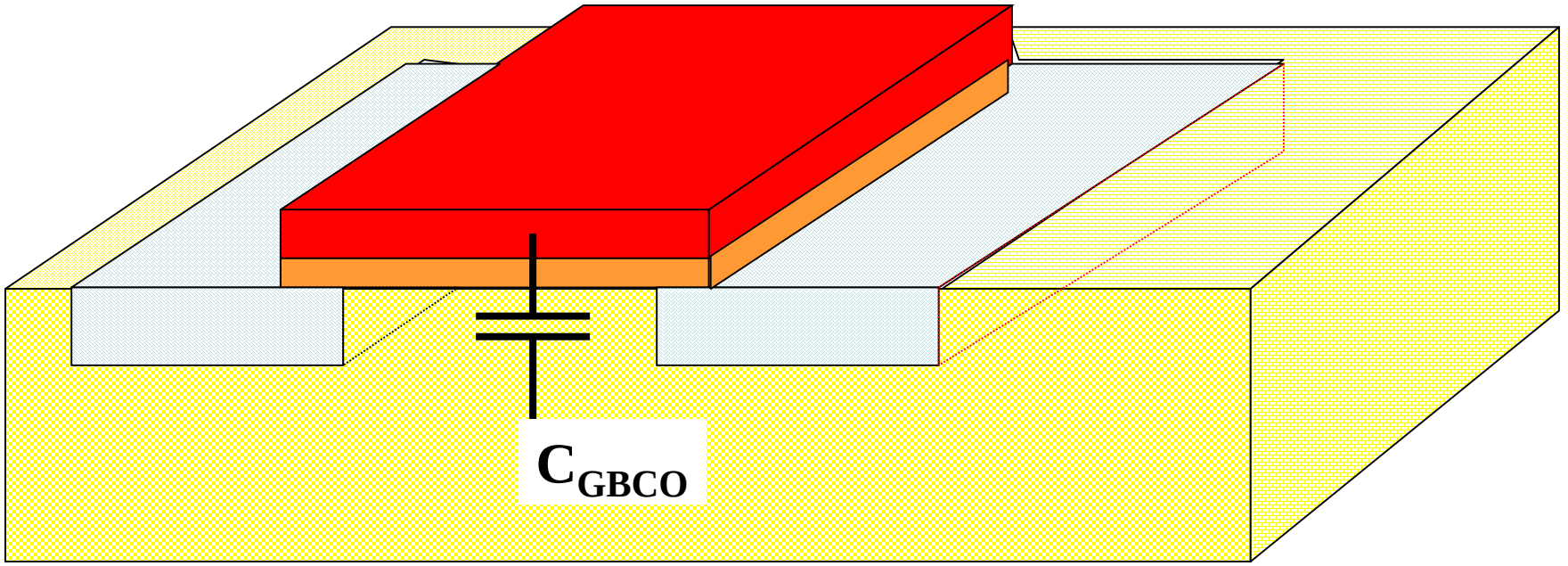
Parasitic Capacitors in MOSFET

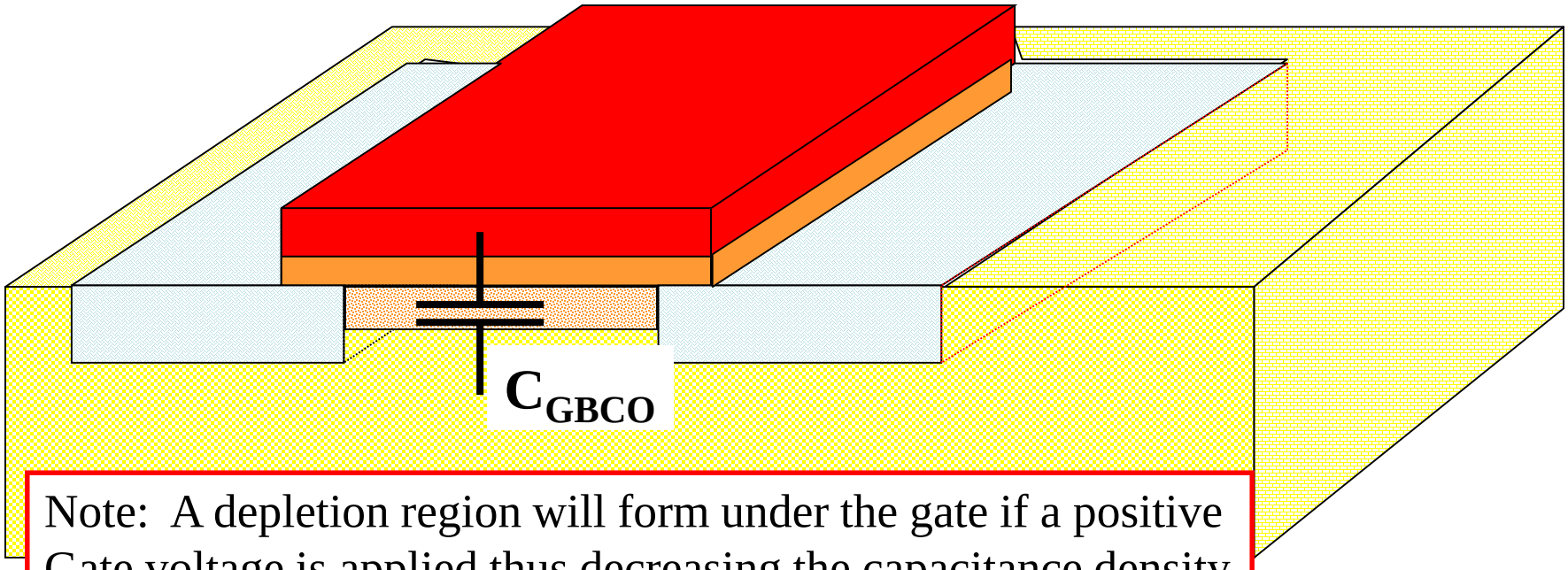
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

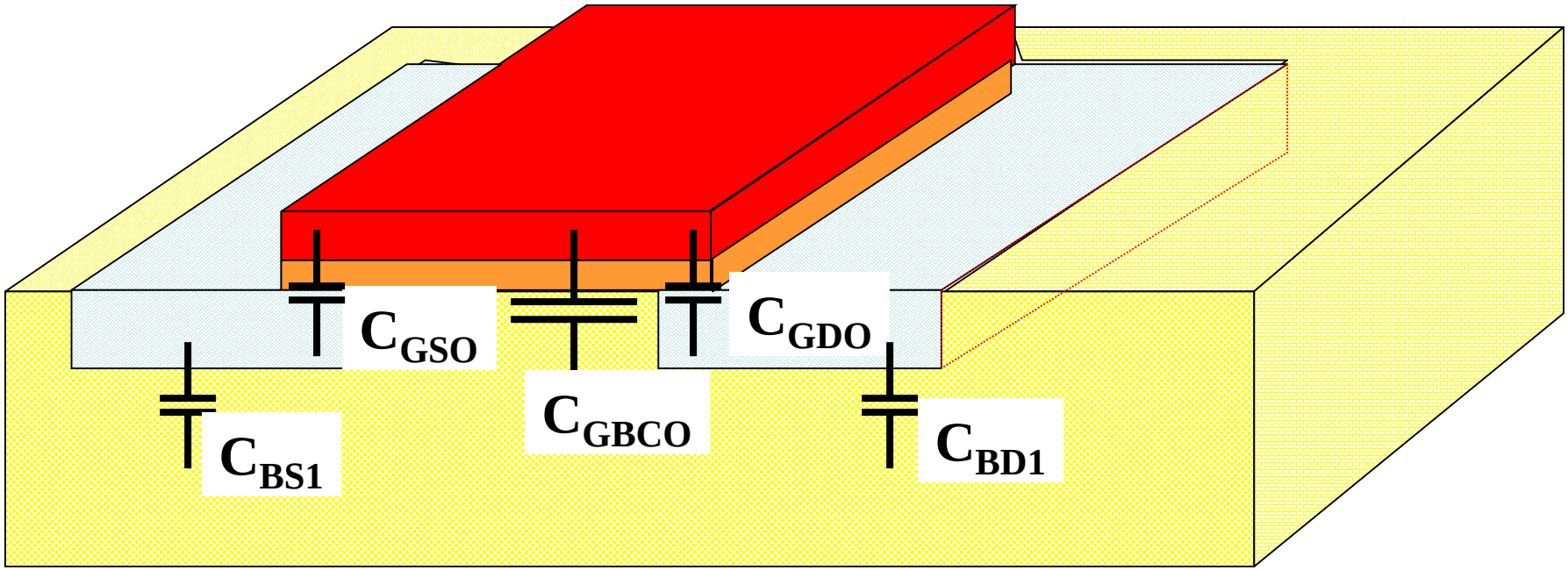


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

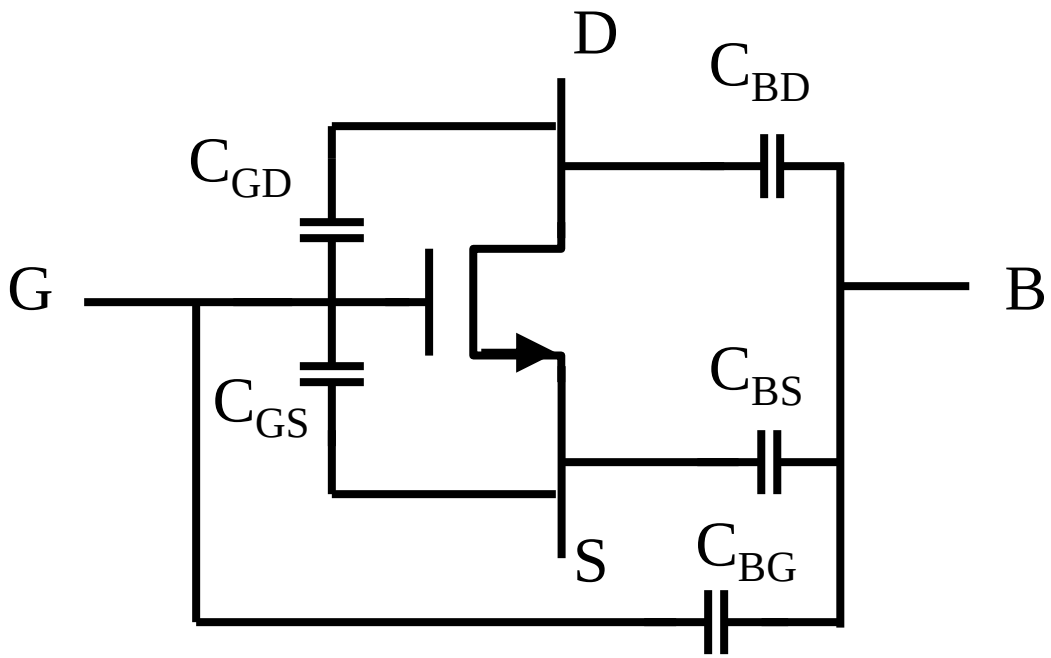


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

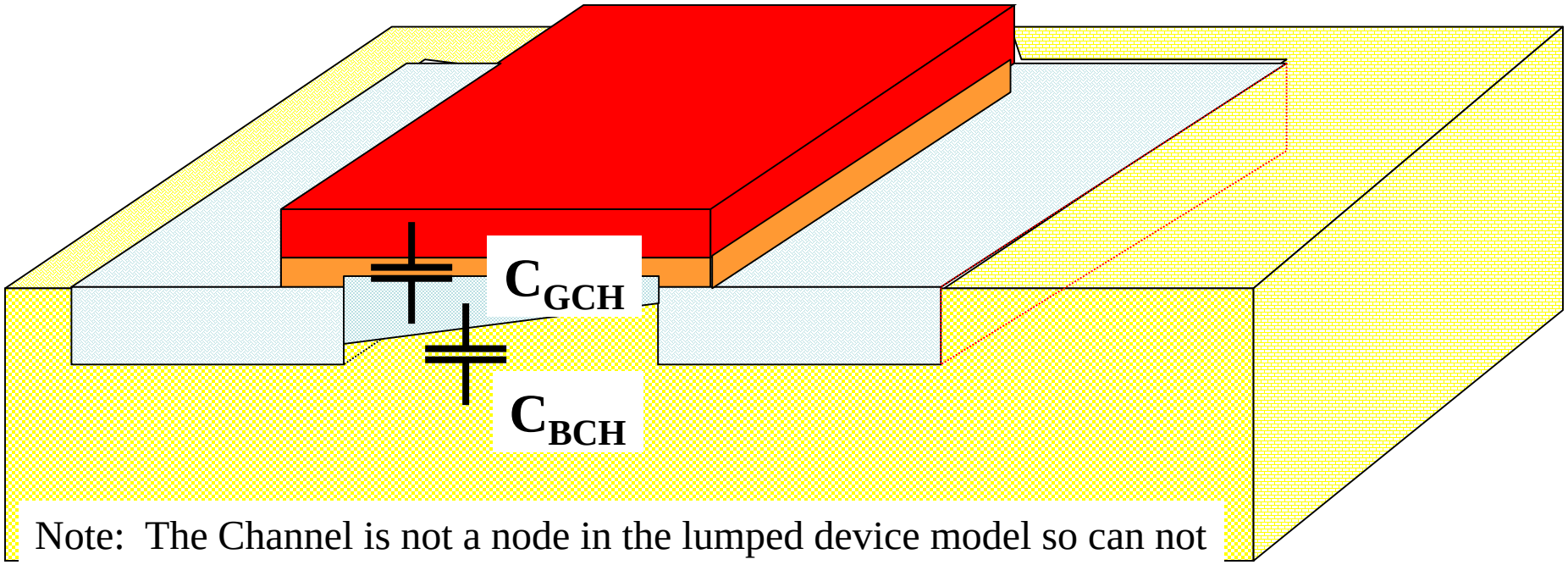
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$		
C_{GD}	$CoxWL_D$		
C_{BG}	CoxWL (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$		
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$		

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



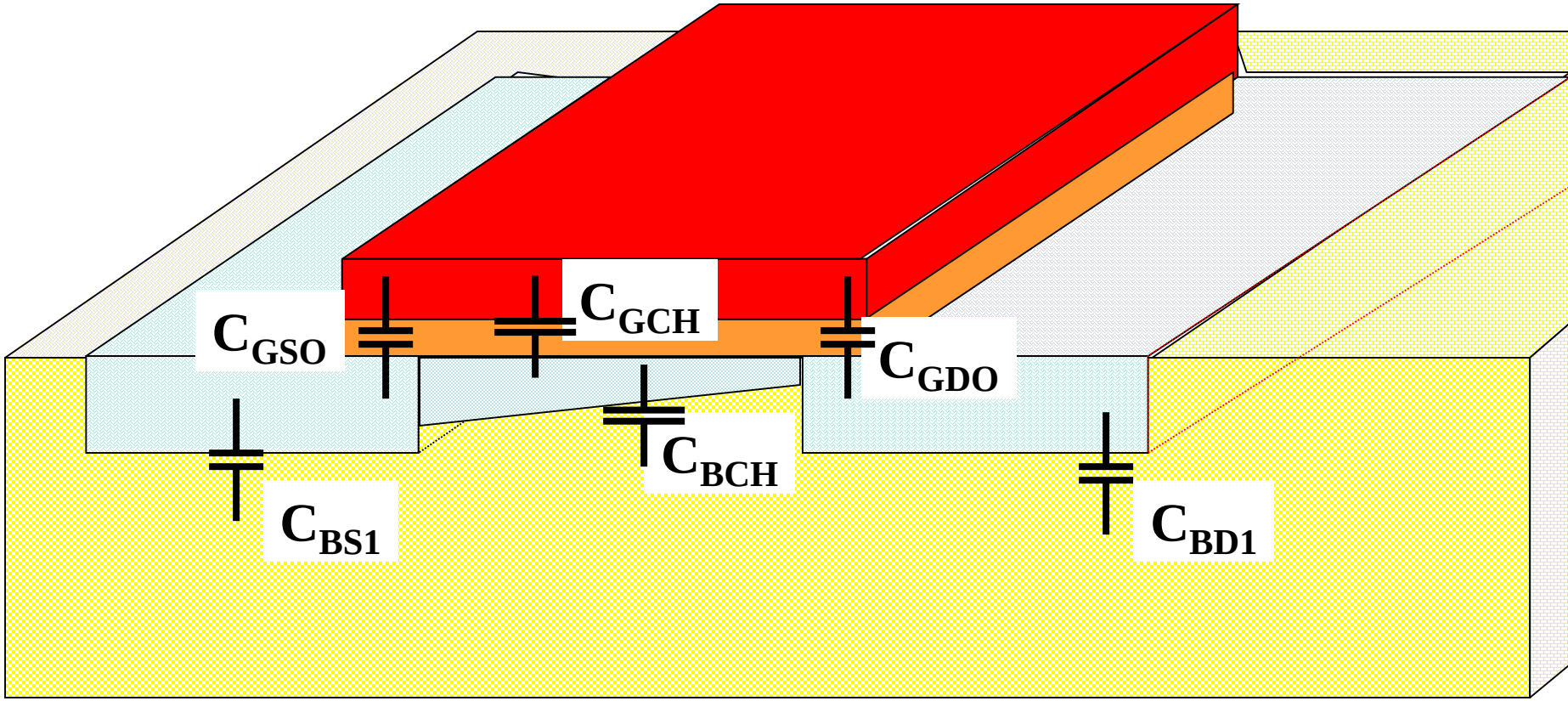
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

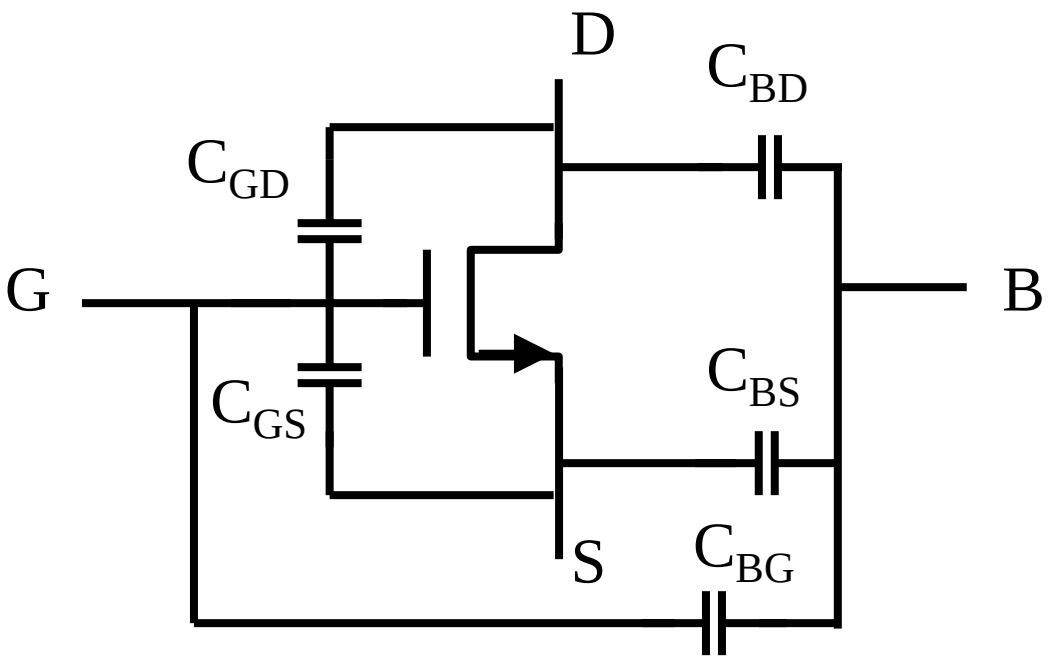


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH}, C_{BCH}

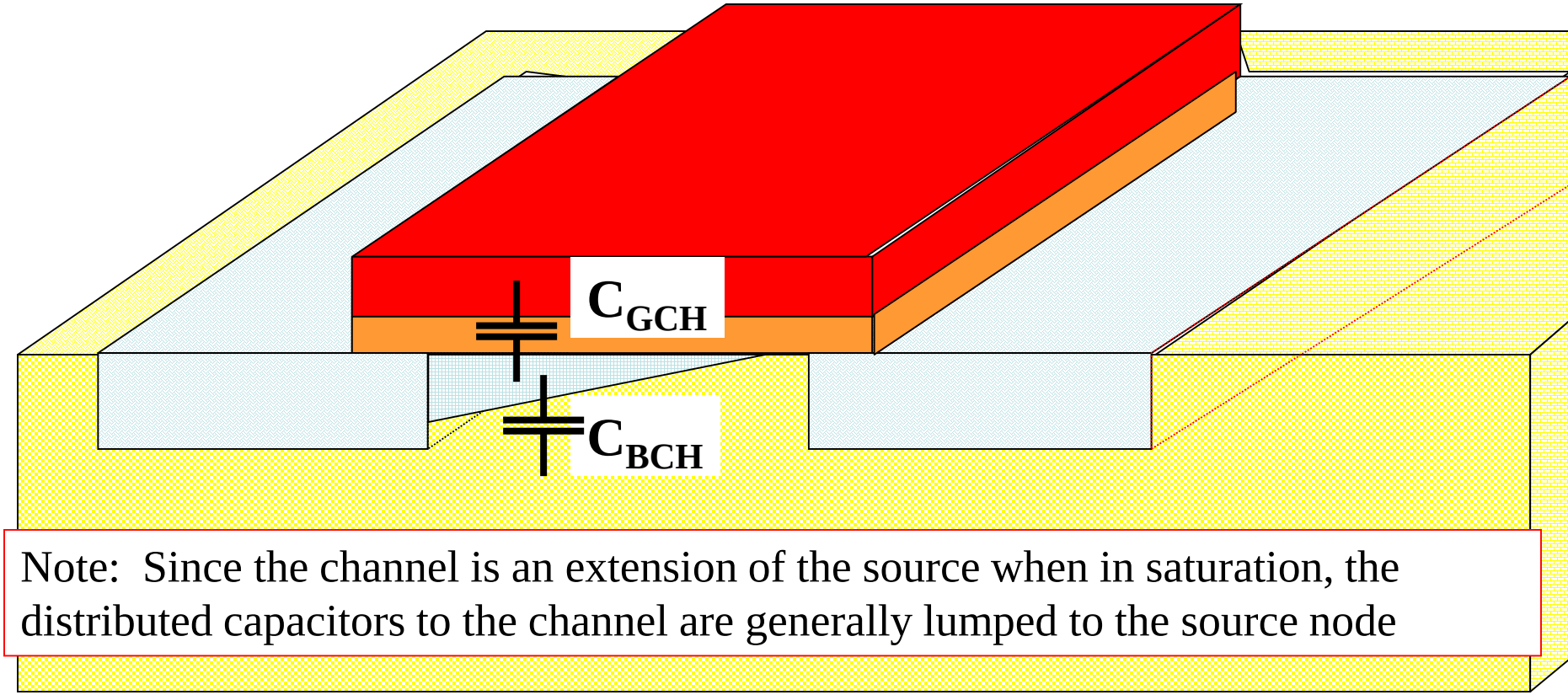
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	
C_{GD}	$CoxWL_D$	$CoxWL_D$	
C_{BG}	CoxWL (or less)	0	
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

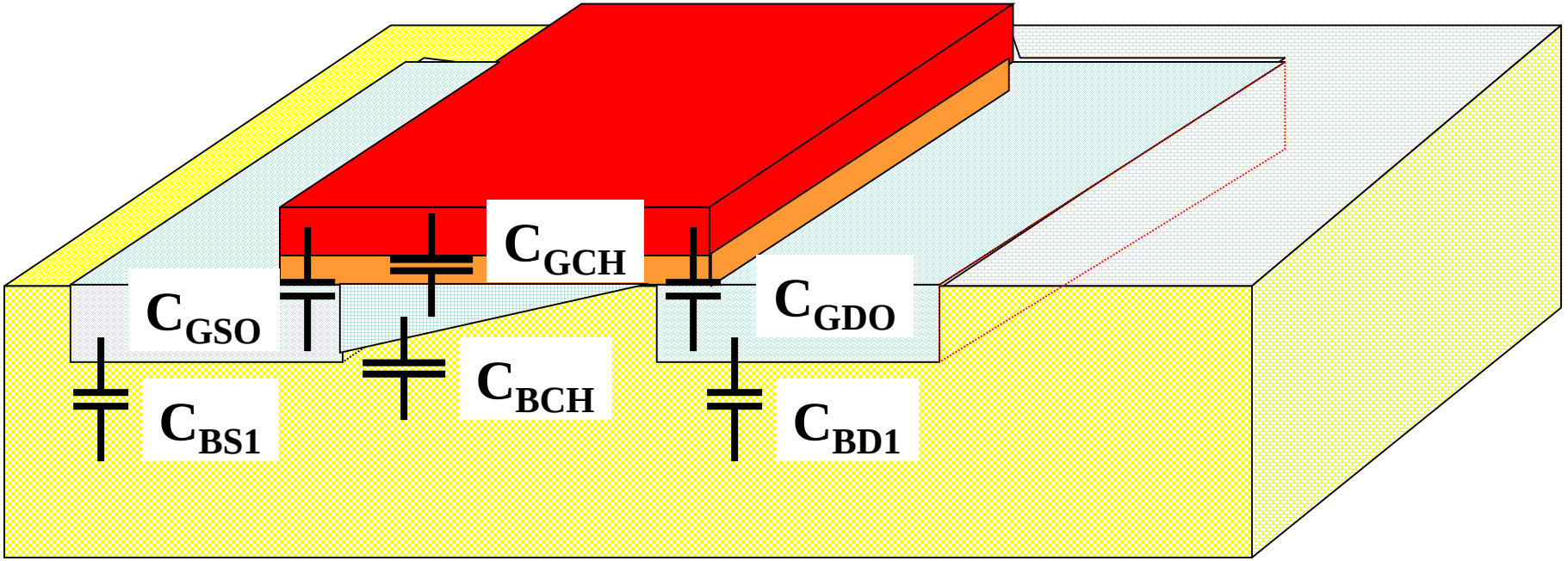


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation



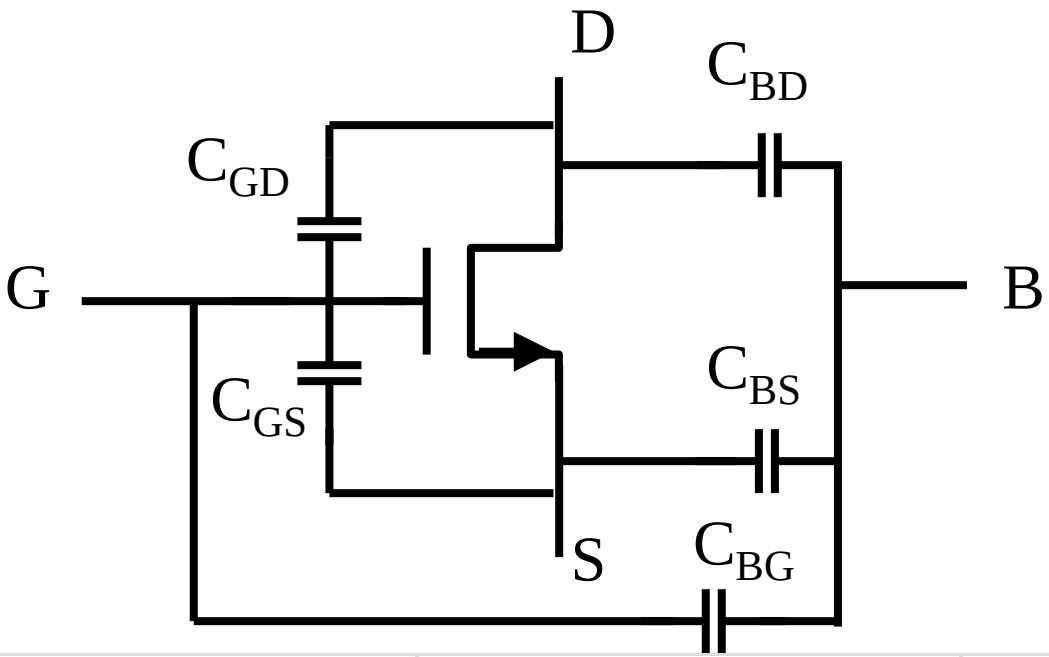
Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Saturation Capacitors: C_{GCH} , C_{BCH}

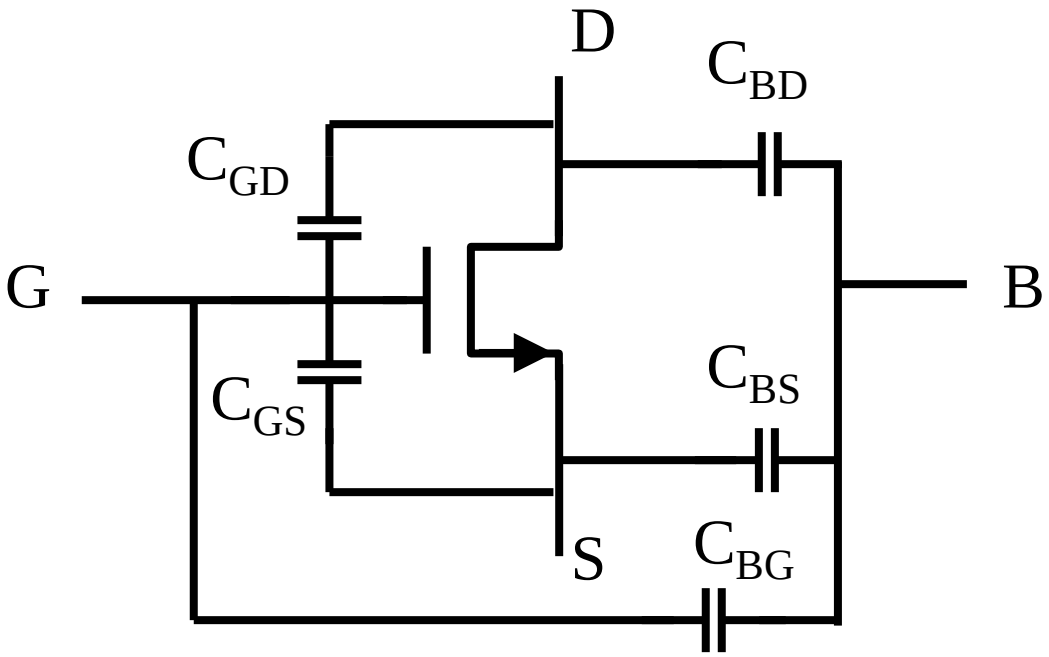
- 2/3 $C_{OX}WL$ is often attributed to C_{GCH} to account for LD and saturation
- This approximation is reasonable for minimum-length devices but not so good for longer devices

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

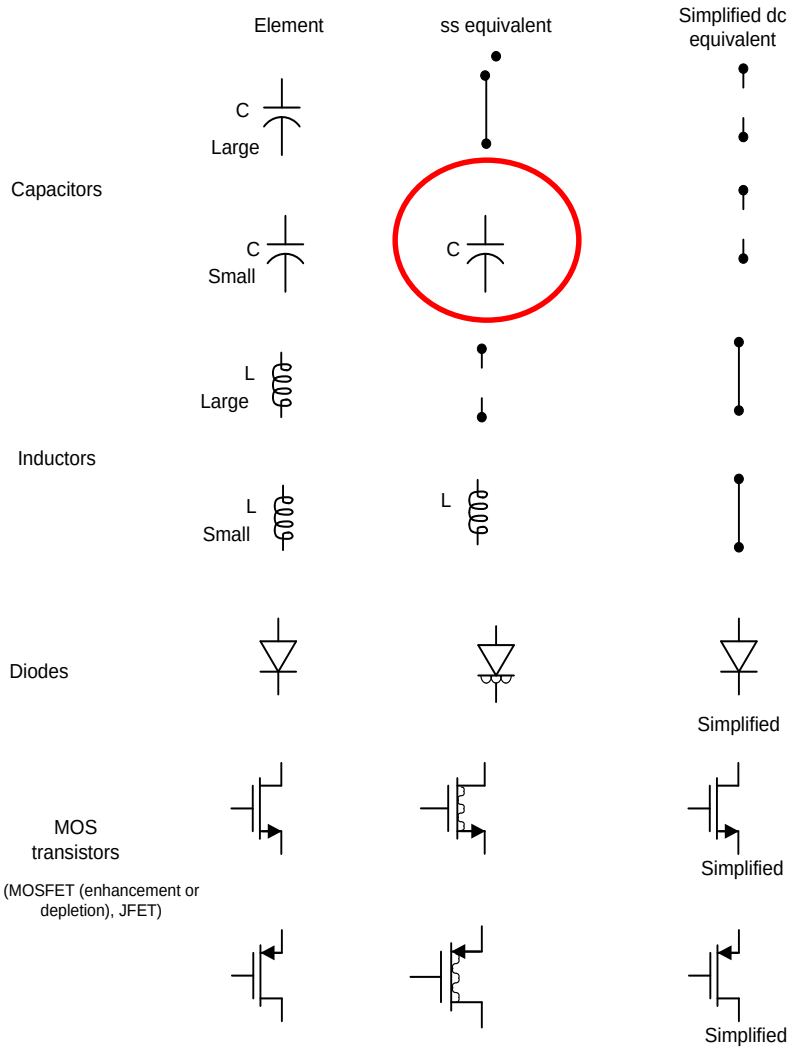
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Recall:

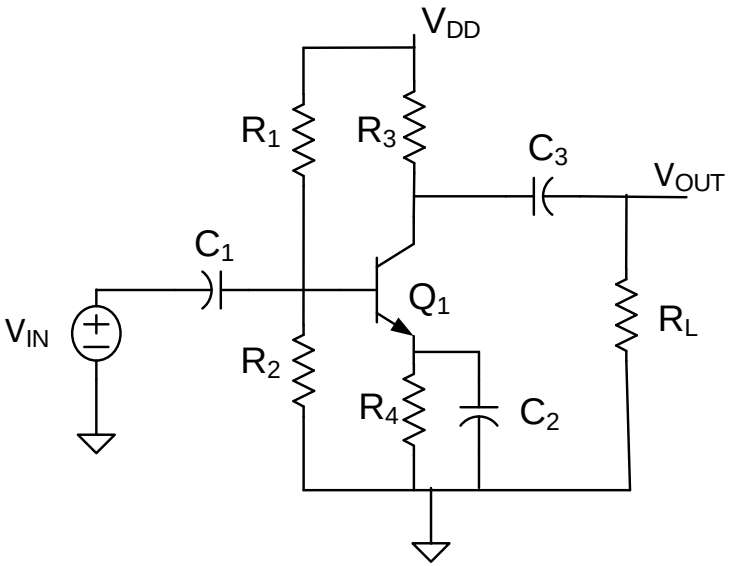
Small-signal and simplified dc equivalent elements



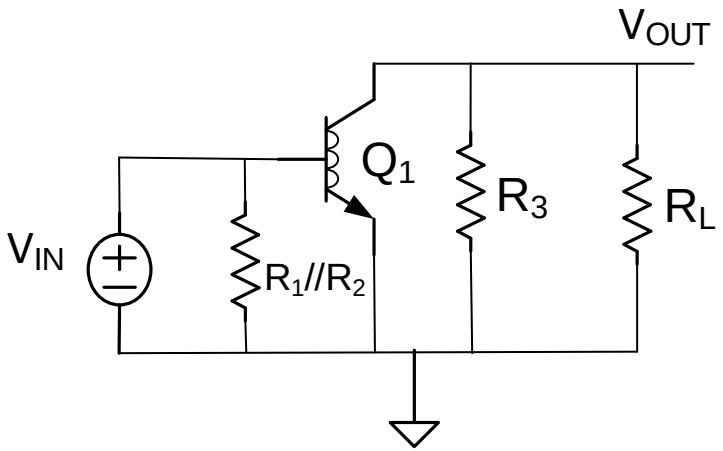
Have not yet considered situations where the small capacitor is relevant in small-signal analysis

Amplifiers with Small Capacitors

Recall:



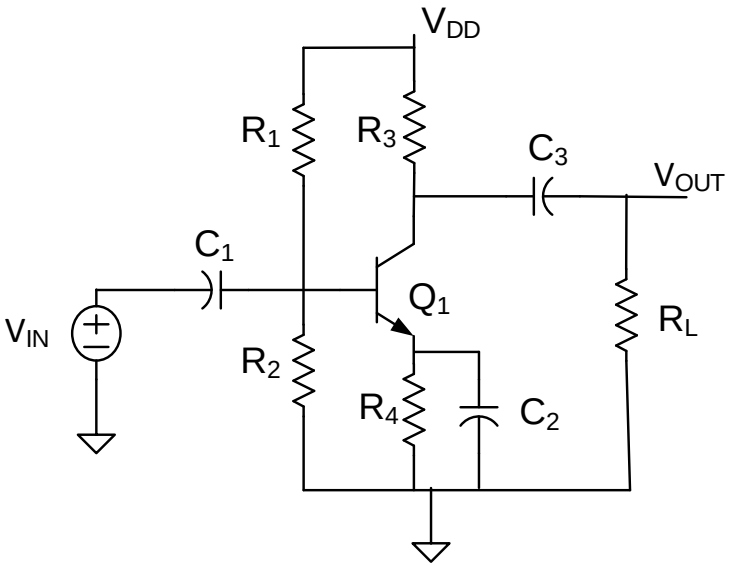
If capacitors are large

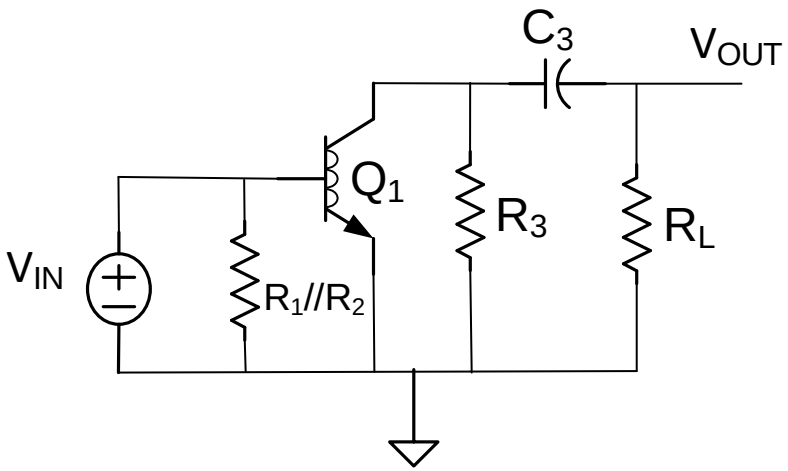


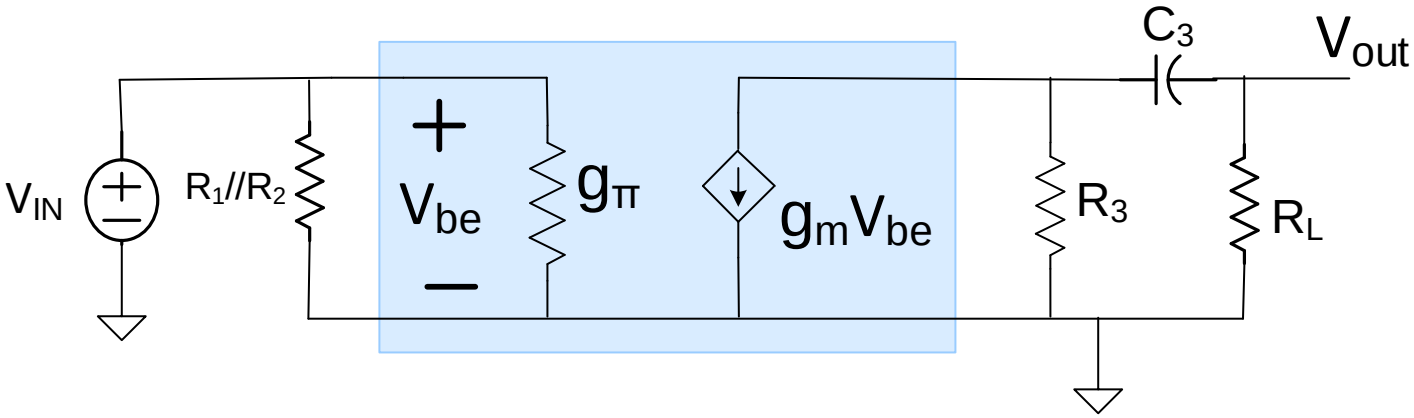
$$A_V = -g_{m1} \bullet R_3 \,//\, R_L$$

Amplifiers with Small Capacitors

What if C_1 and C_2 large but C_3 not large?:

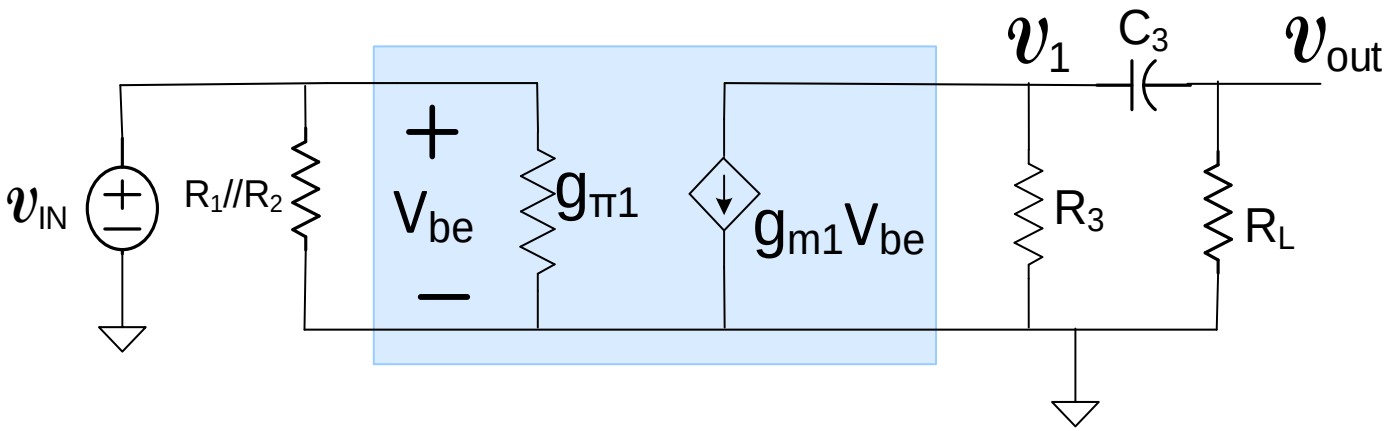






Amplifiers with Small Capacitors

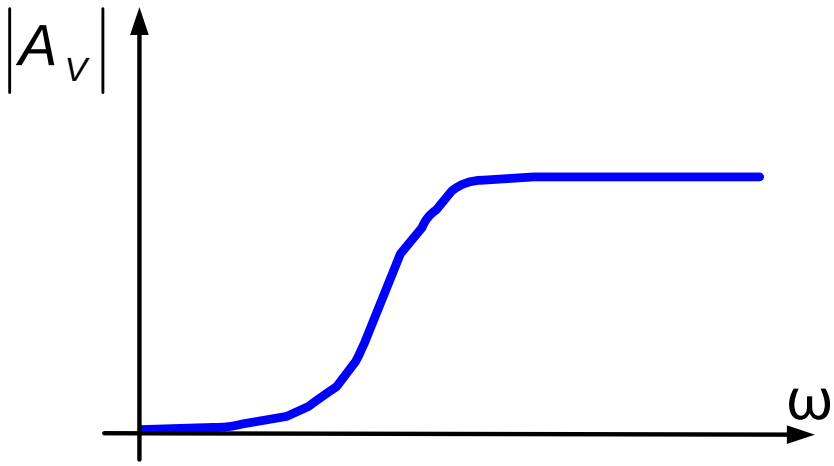
What if C_1 and C_2 large but C_3 not large?:



From KCL:

$$\left.\begin{aligned} v_{OUT}\left(sC_3+G_L\right) &= v_1 sC_3 \\ v_1\left(sC_3+G_3\right)+g_{m1}v_{IN} &= v_{OUT}sC_3 \end{aligned}\right\}$$

Serves as a first-order high-pass filter



Solving:

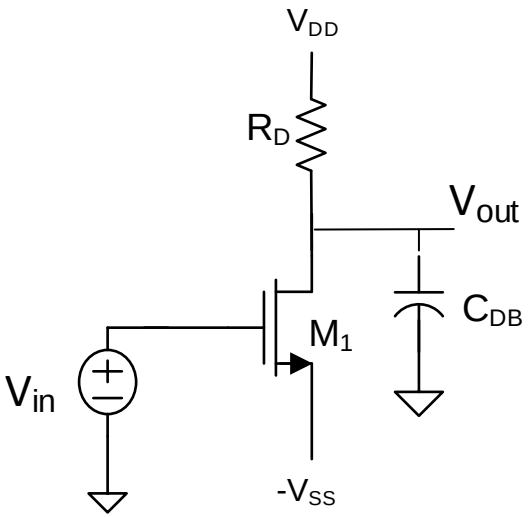
$$\frac{v_{OUT}}{v_{IN}} = -\frac{-sC_3 g_{m1}}{sC_3\left(G_L+G_3\right)+G_3G_L}$$

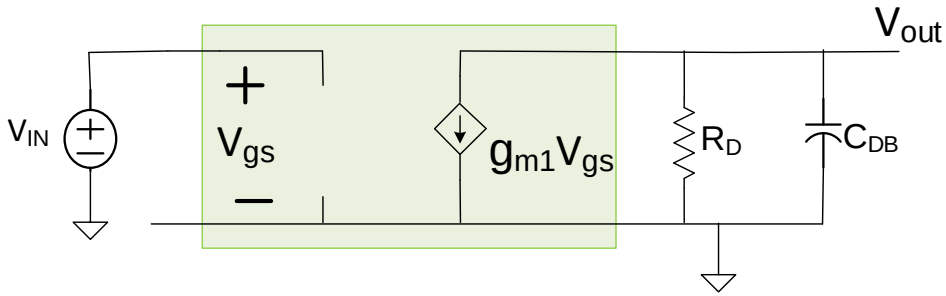
Equivalently:

$$\frac{v_{OUT}}{v_{IN}} = -\frac{g_{m1}sC_3R_3R_L}{sC_3\left(R_L+R_3\right)+1}$$

Amplifiers with Small Capacitors

Consider parasitic C_{DB}





By KCL:

$$v_{OUT}\left(sC_{DB}+G_D\right)=-g_{m1}v_{IN}$$

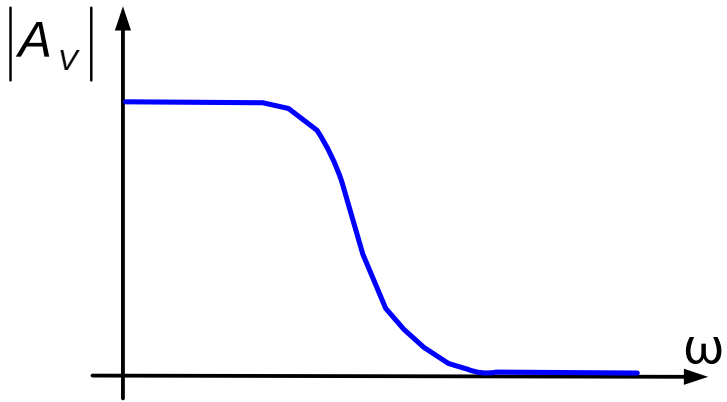
Causes gain to decrease at high frequencies

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}}{sC_{DB}+G_D}$$

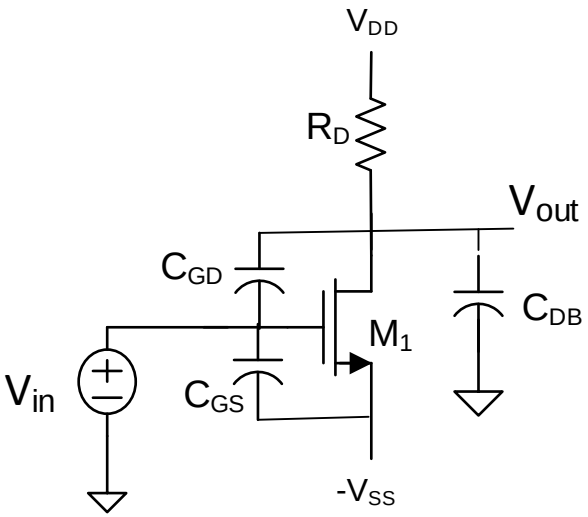
Equivalently:

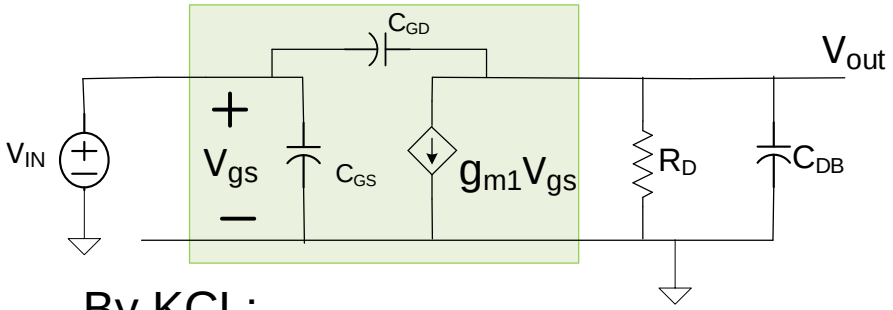
$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}R_D}{sC_{DB}R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}





By KCL:

$$v_{OUT}\left(s\left[C_{DB}+C_{GD}\right]+G_D\right)=-g_{m1}v_{IN}+sC_{GD}v_{IN}$$

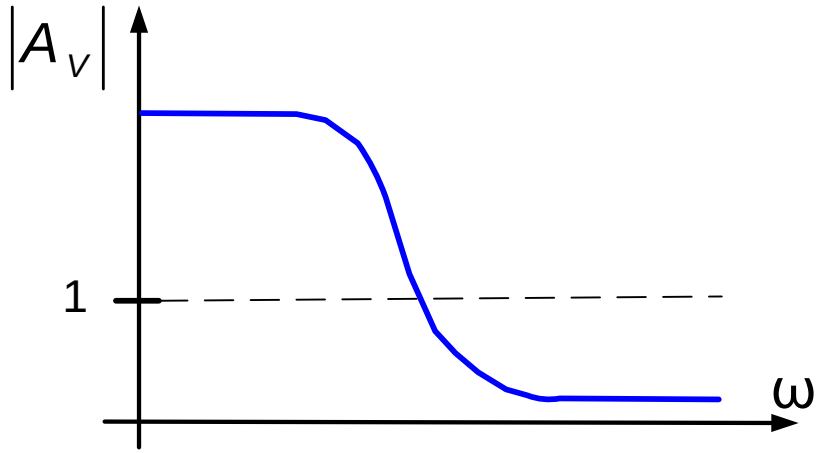
Causes gain to decrease at high frequencies
Has one LHP pole and one RHP zero

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}+sC_{GD}}{s\left[C_{DB}+C_{GD}\right]+G_D}$$

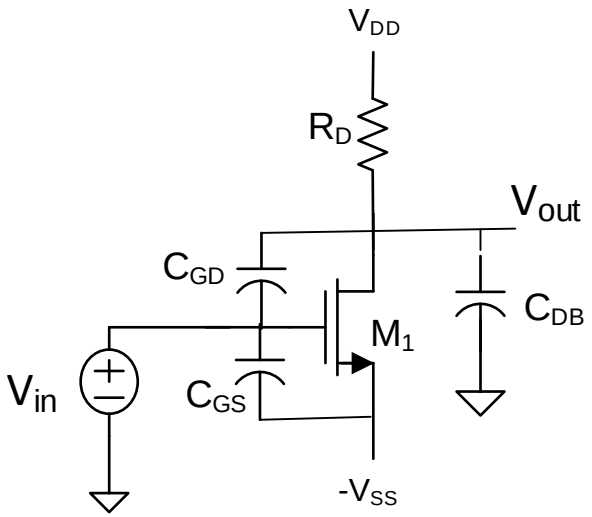
Equivalently:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-R_D\left(g_{m1}-sC_{GD}\right)}{s\left[C_{DB}+C_{GD}\right]R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}



Device parasitics problematic at high frequencies

C_{DB}, C_{GD} and C_{GS} effects can be significant

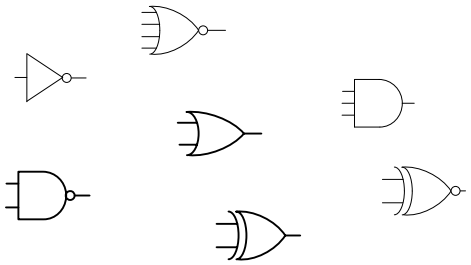
Value of parasitic capacitances strongly dependent upon layout

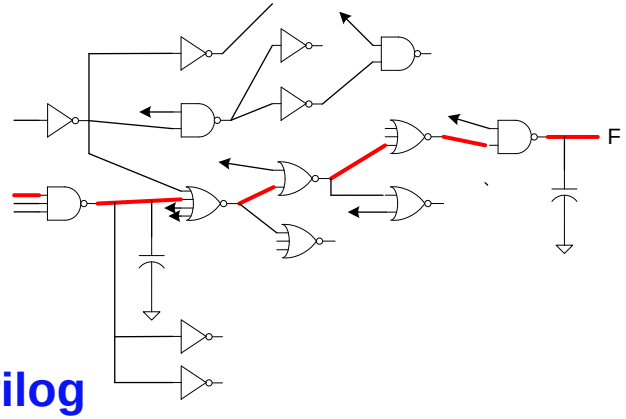
Device parasitics usually not a problem at audio frequencies

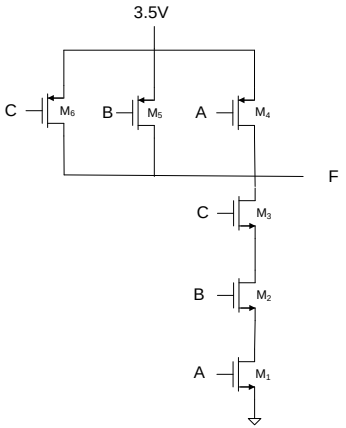
Causes gain to decrease at high frequencies:
has one high frequency LHP pole and one high frequency RHP zero.

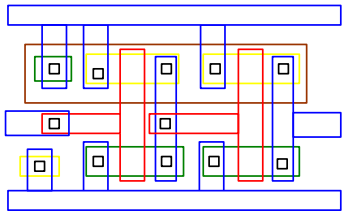
Digital Circuit Design

Most of the remainder of the course will be devoted to digital circuit design







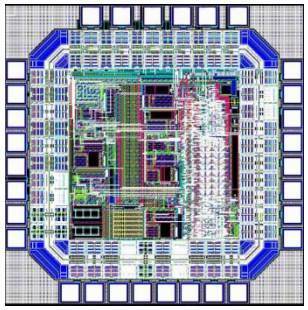


Verilog

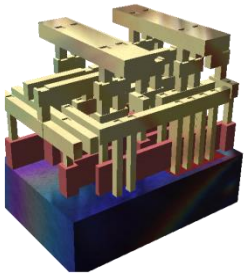
```
module gates (input logic [3:0] a,b,
              output logic [3:0] y1,y2,y3,y4,y5);
  assign y1 = a&b;  //AND
  assign y2 = a | b;  //OR
  assign y3 = a ^ b;  //XOR
  assign y4 = ~(a & b);  //NAND
  assign y5 = ~( a | b);  //NOR
endmodule
```

VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity gates is
   port(a,b: in STD_LOGIC_VECTOR(3 dowto 0);
        y1,y2,y3,y4,y5:out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture synth of gates is
begin

y1 <= a and b;
y2 <= a or b;
y3 <= a xor b;
y4 <= a nand b;
y5 <= a nor b;
end;
```



A rendering of a small standard cell with three metal layers (dielectric has been removed). The sand-colored structures are metal interconnect, with the vertical pillars being contacts, typically plugs of tungsten. The reddish structures are polysilicon gates, and the solid at the bottom is the crystalline silicon bulk

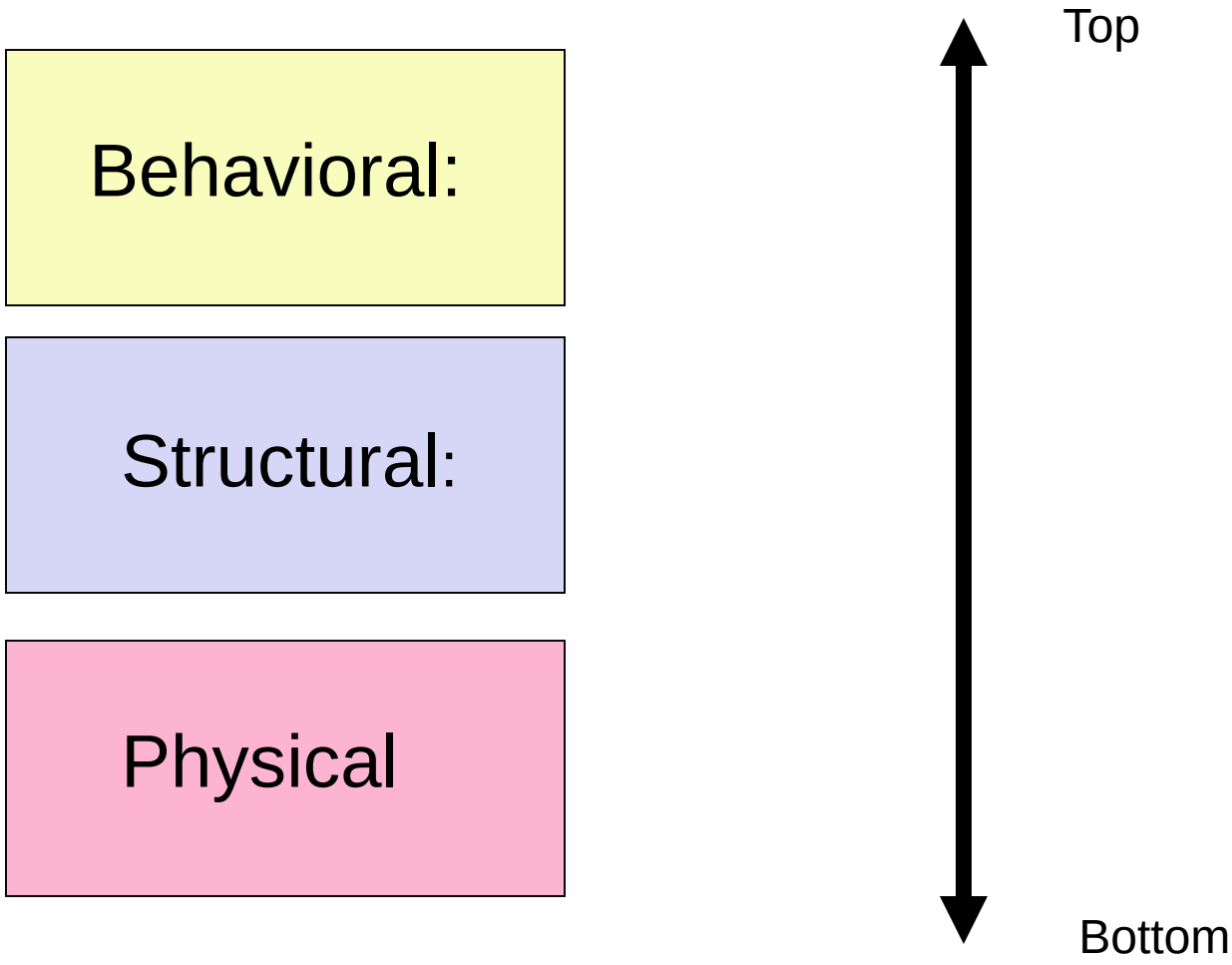


Standard Cell Library

Digital Circuit Design

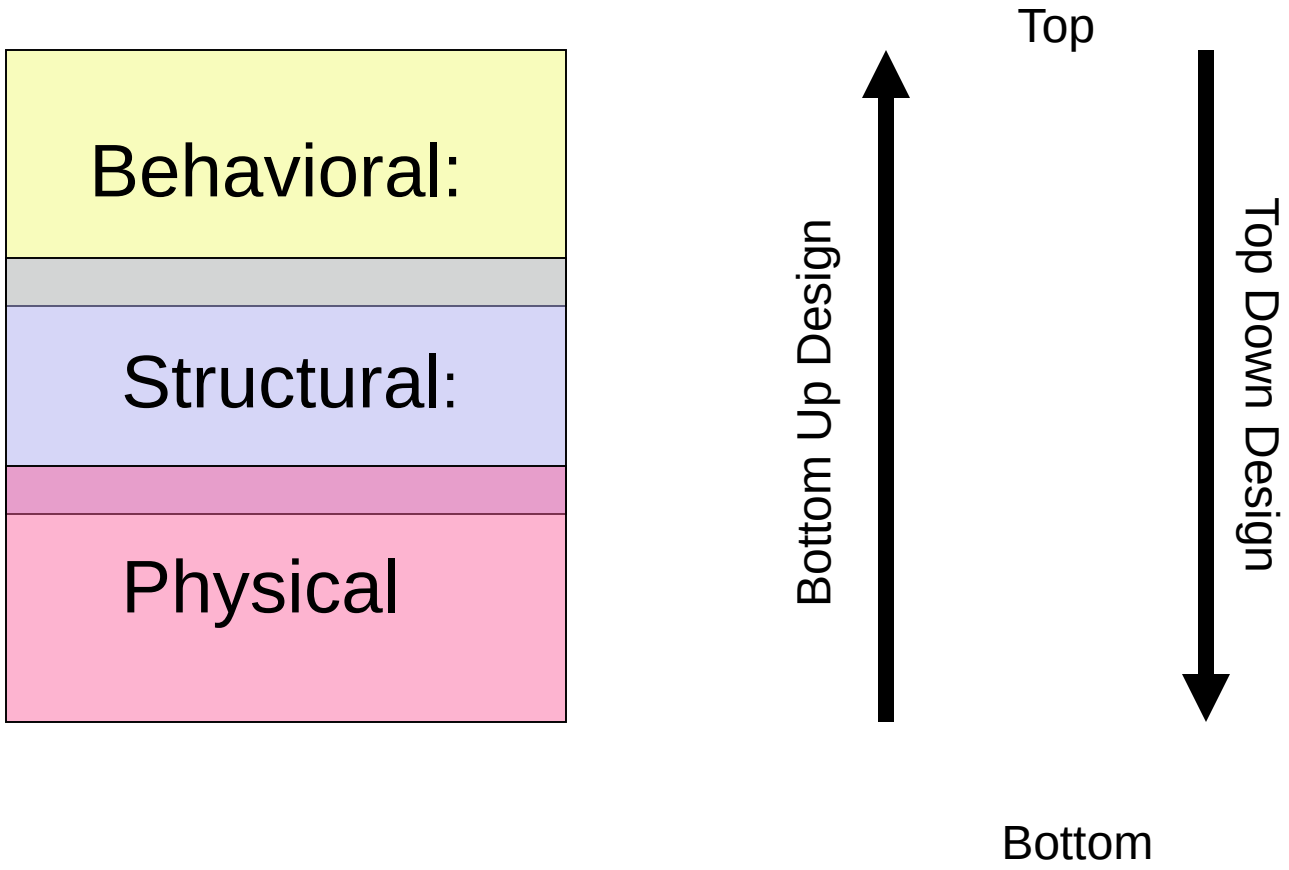
- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

Hierarchical Digital Design Domains:

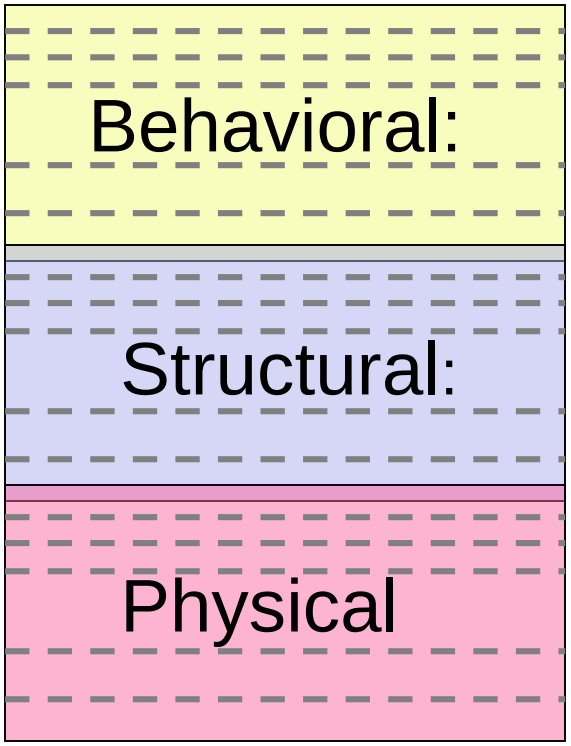


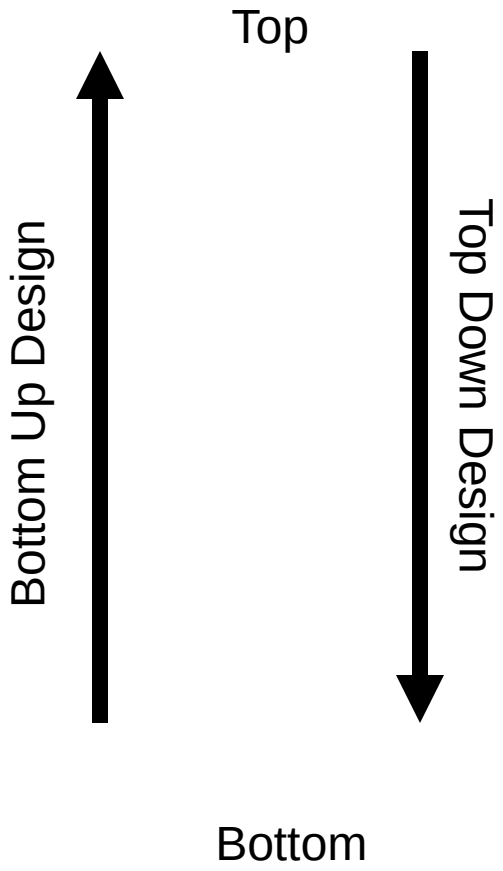
Multiple Levels of Abstraction

Hierarchical Digital Design Domains:



Hierarchical Digital Design Domains:





Multiple Sublevels in Each Major Level

All Design Steps may not Fit Naturally in this Description

Hierarchical Digital Design Domains:

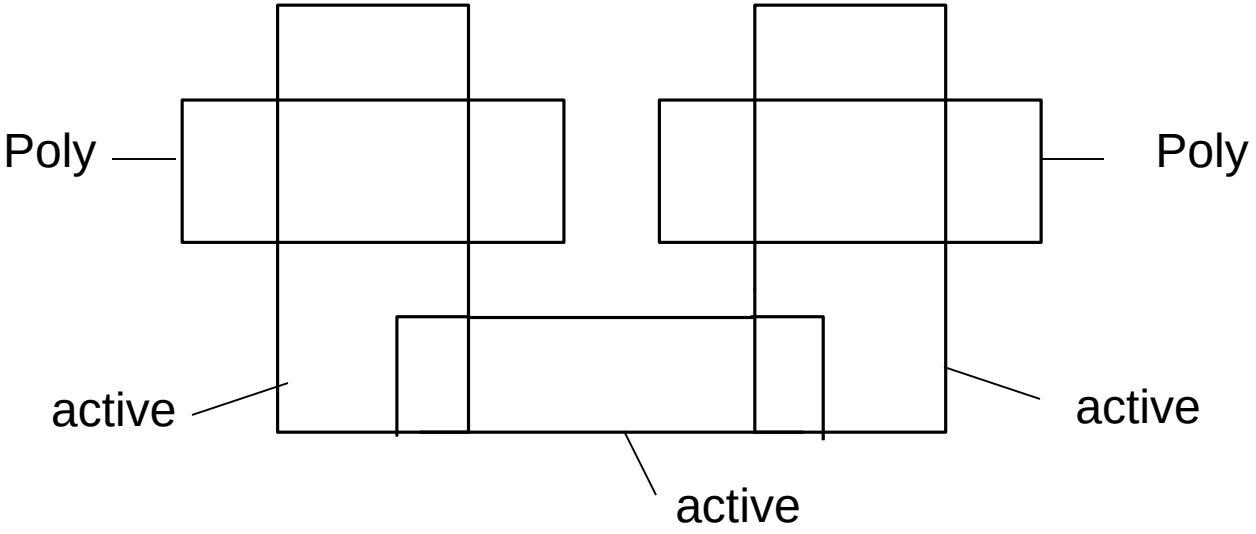
Behavioral : Describes what a system does or what it should do

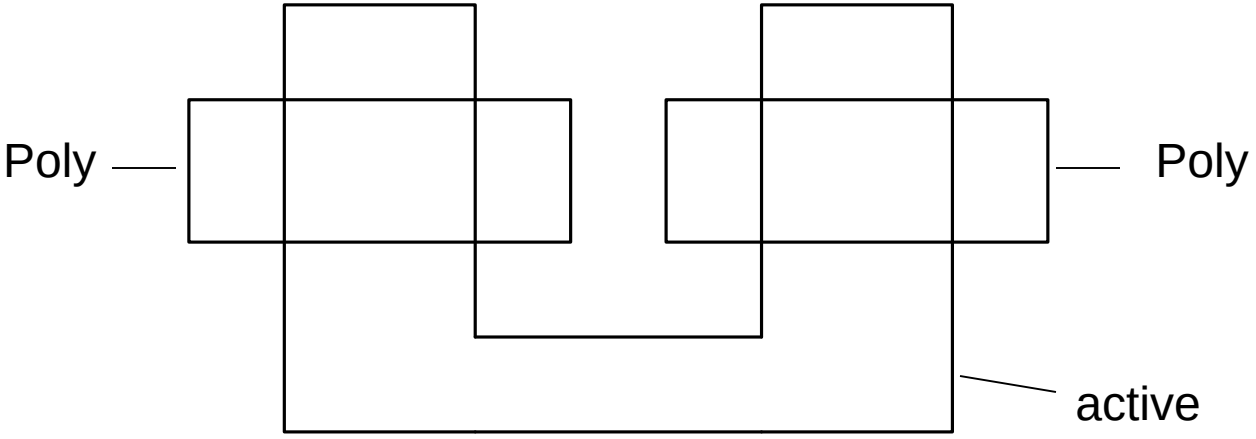
Structural : Identifies constituent blocks and describes how these blocks are interconnected and how they interact

Physical : Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

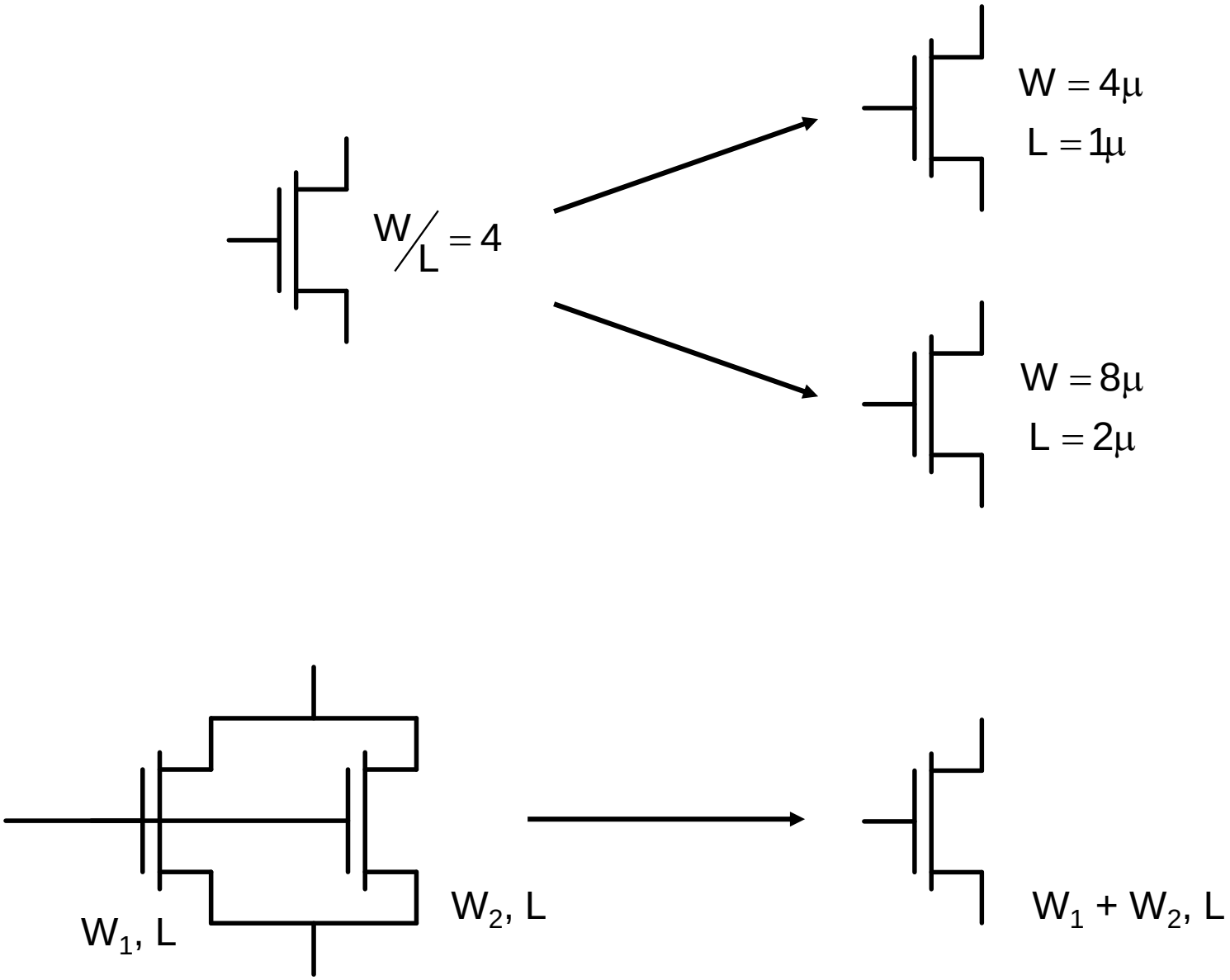
Multiple representations often exist at any level or sublevel

Example: Two distinct representations at the physical level (polygon sublevel)

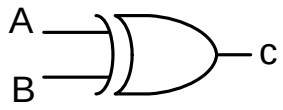




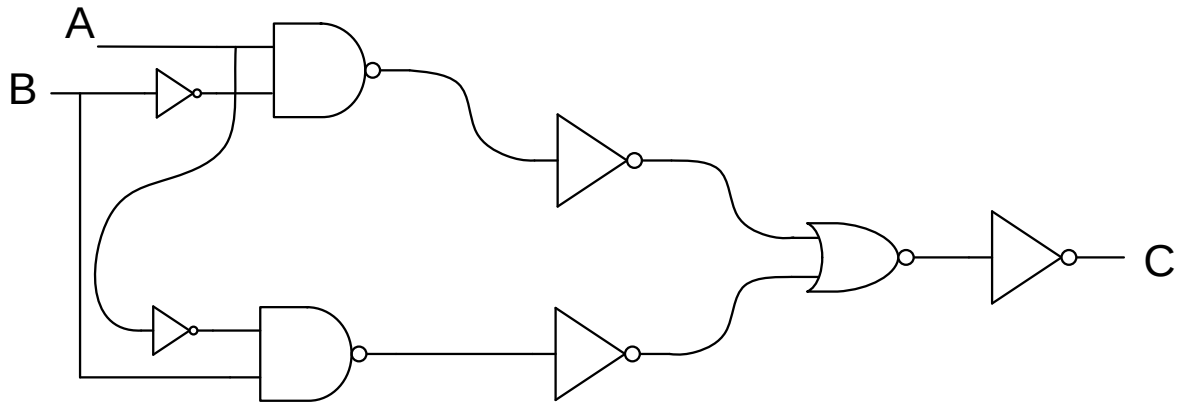
Example: Two distinct representations at physical level (schematic sublevel)

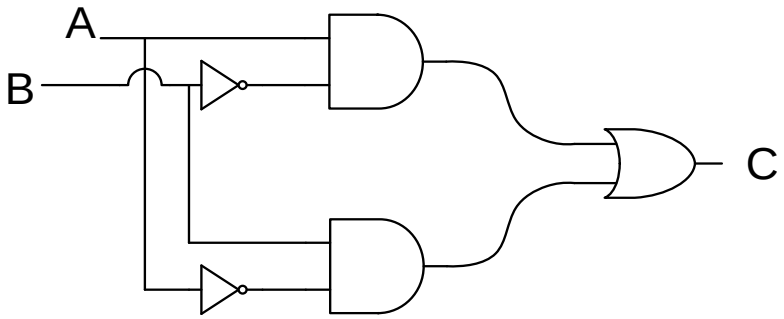


Example: Two distinct representations at the structural/behavioral level (gate sublevel)



$$C = A \oplus B$$





In each domain, multiple levels of abstraction are generally used.

Consider Physical Domain

– Consider lowest level to highest

0 - placement of diffusions, thin oxide regions, field oxide, ect. on a substrate.

1 - polygons identify all mask information (not unique)

2 - transistors (not unique)

3 - gate level (not unique)

4 - cell level Adders, Flip Flop, MUTs,…

Information Type

PG data
G.D.F
Netlist
HDL Description

Structural Level:

- DSP
- Blocks (Adders, Memory, Registers, etc.
- Gates
- Transistor

Information Type

HDL

Netlists

Behavior Level (top down):

- Application
- Programs
- Subroutines
- Boolean Expressions

Information Type

High-Level Language
HDL

Representation of Digital Systems

Standard Approach to Digital Circuit Design

8 – level representation

1. Behavioral Description
   - Technology independent
2. RTL Description (Register Transfer Level)

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis

   Generally use a standard call library for synthesis

(sublevels 6-8 not shown on this slide)

Frontend design

Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description
   - Technology independent
2. RTL Description

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer

5. Logic Synthesis

   Generally use a standard call library for synthesis

Backend design

6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   - DRC
   - Back Annotation
8. Post Layout simulation

   May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles

Logic Optimization

What is optimized (or minimized) ?

- Number of Gates
- Number or Levels of Logic
- Speed
- Delay
- Power Dissipation
- Area
- Cost
- Peak Current
- • •

Depends Upon What User Is Interested In

Standard Cell Library

- Set of primitive building blocks that have been pre-characterized for dc and high frequency performance
- Generally includes basic multiple-input gates and flip flops
- P-cells often included
- Can include higher-level blocks
  - Adders, multipliers, shift registers,counters,…
- Cell library often augmented by specific needs of a group or customer

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

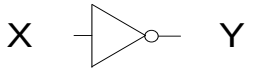
Logic Circuit Block Design

Many different logic design styles

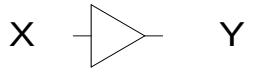
- Static Logic Gates
- Complex Logic Gates
- Pseudo NMOS
- Pass Transistor Logic
- Dynamic Logic Gates
  - Domino Logic
  - Zipper Logic
  - Output Prediction Logic

Various logic design styles often combined in the implementation of one logic block

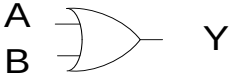
The basic logic gates



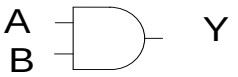
$$Y = \overline{X}$$



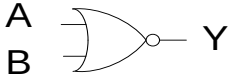
$$Y = X$$



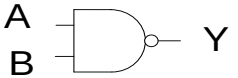
$$Y = A + B$$



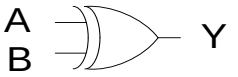
$$Y = A \bullet B$$



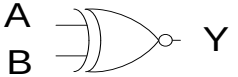
$$Y = \overline{A + B}$$



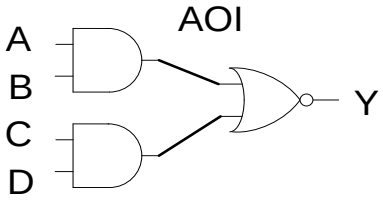
$$Y = \overline{A \bullet B}$$



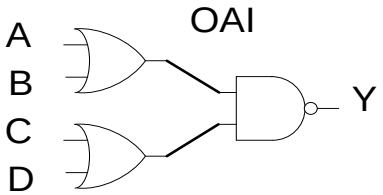
$$Y = A \oplus B$$



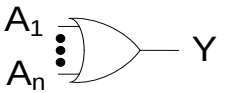
$$Y = \overline{A \oplus B}$$



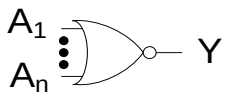
$$Y = \overline{A \bullet B + C \bullet D}$$



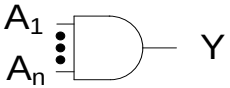
$$Y = \overline{(A + B) \bullet (C + D)}$$



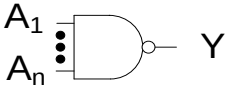
$$Y = A_1 + A_2 + \ldots A_n$$



$$Y = \overline{A_1 + A_2 + \ldots A_n}$$

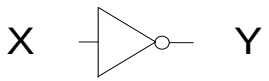


$$Y = A_1 \bullet A_2 \bullet \ldots A_n$$

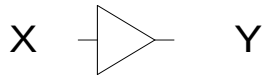


$$Y = \overline{A_1 \bullet A_2 \bullet \ldots A_n}$$

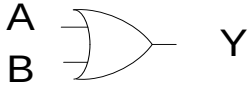
The basic logic gates



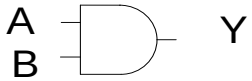
$$Y = \overline{X}$$



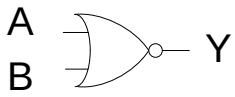
$$Y = X$$



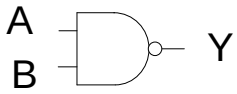
$$Y = A + B$$



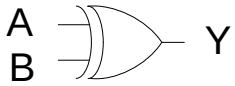
$$Y = A \bullet B$$



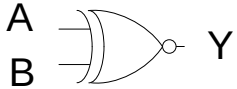
$$Y = \overline{A + B}$$



$$Y = \overline{A \bullet B}$$



$$Y = A \oplus B$$



$$Y = \overline{A \oplus B}$$

Question: How many basic one and two input gates exist and how many of these are useful?

The basic logic gates

The set of NOR gates is complete

Any combinational logic function can be realized with only multiple-input NOR gates

The set of NAND gates is complete

Any combinational logic function can be realized with only multiple-input NOR gates

Performance of the BASIC gates is critical!

The basic logic gates

A gate logic family can be formed based upon a specific design style for implementing logic functions

Many different gate logic family types exist

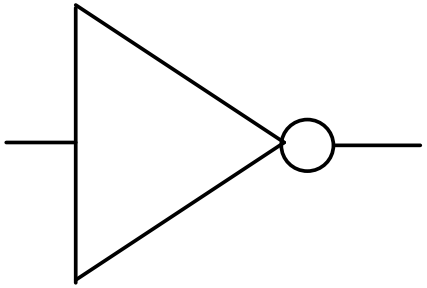
NMOS, PMOS, CMOS, TTL, ECL, RTL, DCTL,…

Substantial differences in performance from one family type to another

Power, Area, Noise Margins, ….

The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.



What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

What restrictions are there on the designer for building Boolean circuits?

- None !!!!
- It must “work” as expected
- Designer is Master of the silicon !

Desirable and/or Required Logic Family Characteristics

What are the desired characteristics of a logic family?

Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements

Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools
12. Characteristics do not degrade too much with temperature
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools
12. Characteristics do not degrade too much with temperature
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

Desirable and/or Required Logic Family Characteristics

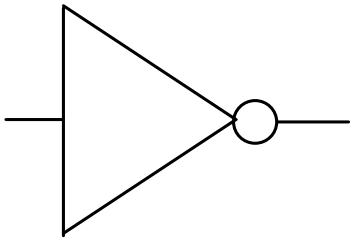
Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

What properties of an inverter are necessary for it to be useful for building a logic family

What are the logic levels for a given inverter of for a given logic family?

What are the logic levels for a given inverter of for a given logic family?



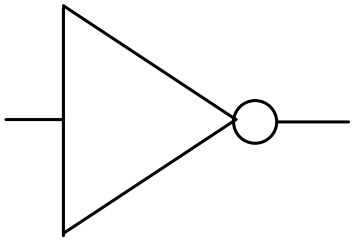
V_H=?

V_L=?

Can we legislate them ?

- Some authors choose to simply define a value for them
- Simple and straightforward approach
- **But what if the circuit does not interpret them the same way they are defined !!**

What are the logic levels for a given inverter of for a given logic family?



V_H=? V_L=?

Can we legislate them ?

In 1897 the Indiana House of Representatives unanimously passed a measure redefining the area of a circle and the value of pi. (House Bill no. 246, introduced by Rep. Taylor I. Record.) The bill died in the state Senate.

End of Lecture 36