EE330 Homework 7 Spring2018 TA: George Alphonse

Problem 1

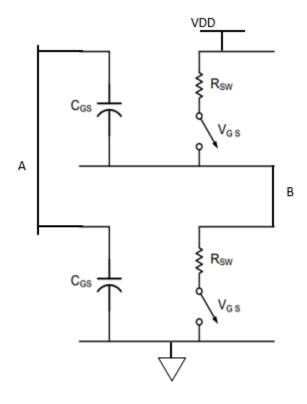
For the circuit on the left, the anode voltage can't exceed the cathode voltage of 15 V, so diode is off.

$$I_1 = \frac{7}{2k + 2k} = 1.75 \, mA$$

For the circuit on the right, the resistors act as a voltage divider so $V_D = 15*(4/6) = 10 \text{ V}$, so diode is on.

$$I_1 = \frac{9.6}{4k} = \frac{2.40 \ mA}{4k}$$

Problem 2

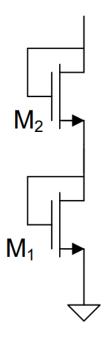


$$R_{sqn} = \frac{1}{\frac{\mu C_{ox}W}{L}(V_{GS} - V_T)} = \frac{1}{\frac{350\mu A}{V^2} * \frac{5\mu}{1\mu} * (3.5 - 0.5)} = \frac{190\Omega}{V^2}$$

$$R_{sqp} = \frac{1}{\frac{70\mu A}{V^2} * \frac{20\mu}{2\mu} * (3.5 - 0.5)} = 476\Omega$$

$$C_{GSN} = C_{OX}WL = (2.5fFu^{-2})(5\mu * 1\mu) =$$
12.5 fF

$$C_{GSP} = (2.5 fF \mu^{-2})(20 \mu * 2 \mu) = \frac{100 fF}{2}$$



Assume both transistors are in saturation

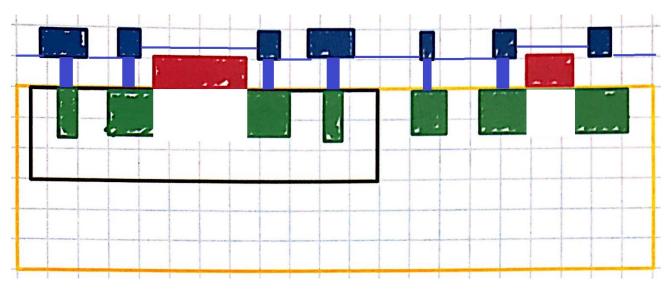
$$u_{n}C_{OX} * \frac{W_{1}}{2L_{1}} * (V_{out} - V_{SS} - V_{T})^{2} = u_{n}C_{OX} * \frac{W_{2}}{2L_{2}} * (V_{DD} - V_{out} - V_{T})^{2}$$

$$u_{n}C_{OX} * \frac{W_{1}}{2L_{1}} * (1V - 0V - 0.5V)^{2} = u_{n}C_{OX} * \frac{W_{2}}{2L_{2}} * (2.5V - 1V - 0.5V)^{2}$$

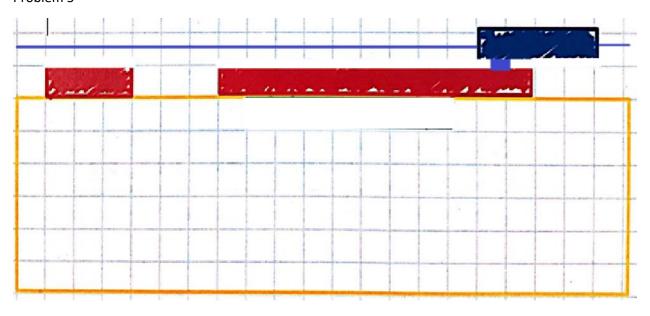
$$\frac{W_{1}}{L_{1}} * (1V - 0.5V)^{2} = \frac{W_{2}}{L_{2}} * (2.5V - 1V - 0.5V)^{2}$$

$$\frac{W_{2}}{\frac{U_{1}}{L_{1}}} = \frac{(1V - 0.5V)^{2}}{(2.5V - 1V - 0.5V)^{2}} = 0.25$$

$$If \frac{W_1}{L_1} = \frac{9.6\mu}{0.6\mu} = 16 \ then \frac{W_2}{L_2} = \frac{2.4\mu}{0.6\mu} = 4$$



Problem 5



Problem 6

Same as problem 5

A.)

$$\alpha = \frac{I_C}{I_E} = \frac{1.00mA}{1.0250mA} = 0.9756$$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.9756}{1 - 0.9756} = \frac{40}{1}$$

B.)

$$\alpha = \frac{1.00mA * 1.005}{1.0250 * (1 - .005)} = 0.985$$

$$\beta = \frac{0.985}{1 - 0.985} = 67.56$$

$$Error = \frac{67.56 - 40}{40} = 0.689 = \frac{68.9\%}{6}$$

Problem 8

$$I_B = \frac{I_C}{\beta} = \frac{1.00mA}{40} = 25\mu A$$

$$\beta = \frac{I_C}{I_B} = \frac{1.00mA * 1.005}{25\mu A * 0.995} = 40.402$$

$$Error = \frac{40.402 - 40}{40} = 0.01005 = \frac{1.005\%}{1.005\%}$$

$$I_C = \frac{8V - 5V}{3k\Omega} = 1.00mA$$

$$V_t = \left(8.617 * 10^{-5} \frac{eV}{K}\right) (300K) = 25.85 mV$$

$$I_C = J_s A_E e^{\frac{V_{BE}}{V_t}} = 10^{-14} * 100 * e^{\frac{V_{BE}}{25.85mV}} \rightarrow V_{BE} = 0.536V$$

B.)

$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} = 10^{-14} * 100 * e^{\frac{0.536V - 10uV}{25.85mV}} = 999.6uA$$

$$V_C = 8V - 3k\Omega * 999.6uA = 5.00118 V$$

$$Change = \frac{5V}{5.00118V} = \frac{0.023\%}{0.023\%}$$

C.)

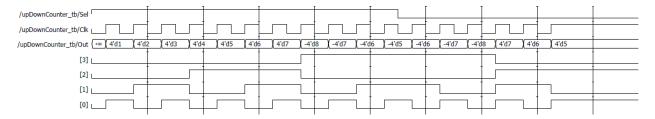
$$V_t = \left(8.617 * 10^{-5} \frac{eV}{K}\right) (301K) = 25.93 mV$$

$$I_C = J_s A_E e^{\frac{V_{BE}}{V_t}} = 10^{-14} * 100 * e^{\frac{V_{BE}}{25.93mV}} \rightarrow V_{BE} = 0.537V$$

D.)

Small changes in V_X and T, result in about 1mV change at the output.

Problem 10 and 11



```
"U:/ee330hw11/upDownCounter2.v (/upDownCounter_tb/my_gate) - Default
  Ln#
         timescale 1ns/1ps
       module upDownCounter2(out, sel, clk);
   3
                  output [3:0] out;
                  input sel, clk;
   5
                  reg [3:0] out;
   6
                  initial
                          out = 0;
                  always @(posedge clk)
                          if (sel) begin
                                  out <= out + 1;
  10
  11
                          end else begin
  12
                                  out <= out - 1;
  13
                          end
  14
        endmodule
  15
```

```
U:/ee330hw11/upDownCounter_tb.v (/upDownCounter_tb) - Default =
  Ln#
           `timescale 1ns/1ps
         pmodule upDownCounter_tb();
                     reg Sel, Clk;
                     wire [3:0] Out;
                     upDownCounter2 my_gate(.sel(Sel), .clk(Clk), .out(Out));
                    initial
                    begin
                              $monitor(Sel, Clk, Out);
Clk = 1'b0; Sel = 1'b1;
   10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
                              Clk = 1'b1; Sel = 1'b1;
                              Clk = 1'b0; Sel = 1'b1;
                              Clk = 1'b1; Sel = 1'b1;
                              Clk = 1'b0; Sel = 1'b1;
                              Clk = 1'b1; Sel = 1'b1;
                              Clk = 1'b0; Sel = 1'b1;
                              Clk = 1'b1; Sel = 1'b1;
                              Clk = 1'b0; Sel = 1'b1;
                              Clk = 1'b1; Sel = 1'b1;
   29
30
31
32
                              Clk = 1'b0; Sel = 1'b1;
                              Clk = 1'b1; Sel = 1'b1;
   33
34
35
                              Clk = 1'b0; Sel = 1'b1;
                              Clk = 1'b1; Sel = 1'b1;
```