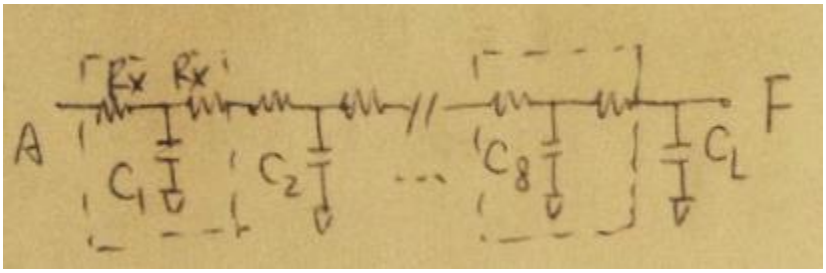
EE330 HW 15 Spring 2018

1)



$R_x = \frac{50}{2} * 20 = 500\ \Omega, C_x = 0.5f * 50 * 2 = 50\ fF$

$t_{pd} = \sum_{i=1}^{8} t_{pd\,i} = \frac{R_x}{2} * C_x + \frac{3R_x}{2} * C_x + \frac{5R_x}{2} * C_x + \cdots + \frac{15R_x}{2} * C_x + \frac{16R_x}{2} * C_L = 1\ ns$

2)

a) $R_x = \frac{\frac{50}{4}}{2} * 20 = 125\ \Omega \rightarrow R_T = \frac{R_x}{2} = 62.5\ \Omega, C_T = 0.5f * \frac{50}{4} * 2 = 12.5\ fF$

b) $t_{pd} = \sum_{i=1}^{4} t_{pd\,i} = \frac{R_x}{2} * C_x + \frac{3R_x}{2} * C_x + \frac{5R_x}{2} * C_x + \frac{7R_x}{2} * C_x + \frac{8R_x}{2} * C_L = 262.5\ ps$

c) Spice Simulation

3)

$\bar{A}B + \bar{B}A = \overline{(\overline{\bar{A}B})(\overline{\bar{B}A})}$

Assuming $\bar{A}\ and\ \bar{B}$ are available, this can be done in 3 2-input NAND gates and 1 NOT gate. So 14 transistors and 3 logic levels.

4)

a) $P = f * C_l * V_{DD}^2 = 10k * 600f * 2^2 = 24\ nW$

b) No change in frequency, load capacitance or supply voltage, so 24 nW.

c)$R_{PU} = \frac{L_p}{\mu_p C_{ox} W_p (V_{DD} - (-V_T))} = 42.86\Omega$

$R_{PD} = \frac{L_n}{\mu_n C_{ox} W_n (V_{DD} - V_T)} = 34.29\Omega$

$t_{HL} = R_{PD} * C_L = 20.57ps, \qquad t_{LH} = R_{PU} * C_L = 25.71ps \rightarrow f_{Max} = \frac{1}{t_{LH}} = 38.89\ GHz$

5)

$E_{HL} = E_{LH} = C_L * V_{DD}^2, \qquad C_L = 0.2 * 0.2 * 8fF = \ 0.32\ fF \rightarrow E_{Total} = 2.56fJ$

$P = \frac{1{,}000{,}000}{2} * E_{HL} * 1.5\ GHz = 960\ mW$

6)

$P = f * C_l * V_{DD}^2 = 300MHz * 25pF * 2^2 = 30mW$

7)

$P = f * C_l * V_{DD}^2 = \frac{800}{2} MHz * (32 * 4)pF * 2^2 = 204.8\ mW$

8)

Using a min sized inverter, we get $t_{LH} = R_{PU} * C_L = 5.71ps \rightarrow f_{Max} = \frac{1}{t_{LH}} = 175\ MHz$. So we can use the min sized inverter and one stage drive to minimize power dissipation and satisfy clock speed

9)

$C_{Ref} = 0.2 * 0.2 * 8fF = \ 0.32\ fF, C_L = 2\ pF \rightarrow n_{opt} = \ln\left(\frac{C_L}{C_{Ref}}\right) = 8.7 \cong 9$

$t_{Ref} = R_{PU} * C_{Ref} = 30.48\ ps, \theta = e \rightarrow t_{Prop_{Min}} = t_{Ref} * \frac{\theta}{\ln \theta} * n_{opt} = 745.68ps \rightarrow f_{Max} = 1.3\ GHz$

10)

a) Without OD, $t_{Prop} = t_{Ref}(F_{I1} * B_{I1} + F_{I2} * B_{I2} + F_{I3} * B_{I3}) = t_{Ref}\left(1 * 1 + 1 * 1 + \frac{50}{2} * 1\right) = 27t_{Ref}$

b) Without OD,$t_{Prop} = t_{Ref}(F_{I1} * B_{I1} + F_{I2} * B_{I2} + F_{I3} * B_{I3}) = t_{Ref}\left(\frac{1}{5} * 1 + \frac{1}{5} * 1 + \frac{50}{2} * 1\right) = \frac{127}{5} t_{Ref}$

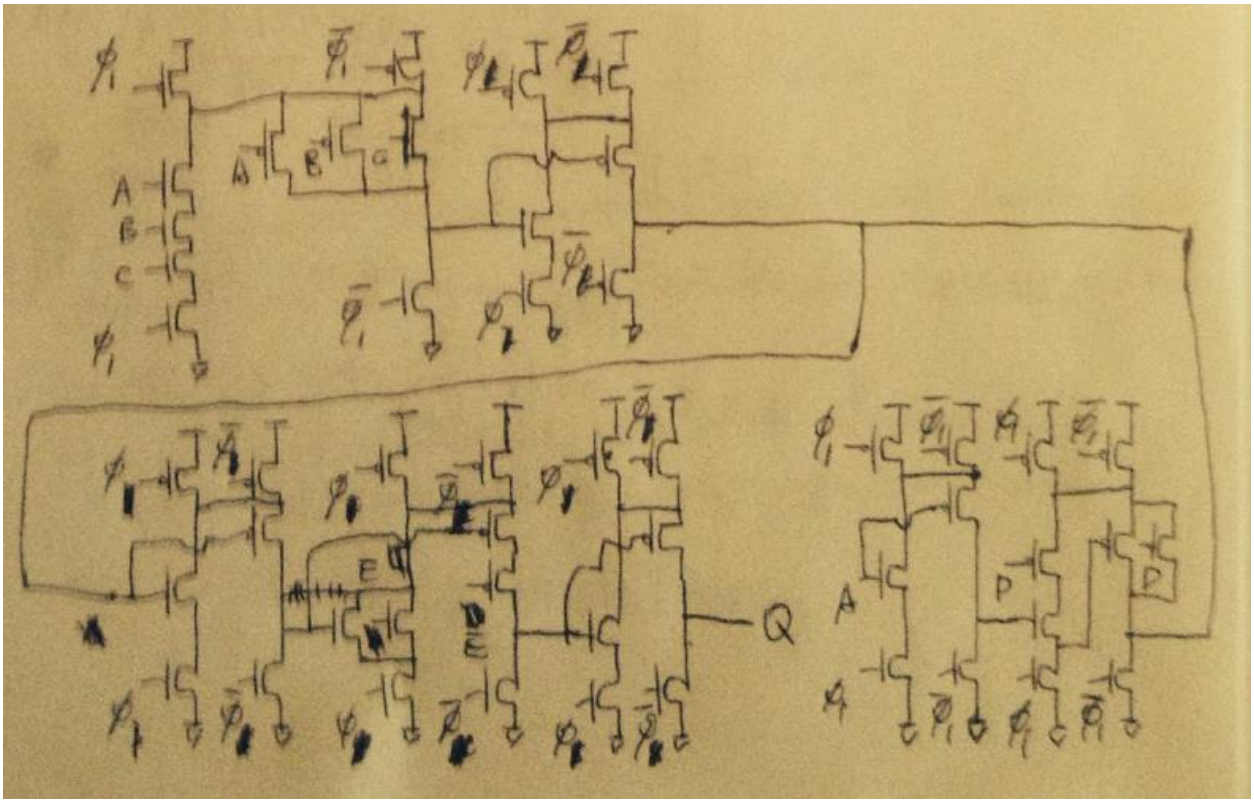
c) $C_{Ref} = 6 * .2 * .2 * 8, C_{total} = 2C_{Ref} + C_L = 53.84fF \rightarrow P = 10M * 53.84f * 2^2 = 2.15\mu W$

d) $C_{Ref} = 2 * .2 * .2 * 8, C_{total} = 2C_{Ref} + C_L = 51.28fF \rightarrow P = 10M * 51.28f * 2^2 = 2.05\mu W$

11)

For domino logic $V = \frac{V_{DD}}{2}, but\ C_L\ is\ the\ same \rightarrow P = f * C_L * V^2 \rightarrow P_{CMOS} = 4\ P_{Domino}$

12)



13)

$t_{Prop} = R_{ref} * C_L = \frac{L_n}{\mu_n C_{ox} W_n (V_{DD} - V_T)} * 2 * L_\mu * W_\mu * C_{ox} = 987.43 * 10^{-15}\ s$

We need $f = \frac{1}{2 * t_{prop} * n} = 80MHz \rightarrow t = 12.5\ ns, and\ t_{Prop} \propto L^2$

Choose seven-stage oscillator and solve for L $\rightarrow L_n = 30.07\ L_{Min}, W_n = W_{Min}, L_P = L_{Min}, W_p = 5\ W_{Min}$

14)

A footed domino gate has an extra NMOS between the pull-down network and the ground. This transistor is forced off during precharging, preventing any current from shooting through the gate if the pull-down network is active. But, it requires an extra transistor for each gate and a complementary clock signal.

15)

$$t_{write} = \frac{1}{2} t_{clk} = R * C, where\ R = \frac{L_n}{\mu_n C_{ox} W_n (V_{DD} - V_T)}, and\ C = 2 * L_n * W_n * C_{ox}$$

$$\rightarrow W_5 = \frac{L_{Min}^2 * 4 * f_{clk}}{\mu_n (V_{DD} - V_T)} * W_{Min}$$

16)

Because we neglect the off path elements, this is the same problem as 1).