EE 330 Fall 2012
Homework 5

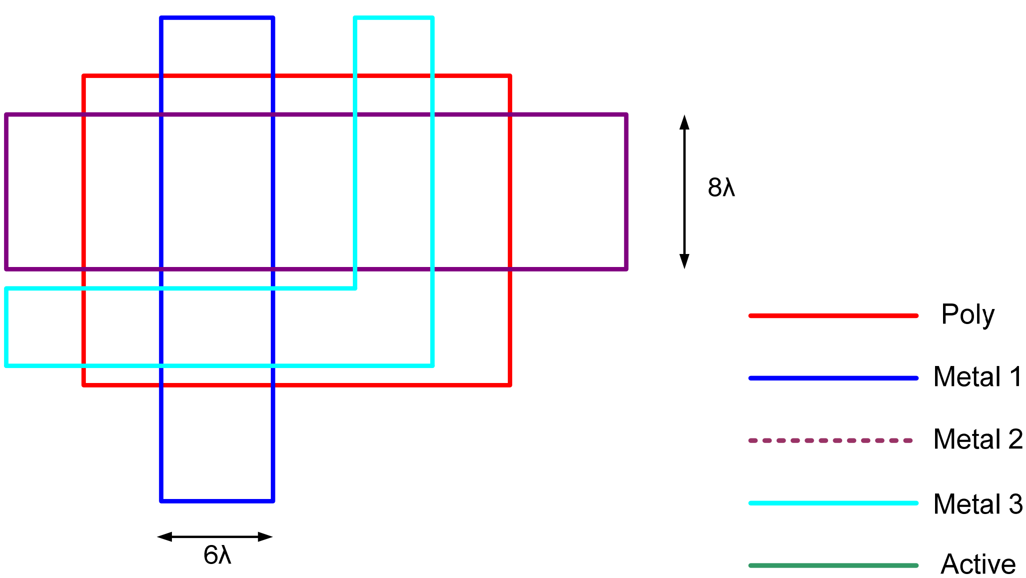
Due Friday September 21 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

If parameters are needed for process characterization, use the measured parameters from the ON (formerly AMI) T6AU process run that is attached at the end of this HW. On those problems that involve the design of passive components, a sketch of the design is sufficient provided you indicate dimensions (i.e. it need not be done in Cadence).

Problem 1 (10 points):
Design an 8k resistor in the ON 0.5u CMOS process. Use Poly 1 for the resistor. The width-to-length ratio of an imaginary box contacting on 4 sides but enclosing the resistor should be between 1:2 and 2:1.

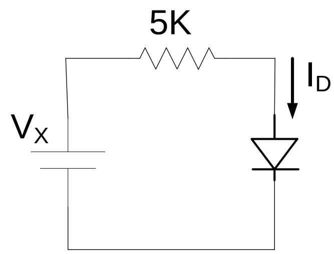
Problem 2 (10 points):
Design a 2pF capacitor in the ON 0.5u CMOS process.

Problem 3 (15 points):
Four non-contacting regions are shown. Identify the parasitic capacitances and their size if this is fabricated in the 0.5u CMOS process. Don't forget that there is substrate below all layers. (Assume this drawing is to scale).



Problem 4 (10 points):
If the voltage of a forward-biased pn junction is varied from 0.55V to 0.65V, what is the corresponding range in the diode current? The area of the diode is 50um^2 and $J_S=10^{-15}\text{A/u}^2$.

Problem 5 (10 points):
Accurately determine the current I_D if V_X=5V for the below circuit. Repeat if V_X=450mV.



Problem 6 (5 points):
Assume a 1kΩ resistor has a resistance of 1.0345kΩ at T=250°K. If the TCR of this resistor is constant and equals 100ppm/°C, what will be the resistance at T=400°K?

Problem 7 (20 points):
Diodes are often used to build temperature sensors. Assuming that the standard diode equation accurately characterizes the I-V relationship for the diode under modest forward bias, and then taking the natural logarithm of both sides, an alternate equivalent expression for the diode equation can be written as:

$$I_D = I_S e^{\frac{V_D}{V_t}} \qquad \rightarrow \qquad V_D = T\left(\frac{k}{q}\right)\ln\left(\frac{I_D}{I_S}\right)$$

where T is in K. In the second equation, we have replaced V_t with kT/q to explicitly show the temperature dependence of this term. Looking at the second form, it could be argued that if a constant current were used to excite the diode, then the diode voltage would be proportional to temperature, and thus the diode could serve as a very linear temperature sensor. Unfortunately, this argument falls apart because the parameter I_S in the diode equation itself has some temperature dependence. However, the following equation explicitly shows the full temperature dependence of the diode equation:

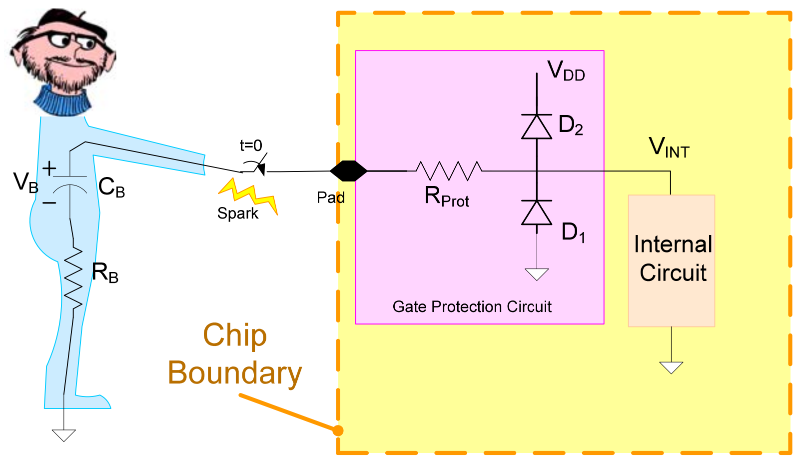
$$I(T) = \left(J_{SX} A\left[T^m e^{\frac{-V_{G0}}{V_t}}\right]\right) e^{\frac{V_D}{V_t}}$$

where the parameters J_{SX} , $V_{GO,}$ and m are constants that are independent of temperature and where A is the cross-sectional area of the diode.

a) If $J_{SX}=0.45A/\mu^2$, V_{G0}=1.17V, m=2.3, and A=100 μ^2, obtain an expression for I_S and plot it versus temperature from T=0°C to T=100°C.
b) If I_S was measured in the laboratory at t=27°C, what percent change in I_S would occur if the temperature in the room is increased to 30°C.
c) Comment on the accuracy you can expect to obtain in measuring I_S in the laboratory if the heating/cooling in the room has a ripple temperature of 2°C peak to peak.

Problem 8 (20 points):

Gate protection circuits are used to protect the sensitive gate oxide of devices connected to the input of an integrated circuit from modest short-duration over voltages. Although no input protection circuit can protect from all unknown over-voltages, the Human Body Model (HBM) is often used to model the type of over-voltages that are common when humans might become statically charged during normal activities. Such a model is shown below. In this model, R_B is the body resistance, C_B is the body capacitance and V_B is the charge on the body capacitance. At t=0 it is assumed that the switch is closed and this inserts a voltage into the input pad of the IC. In the absence of the gate protection circuit, the pad voltage will appear directly on the voltage V_{INT}.

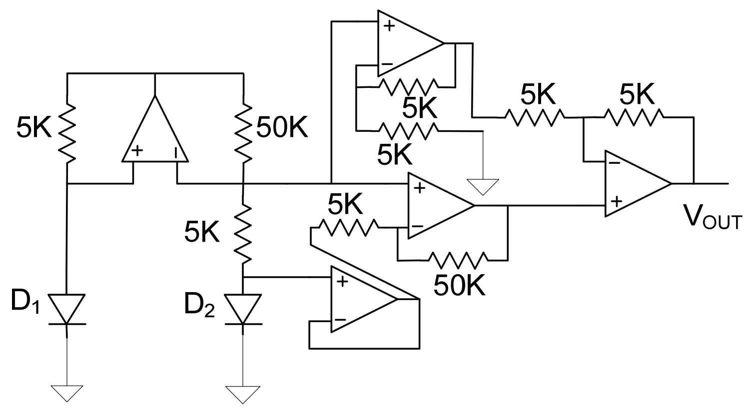


Assume the Internal Circuit has an input that is the two gates of a minimum sized inverter designed in the ON 0.5u CMOS process. Assume that the diodes D_1 and D_2 can be modeled as an ideal diode with $J_S=10^{-20}A/u^2$, and that the area of the two diode junctions is $1000u^2$. Consider two HBMs. One is termed a low-voltage model and the other a high-voltage model. These are characterized respectively by:

HBM_1: V_B =250V, C_B=150pF, R_B=1.5K
HBM_2: V_B =2KV, C_B=150pF, R_B=1.5K

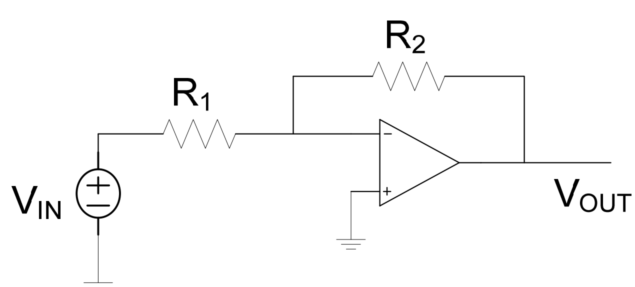
a) What will be the peak value of the voltage V_{INT} when the switch is closed if the gate protection circuit is absent (i.e. the Pad is directly connected to the Internal Circuit) with each of the models.
b) What will be the peak value of the voltage V_{INT} with each of the models when the switch is closed if the gate protection circuit is present? Assume R_{PROT}=15K.
c) What will be the peak current in D_2 with each of the models? Assume R_{PROT}=15K.
d) What is the purpose of including the resistor R_{PROT} and what are the disadvantages of including this resistor in the gate protection circuit?

Problem 9 (10 points, not required but will count for extra credit):
Obtain an expression for the output voltage versus temperature for the circuit shown below. Assume D_1 and D_2 are matched.



Problem 10 (10 points, not required but will count for extra credit):
The audio amplifier shown below has a gain determined by the resistors R_1 and R_2. R1 is a 1k ideal resistance, while R_2 is 10k when the voltage across it is 0V and has a voltage coefficient of resistance of 400ppm/V.

a) If V_{IN}=0.1sin2000t, what is the maximum error this amplifier will make in amplifying this signal due to the voltage coefficient of R_2?
b) Repeat part a) if V_{IN}=sin2000t



MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms

	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms
Gate Oxide Thickness	142			angstrom

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate

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COMMENTS: SUBMICRON
T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 11/07
* LOT: T6AU                  WAF: 7101
* Temperature_parameters=Default

.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 1.42E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = 0.629035
+K1      = 0.8976376      K2      = -0.09255       K3      = 24.0984767
+K3B     = -8.2369696     W0      = 1.041146E-8    NLX     = 1E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.7123969      DVT1    = 0.4232931      DVT2    = -0.1403765
+U0      = 451.2322004    UA      = 3.091785E-13   UB      = 1.702517E-18
+UC      = 1.22401E-11    VSAT    = 1.715884E5     A0      = 0.6580918
+AGS     = 0.130484       B0      = 2.446405E-6    B1      = 5E-6
+KETA    = -3.043349E-3   A1      = 8.18159E-7     A2      = 0.3363058
+RDSW    = 1.367055E3     PRWG    = 0.0328586      PRWB    = 0.0104806
+WR      = 1              WINT    = 2.443677E-7    LINT    = 6.999776E-8
+XL      = 1E-7           XW      = 0              DWG     = -1.256454E-8
+DWB     = 3.676235E-8    VOFF    = -1.493503E-4   NFACTOR = 1.0354201
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.342963E-3    ETAB    = -1.5324E-4
+DSUB    = 0.0764123      PCLM    = 2.5941582      PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3    PDIBLCB = -0.0431505     DROUT   = 0.9919348
+PSCBE1  = 6.611774E8     PSCBE2  = 3.238266E-4    PVAG    = 0
+DELTA   = 0.01           RSH     = 83.5           MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.32E-10       CGSO    = 2.32E-10       CGBO    = 1E-9
+CJ      = 4.282017E-4    PB      = 0.9317787      MJ      = 0.4495867
+CJSW    = 3.034055E-10   PBSW    = 0.8            MJSW    = 0.1713852
+CJSWG   = 1.64E-10       PBSWG   = 0.8            MJSWG   = 0.1713852
+CF      = 0              PVTH0   = 0.0520855      PRDSW   = 112.8875816
+PK2     = -0.0289036     WKETA   = -0.0237483     LKETA   = 1.728324E-3     )
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.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 1.42E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.9232867
+K1      = 0.5464347      K2      = 8.119291E-3    K3      = 5.1623206
+K3B     = -0.8373484     W0      = 1.30945E-8     NLX     = 5.772187E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.0973823      DVT1    = 0.5356454      DVT2    = -0.1185455
+U0      = 220.5922586    UA      = 3.144939E-9    UB      = 1E-21
+UC      = -6.19354E-11   VSAT    = 1.176415E5     A0      = 0.8441929
+AGS     = 0.1447245      B0      = 1.149181E-6    B1      = 5E-6
+KETA    = -1.093365E-3   A1      = 3.467482E-4    A2      = 0.4667486
+RDSW    = 3E3            PRWG    = -0.0418549     PRWB    = -0.0212201
+WR      = 1              WINT    = 3.007497E-7    LINT    = 1.040439E-7
+XL      = 1E-7           XW      = 0              DWG     = -2.133809E-8
+DWB     = 1.706031E-8    VOFF    = -0.0801591     NFACTOR = 0.9468597
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.4060383      ETAB    = -0.0633609
+DSUB    = 1              PCLM    = 2.2703293      PDIBLC1 = 0.0279014
+PDIBLC2 = 3.201161E-3    PDIBLCB = -0.057478      DROUT   = 0.1718548
+PSCBE1  = 4.876974E9     PSCBE2  = 5E-10          PVAG    = 0
+DELTA   = 0.01           RSH     = 105.3          MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 3.12E-10       CGSO    = 3.12E-10       CGBO    = 1E-9
+CJ      = 7.254264E-4    PB      = 0.9682229      MJ      = 0.4969013
+CJSW    = 2.496599E-10   PBSW    = 0.99           MJSW    = 0.386204
+CJSWG   = 6.4E-11        PBSWG   = 0.99           MJSWG   = 0.386204
+CF      = 0              PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 7.286716E-4    LKETA   = -4.768569E-3
)
*
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