EE 330
Section 5, 8:00 am
Layout, DRC, and LVS

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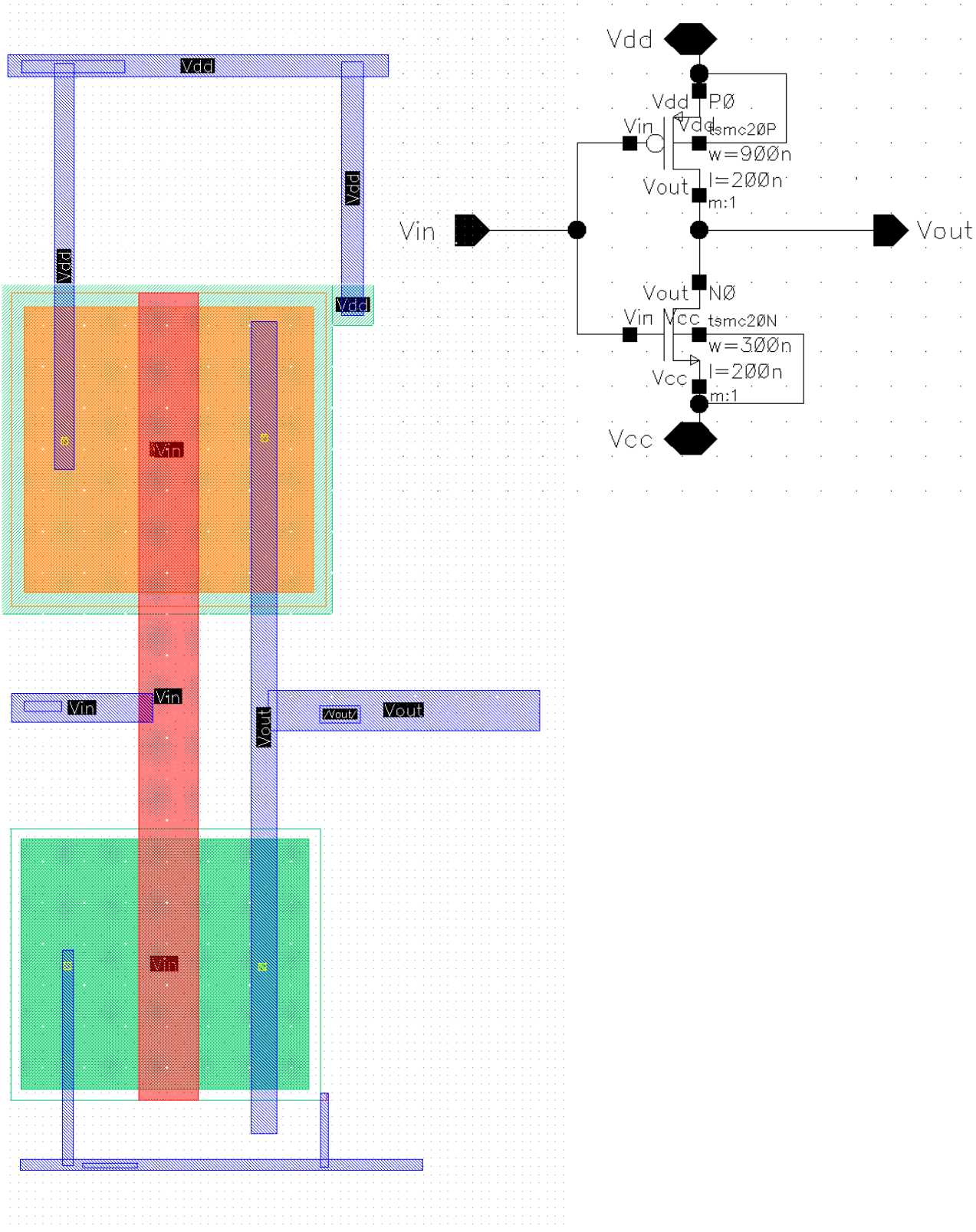
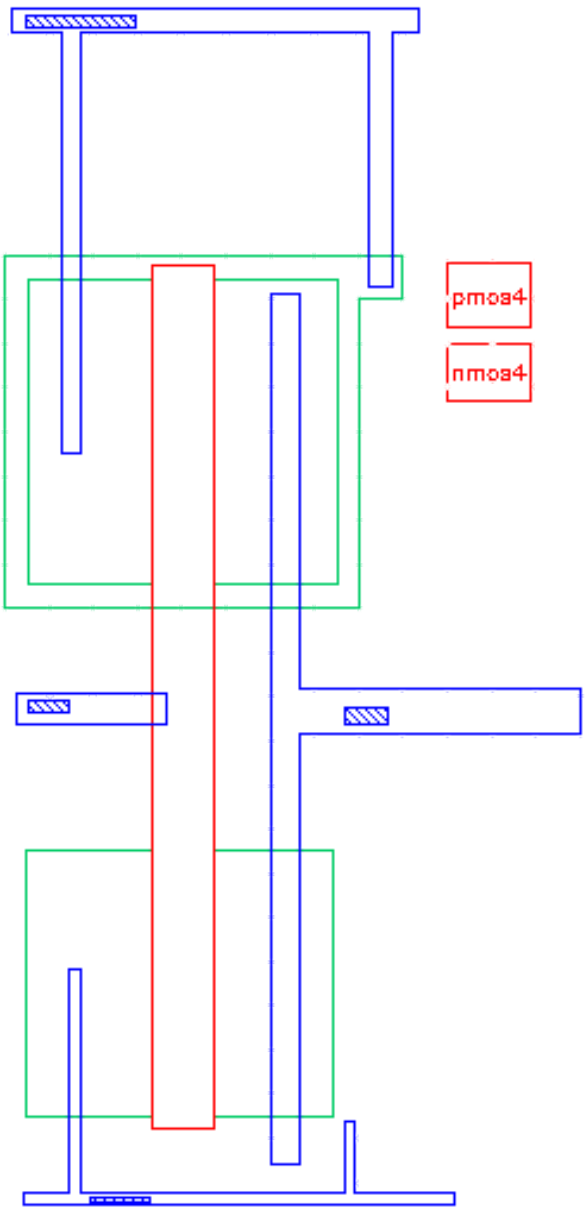
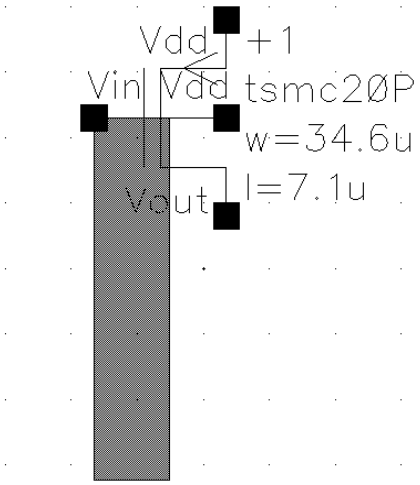
Introduction:
This experiment vaguely focuses on the concept of integrated circuits and the use of cadence to create layouts. While the directions were difficult to follow as a beginner, they detail the link between layouts and their extracted views with the creation of several gates.

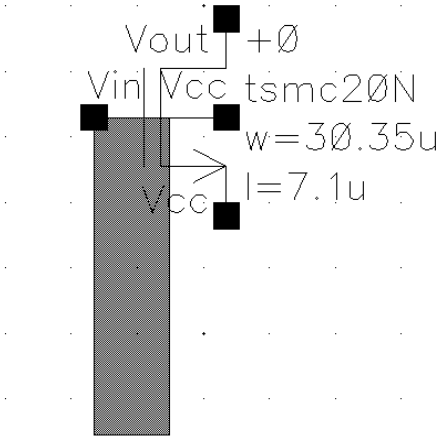
1. **Creating a layout.**

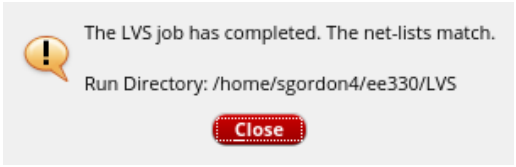


2. Extracted View.







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Getting layout propert bagGetting schematic propert bagGetting schematic propert bag
Getting schematic propert bag
Getting layout propert bagGetting layout propert bagLVS job is now started...
The LVS job has completed. The net-lists match.

Run Directory: /home/sgordon4/ee330/LVS
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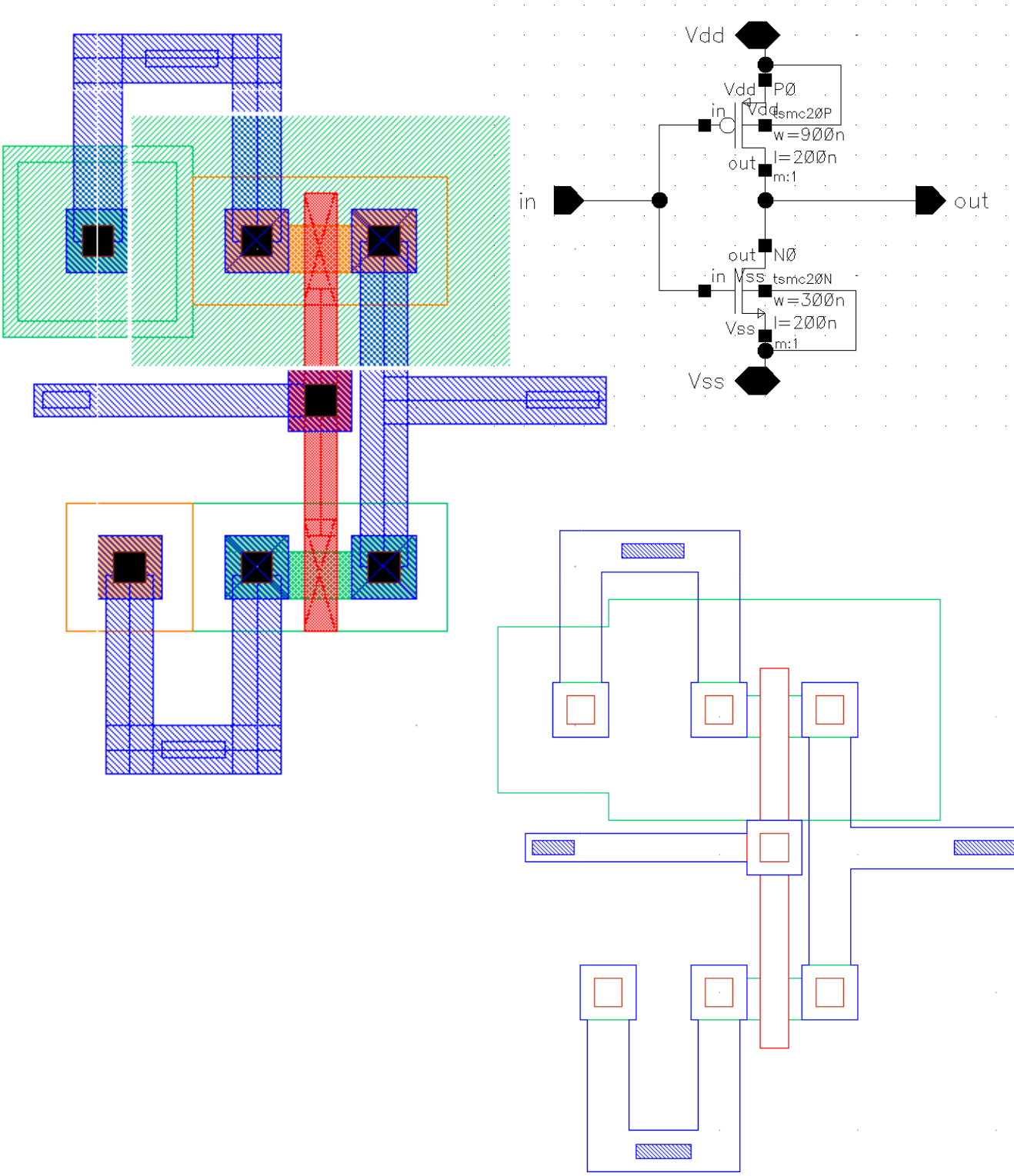
3. Using P Cells.



4. Nand xor Nor.

I built a Nand gate for this section of the lab