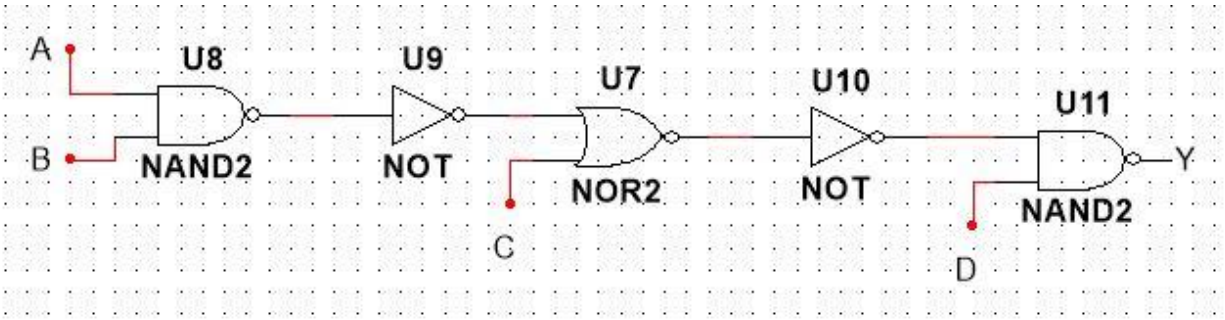
Homework 3 Fall 2017 TA: Robert Buckley

Problem 1:

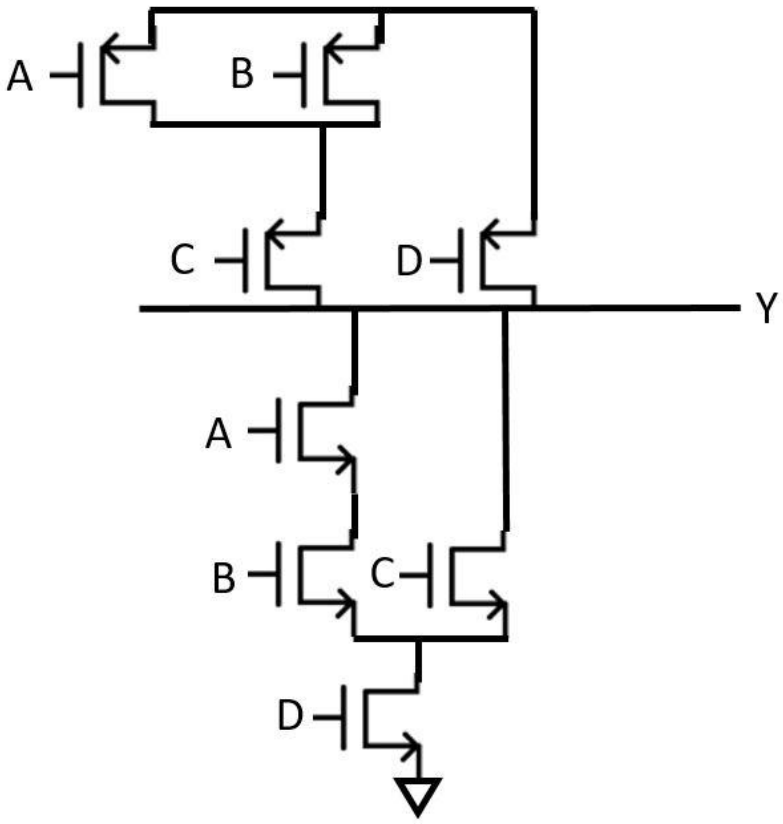
$Y = \overline{(AB + C)D}$

One possible design with static CMOS gates,



This design uses 16 transistors.

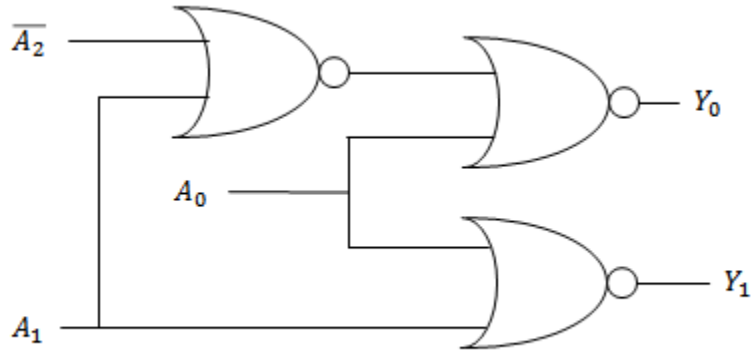
The below is one design for a compound CMOS gate



This design uses 8 transistors

Problem 2:

$Y_0 = \overline{A_0}(A_1 + \overline{A_2})$
$Y_1 = \overline{A_0} * \overline{A_1}$



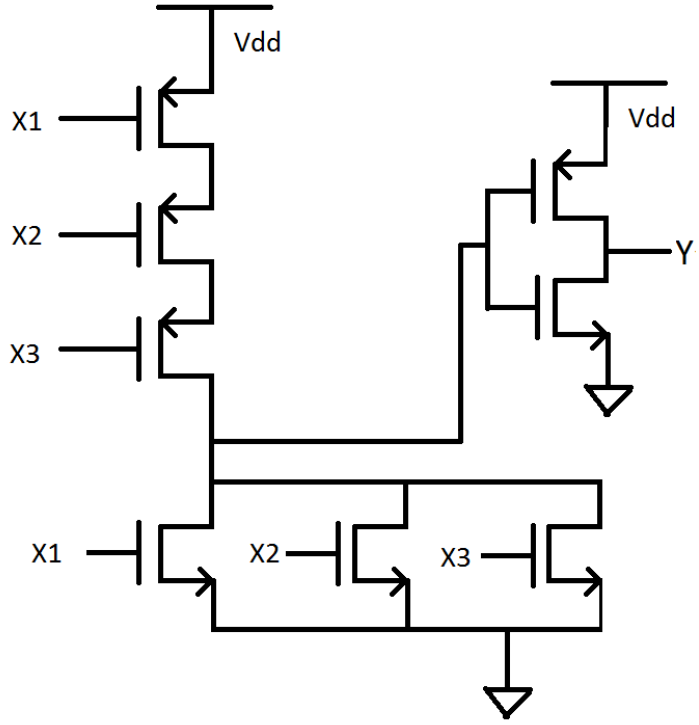
Problem 3:

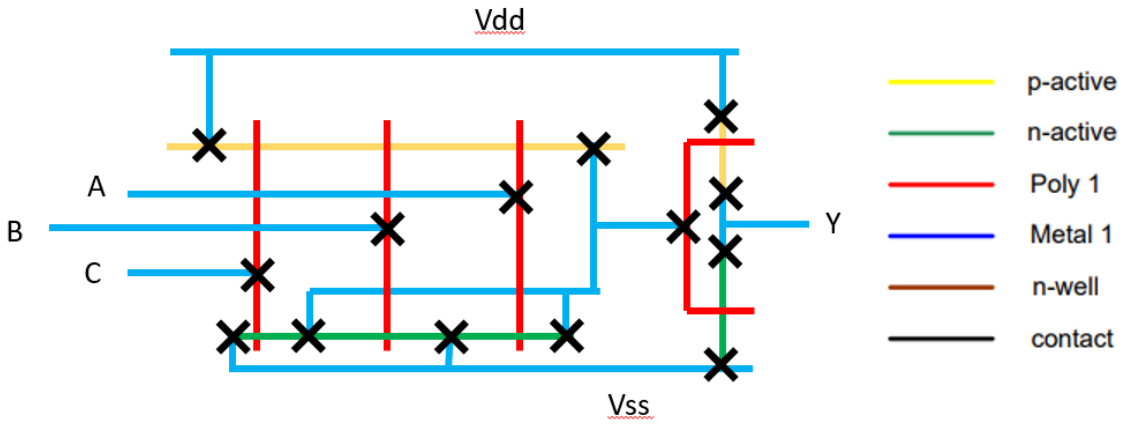
For minimum sized 2 input NAND,

$R_{SWN} = 2k\Omega, R_{SWP} = 6k\Omega, C = 40fF$

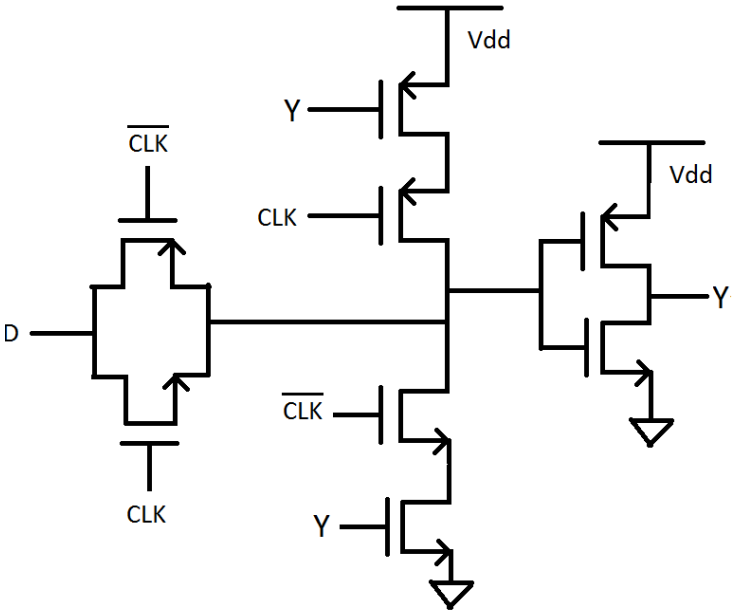
$T_{HL} = 2 * R_{SWP} * C = 12k * 40f = 480 * 10^{-12} seconds = 480\ pS$

Problem 4


Vdd
X1
X2
X3
Vdd
Y
X1
X2
X3

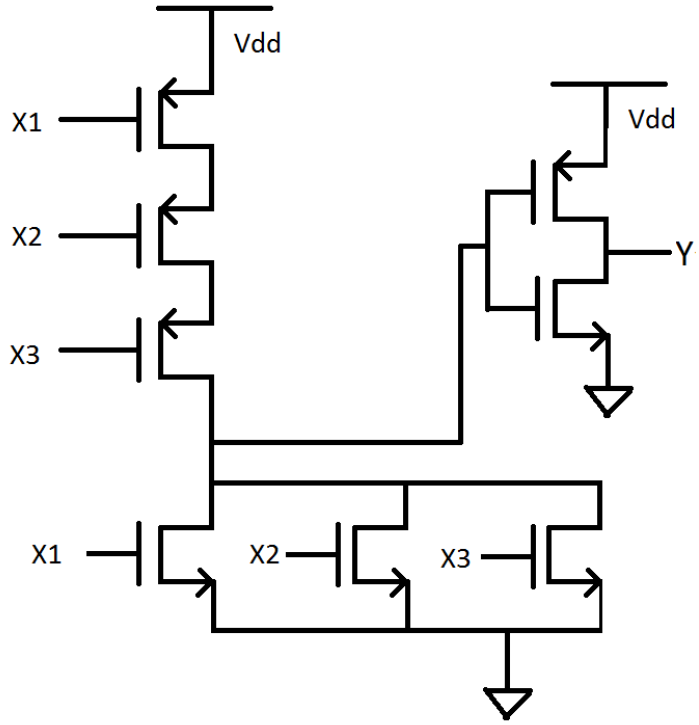

Vdd
A
B
C
Y
Vss
p-active
n-active
Poly 1
Metal 1
n-well
contact

Problem 5

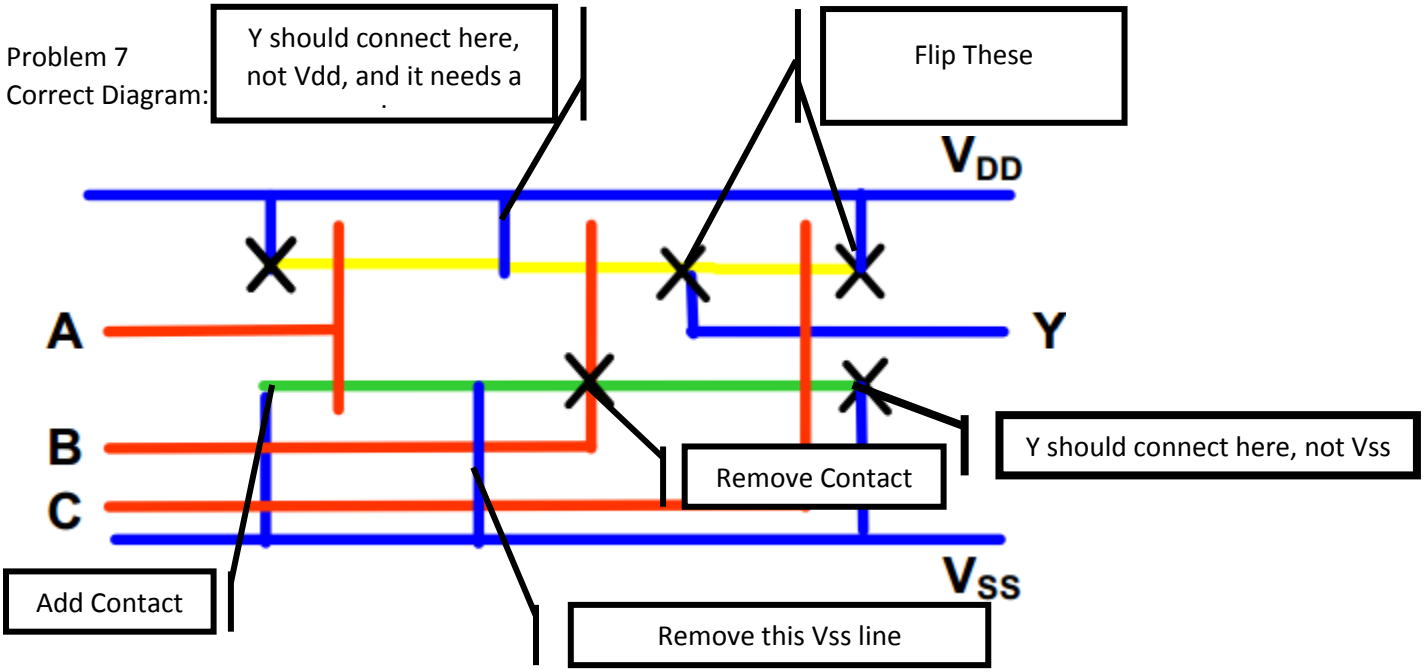


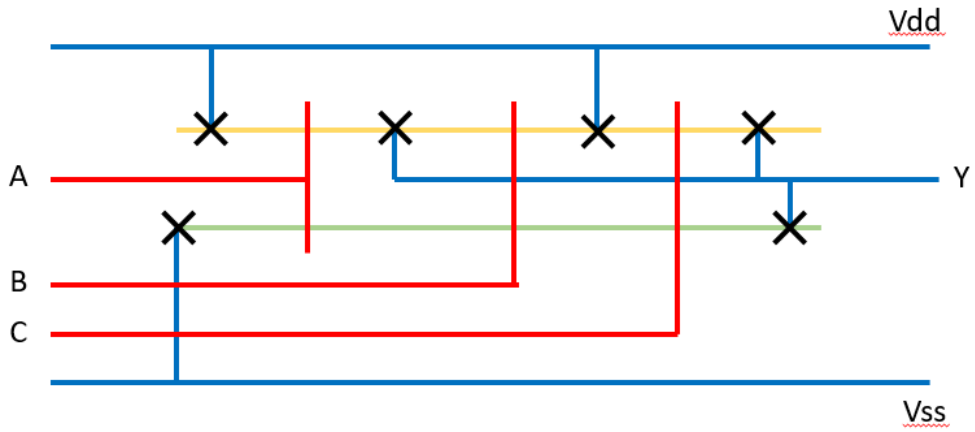
The second inverter is combined with the transmission gate, rather than two separate components.

Problem 6



Problem 7
Correct Diagram:





Problem 8

a) $R_{W\_Aluminum} = \frac{2.8*10^{-8}}{0.2*10^{-6}} * \frac{180}{5} + \frac{2.8*10^{-8}}{0.2*10^{-6}} * \frac{40-5}{5} = 6.02\Omega$

$V_{wire} = 5 * \frac{6.02}{100 + 6.02} = 283.9\ mV$

$V_{Resistor} = 5V - V_{wire} = 5 - 0.2839 = 4.716\ V$

b) $R_{W_{Copper}} = 3.655\ \Omega$

$V_{wire} = 5 * \frac{3.655}{100 + 3.655} = 0.176\ V$

$V_{Resistor} = 5 * \left(\frac{100}{100 + 3.655}\right) = 4.824\ V$

c) $V_{RW} < 5V * 5\% = 0.25V$

$5V * \left(\frac{R_W}{100 + R_W}\right) < 0.25V \rightarrow R_W < 5.263\ \Omega$

$R_W = 6.02 * \frac{5\mu m}{Width_{wire}} \rightarrow Width_{Wire} \geq 5.72\ \mu m$

Problem 9:

Each inverter has $C_L = 1.5\ fF + 1.5\ fF = 3fF$
total load capacitance $C = 3\ pF * 6 = 18\ fF$
$R_{SWp} = 6k\Omega \rightarrow T_{LH} = 6\ k * 18\ f = 108 * 10^{-12} S = 108\ pS$

Problem 10

Base Code

```
module NOR2 (i_A, i_B, o_F);
  input i_A, i_B;
  output o_F;

  assign o_F = ~(i_A||i_B);

endmodule
```

```
module OR2 (i_A, i_B, o_F);
  input i_A, i_B;
  output o_F;
  wire A_nor_B;

  NOR2 nor0(.i_A(i_A), .i_B(i_B), .o_F(A_nor_B));
  NOR2 nor1(.i_A(A_nor_B), .i_B(A_nor_B), .o_F(o_F));

endmodule
```

```
module AND2 (i_A, i_B, o_F);
  input i_A, i_B;
  output o_F;
  wire A_not, B_not;

  NOR2 nor0(.i_A(i_A), .i_B(i_A), .o_F(A_not));
  NOR2 nor1(.i_A(i_B), .i_B(i_B), .o_F(B_not));
  NOR2 nor2(.i_A(A_not), .i_B(B_not), .o_F(o_F));

endmodule
```

```
module Mux_2_1 (i_A, i_B, i_S, o_F);
  input [1:0] i_A, i_B;
  input i_S;
  output [1:0] o_F;
  wire [1:0] AS, BS;
  wire w_Sn;

  NOR2 nor0(.i_A(i_S), .i_B(i_S), .o_F(w_Sn))  ;
  AND2 and0(.i_A(i_A[1]), .i_B(i_S), .o_F(AS[1]));
  AND2 and1(.i_A(i_A[0]), .i_B(i_S), .o_F(AS[0]));
  AND2 and2(.i_A(i_B[1]), .i_B(w_Sn), .o_F(BS[1]));
  AND2 and3(.i_A(i_B[0]), .i_B(w_Sn), .o_F(BS[0]));
  OR2  or0 (.i_A(AS[0]), .i_B(BS[0]), .o_F(o_F[0]));
  OR2  or1 (.i_A(AS[1]), .i_B(BS[1]), .o_F(o_F[1]));

endmodule
```

Test bench Code

```
module Mux_2_1_TB();
  reg [1:0] r_A, r_B;
  reg r_S;
  wire [1:0] w_F;

  initial
  begin
    r_A = 1'b0;
    r_B = 1'b0;
    r_S = 1'b0;
  end

  always
    #10 r_S = ~r_S;
  always
    #20 r_A = r_A+1;
  always
    #40 r_B = r_B+1;

  Mux_2_1 testcomp(.i_A(r_A), .i_B(r_B), .i_S(r_S), .o_F(w_F));

endmodule
```

Simulation results