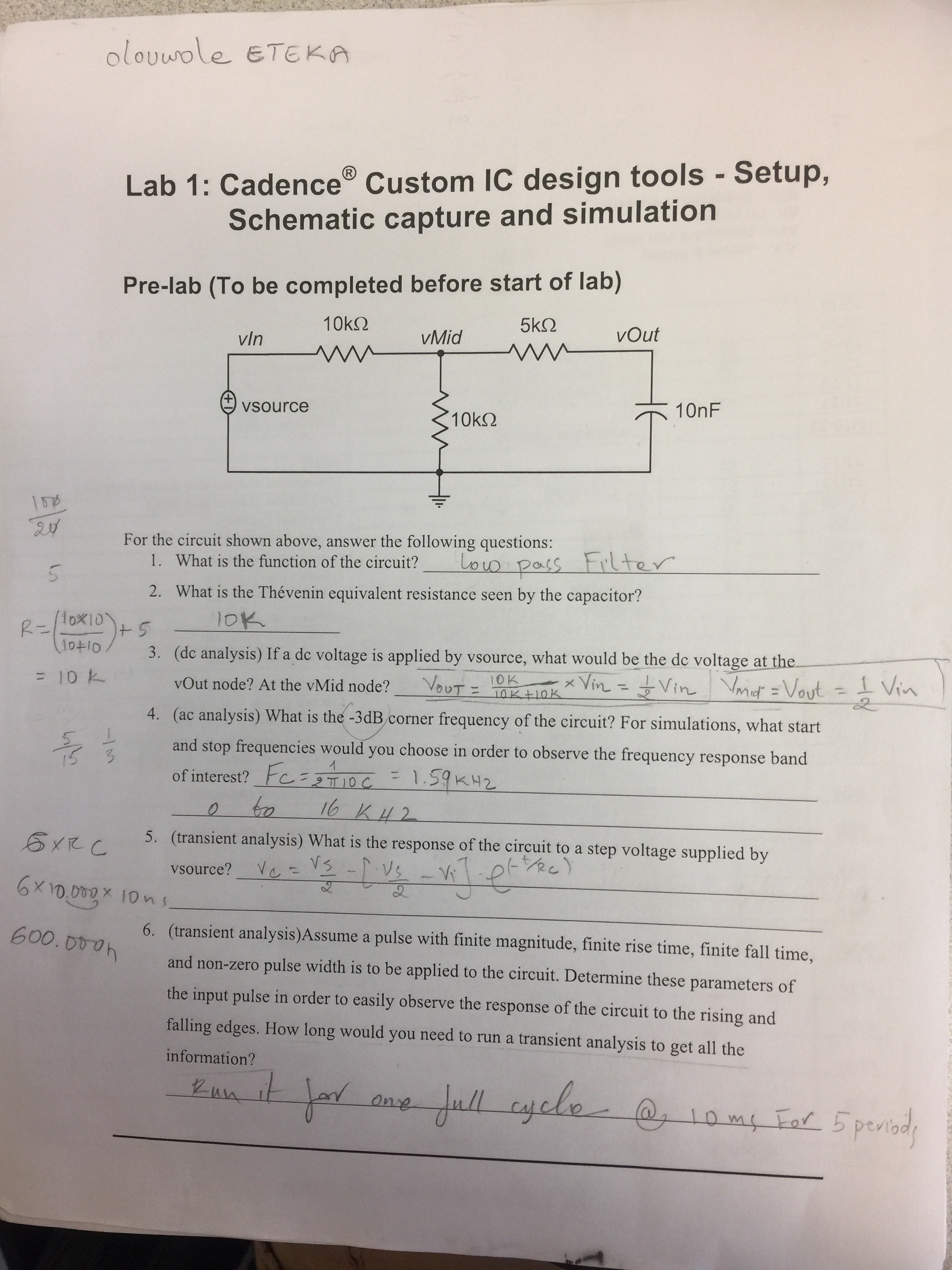
**Olouwole Eteka**

**EE330 lab1 Report Section C**

**Prelab**



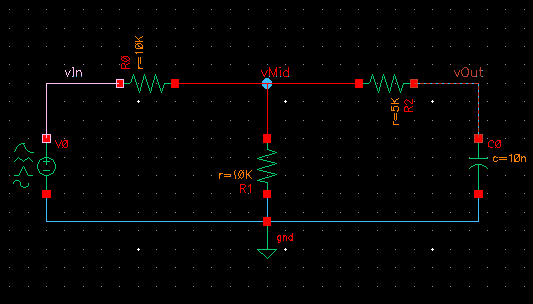
**Introduction**

In this lab installed the software to and familiarize ourselves with it. We run a stimulation on a simple RC circuit with DC, AC, and Transient signals as source. We learned Cadence Custom IC design tool, Virtuoso, and the basics of using Schematics Editor.

**Part 1**

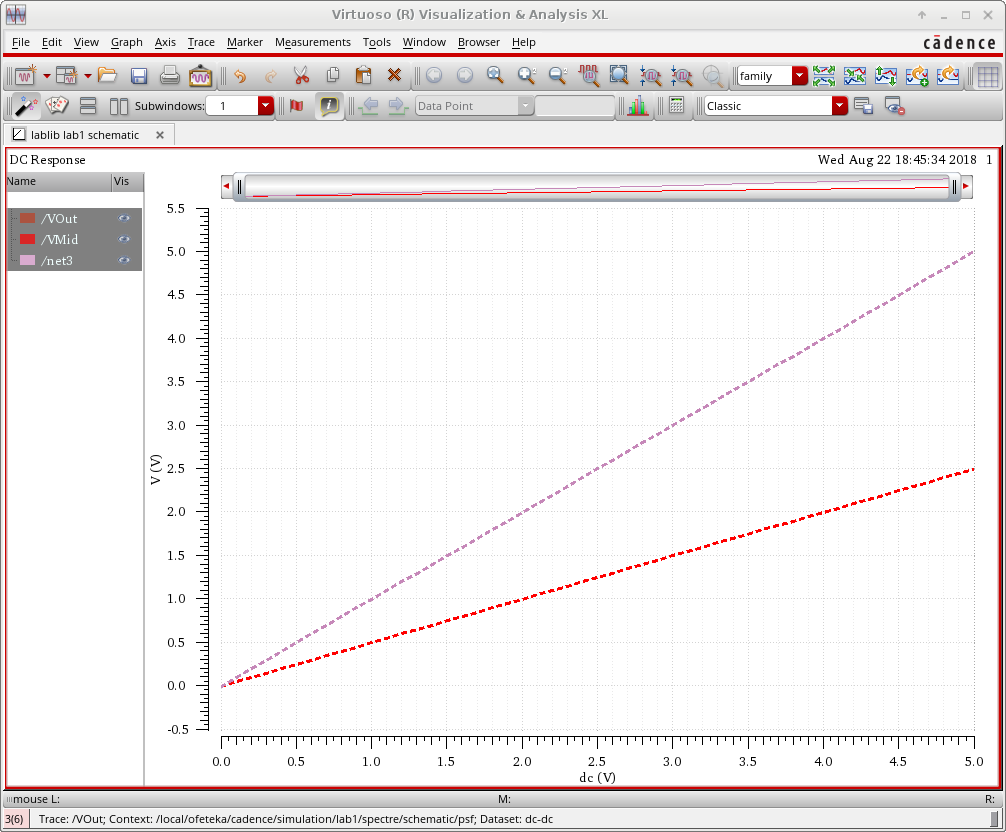
**DC analysis**

Implementation of the RC circuit in Cadence after setting up the software. My circuit it composed of 3 resistors and a capacitor with a DC source voltage for my first stimulation.



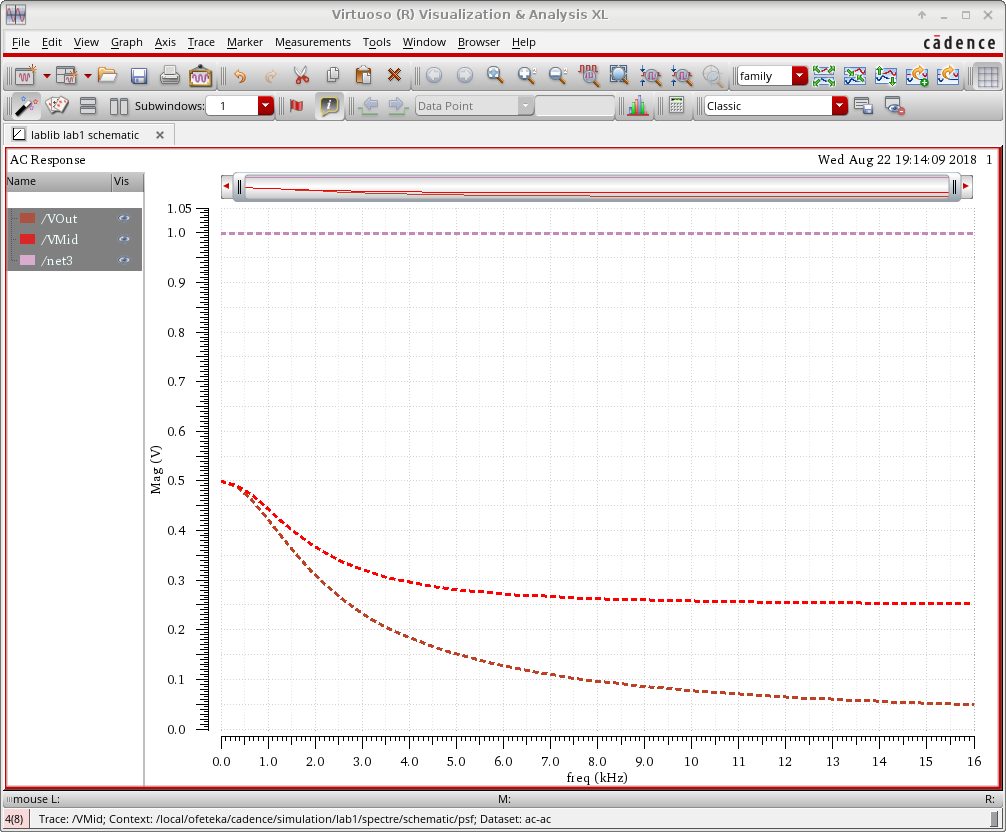
The calculations in Pre-Lab are demontrated trhough the graph below that vMid is similar to vOut and they are increasing as the input voltage increase. It shows to be true as vMid=vOut=vSource/2.

We can also observe that the slope of vIn is 2x of the slope of vMid and vOut, which still supports my calculation.



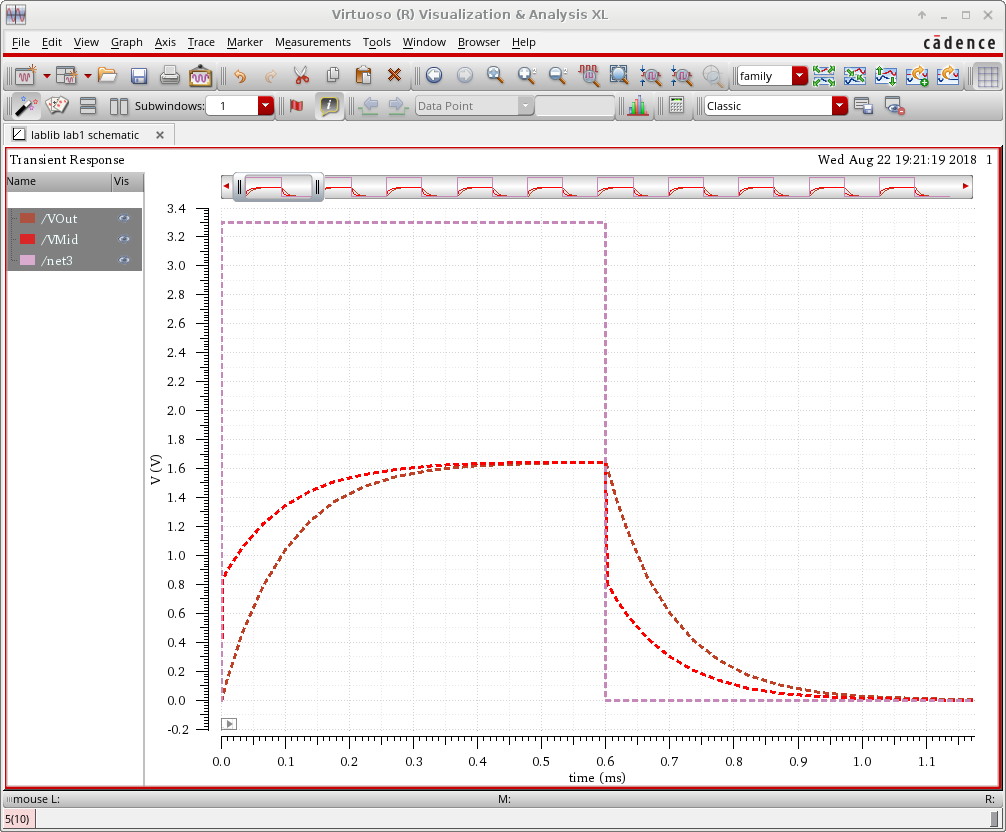
**AC analysis**

The second part was to run an AC analysis. I sweep the frequency from 1Hz to 1MHz. As we observe from the graph, vOut and vMid maintain at 0.5v for frequency <100Hz. Then, the both start reduces exponentially. vMid begins to maintain at 0.25v at about 10kHz while vOut begins to maintain at 0 starting 100kHz. The result was much of what I was expecting. In the prelab, I found that 1.59kHz for -3dB corner frequency. According to the graph, the maximum magnitude is 0.5v therefore (0.707\*0.5v = 0.3535v) is the -3dB magnitude and magnitude 0.3535v lies between 1kHz and 10kHz which I not far from the answer.



**TRANSIENT analysis**

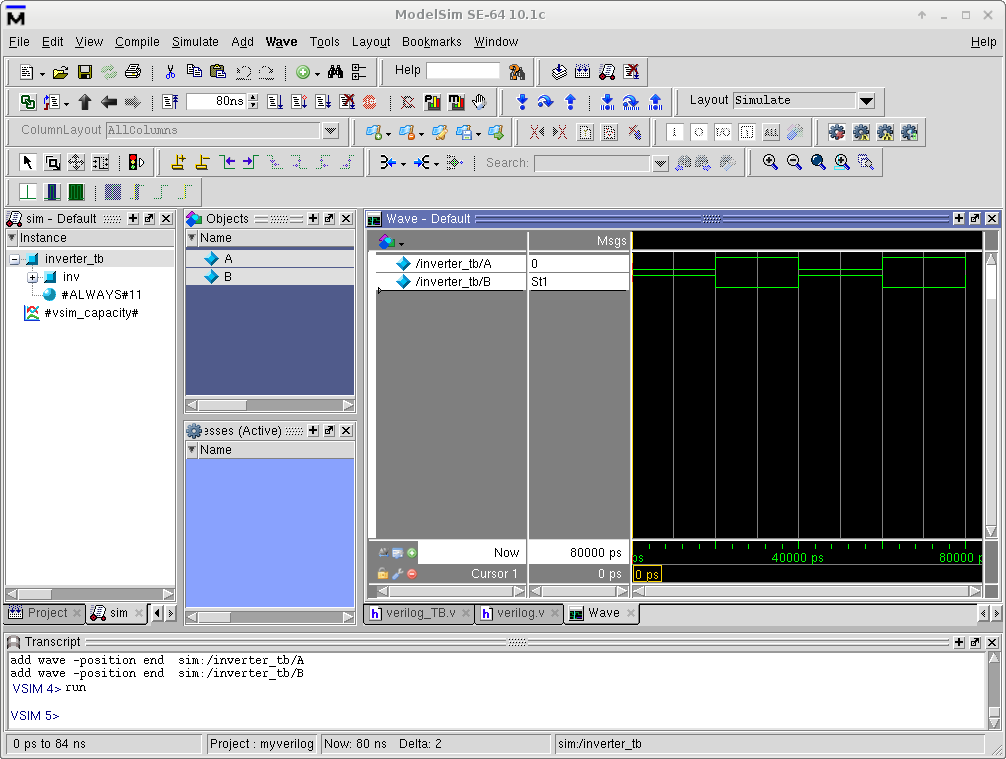
we know that the unit step response from the capacitors determine the level of our transient. From our graph below we can see the whole discharging and charging effect of the capacitor and the full period. The capacitor start charging until 0.6ms where is start discharging to 1.1 and will repeat the cycle. The graph shows the input (step input) VS vMid VS vOut and the all follow the same pattern.



**part2**

**Inverter**

We implemented an inverter using the Modelsim stimulation. The Verilog code for an inverter and the it stimulation code (testbench module) was provided I used to create “inverter.v” and “inverter\_tb.v”. from there I create a simulation waveform window and simulate the design with 80ns as the length of time I would like to simulate.



**Conclusion**

in this lab, I’ve learned the basics on setting up Cadence and ModelSim on a Linux operated computer. Linux operating system was unfamiliar to me but learning the commands as they will help me achieve most objectives by just typing out commands in the terminals. Also I learned that Cadence is a very convenient software for engineers to reduce time needed to do the calculations step-by-step or having a physical circuit which also save a lot in costs.