Olouwole Eteka

330 lab Report 3

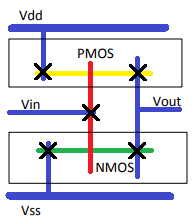
Section C

**Introduction**

In this lab we built a CMOS inverter layout then we repeat it using the NMMOS and PMOS built into the software. We will then build the schematic of a NAND and make the symbol of it then build a test bench to test it.

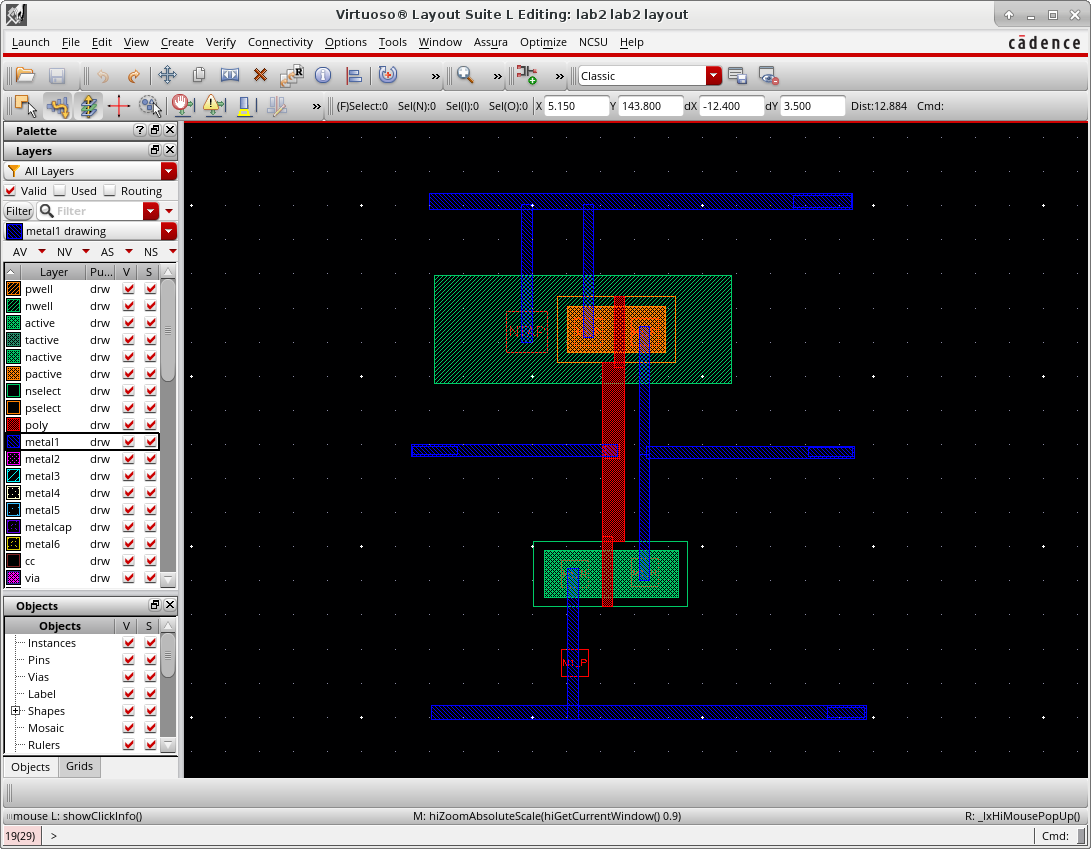
**Part 1 creating a layout**

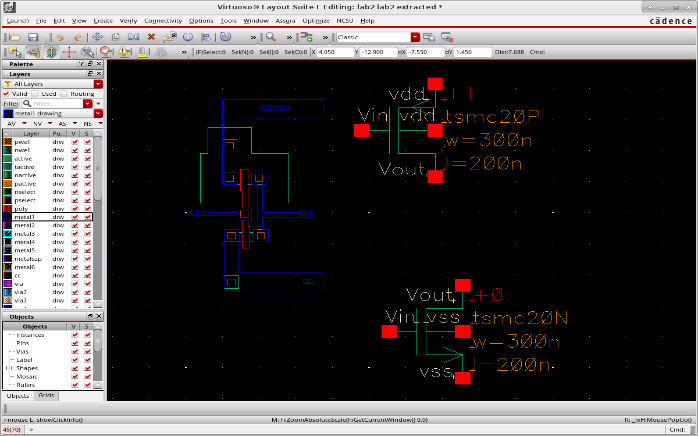
In the previous lab we made the layout of PMOS in this lab we made the NMOS and connect them to make an CMOS inverter



As shown in the layout above, bulk connections such as M1\_P, M1\_N, NTAP, M1\_POLY was added at desired locations that connecting the metal1. Then, pins are labelled based on the stick diagram below. Warning: the input and output pins names are case sensitive so it has to be the same as the schematic design to pass the LVS test later

I went to the Stick Diagram showing above to Physical Layer below





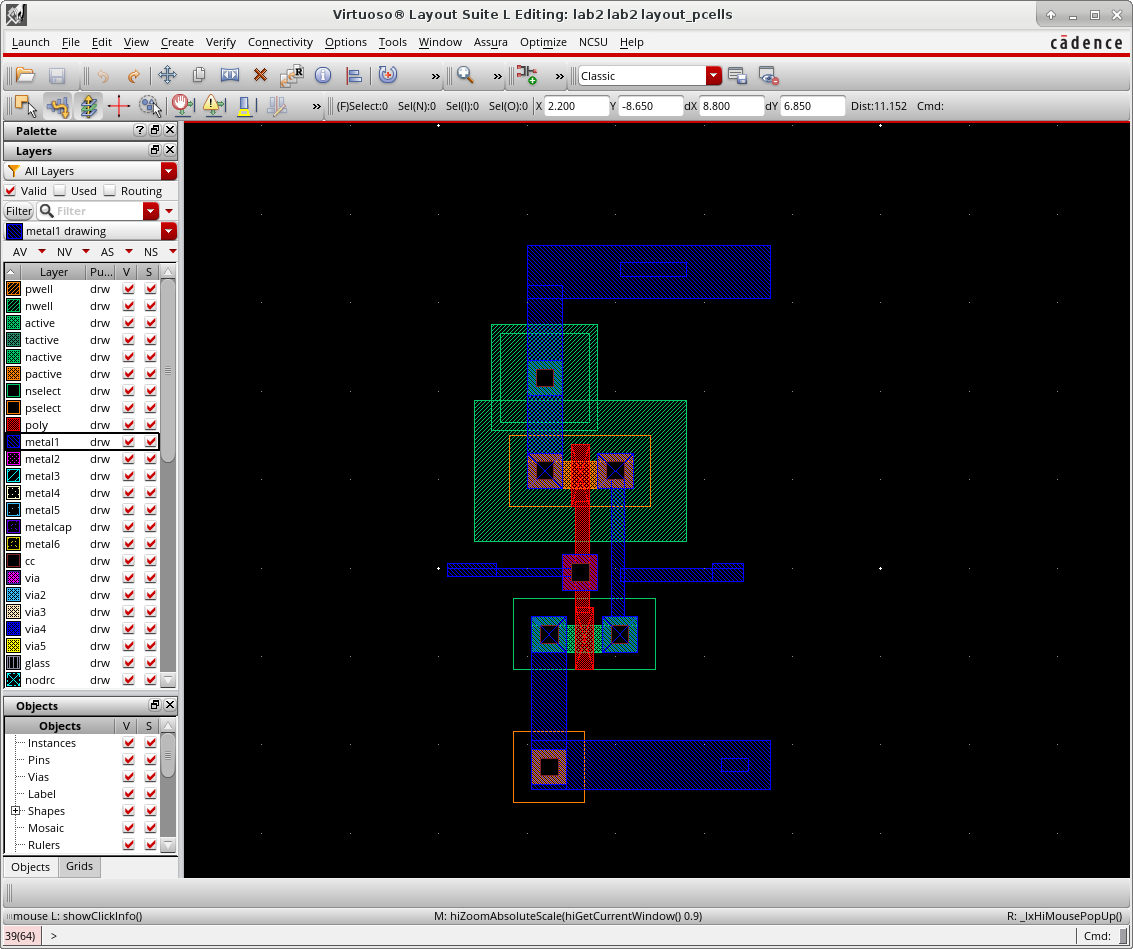
**Part 2 Extracted View**

Layout vs. Schematic (LVS) comparison:

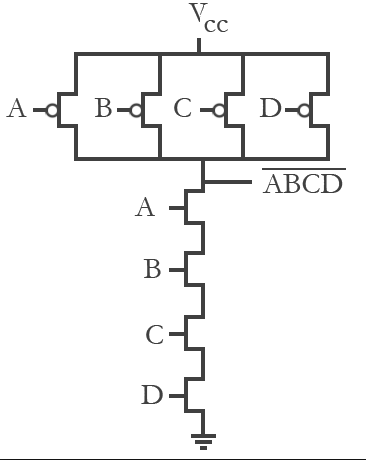
To verify the layout of my inverter I created an extracted file that will show the type transistors I used in my layout.

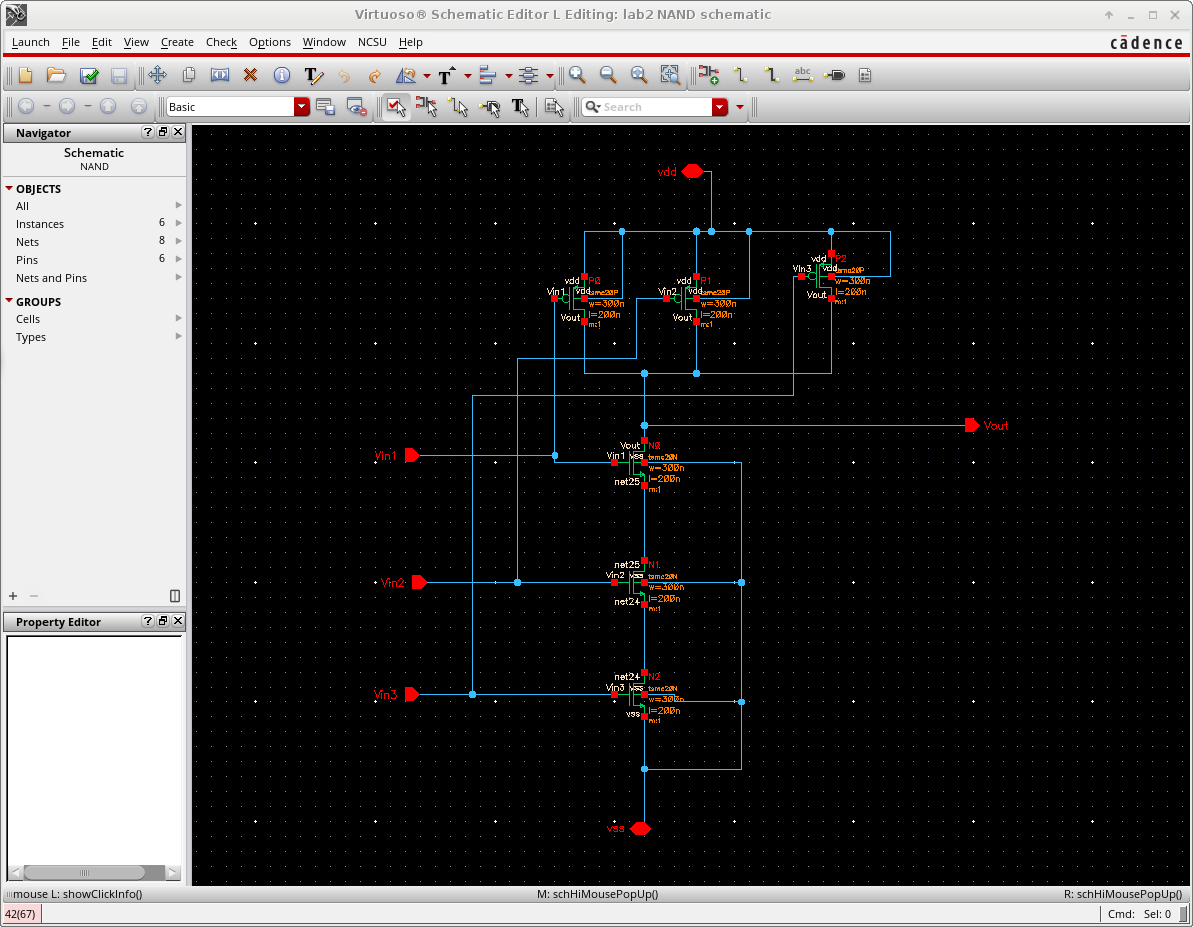
**Part 3 Using P cells**

By using the “new Instance (shortcut “I”)” feature as well as a new introduced “Path (shortcut “P”)” feature in the layout design page, I was able to design a similar inverter a lot faster using the existing PMOS and NMOS design. The layout is showing below



**Part 4 NAND xor NOR**

In this part of lab, we are spited in groups of two. One person will do the NOR gate and the other person the NAND. I choose to make the design of the NAND gate. I will be creating a 3-input NAND gate schematic design and verify it running a test bench I will show later in the report. I followed the circuit diagram to build my schematic in cadence

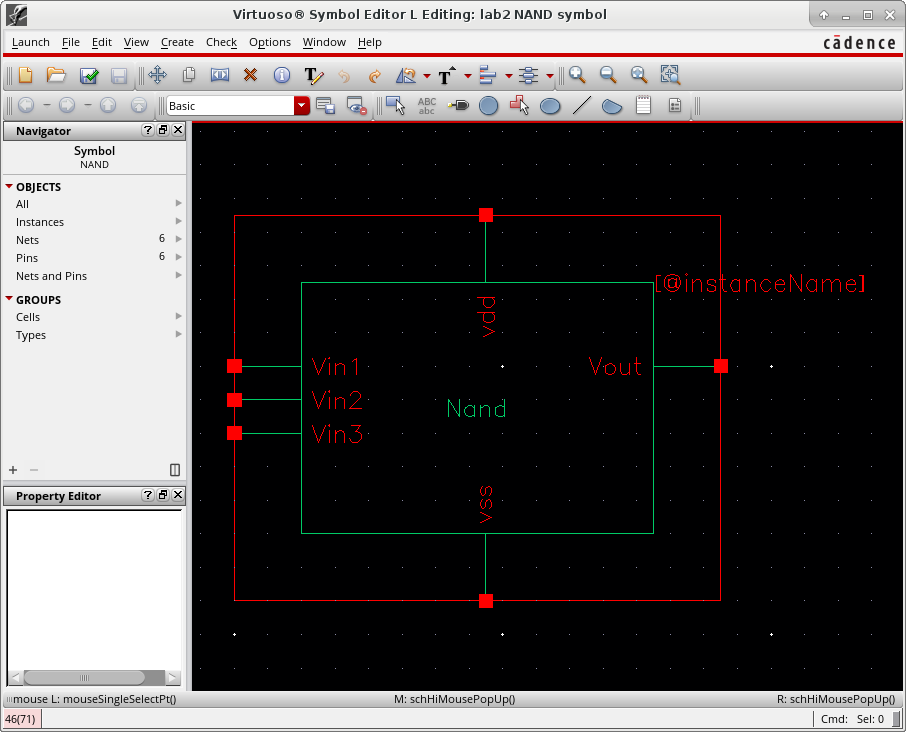


**The symbol of the of the NAND gate**

To create the symbol of my gate I followed the procedure bellow from the schematic window

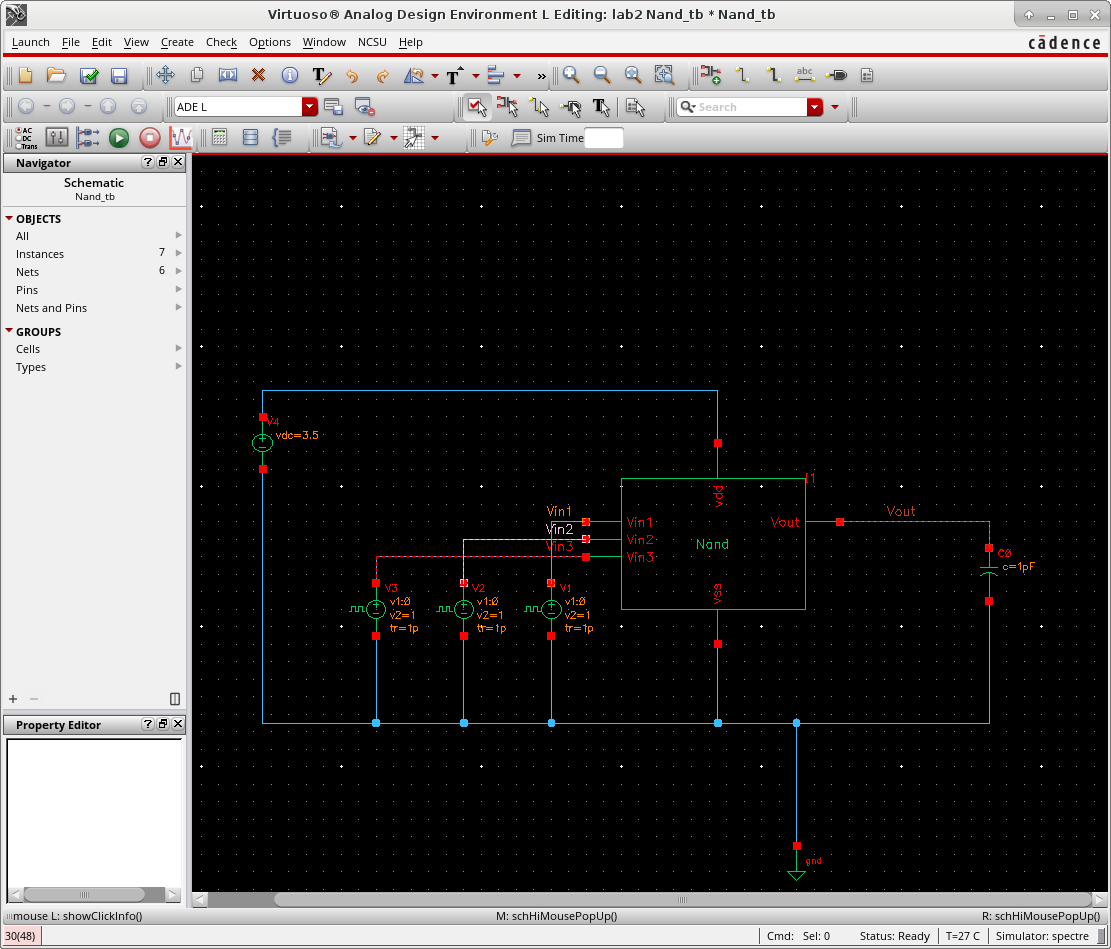
Create→ Cell view→ From Cell view

Then I gave it a name and pressed ok. (I will give you the option to change the design graphic if you want)

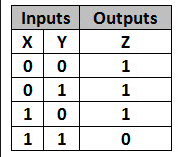


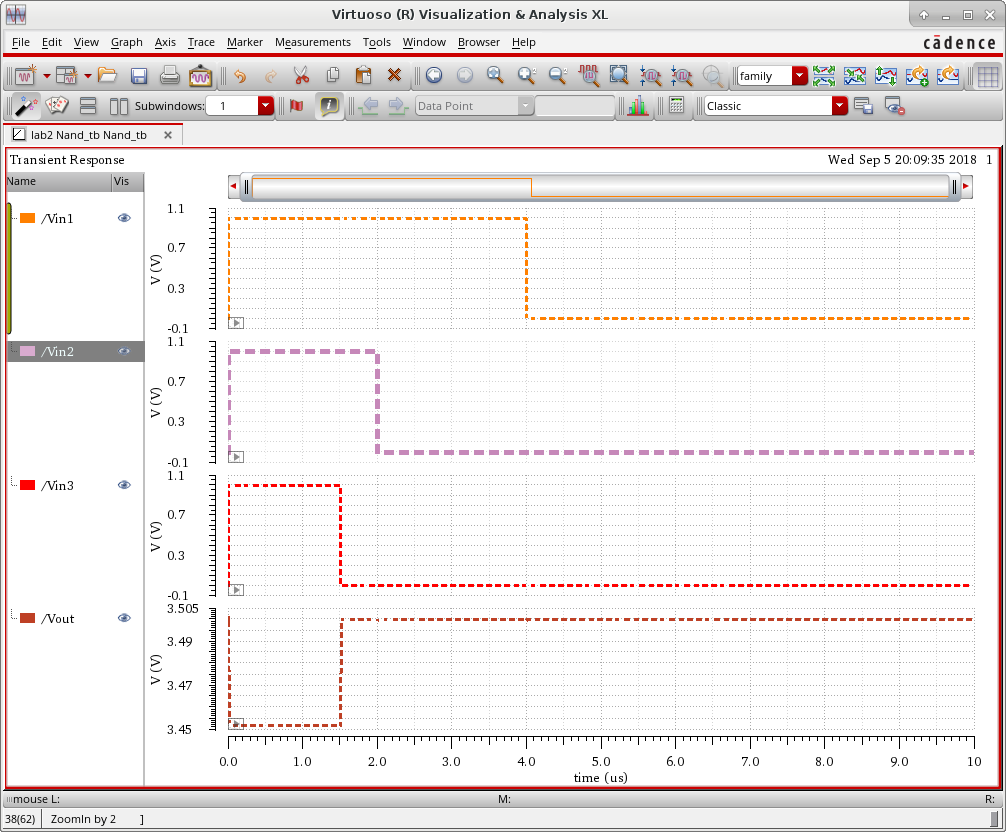
**Test bench analysis**

The last part consisted to create a test bench to test my NAND gate. Since this is a 3-input NAND gate I send 3 input in the different port of the NAND gate but with different time delay and also one 3.5V DC source to supply the VD of my NAND gate. So I can have the different combination possible of inputs. Below are the test bench schematic and the result plotted



**Test result**

For the parameters here, input at pin A period of 0u s, pin B with 0.5u s, pin C with 15u s. they all have the voltage going has the value between 0V - 1V and they all have risen time and fall time of 1p s. In this way, the input waveform looks exactly like the truth table below. Is used the nand gate trurh table on the right to verify my output. My output is 0 only when my 3 inputs are 1 which macth the table.



**Conclusion**

I’ve learned from this lab about how to perform DRC, LVS, extraction in Cadence to evaluate. It a good way to check if my layout design matches all the design rules. The most important thing I took away is that I shouldn’t edit anything such as moving the PMOS and NMOS words away from on top of the design in the extracted file before running the LVS test. It will bring errors to the LVS test and I will not have much options of fixing it.