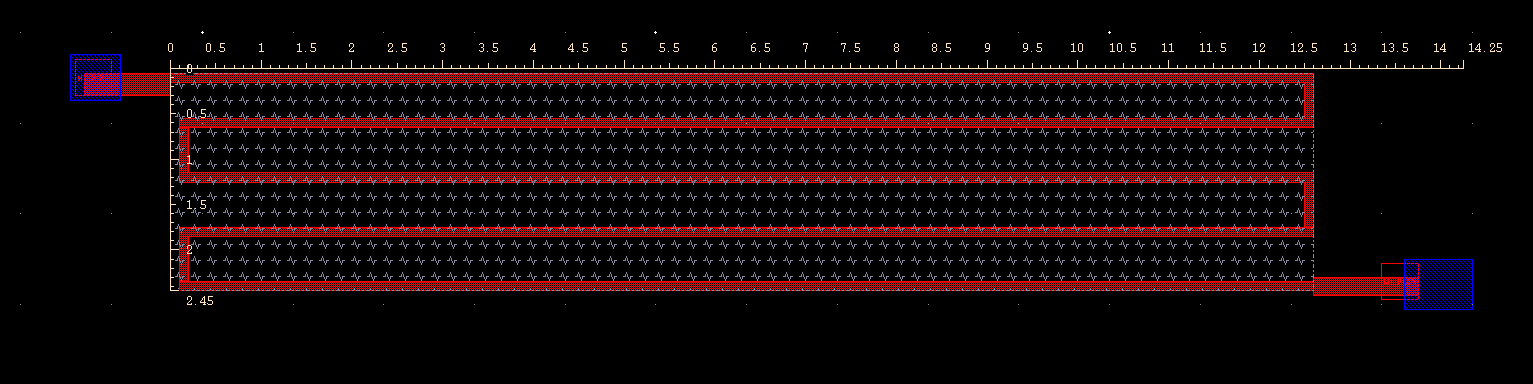
**Olouwole Eteka**

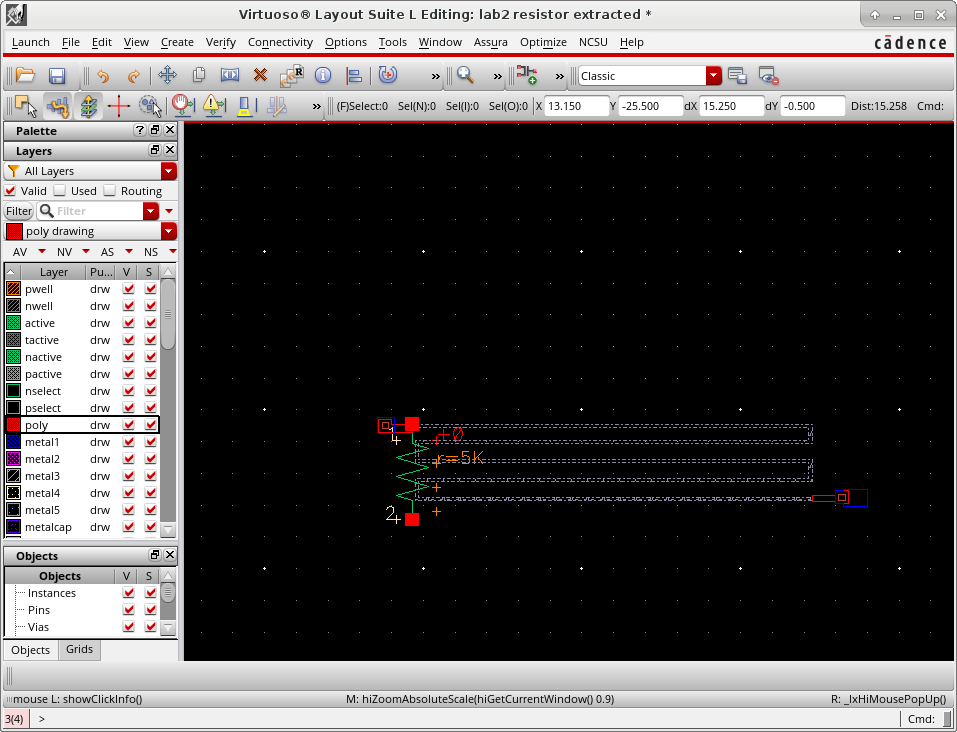
**lab report 5**

**introduction**

In this lab, we will be focusing on creating and designing the layout for resistors, diode, bonding pads, a pad protection circuitry. we will create the test bench to analyze the outcome graph of the circuit. We will also put our previous lab layout into a pad frame.

**Part 1**

The resistor layout above that I have created was using a poly layer. The importance of drawing a resistor’s layout is that we should always keep the terminals at the end of our design. This allows the current to flow through the longest path and therefore, increase the resistance. Besides, we should also not to forget using the “res\_id” cover to identify which part of the poly (or other layers) is a part of the resistor which is going to contribute on the resistance. The “res\_id” is not a physical layer that alters the fabrication process but instead, it’s just an identification layer.

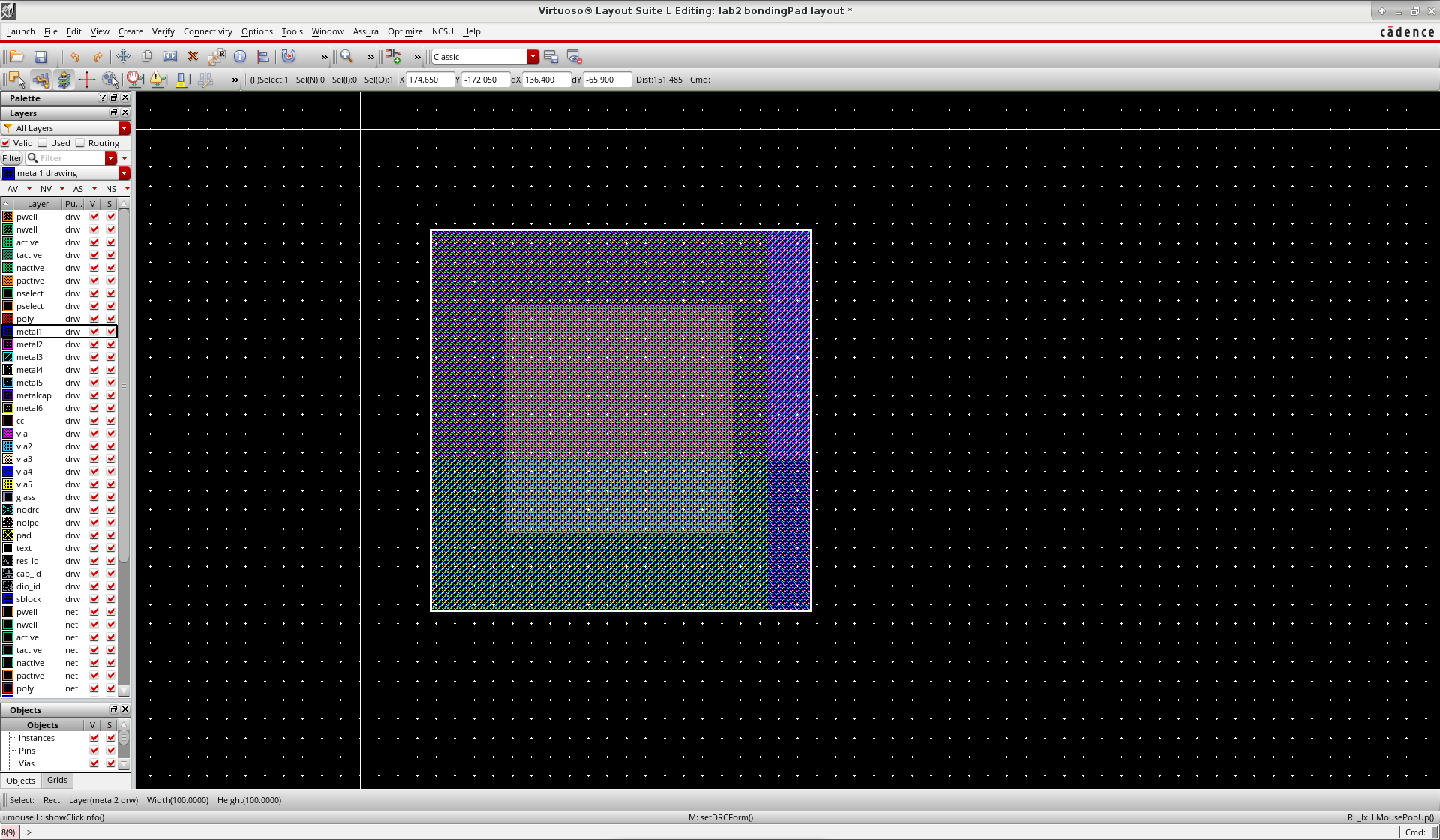


In this part of the lab, I was required to design a 5kOhm resistor. The images above show the layout and the extracted view of the resistor that I've designed. I designed this layout by implementing the U shaped method which creates two corners and an extra square at each turning of the lines. According to our theoretical calculations, a corner is equivalent as 0.55squares. Therefore, when doing the calculations, it’s important to take the total number of boxes and deduct by 0.45\*number of corners to get the actual number of squares that are going to contribute on the resistance. And we can then multiply the # of squares by the sheet resistance

**Part 2: Bonding Pads**

The bonding pad created above consists of all layers of Metal1-6 which metal 6 is at the top layer. They are all connected by using the Stacked Vias (Create->Vias->Choose Stacked Vias). I first started drawing by using the ruler to mark 60um x 60um space and the use the “rectangular” feature (Shortcut ‘R’) and specify the size to 60um x 60um because I want to make sure the opening of glass layer pass the requirement but not making the size of the bonding pad too big. made sure all my metal layers are at least 6um bigger than the part covered by the glass

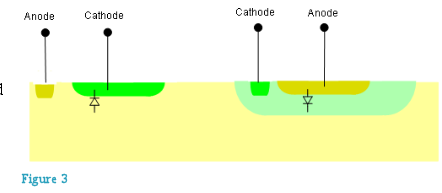
layers.

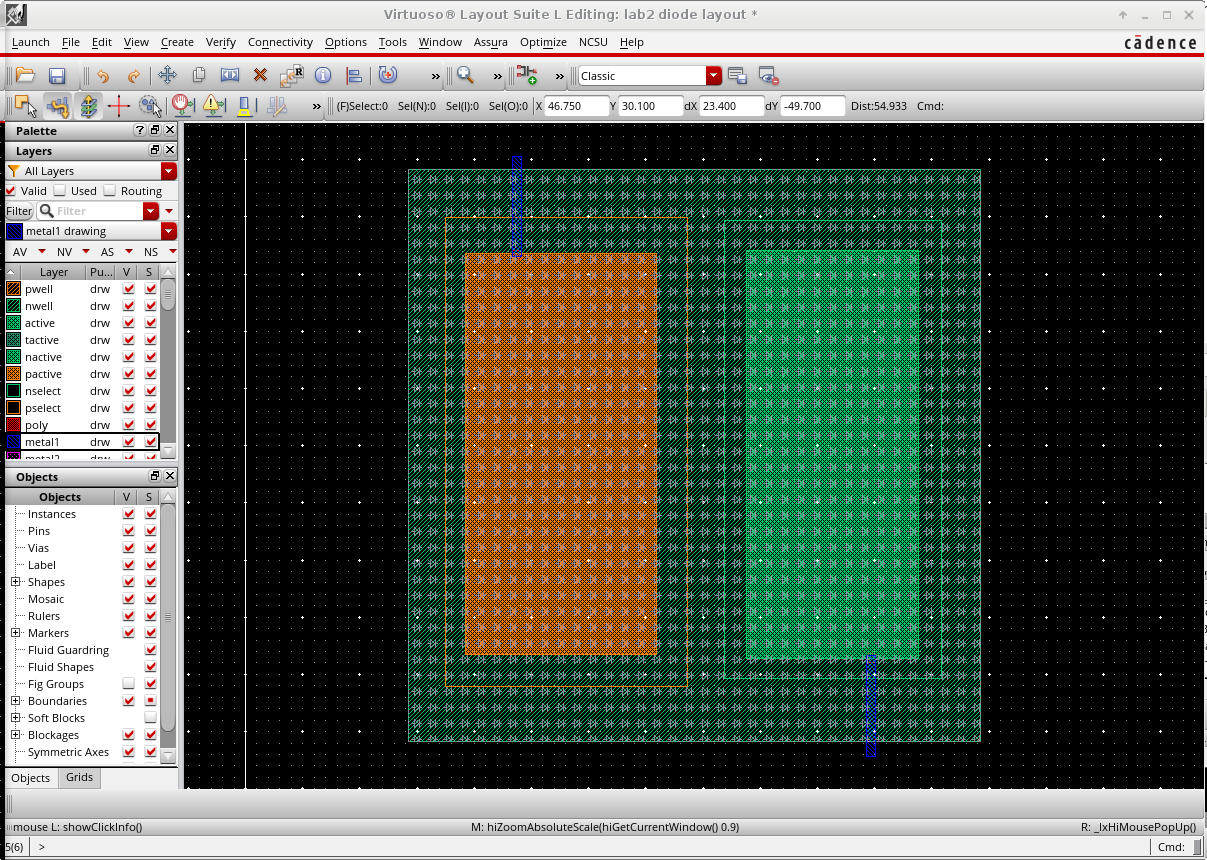


**Part 3: Layout of a diode**

The image shows the two different designs of the diodes. Left side is an n+ diffusion in the substrate and the right side is a p+ diffusion in an n-well. Very similar to creating a resistor, in

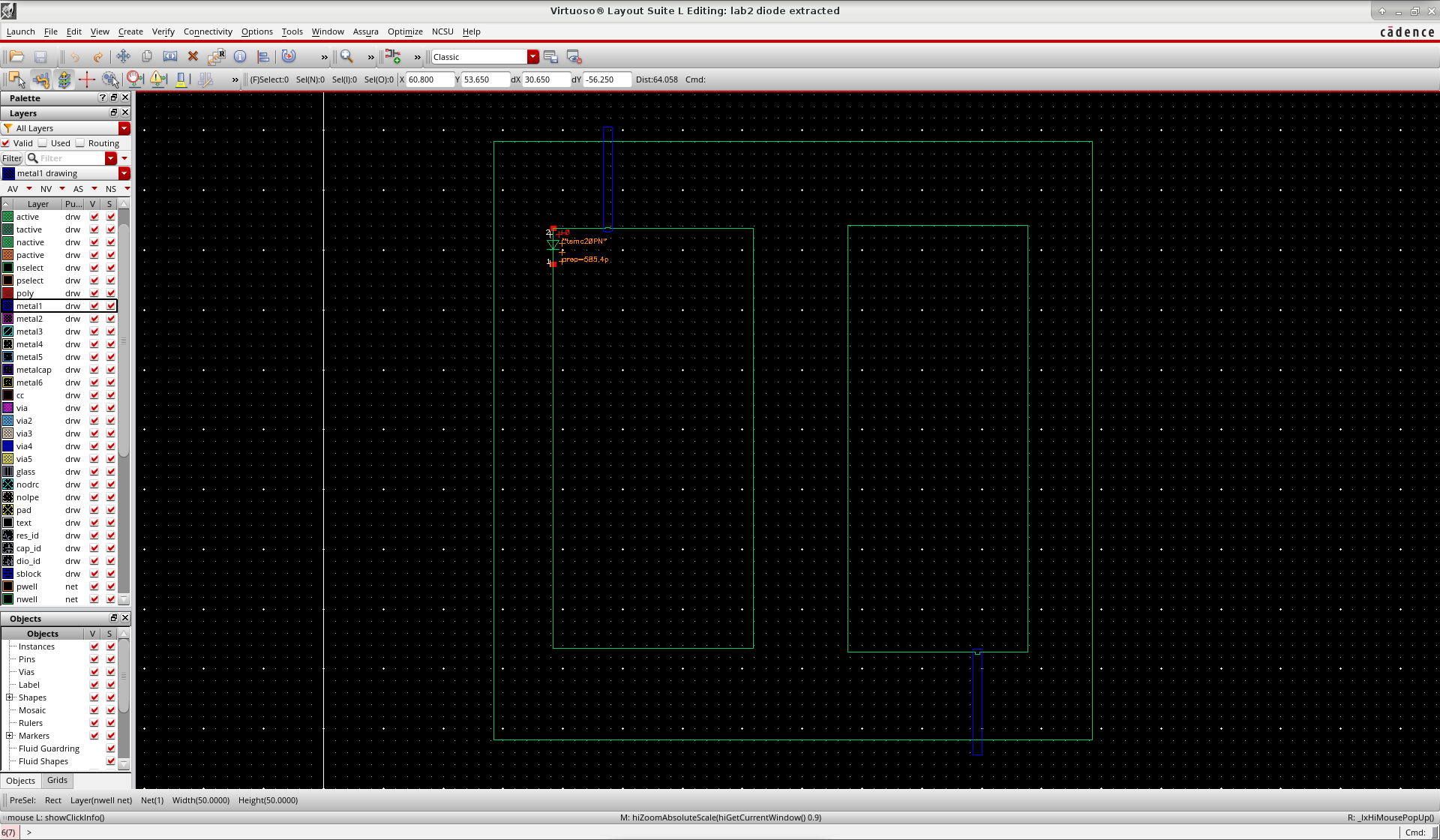
Cadence, we need to let the program know that we are creating a diode by using an identification layer. Therefore, we need to completely cover the diode that we design using the layer “duo\_id” so that it can be recognized as a diode during the extraction.



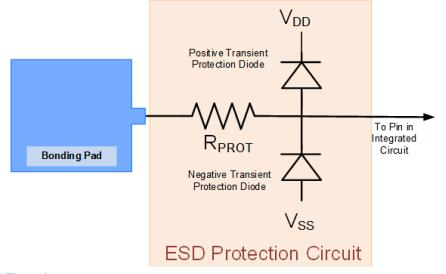


The figure above shown a layout of diode that I've designed for this lab which is using the method of p+ diffusion on the n-well layer. The requirement of this diode is to be at least half the size of my bonding pad, which is a quarter of its area. Therefore, I created a diode that is about 30um x 30um big. And since the larger the diffusion area, the more efficient the diode, I made the diffusion areas as big as possible to increase its efficiency.

Diode tested

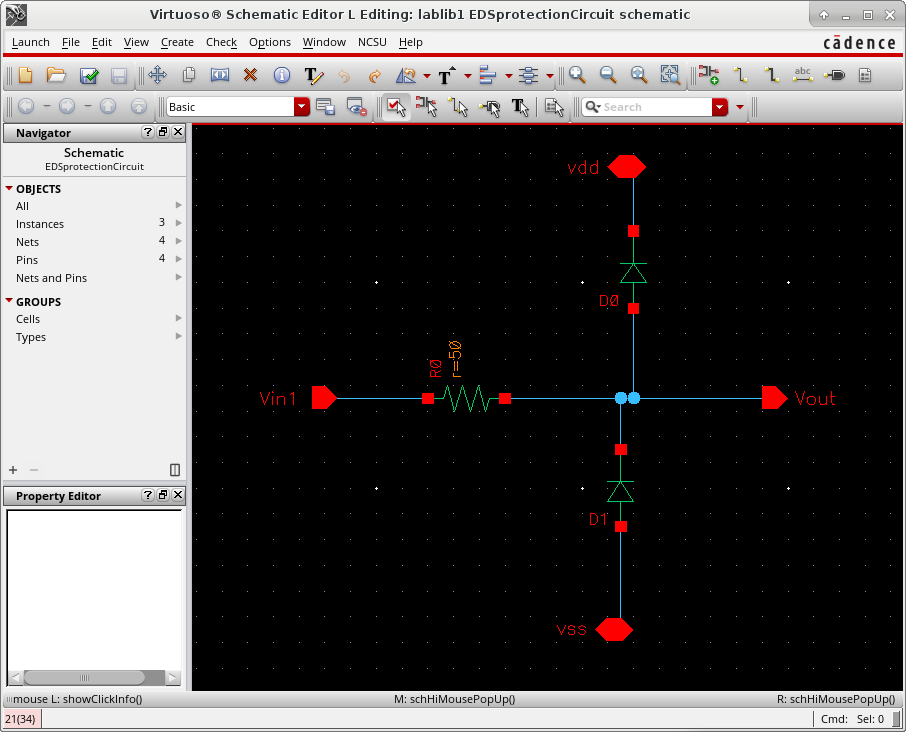


**Part 4: Pad Protection Circuitry**



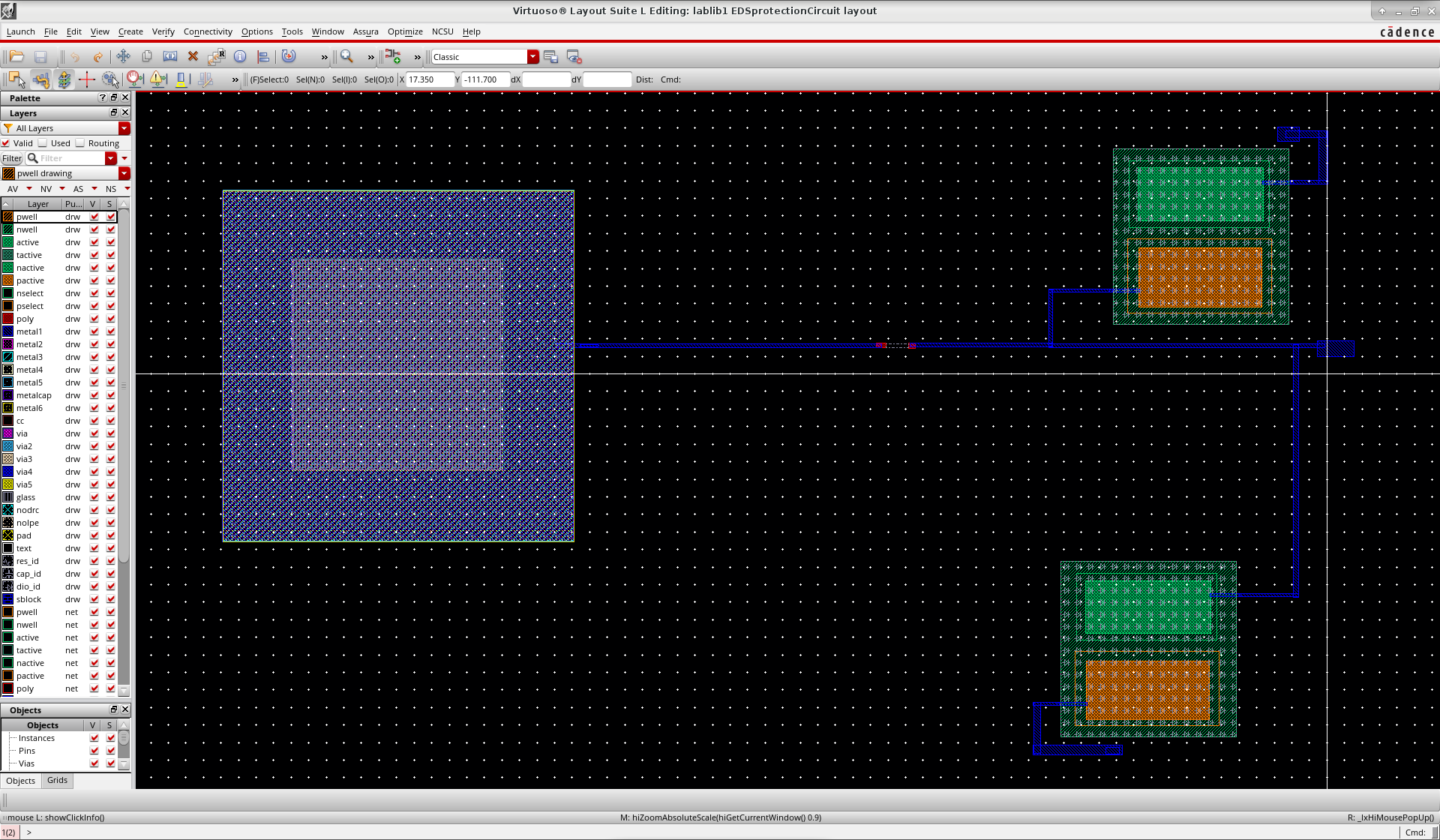
This image shows an example of ESD protection circuit that we are implementing in this lab. I followed the circuit on the right to design my schematic

below is the circuit design and the layout



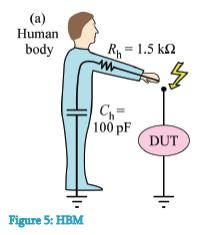
**Part 5: Layout of bonding pad with protection circuit**

In this part, I created a layout of bonding pad with ESD protection, similarly with the schematic created earlier but the layout version. The layout showing bellow.



After creating the layout, and made sure there’s not DRC error. I extracted the layout design and ran the LVS test with the schematic design file. It passed the LVS test as expected, which means it’s working correctly as desired just like the schematic design.

**Part 5.1 Human Body Model**



In this part of the lab I am going to create the test bench for the schematic I created earlier. I followed the image on the right provided by the lab to design it. It also provides me with the values of the component to use

Since the computer doesn’t have a model for diodes, we are required to create a diode model that tells the software how to model the diode in the schematic. In order to do that we follow the steps:

1. Go to terminal and directing to folder containing my diode

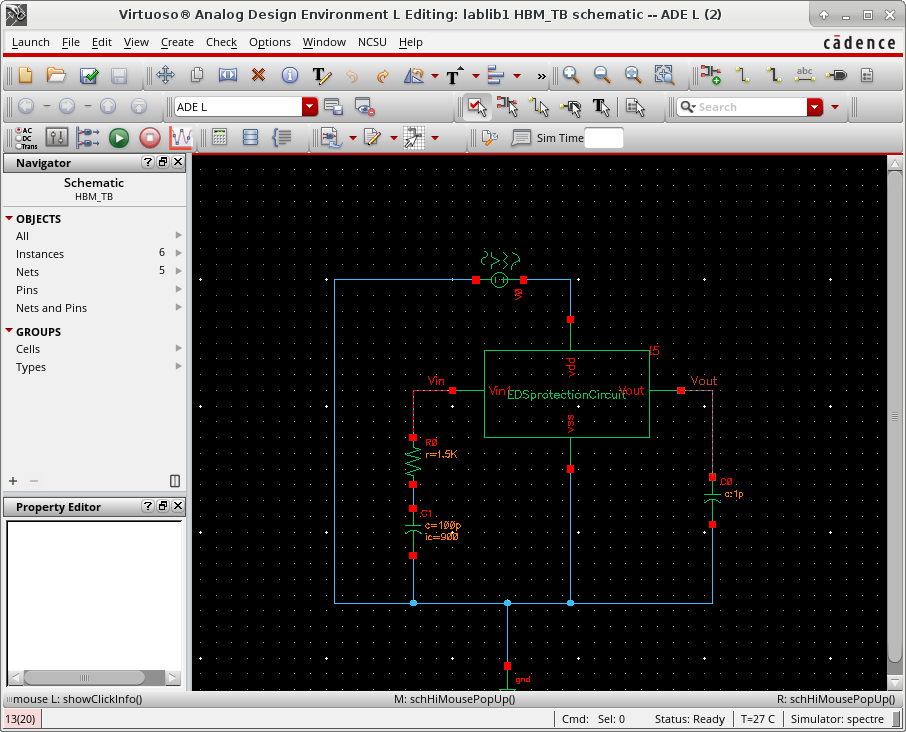
(cd ~/ee330/lablib1/lab5\_diode)

2. Create a text file called diode.scs

(gedit diode.scs)

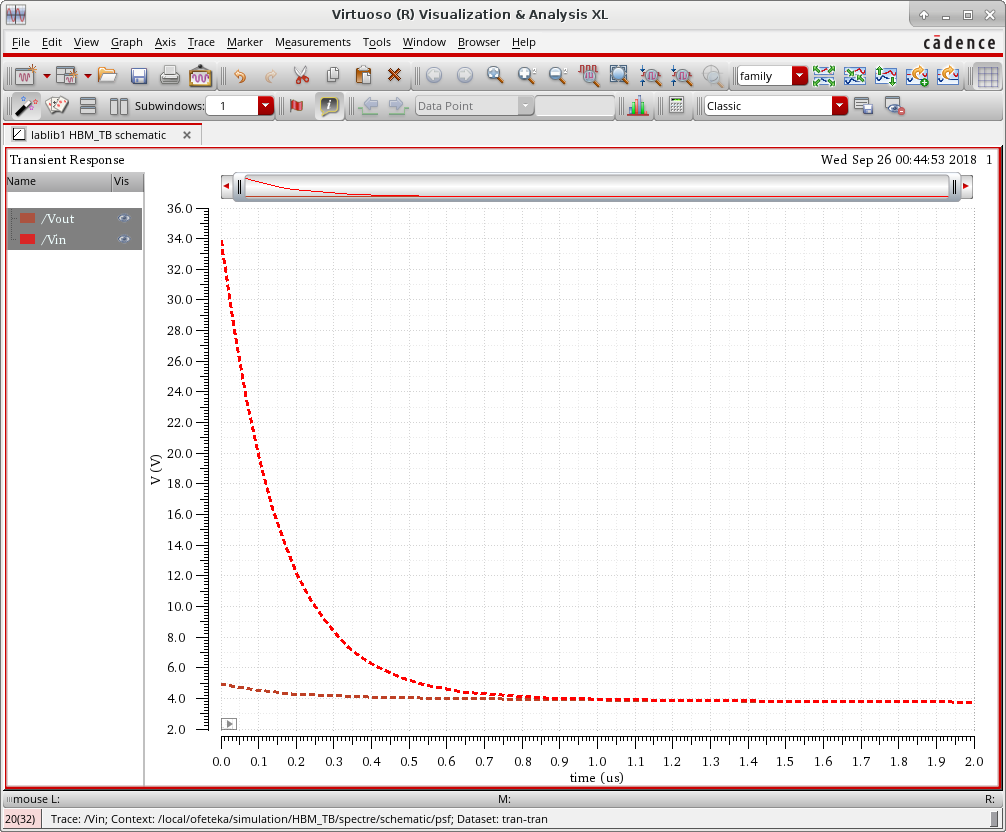
3. Include the text provided in the lab in the text file:

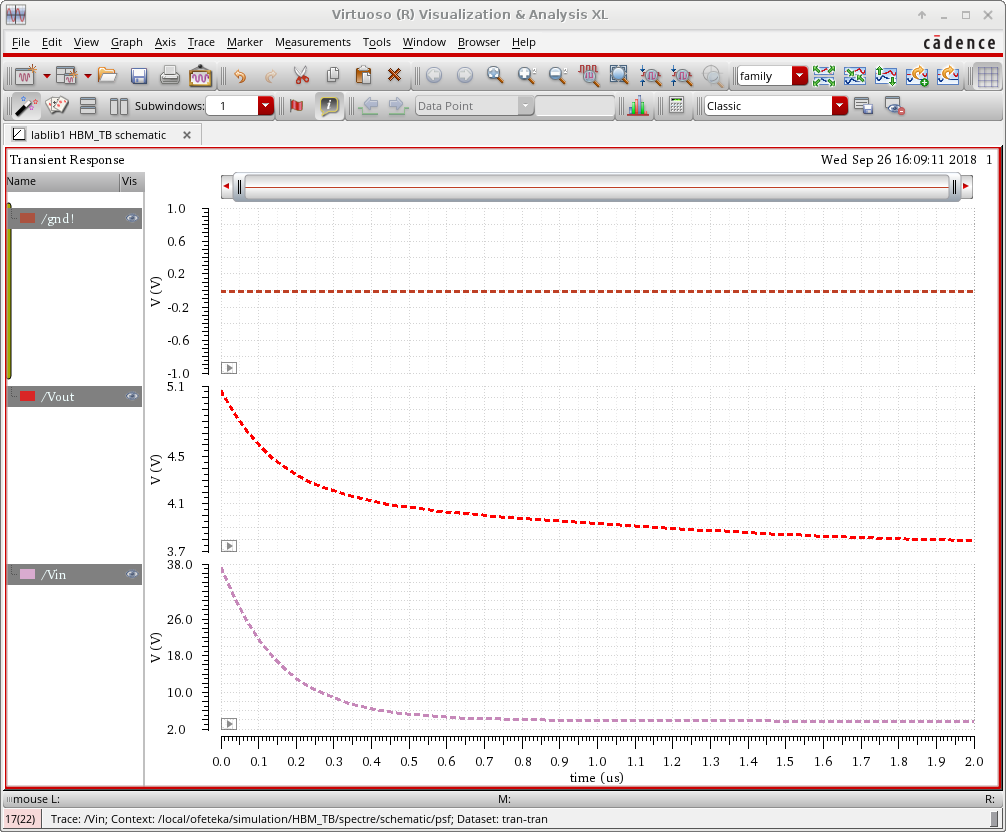
**the test bench circuit showing bellow**

****

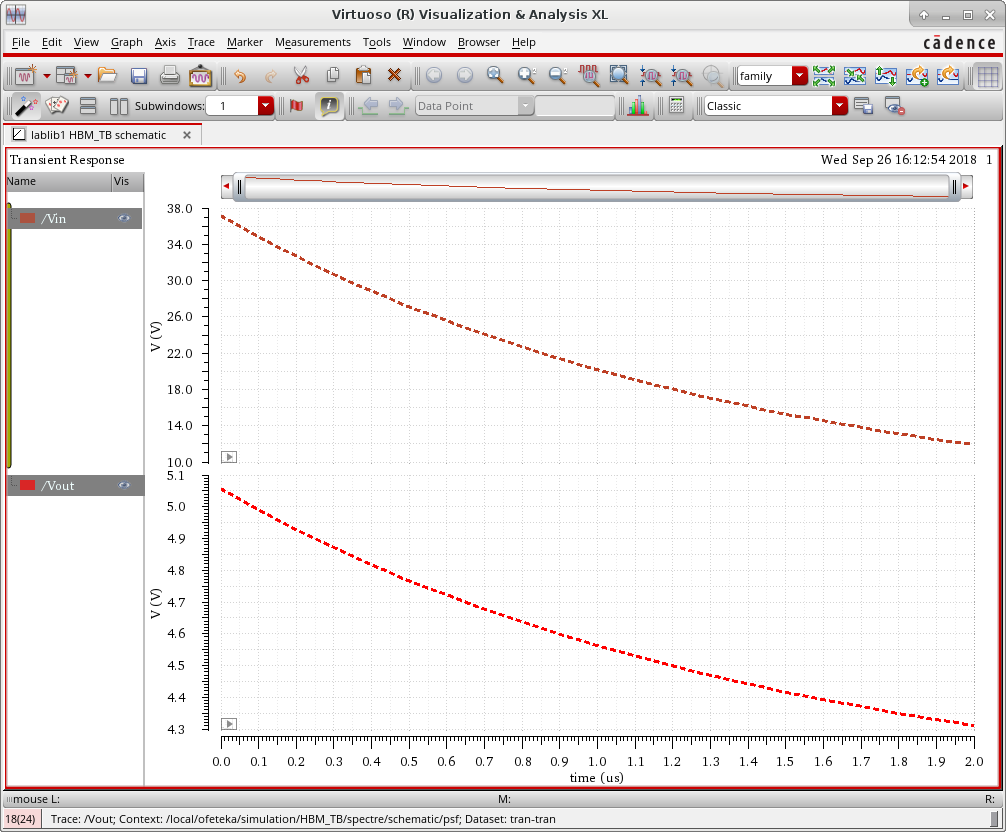
**stimulation showing bellow**

when I set the initial voltage at 900V





When I set the initial voltage at 1000V



In the figures shown above, we can see that the peak voltage of the output doesn’t pass 5V, which is around 4.9611V when the initial condition of the capacitor is set to 900V. While the peak of the output voltage went up to 5.6V when I set the initial condition to 1000V.

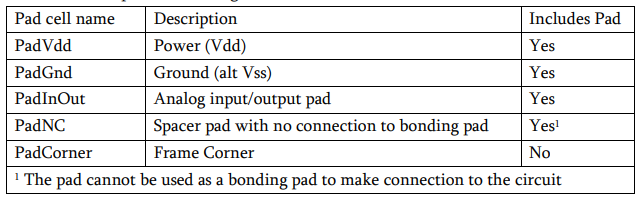
Based on Table 5.1, the device was able to withstand a voltage within a range of 500~1000V but not as high as 1000V~2000V, therefore the device can be graded as class 1B.

**Part 6: Pad Frames**

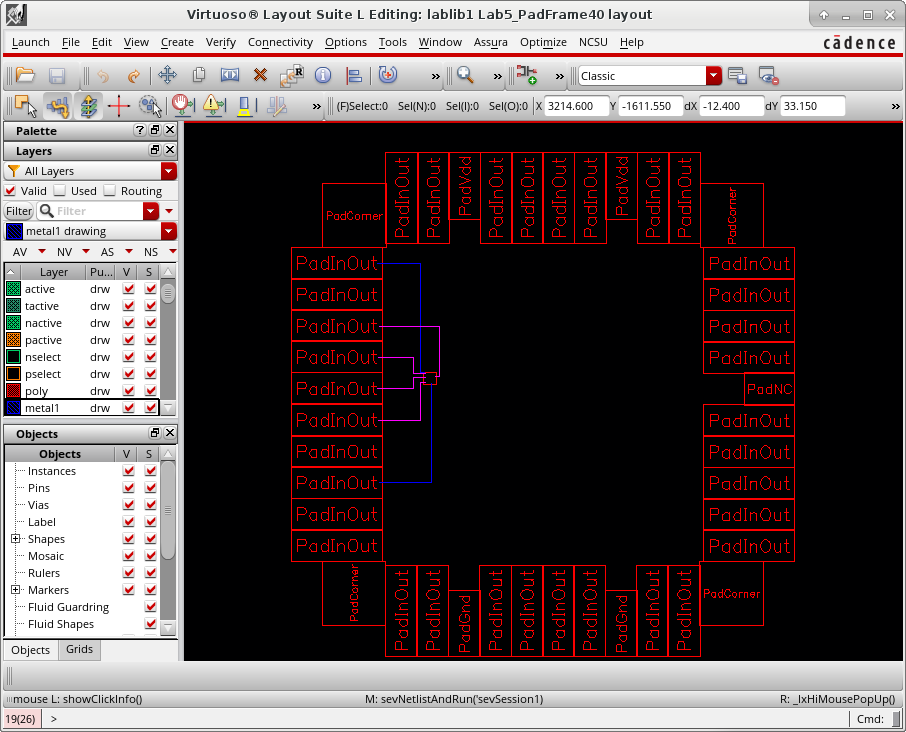
to create the pad frame I followed the procedure bellow Downloading and extracting the pad frame provided in the course Save the file. Create a pad frame based on template Copy the original “PadFrame40” cell in the “ISU\_PadFrames\_tsmc02” library to the “lablib1” library and changing the name to “Lab5\_PadFrame40”. Add the Boolean function from Lab4 and connect them to respective pads.

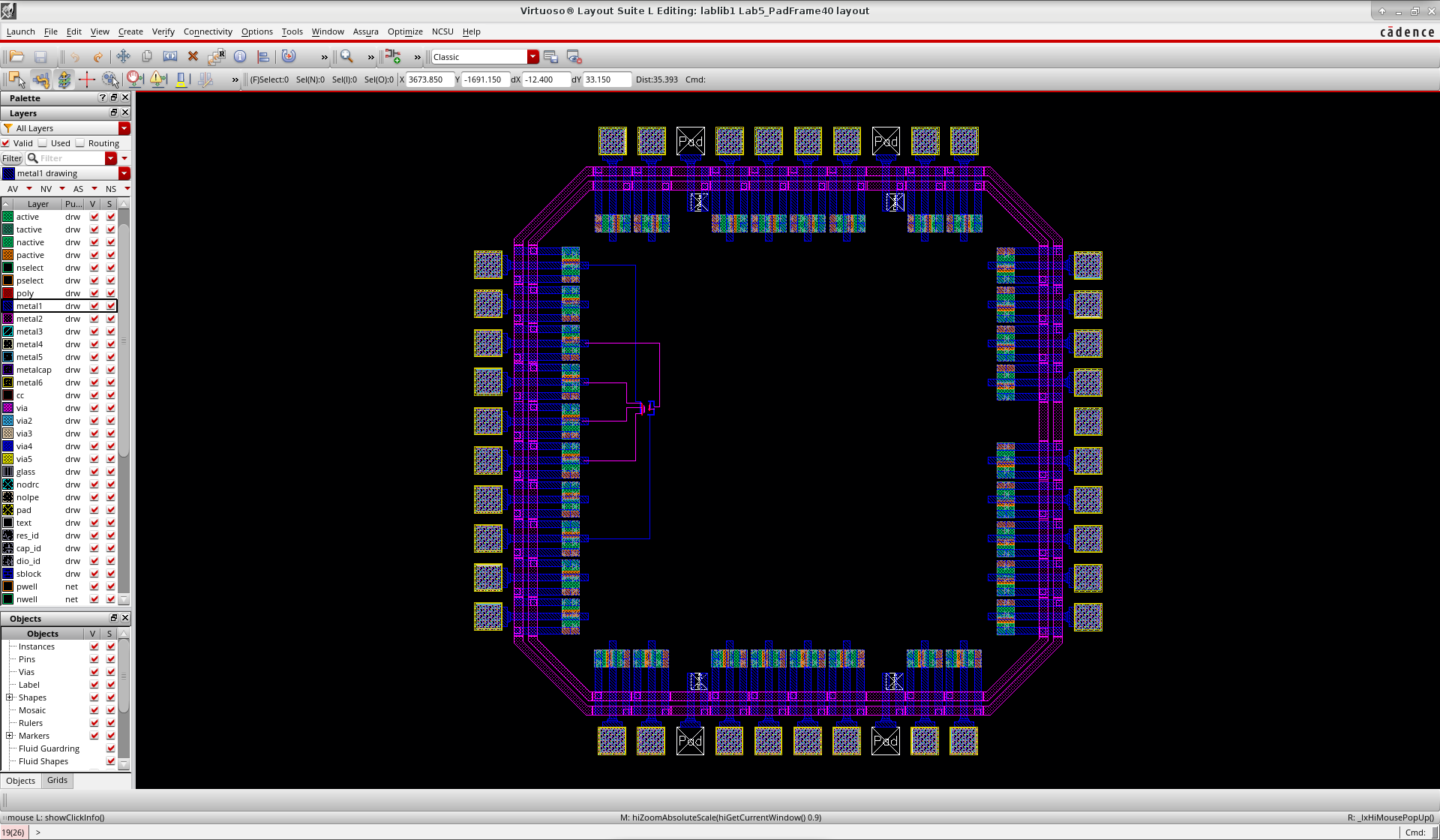
Then, I’ve edited the template file based on what was given to its corresponding pads using the

table:



the layout of the pad frame showing bellow





**Conclusion**:

I’ve learned a lot from this lab about implementing resistors, diodes, and even a bonding pads in CMOS design. Then, also how to put them together to create a working design. Also how to create a model of protection pad to protect the circuit from ESD.