

CprE 381: Computer Organization and Assembly Level Programming

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Administrative

- Lab 1 is this week!
- Textbook
 - Great reference
 - Support lecture
 - Won't include stuff not touched on in lecture
 - Homework problems
- HW0 posted (due next Wed Jan 23)
- HW policies:
 - Published ~1 week prior to due date
 - Due on Canvas as **typeset** pdf
 - Due just before Midnight (**11:59pm**) on due date
 - HW solutions automatically released after due date → no late assignments accepted
 - 12 HWs: HW0 + highest 6 of HW1-10 + HW11 counted
- OH: 321 Durham (3pm Wed, 1:30pm Friday) starting **today**

Review

- Processors everywhere
 - Processors generally look the same at high-level
 - Computer Architecture != Magic
-
- Relevant to all, even programmers

Concept Map In-Class Assessment

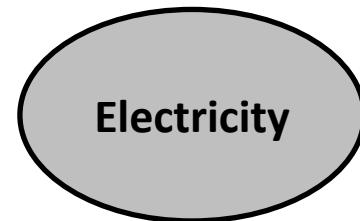
- Help you connect **new information** to your existing knowledge
- Deepen **understanding** and **comprehension**
- Important for this class:
 - Organize the relatively broad topics covered in lecture and homework
 - Help me understand how you are conceptualizing the content of the course
 - Will continue to use during exam reviews

Concept Map In-Class Assessment

1. Brainstorm concepts relating to main concept
2. Organize into categories
3. Draw arrows between related categories (and main concept)
 - Label the connections as well

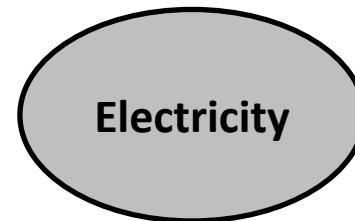
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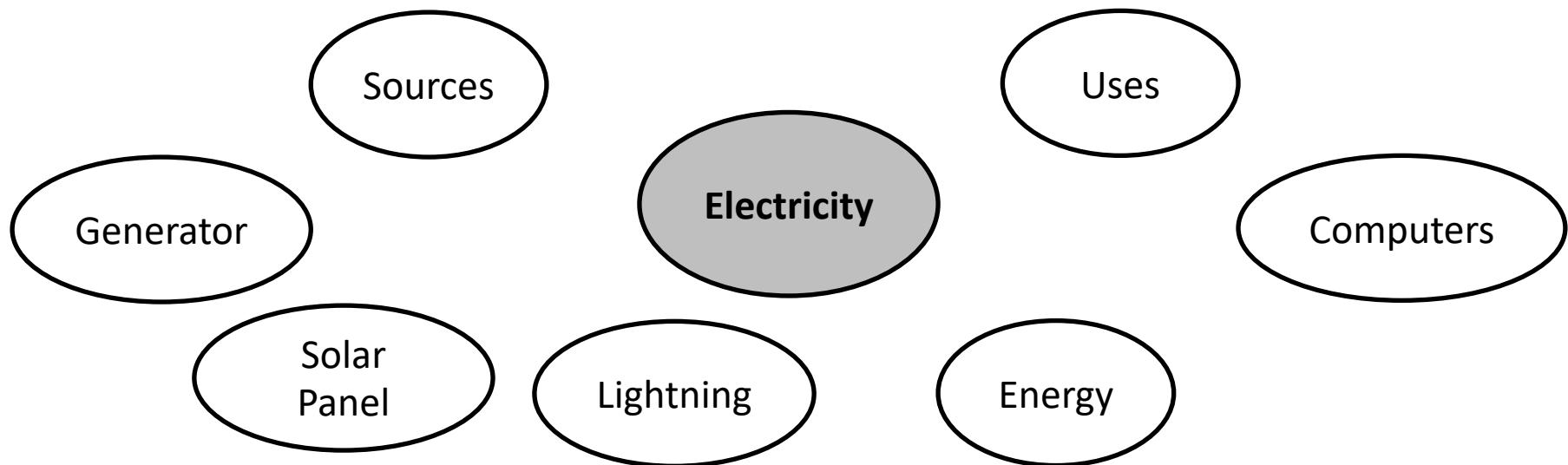
Concept Map In-Class Assessment

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 - Label the connections as well
 - Energy
 - Lightning
 - Generator
 - Solar panel
 - Power
 - Computers



Concept Map In-Class Assessment

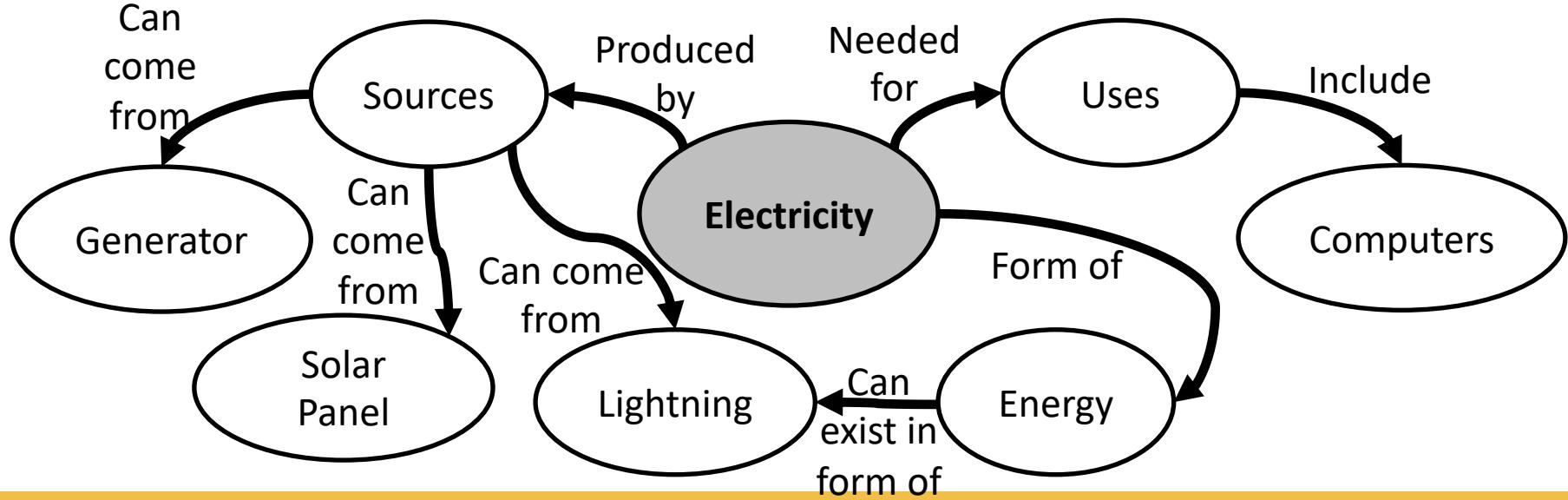
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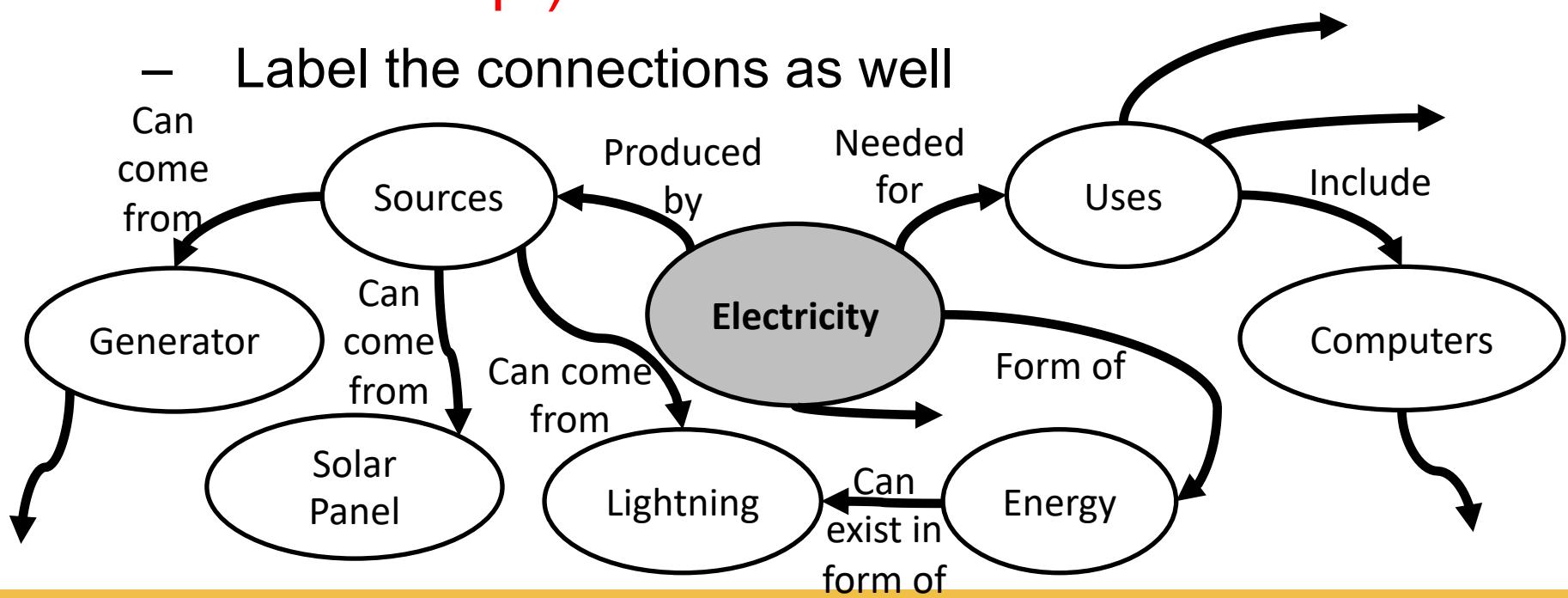
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Concept Map In-Class Assessment

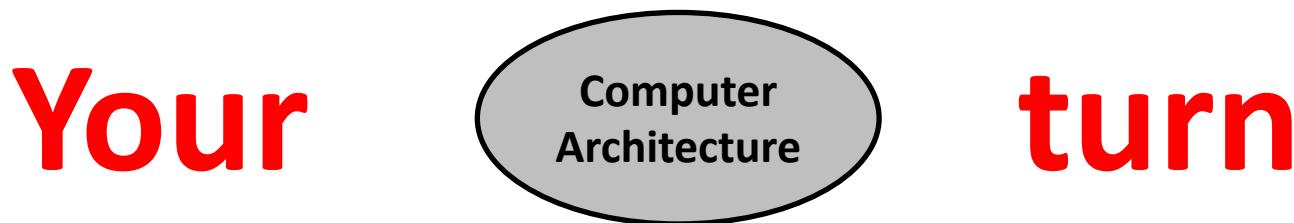
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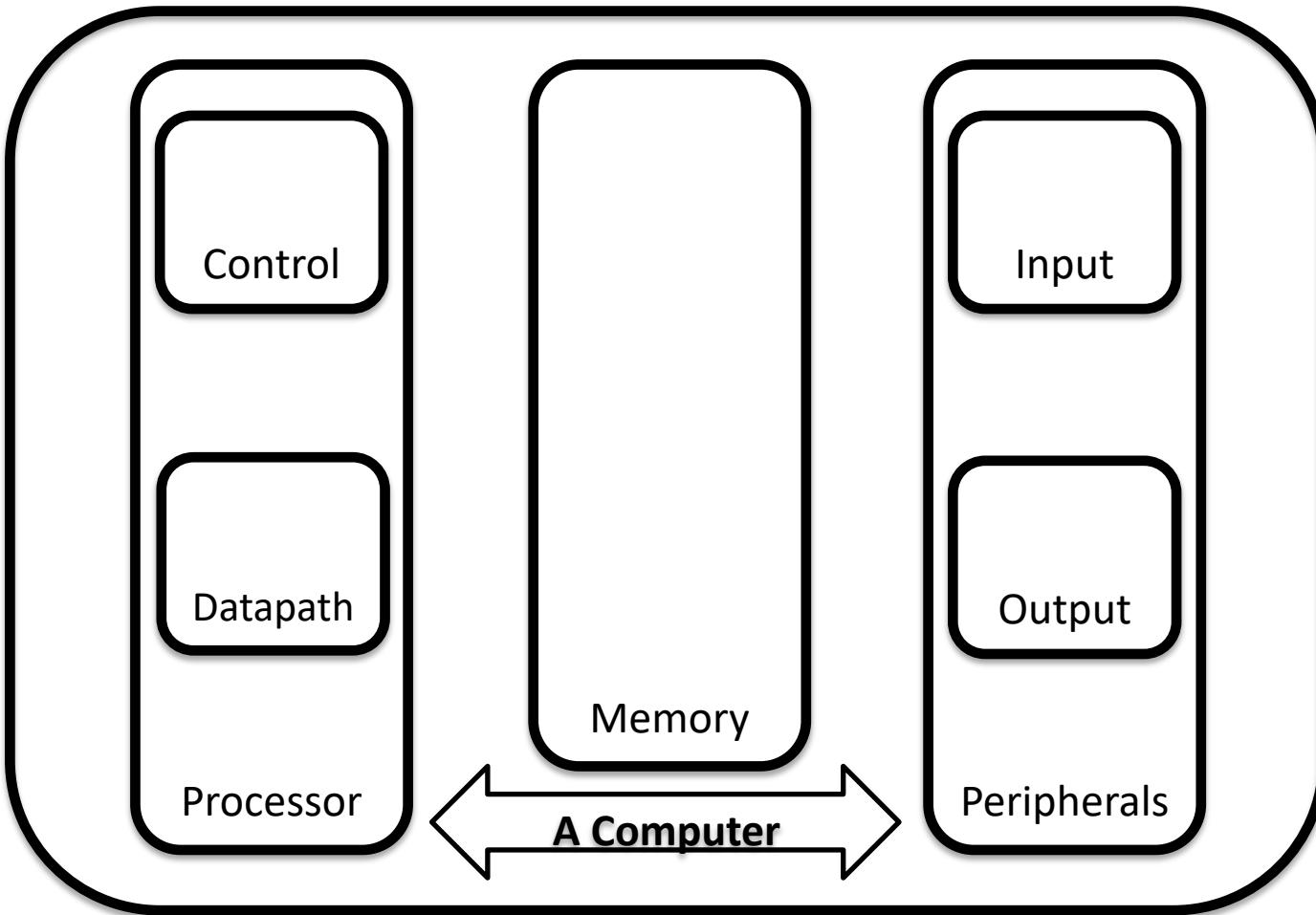


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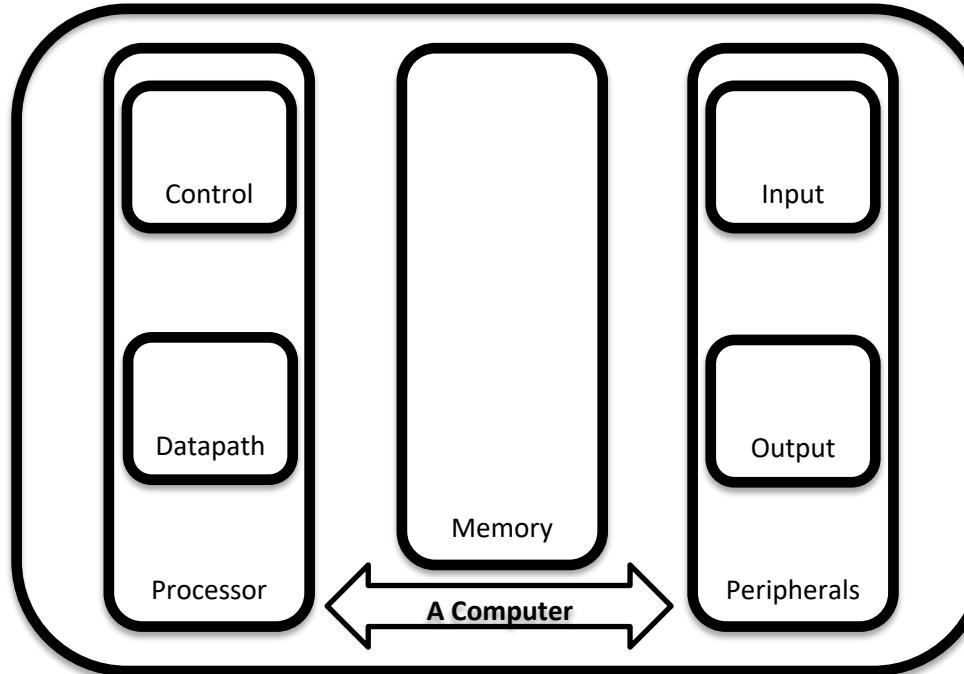


Computers



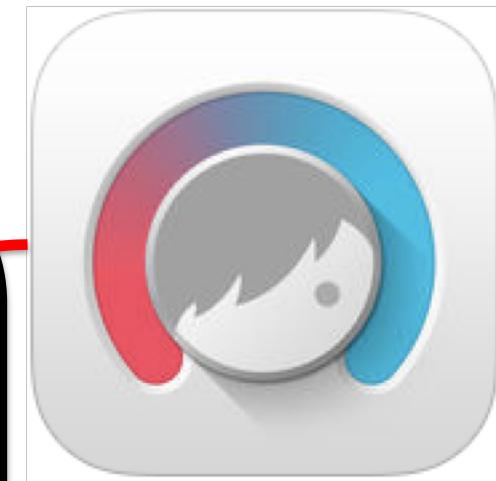
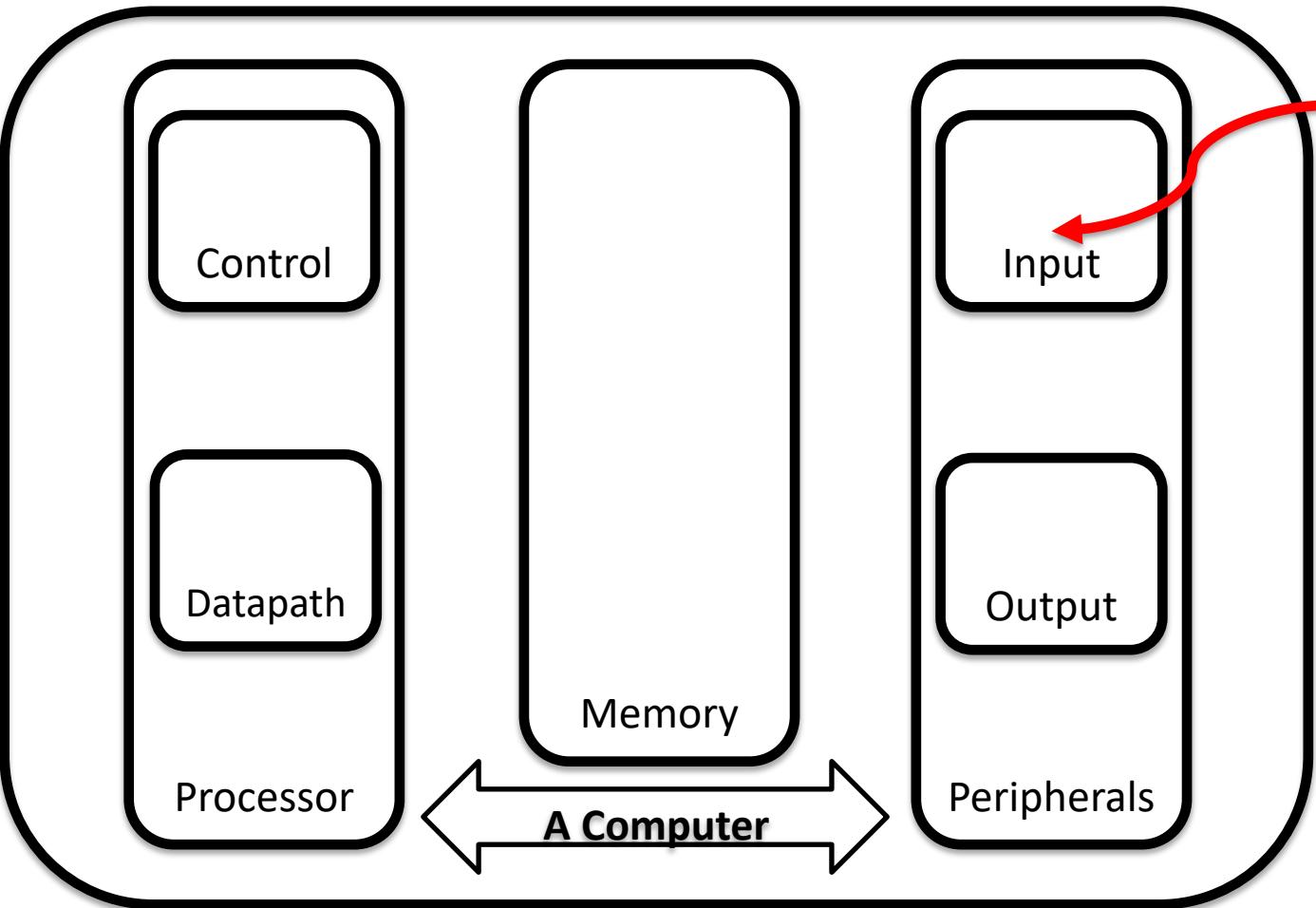
Stored Program Computers

- A la von Neumann Model / Architecture

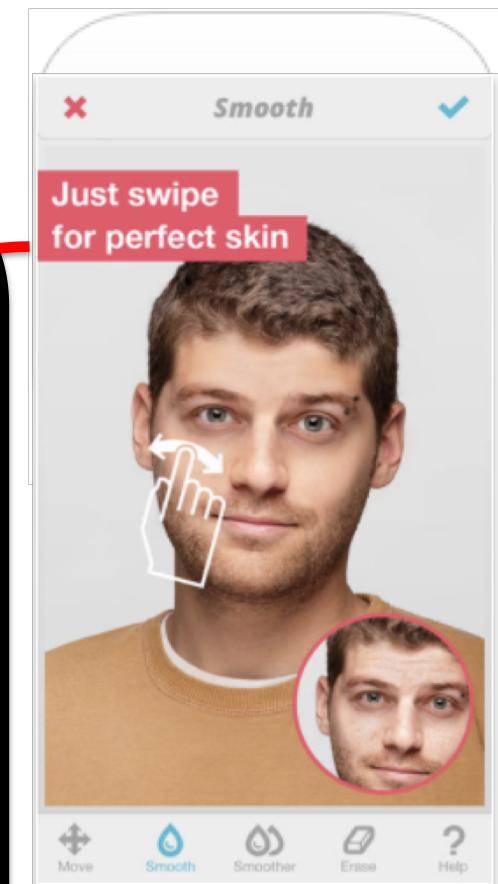
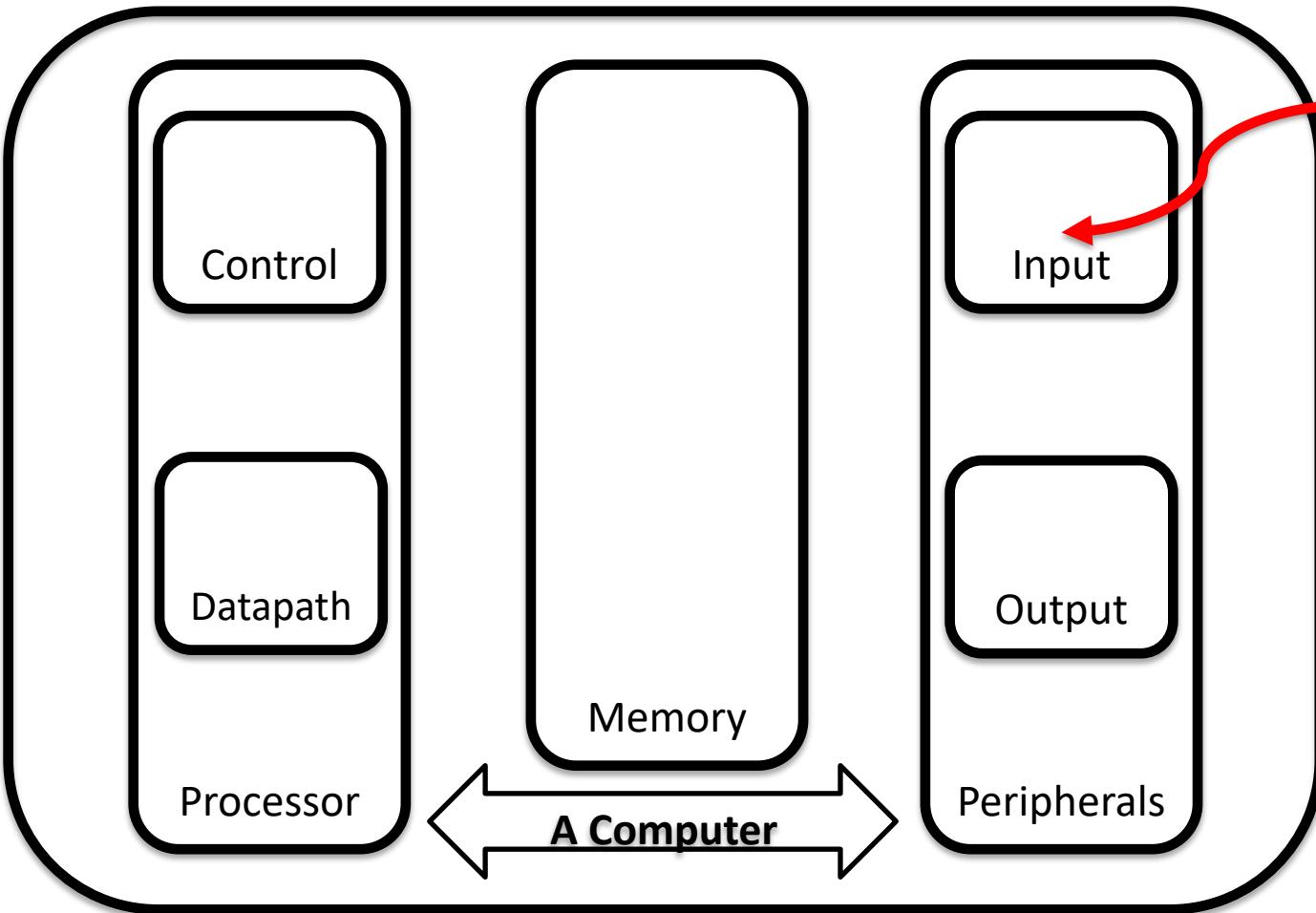


- Two key properties:
 - Instructions stored (as data) in a linear memory array
 - Sequential instruction processing

Input Device Inputs Object Code

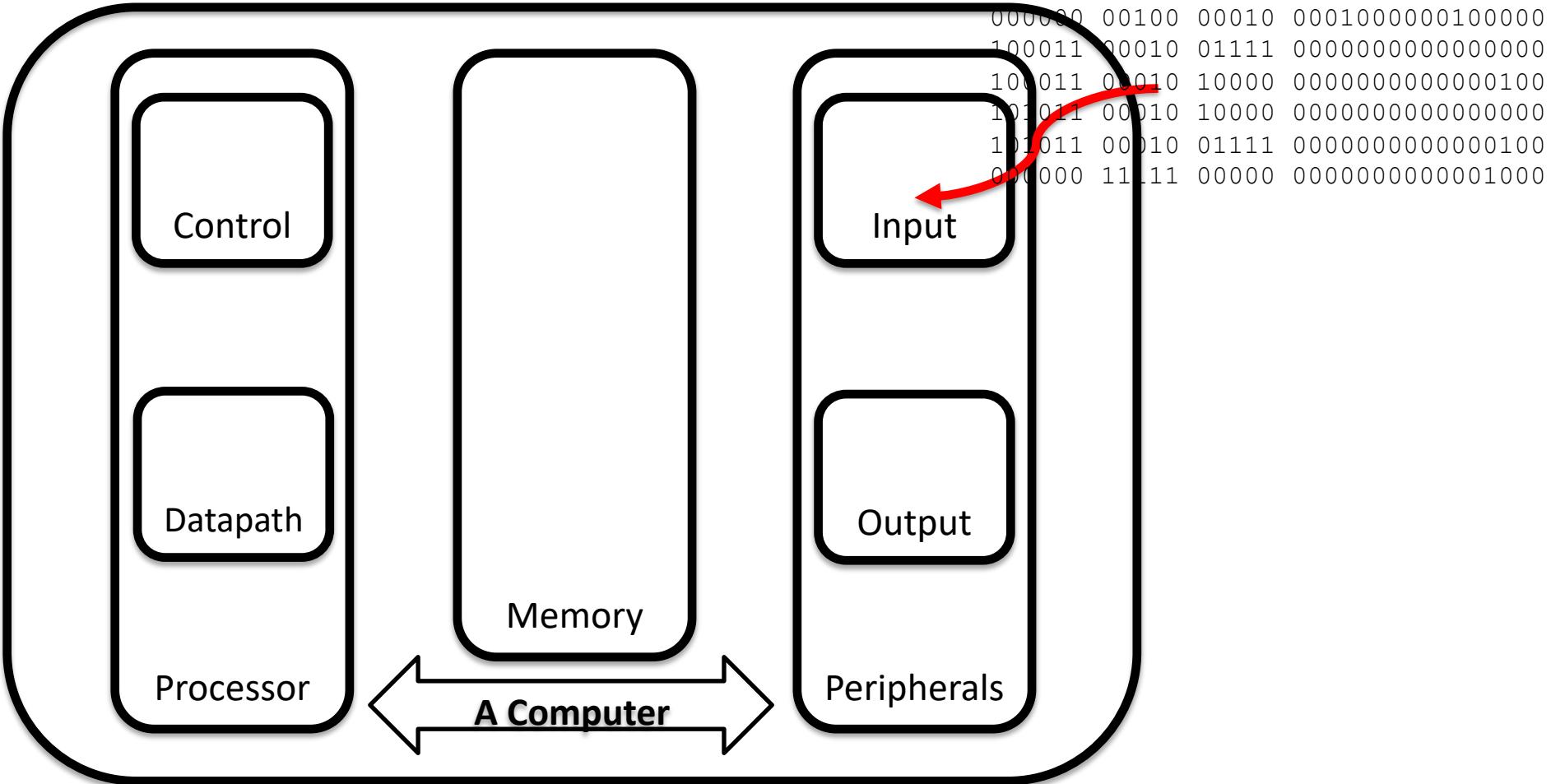


Input Device Inputs Object Code

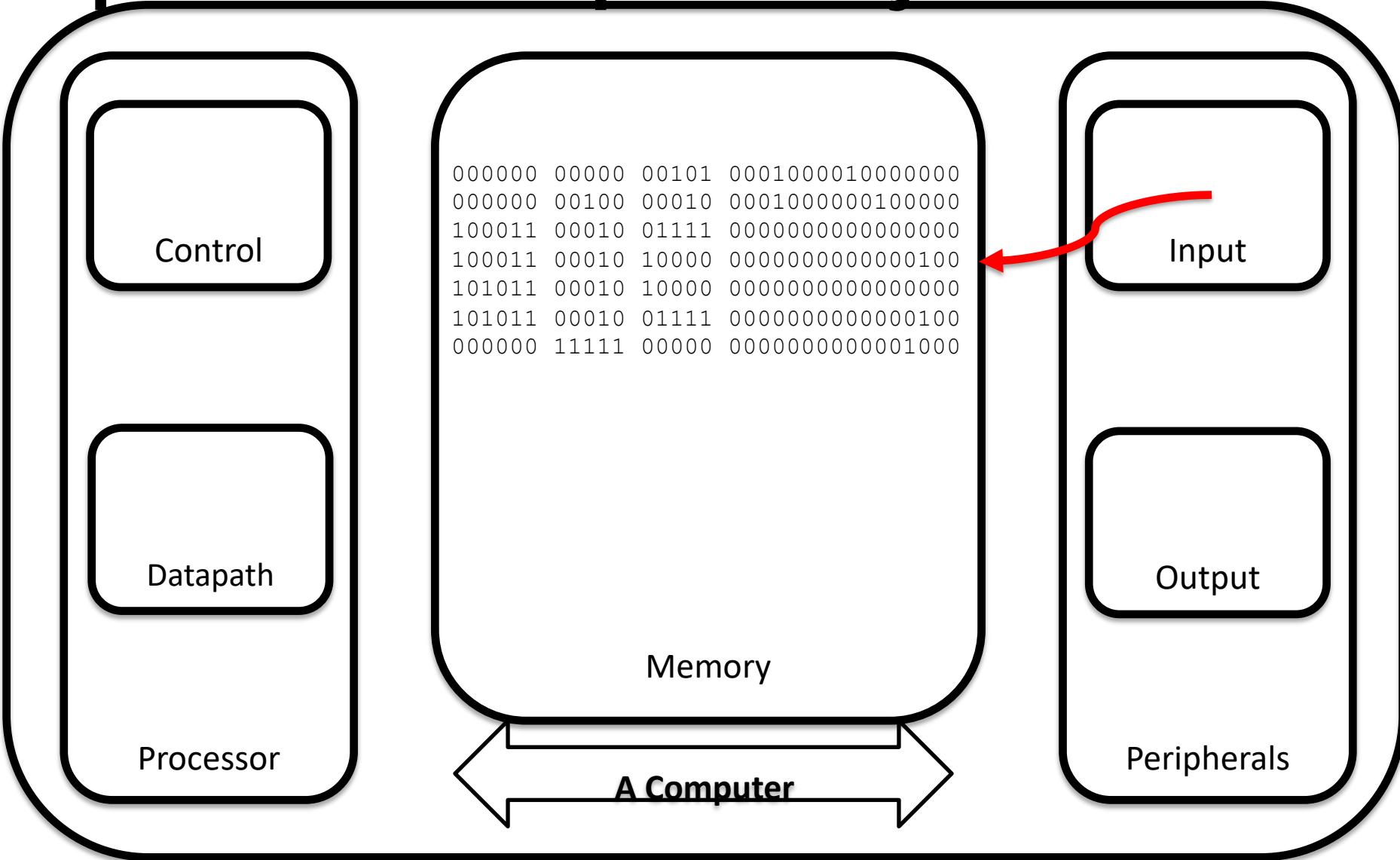


Most downloaded
paid app on iOS 2017

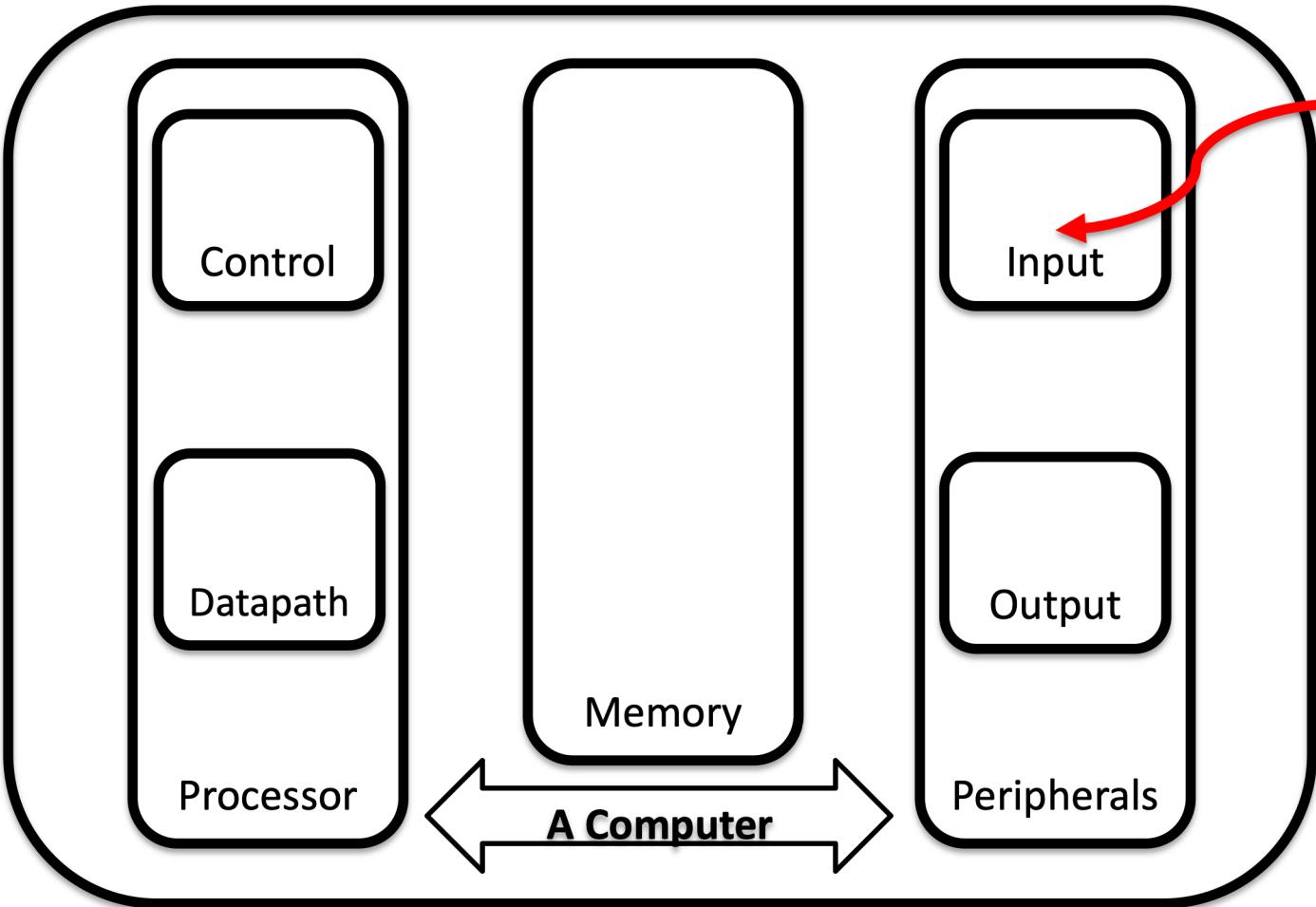
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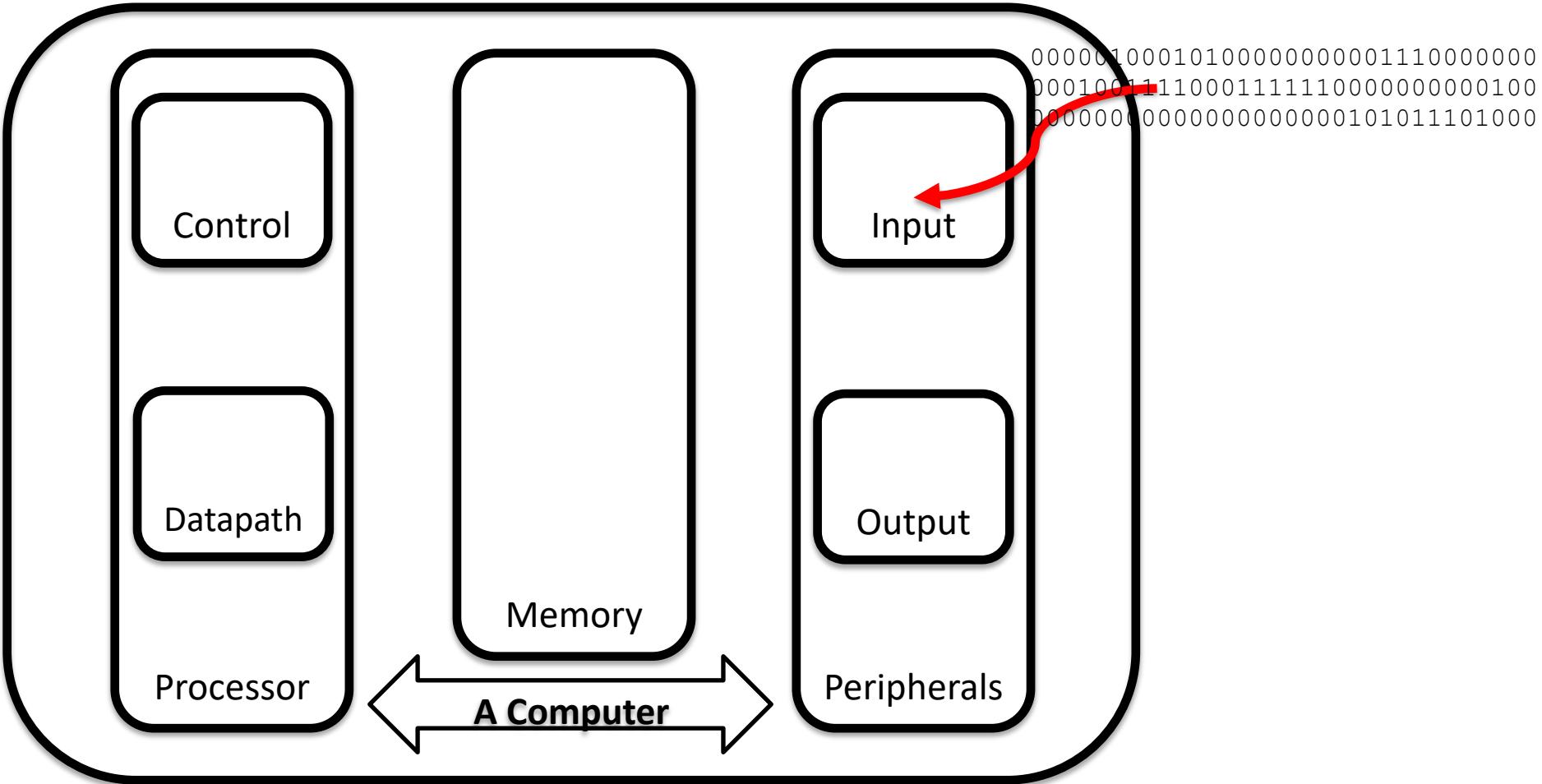
Input Device Inputs Object Code



Input Device Inputs Object Code



Input Device Inputs Object Code



Input Device Inputs Object Code

Control

Datapath

Processor

```
000000 00000 00101 0001000010000000  
000000 00100 00010 0001000000100000  
100011 00010 01111 0000000000000000  
100011 00010 10000 000000000000100  
101011 00010 10000 0000000000000000  
101011 00010 01111 000000000000100  
000000 11111 00000 00000000001000
```

```
0000010001010000000001110000000  
000100111000111110000000000100  
00000000000000000000000101011101000
```

Memory

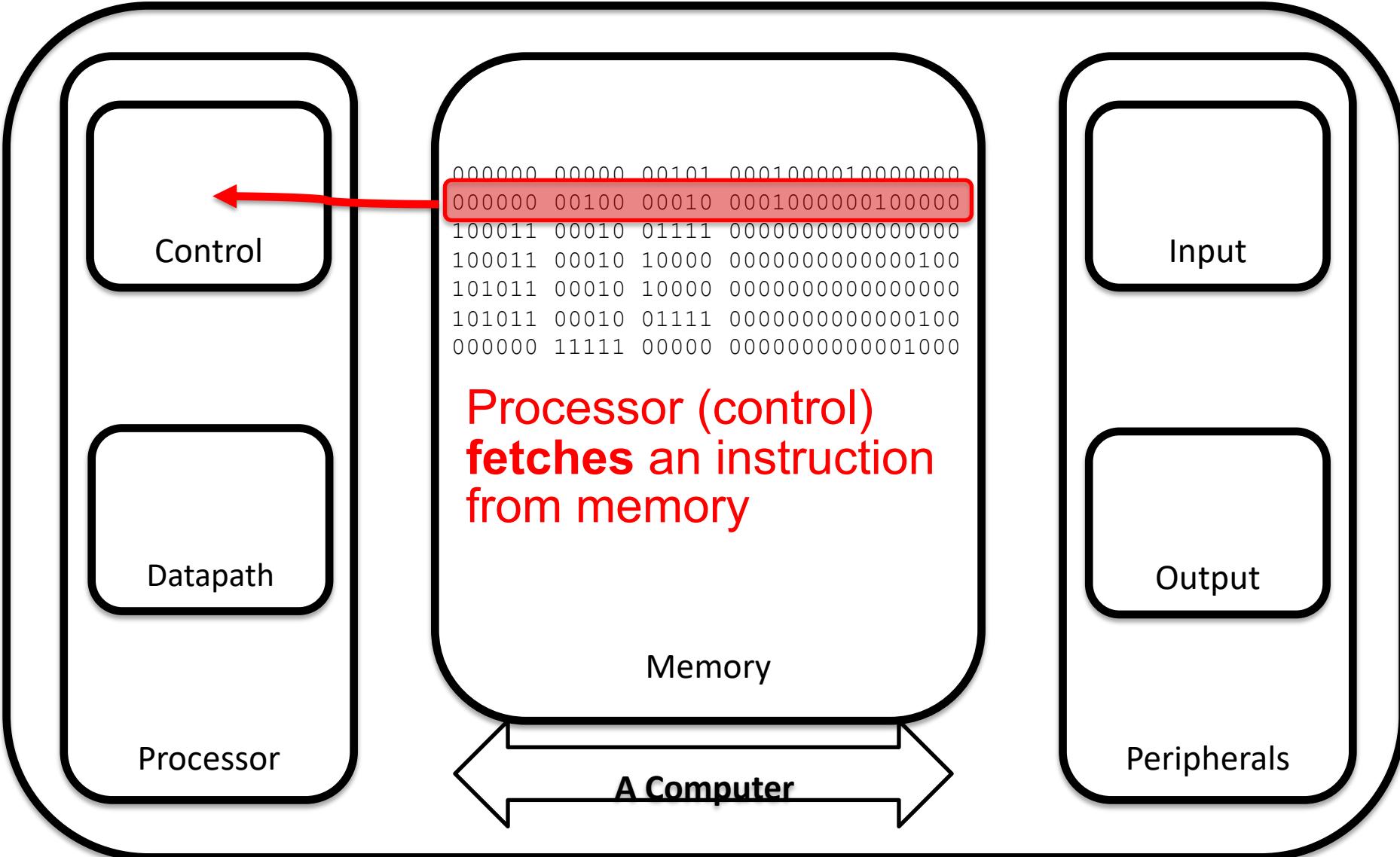
A Computer

Input

Output

Peripherals

Instruction Fetch



Control Decodes the Instruction

000000 00100 00010 000100000100000

Control

Control **decodes** the
instruction to determine
what to execute

Datapath

Processor

Memory

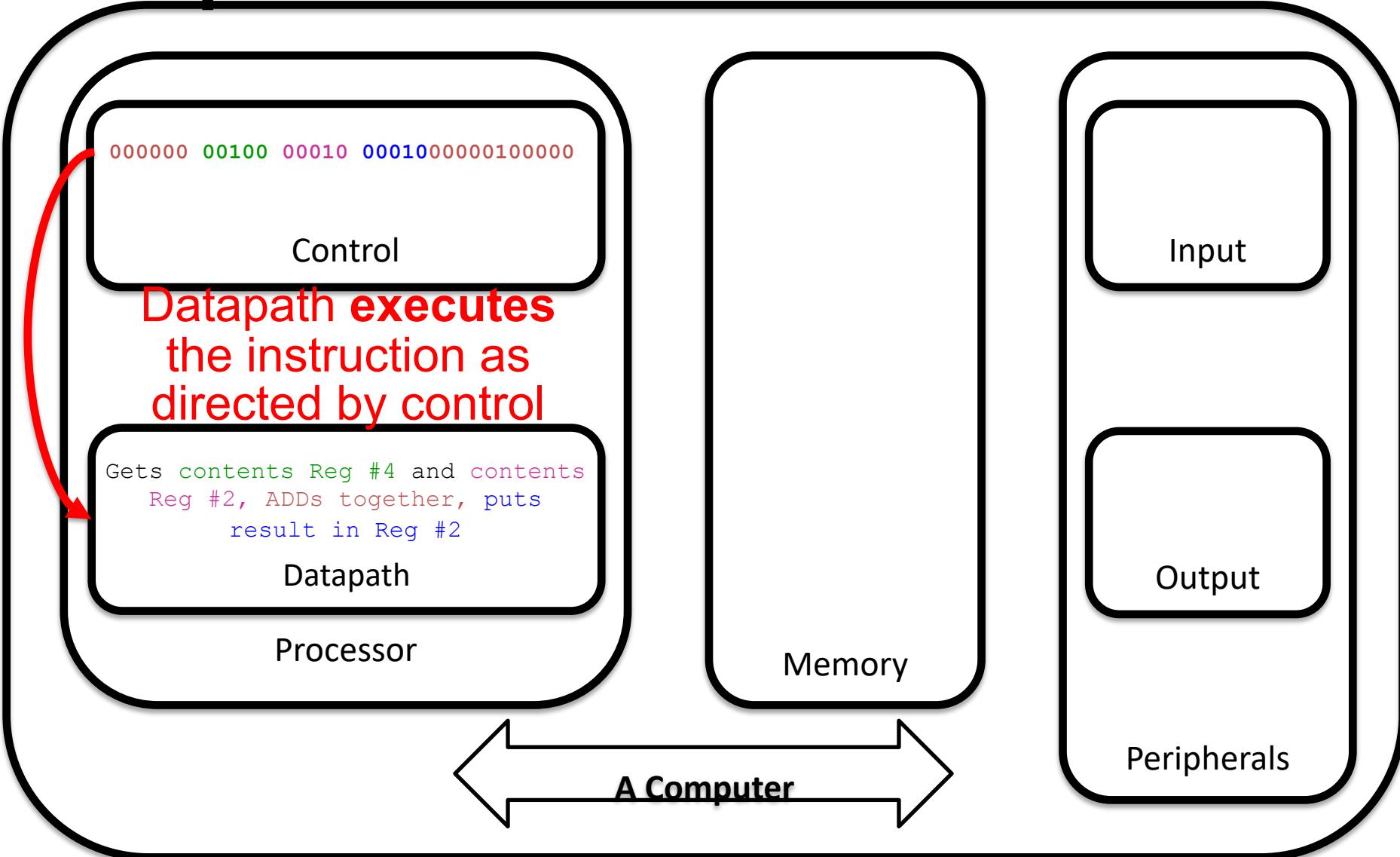
Input

Output

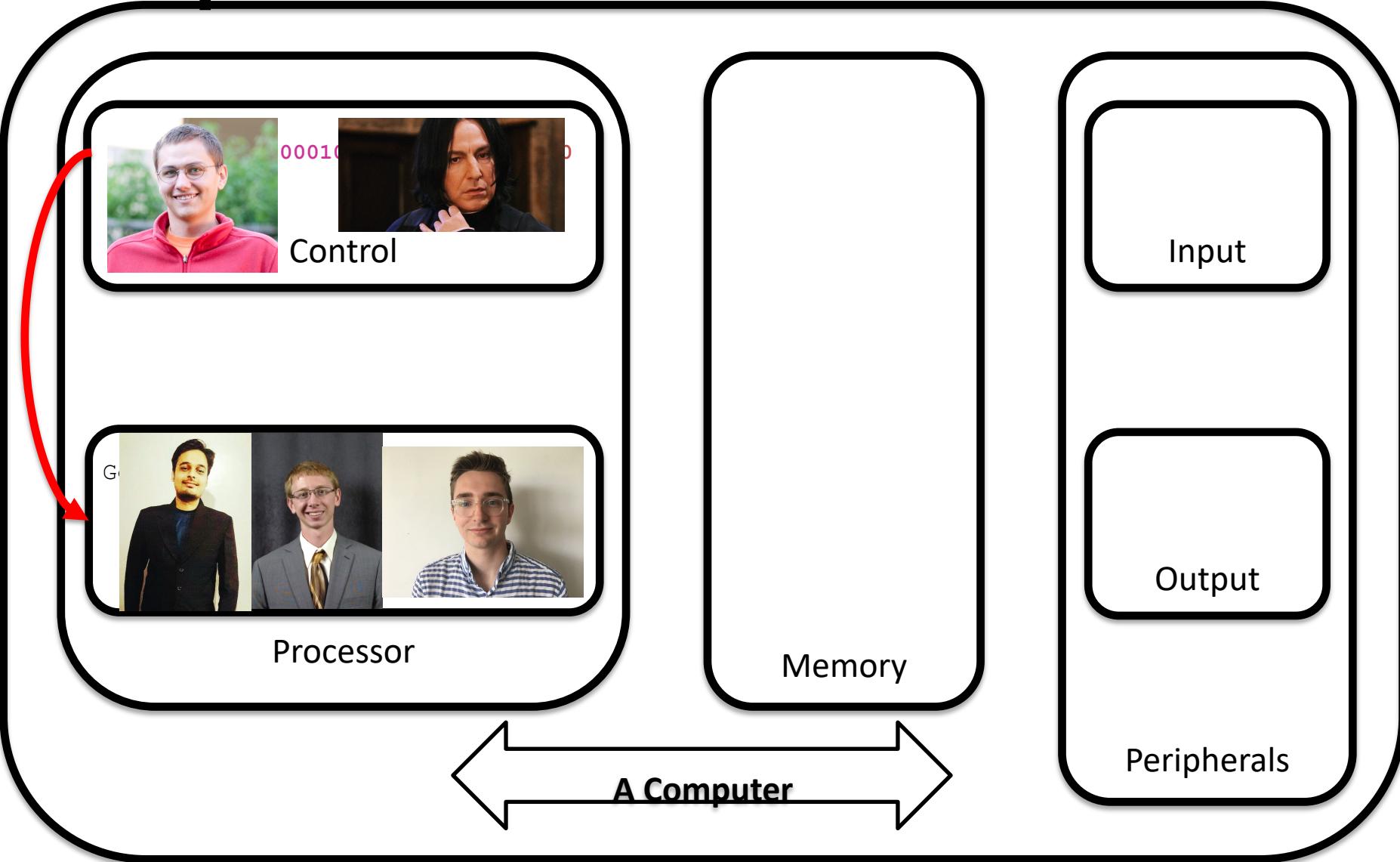
Peripherals

A Computer

Datapath Executes the Instruction



Datapath Executes the Instruction



What Happens Next?

Control

Datapath

Processor

```
000000 00000 00101 0001000010000000  
000000 00100 00010 0001000000100000  
100011 00010 01111 0000000000000000  
100011 00010 10000 000000000000100  
101011 00010 10000 0000000000000000  
101011 00010 01111 000000000000100  
000000 11111 00000 00000000001000
```

```
0000010001010000000001110000000  
0001001111000111110000000000100  
0000000000000000000000101011101000
```

Memory

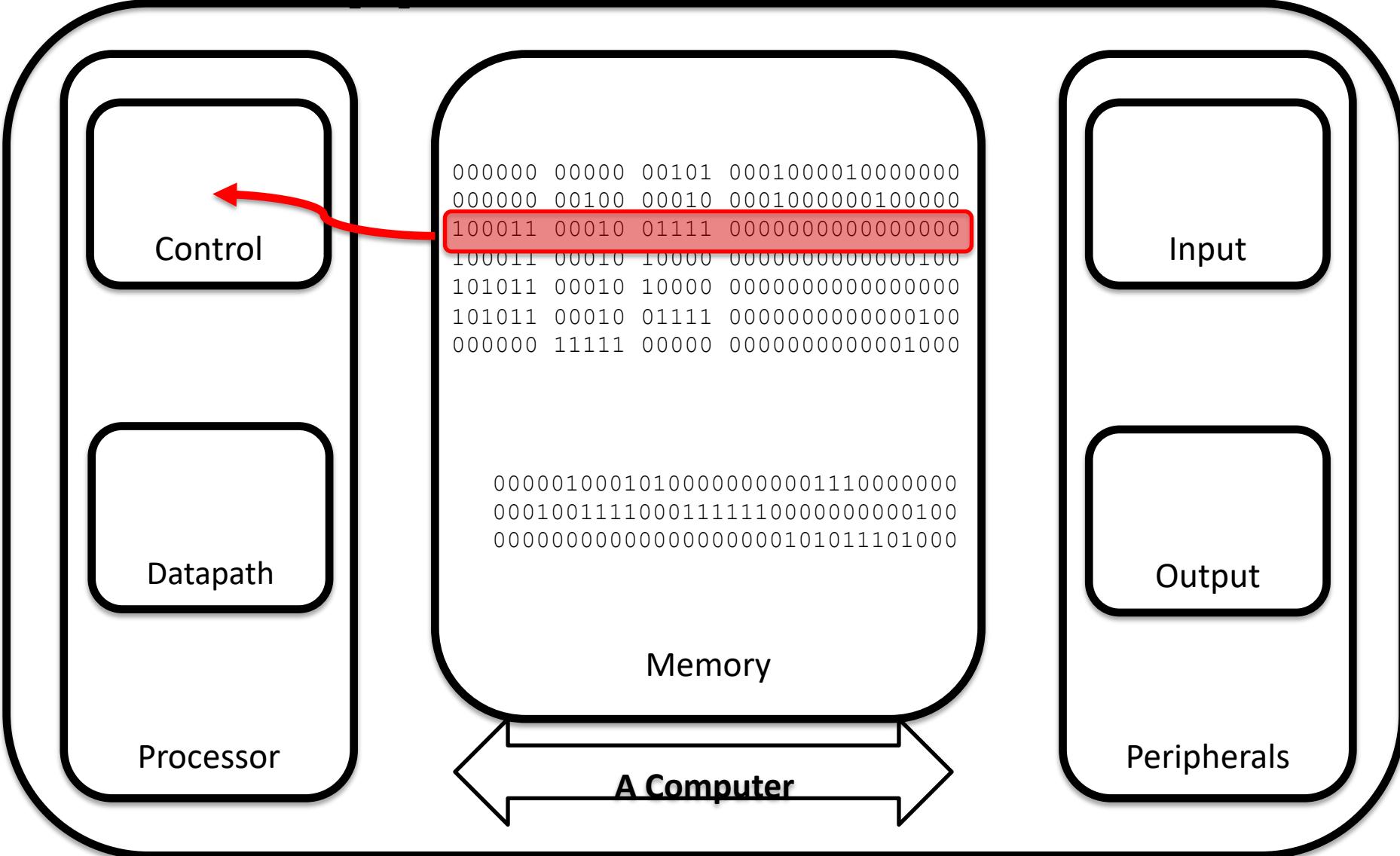
A Computer

Input

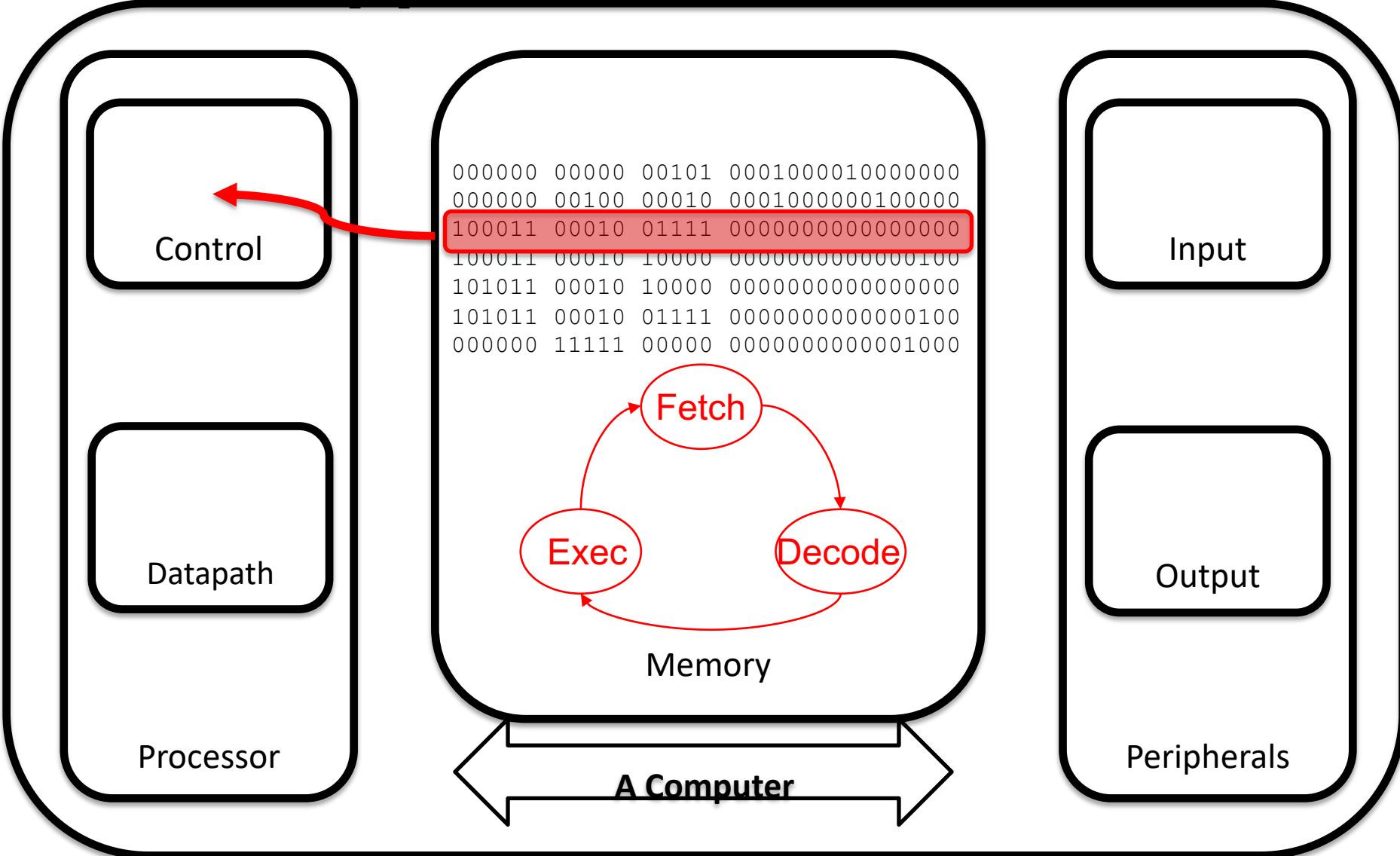
Output

Peripherals

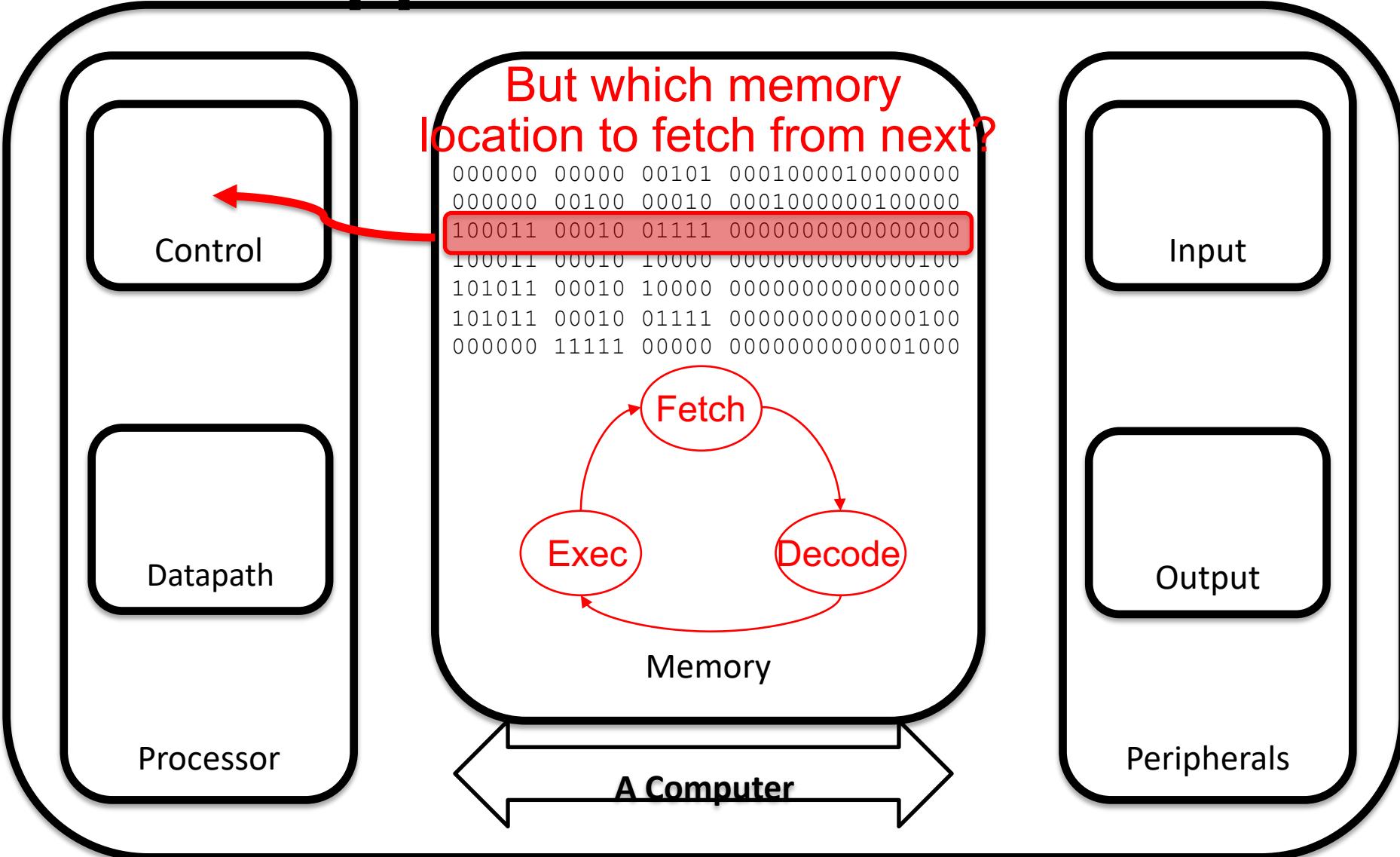
What Happens Next?



What Happens Next?



What Happens Next?



Processor Organization

- Control needs to have circuitry to
 - Decide which is the next instruction and input it from memory
 - Decode the instruction
 - Issue signals that control the way information flows between datapath components
 - Control what operations the datapath's functional units perform
- Datapath needs to have circuitry to
 - Execute instructions - functional units (e.g., adder) and storage locations (e.g., register file)
 - Interconnect the functional units so that the instructions can be executed as required
 - Load data from and store data to memory

Output Data Stored in Memory

Control

Datapath

Processor

```
000000 00000 00101 0001000010000000  
000000 00100 00010 0001000000100000  
100011 00010 01111 0000000000000000  
100011 00010 10000 000000000000100  
101011 00010 10000 0000000000000000  
101011 00010 01111 000000000000100  
000000 11111 00000 0000000000001000
```

Data to be output
resides in memory

```
00001000101000000000000000000000  
00000000010011100000000000000000  
00000011110000000000000000000000
```

Memory

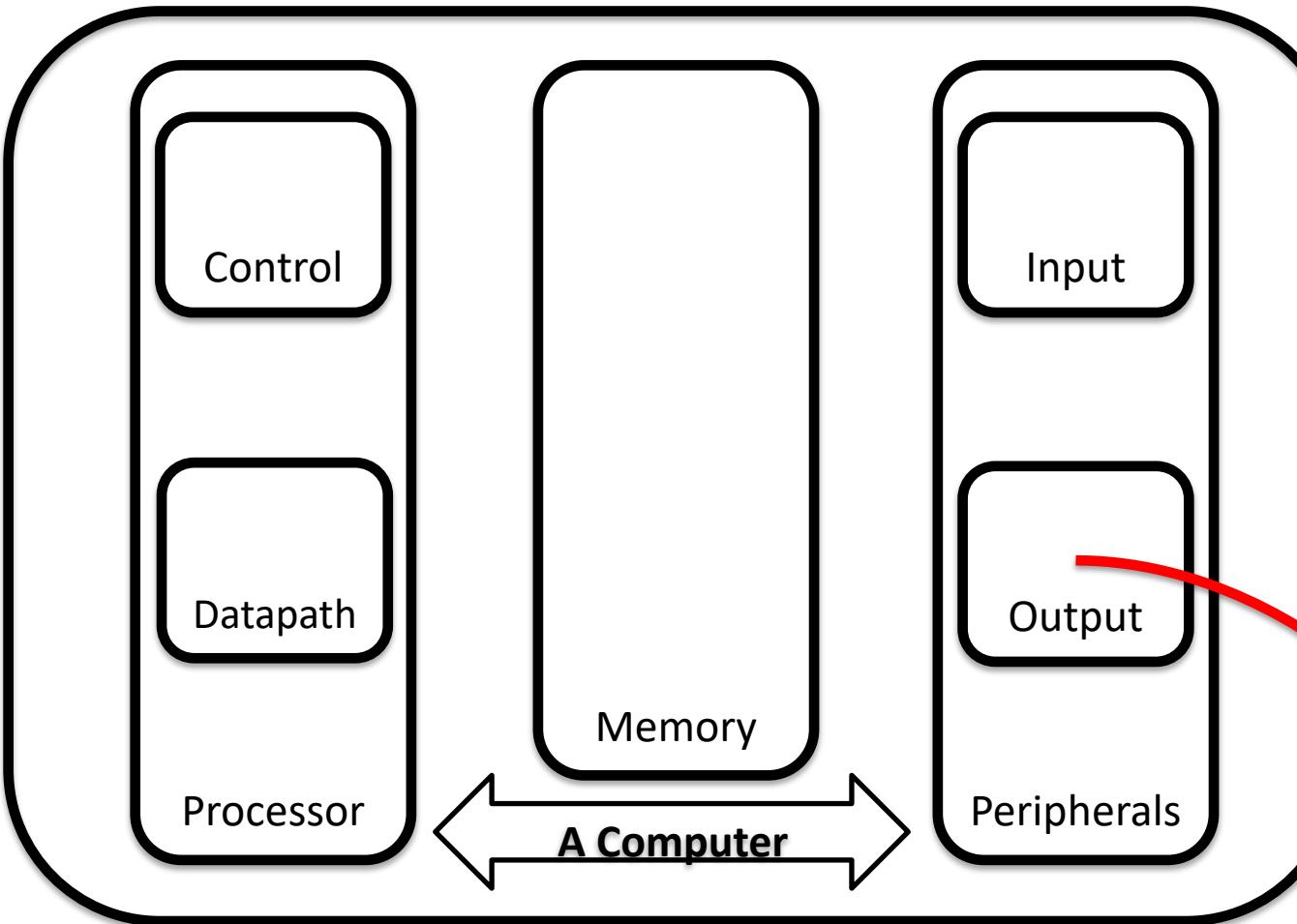
A Computer

Input

Output

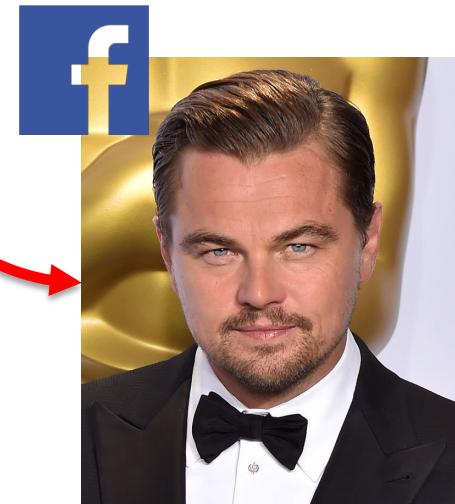
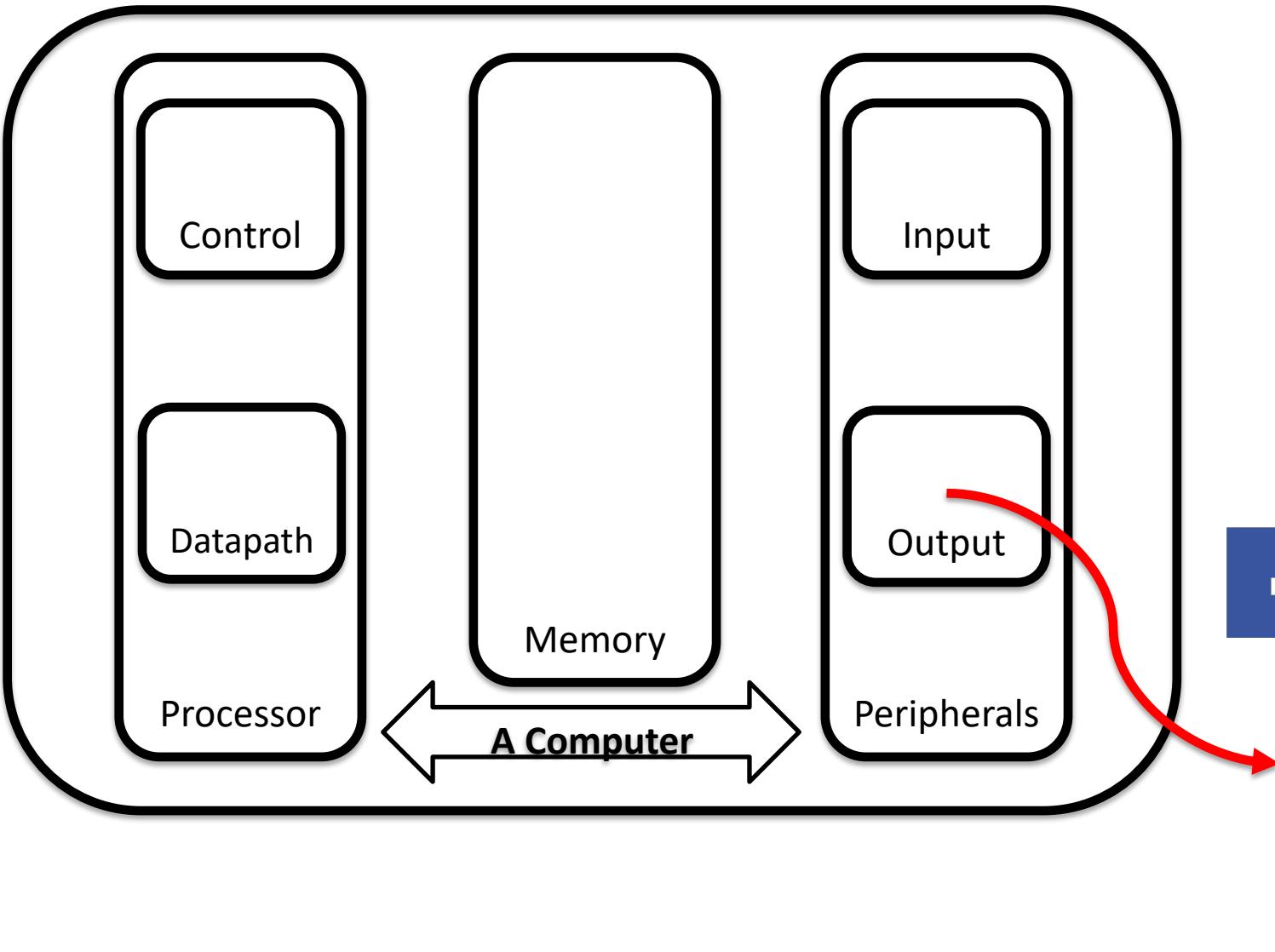
Peripherals

Output Device Outputs Data



00000100010100000000000000000000
00000000010011110000000000000000100
000000111110000000000000000000001000

Output Device Outputs Data



Machine Organization Summary

- Capabilities and performance characteristics of the principal Functional Units (FUs)
 - e.g., register file, ALU, multiplexors, memories, ...
- The ways those FUs are interconnected
 - e.g., buses
- Logic and means by which information flow between FUs is controlled
- **Register Transfer Level (RTL) machine description**
- **The machine's Instruction Set Architecture (ISA)**

Below the Program

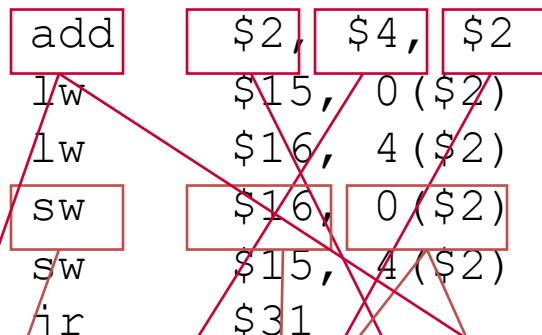
- High-level language program (in C)

```
swap (int v[], int k)
```

...

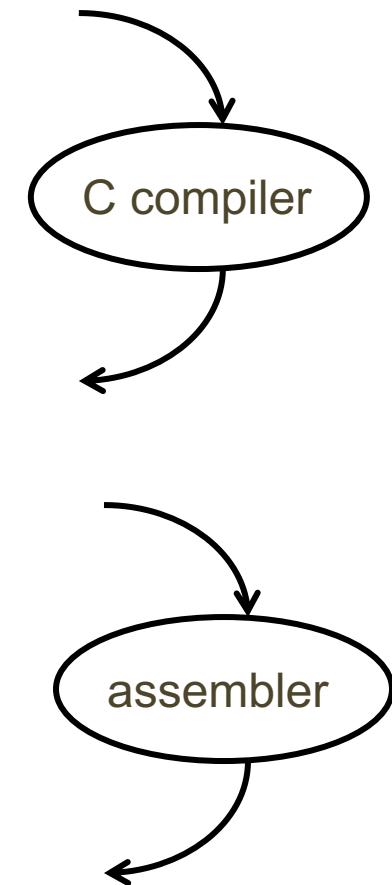
- Assembly language program (for MIPS)

```
swap:    sll      $2, $5, 2
```



- Machine (object) code (for MIPS)

| | | | |
|--------|--------|-------|------------------|
| 000000 | 000000 | 00101 | 0001000010000000 |
| 000000 | 00100 | 00010 | 0001000000100000 |
| 100011 | 00010 | 01111 | 0000000000000000 |
| 100011 | 00010 | 10000 | 0000000000000100 |
| 101011 | 00010 | 10000 | 0000000000000000 |
| 101011 | 00010 | 01111 | 0000000000000100 |
| 000000 | 11111 | 00000 | 0000000000001000 |

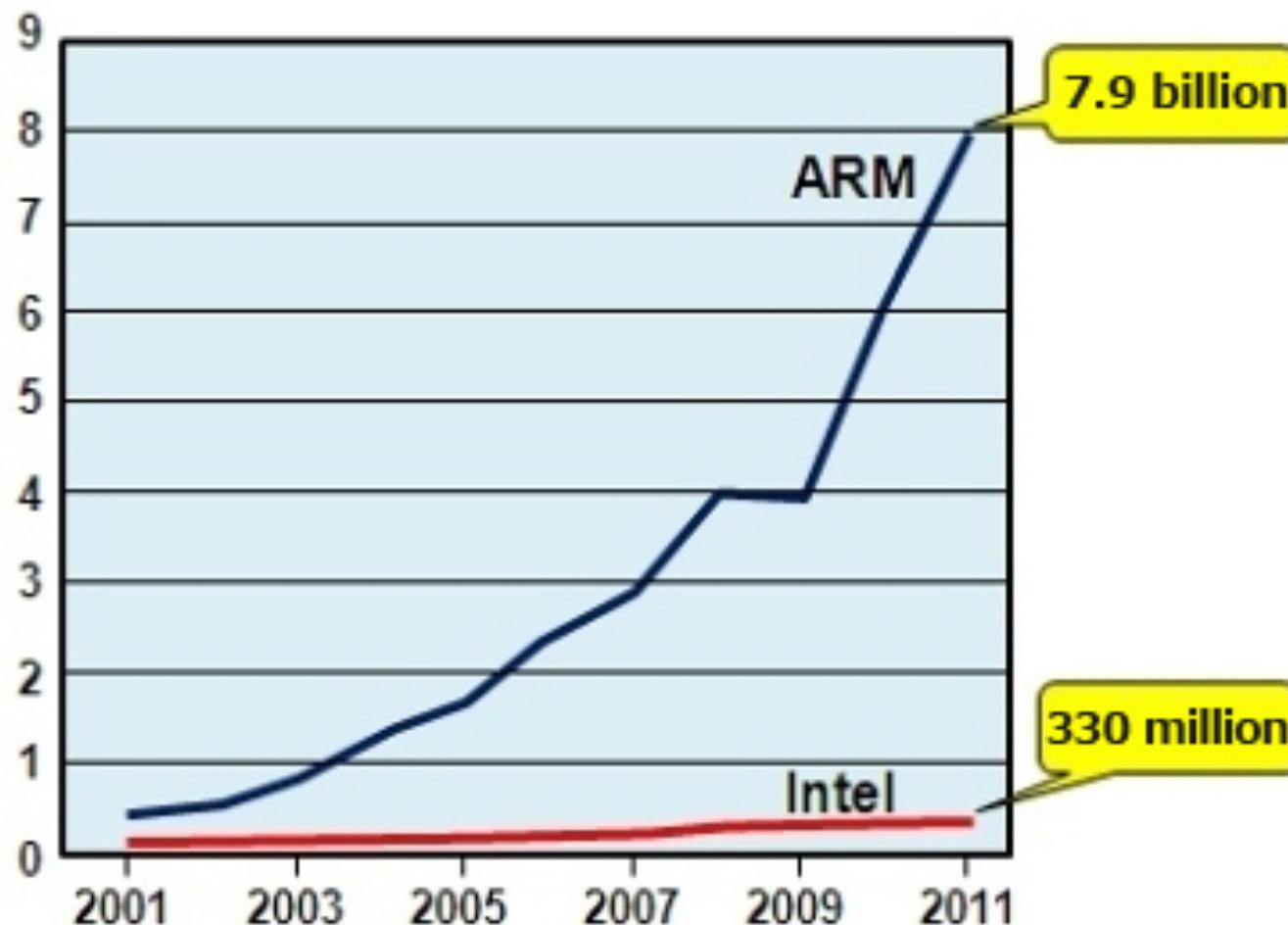


Advantages of Higher-Level Languages?

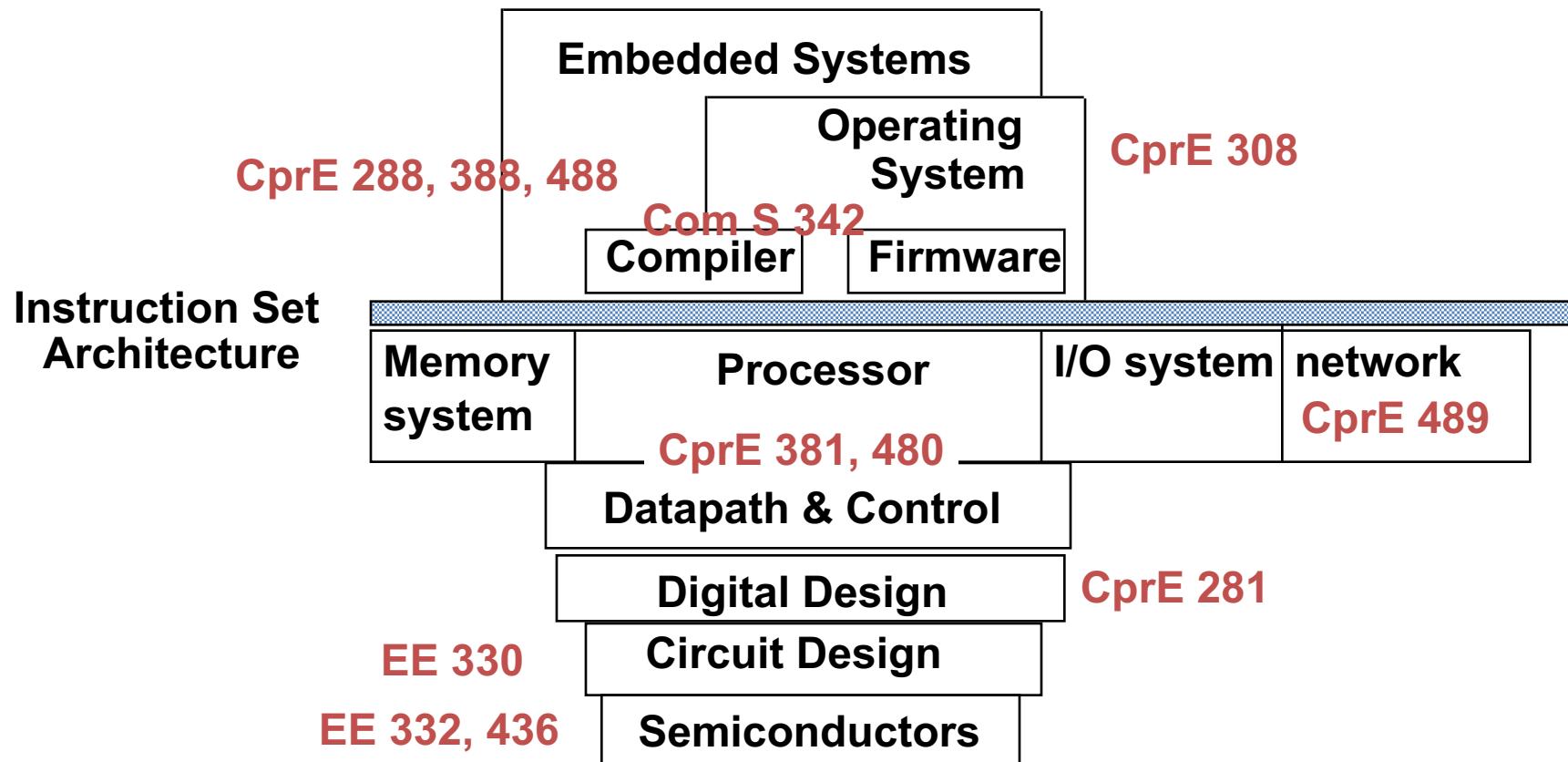
- Higher-level languages:
 - Allow the programmer to think in a **more natural language** and for their intended use (Fortran for scientific computation, C# for desktop GUI applications, Scheme for symbol manipulation, Javascript for web programming, ...)
 - Improve **programmer productivity** – more understandable code that is easier to debug and validate
 - Improve **program maintainability**
 - Allow programs to be **independent of the computer** on which they are developed (compilers and assemblers can translate high-level language programs to the binary instructions of any machine)
 - Emergence of **optimizing compilers** that produce very efficient assembly code optimized for the target machine
- As a result, very little programming is done today at the assembler level

ISA Sales Trends

Number of chips sold (billions)



How do the Pieces Fit Together?



Preview: the MIPS ISA

- Instruction Categories
 - Load/Store
 - Computational
 - Jump and Branch
 - Floating Point
 - coprocessor
 - Memory Management
 - Special

3 Instruction Formats: all 32 bits wide

Registers

R0 - R31

PC

HI

LO

STATUS

CAUSE

| | | | | | |
|----|-------------|----|-----------|----|-------|
| OP | rs | rt | rd | sa | funct |
| OP | rs | rt | immediate | | |
| OP | jump target | | | | |

Acknowledgments

- These slides contain material developed and copyright by:
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