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EEG/2017/029
Section A EEE 301

Quiz 8

1) PDK enables the EDA tools to convert the IPs into real result. This is where all the information needed to actually make something concrete realizable. The PDK affects the the rest of the design. PDK is so fundamental in designing process

2) MPW shuttle is an efficient fully secured way for customers to get the functional validation and process compatibility of IP blocks.

3) From Moore's prediction, advancement in digital electronics serve as the driving force to gradual changes between the achievable transistor density and the actual transistor density that EDA tooling is able to provide.

4) AutoML is a Google cloud AI tool that lets you train a custom model on your own data. It allows training a model that detects listed components on a circuit board. By using AutoML, you can either allow Google to host the model for you in the cloud and access it through a standard REST API or client library or export the model to Tensorflow for offline usage.

5)

Hardware Engineer	Software Engineer
Creative	Analytic thinking
Attention to detail	Information ordering
Trouble shooting	Technology design

6) The Tensor Processing Unit (TPU) is an equivalent of tensorflow and an AI accelerator application specific integrated circuit (ASIC) developed by Google for machine learning. It is a chip specifically designed for Google's Tensorflow framework.

8) The components for PDK and silicon IP are: silicon photonics, InP, polymer, $LiNbO_3$, glass, pol converter, phase modulator, waveguide, amplifier

9) A standard cell library is a collection of low-level electronic logic functions such as AND, OR, NOT, flipflops, latches and buffers. It is a group of transistor that interconnects structure that provides a boolean logic function. Examples of cells in a standard cell library are: combinational logic cells (NAND, NOR etc), Sequential cells, clock cells.

10) NDA hampered free access to pdks in that non disclosure, confidentiality, and agreements are used to bridge the gap with a third party because data has always been important in the commercial world. Access to free pdks is hindered because no information will be sent to anyone except as permitted by the NDA.

11) Design Rule Checking (DRC) specifies as to whether a specific design meets the constraints imposed by the process technology to be used for its manufacturing. It a an essential part of physical design flow and ensures the design meets manufacturing requirements and will not result in a chip failure. Examples are: metal to metal spacing, minimum metal width, poly density, metal fill density etc. DRC is a computational intense task run on each subsection of the ASIC to minimize the number of errors that are detected at the top level. Full chip DRC's may run in much shorter times as quick as one hour depending on the chip complexity and size.

Layout Versus Semantic (LVS) compares the extracted netlist from the layout to the original schematic netlist to determine if they match. LVS determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. LVS involves: extraction, reduction and comparison. Errors encountered during LVS include: shorts, opens, missing components, components mismatch, parameter mismatch.

Parasitic Extraction (PEX) in electronic design automation (EDA) is the calculation of parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit,

parasitic capacitances, parasitic resistances, parasitic inductances. Major effects of interconnect parasitics include signal delays, signal noise, IR drop.

10) The OpenROAD project was launched in June 2018 within the DARPA IDEA program. OpenROAD aims to bring down the barriers of cost, expertise and unpredictability that currently block designers access to hardware implementation in advanced technologies. OpenROAD flow supports TSMC65LP and GF14. The pdks and platform specific files for these kits cannot be provided due to NDA restrictions.

OpenROAD is an integrated chip physical design tool that takes a design from synthesized Verilog to routed layout. The steps used to build a chip using OpenROAD are:

i) Defining the chip size and cell rows
ii) Placement of the pins
iii) Placement of macro cells
iv) Insertion of substrate tap cells
v) Insertion of power distribution network
vi) Macro placement of macro cells
vii) Global placement of standard cells
viii) Repair of max slew, max capacitance and max fanout & long wires
ix) Clock tree synthesis
x) Setup optimization
xi) Insertion of fill cells
xii) Global routing
xiii) Detailed routing

OpenROAD uses the OpenDB database and OpenSTA for static timing analysis. OpenROAD is run using Tcl scripts. Pins are placed on the boundary of the die on the track grid to minimize net wire lengths. Pin placements also create a metal shape for each pin using min-area rules.

Foundries	Nodes
ams	0.35 µm
EMM	0.18 µm
Global Foundries	0.13 µm, 55nm, 45nm, 40nm, 28nm, 22nm, 12nm
IHP	0.25 µm, 0.13 µm
On Semiconductor	0.7 µm, 0.5 µm, 0.35 µm, 0.18 µm,
STMicroelectronics	0.16 µm, 0.13 µm, 65nm, 55nm, 28nm
TSMC	0.18 µm, 0.13 µm, 90nm, 65nm, 40nm, 28nm, 16nm
UMC	0.18 µm, 0.13 µm, 0.11 µm, 65nm, 40nm, 28nm
X-FAB	0.35 µm, 0.18 µm, 0.13 µm,

Foundries	Standard price Eur/mm²	Discounted Eur/mm²
ams 0.35u CMOS C35B4C3 4M/2P4R	640	580
ams 0.35u CMOS C35OPTO 4M/2P5V IO	800	700
ams 0.35u HV CMOS H35B4D3 120V 4M	880	800
ams 0.35u SiGe-BiCMOS S35D4M5/CMOS-RF	880	800
Global Foundries SiGe 8XP	4,200	4,000
Global Foundries 130nm BCDlite	1,500	1,400
Global Foundries 130nm LP	1,500	1,400
Global Foundries 55nm LPe-RF/LPx-NVM	4000	3800
Global Foundries 45RFSOI	7,350	7,000
Global Foundries 40nm 2S/LP-RF/RF mmwave	5000	4,700
Global Foundries 28nm SLPe	10,200	9,700
Global Foundries 22nm FDSOI	14,00	13,200
Global Foundries 12nm LPt	26,000	25,000
IHP SG13B2SV 0.25u SiGeC Bipolar/Analog Ft/fmax=?/?GHz	2,500	2,125
IHP SG25H3 0.25u SiGeC Bipolar/Analog Ft/fmax=110/180GHz	3,800	3,230
SG 25H5_EPIC Bipolar/Analog, Ft/fmax=250/300GHz	8,000	6,800
IHP SG25 PIC (Photonics, Ge Photo-diode)	3,800	3,230
IHP SG13S SiGeC Bipolar/Analog Ft/fmax=255/340GHz	6,300	5,355
IHP SG13C SiGeC CMOS 7M/MiM	4,500	3,825
IHP SG13G2 SiGeC Bipolar/Analog Ft/fmax=300/500GHz	7,300	6,205
IHP SG13G2Cu FEOL process SG13G2 Cu BEOL	7,000	5,950
IHP SG13Cu FEOL process SG13S Cu BEOL	6,100	5,185
IHP BEOL SG13(Mi & Metal layers)+LBE or TSV	1,000	850
Bumping (available for all IHP)	6,500	6,500
Localised backside etching	5,000	4,250
TSV to ground	7,500	7,500
Cu Pillar	18,500	18,500
ON Semi 0.7u C07M-D 2M/1P	300	270
ON Semi 0.7u C07M-A 2M/1P/Poly1/HR	350	315
ON Semi 0.7u C07M-12T 100V-2M	525	485
ON Semi 0.7u C07M-12T 100V-3M	560	525
ON Semi 0.5u CMOS EEPROM CSF8CSN-200mm	1,150	1,100
ON Semi 0.35u C035U 4M (default) + analog options	720	670
ON Semi 0.35u C035U 3M (optional) + analog options	700	650
ON Semi 0.35u C035U 5M (optional) + analog options	800	750
ON Semi 0.35u C035-13T80U 80V 3M	850	800
ON Semi 0.35u C035-13T80U 80V 4M	925	875
ON Semi 0.35u C035-13T80U 80V 5M	1050	995
ON Semi 0.35u C035-18T80U 80V 3M	850	800
ON Semi 0.35u C035-13T50U 50V 3M	925	875
ON Semi 0.35u C035-13T50U 50V 4M	1050	995
ON Semi 0.35u C035-13T50U 50V 5M	750	700
ON Semi 0.35u C035-13T25U 3.3/25V 3M (optional)	770	720
ON Semi 0.35u C035-13T25U 3.3/25V 4M (default)	800	750
ON Semi 0.35u C035-13T25U 3.3/25V 5M (optional)		

ST	28nm	CMOS 28FDSOI	9000	1,500
ST	95nm	BiCMOS055	5,500	1,200
ST	65nm	CMOS065	4,500	1,200
ST	130nm	BiCMOS9MW	2,600	1,000
ST	130nm	H9SOI-FEM	2,200	700
ST	130nm	HCMOS9GP	2,500	700
ST	130nm	HCMOS9A	2,500	700
ST	0.16µm	BCD8sP	2,500	1,000
ST	0.16µm	BCD8s-SOI	2500	1,000
UMC	L180	Logic GII, Mixed-Model/RF	13,400	12,740
UMC	L180	EFLASH Logic GII	17,000	16,160
UMC	L130	Logic/Mixed-Model/RF	22,300	21,200
UMC	L110AE	Logic/Mixed-Model/RF	24,600	23,350
UMC	L65nm	Logic/Mixed-Model/RF-LL/SP	35,350	33,600
UMC	40N	Logic/Mixed-Model-LP	68,450	65,040
X-FAB	XH018	0.18µ 0.18µ HV NVM CMOS E-FLASH (MET3,4,MID,THK)	1605	1,525
X-FAB	XT018	0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	1,635	1,555
X-FAB	XSO18	0.18µ OPTO (MET3, MET4, MET5, METMID)	1,375	1,310
X-FAB	XP018	0.18µ NVM CMOS (MET 3, MET4, METMID, METTHK)	1,415	1,345
X-FAB	XH035	0.35µ HV CMOS (MET4)	1035	985
X-FAB	XR013	0.13µ RF SOI CMOS (METRB, METBQ)	1830	1745
X-FAB	XR013	0.13µ RF SOI CMOS (METTHK1, METRB, METRQ)	2,280	2,165
X-FAB	XMB10	MEMS	10,500	9,800
TSMC	0.18MS RF (min area = 3mm²)		2900	2,510
TSMC	0.18BCD Gen II (min area = 4mm²)		4,370	3,770
TSMC	65LP MS RF (min area = 1mm²)		3,720	3,120
TSMC	40LP MS RF (min area = 3mm²)		15,395	14,626
TSMC	28HPC RF (min area = 1mm²)		9,010	7,240
TSMC	28HPC+RF (min area = 1mm²)		9,010	7,240

Open Source

A company efabless created Ravenna (Foss RTL, Foss Tools) using X-FAB 180nm PDK. efabless proved that you could compile those tools. FOSSI foundation in partner with skywater technology released an open source PDK for 130nm process node (APACHE 2.0) available on github with no restrictions from NDA. If you using python, you will be familiar with sphinx which we working on to be compatible with the PDK. There are multiple sources for libraries.

Library Name	Type
sky130_fd_sc_hd	High density + Low leakage
sky130_fd_sc_hdll	
sky130_fd_sc_hvl	high voltage
sky130_fd_sc_hs	High speed
sky130_fd_sc_ms	Medium speed
sky130_fd_sc_ls	Low speed
sky130_fd_sc_lp	Low power

Specialized Build Spaces

SRAM bit cells + DRC exceptions
SONOS flash bit cells + DRC exceptions
ReRAM
Will need a compiler to turn into macros.
OpenRAM has been used for the SRAM

An Open Source PDK

How To Use Digital Design

theopenroadproject.org is run by Andrew B. Kheang and his team. They have a fully open source digital flow ranging from GDS to parasitic abstraction. The openRoad project wants no human to be

to be involved in the process to take a design from RTL to GDS with no errors. Their current focus is on Global foundries of 12nm node. efabless in conjuction with the American University in Cairo have been able to create OpenLane, an openRoad customized to work with the skywater PDK.

How To Use Analog Design?

This is considered as a bit of blackout. The Blue Cheetah company have been funded with required primitives and prototyping porting Intel's AIB, only that it requires some closed source components.

OpenRAM works with closed tools and without closed tools and is designed with precompiled macros. Matt Guthaus is the founder of OpenRAM

Designing Standard cell libraries

Oklahoma State University previously designed: MOSIS, SRC, DoD, Mentor graphics, Synopsys and cadence design systems, from 0.5µm to 14nm. sky130 osu_sc currently has multiple drive strength of X16, LEF views, full characterization and automated makefile flows extraction

DRC/LVS Checks

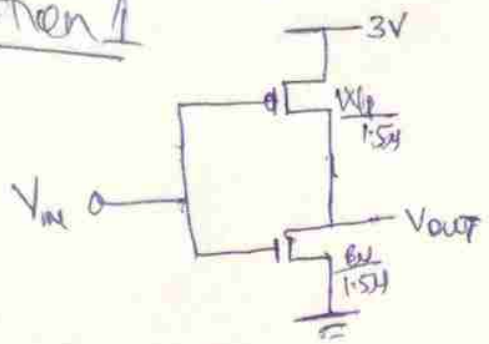
A tool called Magic is the only piece of open source software released in 1980 initially but latest release in 2020; it does comprehensive DRC checking for skywater 130nm. efabless developed "strive" of 1K memory. The first of it was done with SRAM using the openROAD and open source PDK. It is one of the fully open source ASIC.

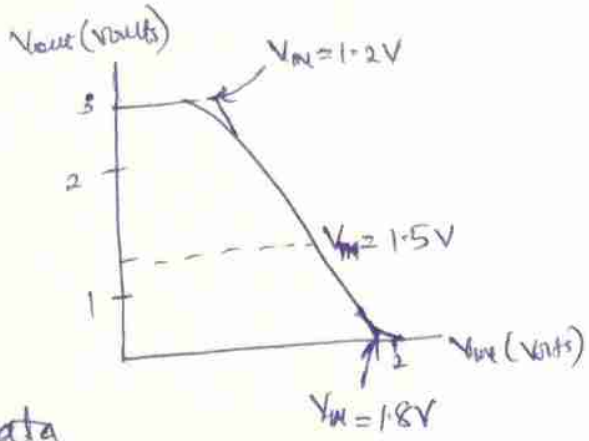
Strive Test Chips

IC	CPU	Standard Cells	Memory size (kbytes)	Memory type
strive	PicoRV32	fd_sc_hd	1	Logic RAM (DFF)
strive 2	PicoRV32	fd_sc_hd	1	OpenRAM
strive 3	PicoRV32	osu_sc	1	Logic RAM (DFF)
strive 4	PicoRV32	osu_sc	1	OpenRAM
strive 5	PicoRV32	fd_sc_hd	8	OpenRAM
	PicoRV32	fd_sc_hd	1	OpenRAM

SECTION B

Question 1





NMOS Data

$\mu_n C_{ox} = 50\mu A/V^2$

$V_{Tn} = 0.5V$

PMOS Data

$\mu_p C_{ox} = 25\mu A/V^2$

$V_{Tp} = -0.5V$

Solutions

a) Calculate W_p such that $-I_{DP} = I_{Dn} = 100\mu A$ at $V_{IN} = V_M$

$$\frac{W_p}{L_p} = \frac{2W_n}{L_n}$$

$$W_p = \frac{2W_n L_p}{L_n} = \frac{2 \times 6 \times 1.5\mu}{1.5} = \frac{18}{1.5} = 12\mu m$$

b) Calculate the NMOS transconductance, g_{mn} at $V_{IN} = V_M$

$$g_{mn} = \frac{W_n}{L_n} \mu_n C_{ox} (V_{GS} - V_{TN})$$

$$= \left(\frac{6}{1.5}\right) \times 50\mu (1.5 - 0.5)$$

$$= 1200\mu S$$

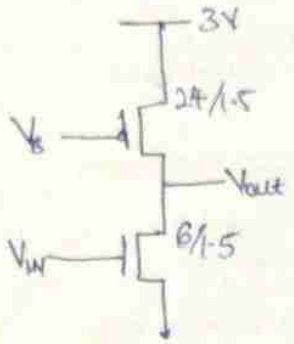
c) Calculate $(\lambda_n + \lambda_p)$

$$\lambda_n = \frac{0.1\mu}{L_n} = \frac{0.1\mu}{1.5\mu} = 0.067V^{-1}$$

$$\lambda_p = \frac{0.1\mu_p}{L_p} = \frac{0.1}{1.5} = 0.067V^{-1}$$

$$(\lambda_n + \lambda_p) = 0.067 + 0.067 = 0.13V^{-1}$$

c) An inverter with p-channel current source has the same current 100 μA flowing through the p and n channel device at $V_{IN} = V_M$ is shown below. The inverter has different p-channel sizing but the same transistor data



NMOS Data
$\mu_n C_{ox} = 50\mu A/V^2$
$V_{tn} = 0.5$

PMOS Data
$\mu_p C_{ox} = 25\mu A/V^2$
$V_{tp} = -0.5V$

d) What is the value of the V_B such that $-I_{DP} = I_{DN} = 100\mu A$ at $V_{IN} = V_M$?

$$-I_{DP} = \frac{W_p}{2L_p} \mu_p C_{ox} (V_{GS} - V_M + V_{tp})^2$$

$V_M = V_B$

$$+100\mu A = \frac{24}{2\times1.5} \times 25\mu (3 - V_B - 0.5)^2$$

$$+0.5 = (2.5 - V_B)^2$$

$$+0.5 = 6.25 - 5V_B + V_B^2$$

$$-V_B^2 + 2.5 = \sqrt{0.5}$$

$$-V_B + 2.5 = 0.71$$

$$V_B = 1.79V$$

e) Calculate the voltage gain at $V_{IN} = V_M$

Gain $A_V = -g_{mn}(r_{on} \| r_{op})$

$$r_{on} \| r_{op} = \frac{1}{(\lambda_n + \lambda_p) I_{on}}$$

$$g_{mn} = \sqrt{2\left(\frac{W_n}{L_n}\right)\mu_n C_{ox} I_{on}} = \sqrt{2\left(\frac{6}{1.5}\right)\cdot 50\mu \times 100\mu} = 0.04\,\mathrm{S}$$

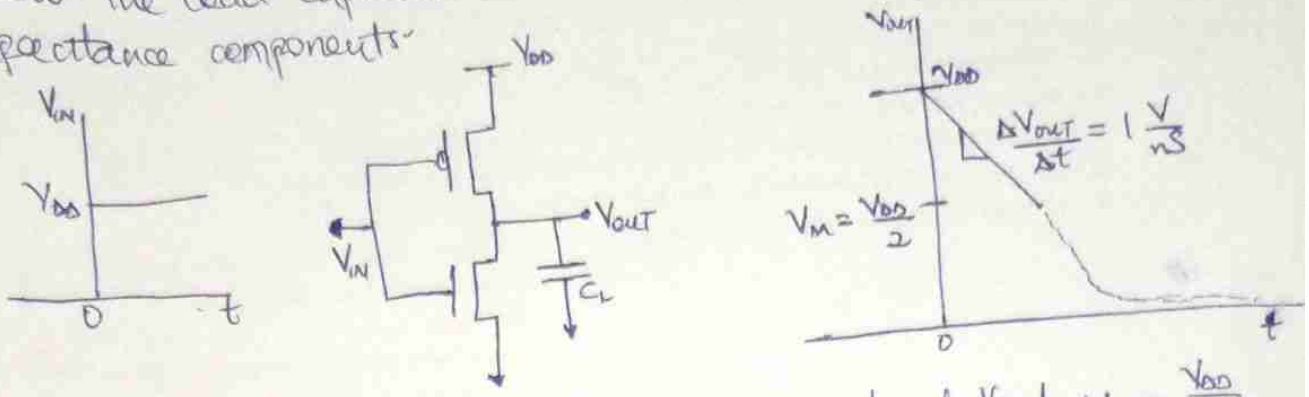
$$r_{on} \| r_{op} = \frac{1}{(\lambda_n + \lambda_p) I_{on}} = \frac{1}{\left(\frac{0.1}{L_n} + \frac{0.1}{L_p}\right) \times 100\mu^2} = 75k\Omega$$

$A_V = -0.04\mathrm{S}(75k\Omega)$

$= -3$

Question 2

You are given a CMOS inverter with a step input voltage from 0 to V_{DD} at $t=0$, resulting in an output voltage V_{OUT} vs t shown below. The load capacitance $C_L = 0.1pF$ accounts for all load capacitance components.



a) Given $V_{DD} = 1.5V$ and ~~that~~ the devices are sized such that $V_M = \frac{V_{DD}}{2}$, calculate t_{PHL}.

$$t_{PHL} = \frac{C_L (V_{DD} - V_M)}{I_D} = \frac{C_L (V_{DD} - V_M)}{\frac{\Delta V_{OUT}}{\Delta t}}$$

$C_L = 0.1pF$, $V_{DD} = 1.5V$, $V_M = \frac{1.5}{2} = 0.75V$, $\frac{\Delta V_{OUT}}{\Delta t} = 1 \frac{V}{ns}$

$$\therefore t_{PHL} = \frac{0.1 \times 10^{-12} (1.5 - 0.75) V}{1 nS} = 7.5 \times 10^{-5} s = 75 \mu s$$

b) Calculate the current I_{Dn} at $0 < t < t_{PHL}$.

At $0 < t < t_{PHL}$, we assume that the MOSFET remains saturated

$$I_{Dn} = \frac{1}{2} k_n (V_M - V_{Tn})^2$$

$V_{Tn} = 1$

$$I_{Dn} = \frac{1}{2} k_n (0.75 - 1)^2 = \frac{1}{2} k_n (0.0625) = (0.0313 k_n) A$$

c) Given $V_{Tn} = 0.5V$ and $\mu_n C_{ox} = \frac{50 \mu A}{V^2}$ find $\frac{W}{L}$ of the NMOS

$t_{PHL} = 75 \mu s$

$$t_{PHL} = \frac{C_L (V_{DD} - V_M)}{I_D} = \frac{C_L V_{DD}}{\frac{W_n}{L_n} \mu_n C_{ox} (V_{DD} - V_{Tn})^2}$$

$$75 \mu s = \frac{0.1pF (1.5)}{\frac{W_n}{L_n} \times 50 \mu A/V^2 (1.5 - 0.5)^2}$$

$$75 \mu s = \frac{1.5 \times 10^{-13}}{\frac{W_n}{L_n} (5 \times 10^{-5})}$$

$$\frac{W_n}{L_n} = \frac{1.5\times10^{-13}}{75\times10^{-6}\times 5\times10^{-5}}$$

$$\frac{W_n}{L_n} = 4\times10^{-5} = 40\mu$$

For parts (d) and (e) assume $V_{DD} = 2.5V$

d) Calculate the new slope of the output voltage $\frac{\Delta V_{out}}{\Delta t}$, at $0 < t < t_{pHL}$

$$t_{pHL} = \frac{C_L(V_{DD} - V_M)}{\frac{\Delta V_{out}}{\Delta t_{new}}}$$

$V_{DD} = 2.5V$

$V_M = \frac{V_{DD}}{2}$

$t_{pHL} = 75\mu s$ and $C_L = 0.1pF$

$$75\mu s = \frac{0.1pF\left(2.5 - \frac{2.5}{2}\right)}{\frac{\Delta V_{out}}{\Delta t_{new}}}$$

$$\frac{\Delta V_{out}}{\Delta t_{new}} = \frac{0.1\times10^{-12}(1.25)}{75\mu s}$$

$$\frac{\Delta V_{out}}{\Delta t_{new}} = 1.7\frac{V}{ns}$$

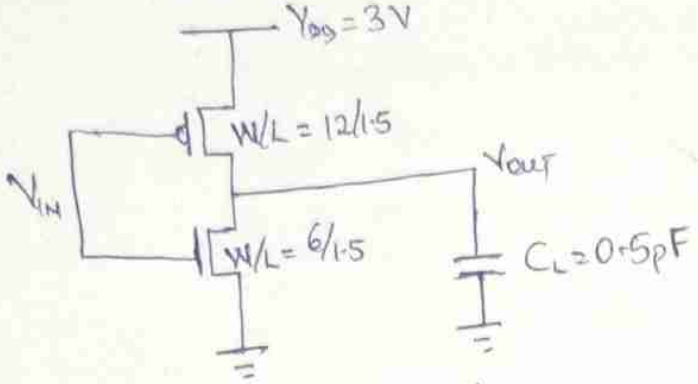
e) Calculate the new t_{pHL}

$$t_{pHL\,new} = \frac{C_L(V_{DD_{new}} - V_M)}{\frac{\Delta V_{out}}{\Delta t}}$$

$$t_{pHL_{new}} = \frac{0.1pF\left(2.5 - \frac{2.5}{2}\right)}{1n} = 12.5\mu s$$

Question 3

Consider the CMOS inverter below. Take channel modulation into consideration.



Parameter	NMOS	PMOS
V_{TO}	0.5V	−0.5V
μ	$220 cm^2/Vs$	$110 cm^2/Vs$
λ	$0.1V^{-1}$	$0.1V^{-1}$
T_{ox}	15nm	15nm

Dimensions of W and L are in μm

a) Calculate V_M, the voltage midpoint

$$V_M = \frac{V_{Tn} + \sqrt{\frac{K_p}{K_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{K_p}{K_n}}}$$

$$K_p = \frac{W_p}{L_p}\mu_p C_{ox} = \left(\frac{12}{1.5}\right) 110\times10^{-4} \times \frac{(3.9 \times 8.85\times10^{-14})}{15\times10^{-9} m}$$

$$K_p = 8(110\times10^{-4})(2.3\times10^{-7})$$

$$K_p = 202\mu A/V^2$$

$$K_n = \frac{W_n}{L_n}\mu_n C_{ox} = \frac{6}{1.5} \times 220\times10^{-4}\left(\frac{3.9\times8.85\times10^{-14}}{15\times10^{-9}}\right)$$

$$= 4 \times 220\times10^{-4}(2.301\times10^{-5})$$

$$K_n = 202\mu A/V^2$$

$$V_M = \frac{0.5 + \sqrt{\frac{202}{202}}(3+0.5)}{1+\sqrt{\frac{202}{202}}} = \frac{0.5+1(3.5)}{2}$$

$$V_M = \frac{4}{2} = 2 \text{ Volts}$$

b) Calculate A_V, the voltage gain at $V_{in} = V_M$

$$A_V = -g_{mn}(r_{on} \| r_p)$$

$$g_{mn} = \frac{W_n}{L_n} \mu_n C_{ox} (V_M - V_{Tn})^2$$

$$= \frac{6}{1.5} \times 220\times10^{-4} (2.301\times10^{-5})(2-0.5)^2$$

$$g_{mn} = \cancel{360\times10^{-6}\,S} \quad 3.04\times10^{-4}\,S$$

$$r_{on} \| r_p = \frac{1}{(\lambda_n + \lambda_p) I_{on}}$$

$$I_{on} = \frac{W_n}{2L_n} \mu_n C_{ox} (V_M - V_t)^2$$

$$= \frac{6}{2(1.5)} \times 220\times10^{-4} (2.301\times10^{-5})(2-0.5)^2$$

$$= 2.3\times10^{-6}\,A$$

$$r_{on} \| r_p = \frac{1}{\left(\frac{0.1}{1.5} + \frac{0.1}{1.5}\right)(2.3\times10^{-6})} = 3.3\,M\Omega$$

$$A_V = -3.04\times10^{-4} \times 3.3\,M\Omega = -9.9$$

c) Calculate N_{ML}, N_{MH}

$$N_{ML} = V_M - \frac{V_{DD} - V_M}{|A_V|} = \frac{3-2}{9.9} = 1.0$$

$$N_{MH} = V_{DD} - V_M\left(1 + \frac{1}{|A_V|}\right)$$

$$= 3 - 2\left(1 + \frac{1}{9.9}\right) = 3 - 2.2 = 0.8$$

d) Calculate t_{pHL} and t_{pLH}

$$t_{pHL} = \frac{C_L V_{DD}}{\frac{W_n}{L_n} \mu_n C_{ox} (V_{DD} - V_{Tn})^2} \quad ; \quad C_L = 0.5\,pF$$

$$t_{pHL} = \frac{0.5\times10^{-12} \times 3}{\left(\frac{6}{1.5}\right)(220\times10^{-4})(2.301\times10^{-5})(3-0.5)^2} = \cancel{296\,ns}\ 119\,ns$$

$$t_{pLH} = \frac{C_L V_{DD}}{\frac{W_p}{L_p} \mu_p C_{ox} (V_{DD} + V_{Tp})^2} = \frac{0.5\times10^{-12} \times 3}{\left(\frac{12}{1.5}\right)(110\times10^{-4})(2.301\times10^{-5})(3-0.5)^2} = 119\,ns$$