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## Question Paper Code : J1501

M.Sc. DEGREE EXAMINATION, FEBRUARY/MARCH 2018.

First Semester

Computer Science

DCS 7101 — COMPUTER ORGANIZATION

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert  $(10111.0101)_2$  in to its equivalent decimal value.
2. Express NAND gate in terms of NOR gates only.
3. Differentiate combinational and sequential circuits.
4. What is decoder?
5. List the different phases involved in the execution of an instruction.
6. Define clock rate.
7. What is paging?
8. What is LRU?
9. What is an interface?
10. What is polling? Give two examples of polling.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Simplify the following function using four variable k-maps :  

$$A'B'C'D' + A'C'D + ACD' + A'BCD + BC'D.$$
 (8)
- (ii) State and prove Demorgan's theorem. (5)

Or

- (b) (i) Implement Boolean expression for EXOR gate using NAND and NOR gates. (8)
- (ii) Using 2's complement perform  $(42)_{10} - (68)_{10}$ . (5)
12. (a) (i) Explain Full adder with its truth table and implementation. (7)
- (ii) Design 3:8 decoder using NOR gates. (6)

Or

- (b) (i) Explain the working of JK-flip flop with its characteristic table. (8)
- (ii) Draw the diagram of 4 bit UP DOWN counter. (5)
13. (a) Explain von-neumann architecture.
- Or
- (b) Compare pipeline and multicore processors.
14. (a) Discuss in detail about cache memory.

Or

- (b) Explain the working of any two page replacement policies.
15. (a) Explain in detail about Interrupt handling.

Or

- (b) Illustrate DMA with suitable diagram.

PART C —  $(1 \times 15 = 15$  marks)

16. (a) Design and implement 16:1 Multiplexer using two 8:1 MUX.

Or

- (b) What is virtual memory? Explain in detail about how virtual memory is implemented with neat diagram.
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## **Question Paper Code : BS2501**

M.Sc. DEGREE EXAMINATION, AUGUST/SEPTEMBER 2017.

First Semester

Computer Science

DCS 7101 — COMPUTER ORGANIZATION

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the given octal number 234.25 into decimal.
2. What are universal gates?
3. Compare combinational and sequential circuits.
4. What do you mean by latch?
5. Define processor.
6. Write the features of multi core processors.
7. What is paging?
8. Write the use of LRU replacement policy.
9. What is full duplex method?
10. Define polling.

PART B — (5 × 13 = 65 marks)

11. (a) Explain how to perform addition and subtraction for signed binary numbers. Illustrate with examples. (13)

Or

- (b) Simplify the Boolean function using K-Map method. (13)

$$F(A, B, C, D) = \Sigma (2, 3, 4, 6, 8, 9, 12, 14).$$

12. (a) With an neat sketch, explain the operation of 4-bit binary adder-subtractor. (13)

Or

- (b) Explain the working of 3-to-8 decoder. Compare it with multiplexer. (13)

13. (a) (i) With a neat sketch, explain the function of Von-Neumann architecture. (7)

- (ii) Explain the concept of instruction formats. (6)

Or

- (b) Write a detailed note on pipelining. (13)

14. (a) With a neat sketch, explain the virtual memory address translation scheme. (13)

Or

- (b) Describe the various cache memory mapping techniques. (13)

15. (a) Explain the function of bus interface circuit. (13)

Or

- (b) Elaborate on the concept of DMA. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Tabulate the comparison of fixed, selectable, parameterized and programmable logic processors. (15)

Or

- (b) With a simple case study, discuss how to handle interrupt mechanism. (15)
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## **Question Paper Code : J1526**

M.Sc. DEGREE EXAMINATION, AUGUST/SEPTEMBER 2016.

(From Academic Year – 2015 – New Question Paper Pattern)

First Semester

Computer Science

DCS 7101 — COMPUTER ORGANIZATION

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the truth table for Ex-OR gate.
2. What is a negative logic?
3. Differentiate combinational and sequential circuits.
4. What is a multiplexer?
5. What is an instruction cycle?
6. What are multi core processors?
7. What is LRU?
8. What is half duplex interaction?
9. What is meant by buffer chaining?
10. What is meant by programmed I/O?

PART B — (5 × 13 = 65 marks)

11. (a) Explain why NAND and NOR gates are called as universal gates.

Or

- (b) Write about Boolean theorem and explain.

12. (a) Discuss the implementation of the full adder with carry propagation.

Or

- (b) Explain JK flip flop with its characteristic table.

13. (a) Explain Von neumann architecture.

Or

- (b) Write about pipeline in detail.

14. (a) Discuss how cache memory improves the speed of a system.

Or

- (b) Describe how TLB is used for address translation in a virtual memory?

15. (a) Write about polling in detail.

Or

- (b) Illustrate DMA with suitable diagram.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Simplify the following boolean function using K-maps (8)

$$f(p, q, r, s) = \Sigma 0, 2, 4, 5, 6, 8, 9, 11, 13, 15$$

- (ii) Construct the logic circuit for the above simplified function. (7)

Or

- (b) Design a 16 bit up counter and explain with timing diagram. (15)

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## Question Paper Code : S1501

M.Sc. DEGREE EXAMINATION, FEBRUARY/MARCH 2016.

First Semester

Computer Science

DCS 7101 — COMPUTER ORGANIZATION

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. If  $(21002)_8 = (2202)_x$ , then what is a value of x?
2. Subtract -72 from -50 using 2's complement method.
3. Distinguish between combinational circuit and sequential circuit.
4. What is the purpose of NAND gate decoder?
5. Give the micro operation for the fetch and decode phases of the instruction cycle.
6. What is software pipelining?
7. What is the use of cache memory? What are its types?
8. Define principle of locality of reference.
9. Define baud rate.
10. Compare isolated I/O and memory mapped I/O.

PART B — (5 × 16 = 80 marks)

11. (a) (i) What are the various methods used to represent the signed numbers in computer memory? Explain. (10)  
(ii) Discuss the different types of binary codes with examples. (6)

Or

11. (b) Simplify the following Boolean function in sum-of-products form by means of a four variable map. Draw the logic diagram with :
  - (i) NAND-OR gates (8)
  - (ii) NAND gate. (8)

$$F(A,B,C,D) = \sum (0, 2, 8, 9, 10, 11, 14, 15)$$

12. (a) (i) Draw a block diagram for 4 bit bidirectional shift register with parallel load and explain the operation. (10)  
(ii) Give an account on different types of ROM. (6)

Or

- (b) Construct and explain the operation of 4-bit composite arithmetic circuit and discuss the arithmetic micro operations with examples. (16)
13. (a) Explain the various memory-reference instructions and the micro-operations needed for the execution of various memory reference instructions. (16)

Or

- (b) (i) A program with the following sequence of instruction is fed to an instruction pipeline. Identify the hazard and propose the solution. (10)

ADD R1, R2

SUB R4, R1

AND R6, R1

- (ii) Write a note on multi-core processors. (6)

14. (a) What is virtual memory? Explain with a diagram how virtual address can be mapped into physical address using paging. (16)

Or

- (b) What are the types of addressing modes? Explain using examples. (16)

15. (a) Discuss the following :

- (i) Interrupt Vector (8)

- (ii) Buffer chaining. (8)

Or

- (b) What are the different modes of data transfer to and from peripherals? Explain each of them and write the advantages and disadvantages of each method. (16)
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## Question Paper Code : 80501

M.Sc. DEGREE EXAMINATION, AUGUST 2015.

First Semester

Computer Science

DCS 7101 — COMPUTER ORGANIZATION

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What do you mean by canonical form of representation?
2. Draw the logic diagram of 3 input ODD and EVEN functions using XOR gates.
3. What are three state gates?
4. What is a transition table?
5. List the different phases involved in the execution of an instruction.
6. Define instruction rate.
7. What is the need for virtual memory?
8. What is cache coherence?
9. What is an interface?
10. Differentiate between half duplex and full duplex communication.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Find out the truth table of the function  $F = xy + xy' + y'z$ . (8)  
(ii) Simplify the following function using four variable K-maps:  
 $A'B'C'D' + AC'D' + B'CD' + A'BCD + BC'D$ . (8)  
Or
- (b) (i) Express the following function in sum of minterms and product of maxterms :  
 $F(A,B,C,D) = BD' + A'D + BD$  (8)  
(ii) Implement the following Boolean function using NAND — AND logic:  $F(A,B,C,D) = \sum (0,1,2,3,4,8,9,12)$ . (8)

12. (a) Design a BCD to decimal decoder using the unused combinations of the BCD code as don't care conditions. (16)

Or

- (b) (i) With a neat diagram, explain the working of a JK flip flop. (8)  
(ii) Explain the working of a 4 bit UP DOWN counter with appropriate diagrams. (8)

13. (a) With a neat block diagram, explain the functions of various units in a Von Newmann architecture. (16)

Or

- (b) What are instruction formats? What are its types? Explain each one of them with examples. (16)

14. (a) Discuss in detail about the working of Cache memory. (16)

Or

- (b) With diagrams, explain the working of any two page replacement policies. (16)

15. (a) (i) What are the different methods of data transfer? Highlight the salient features of each. (8)  
(ii) Write notes on Multilevel interrupts. (8)

Or

- (b) (i) Explain the buffer chaining method of data transfer with diagrams. (8)  
(ii) What are Interrupt vectors? Explain. (8)
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**Question Paper Code : 22452**

M.Sc. DEGREE EXAMINATION, FEBRUARY/MARCH 2015.

First Semester

Computer Science

DCS 7101 — COMPUTER ORGANIZATION

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert  $(10110.0101)_2$  in to its equivalent decimal value.
2. Draw the gate implementation of the Boolean expression :  $F(X,Y,Z) = X + Y'Z$ .
3. What is meant by static and dynamic memory?
4. Differentiate combinational and sequential logic circuits.
5. Define clock rate and instruction rate.
6. What is an instruction set? What are the parts of an instruction?
7. What is the significance of translation took aside buffer?
8. What is meant by cache coherence?
9. State two differences between full duplex and half duplex communication.
10. What is polling? Give two examples of polling.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Reduce the following using K-map reduction technique :

$$F(W,X,Y,Z) = Y' + W'Z' + XZ'. \quad (8)$$

- (ii) Convert the following Boolean expression in POS form into its equivalent SOP form :

$$F(A,B,C) = (A + B' + C)(A' + B + C'). \quad (8)$$

Or

- (b) (i) Prove the following using Boolean theorems :

$$WY'Z' + WZ + YZ + XYZ = XZ + WZ + WY'. \quad (10)$$

- (ii) Express the following Boolean expression in terms of NAND gates only :

$$F(A,B,C,D) = C'D' + CD + ABD. \quad (6)$$

12. (a) (i) Explain the working of SR flip flop with its characteristic equation and characteristic table. (10)

- (ii) Explain half subtractor with its truth table and implementation. (6)

Or

- (b) (i) Explain 4 bit priority encoder with its truth table and logic diagram. (8)

- (ii) Explain the working of 2 bit synchronous up counter with its timing diagram. (8)

13. (a) (i) Explain the components of a processor and describe the categories of processors. (8)

- (ii) Write a note on pipeline architecture. (8)

Or

- (b) (i) Explain the steps in a fetch-execute cycle. (8)

- (ii) Explain the hardware components required to deal with the concept of stored programs. (8)

14. (a) (i) Describe the mechanism to translate virtual address to physical address. (10)

- (ii) Explain a cache replacement policy. (6)

Or

- (b) (i) Explain the different types of cache memories and describe cache mapping. (8)

- (ii) Describe the organization of physical memory. (8)

15. (a) (i) Describe the mechanisms for handling an interrupt. (10)  
(ii) Describe the characteristics of a bus and explain bus interface. (6)

Or

- (b) (i) Describe buffer chaining and operation chaining for I/O optimization. (10)  
(ii) Explain programmed I/O. (6)
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## Question Paper Code : 46451

M.Sc. DEGREE EXAMINATION, AUGUST 2014.

First Semester

(Computer Science)

DCS 7101 – COMPUTER ORGANIZATION

(Regulation 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert  $(22.64)_{10}$  into its equivalent hexadecimal value.
2. Express NAND gate in terms of NOR gates only.
3. What is carry propagation delay in binary adder?
4. Give the characteristic equation and characteristic table of RS flip flop.
5. What are stored programs?
6. Define clock rate.
7. What is the need for address translation?
8. State the role of cache memory.
9. What are interrupt vectors?
10. What is meant by chaining?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Reduce the following using K-map reduction technique :  
$$F(A,B,C,D) = \sum(0, 1, 4, 8, 9, 10). \quad (8)$$
- (ii) Give the NOR representation of  $F(A,B,C) = \sum(0, 1, 3, 5). \quad (8)$

Or

- (b) Implement the following Boolean expression with exclusive-OR and AND gates only.

$$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D \quad (16)$$

12. (a) (i) Explain the working of JK-flip flop with its characteristic table and equation. (10)  
(ii) Implement  $\sum(1, 3, 5, 6)$  using 2:1 Mux. (6)

Or

- (b) (i) Explain the characteristic table and characteristic equation of a full adder circuit. Also design a combinational circuit for full adder using two half adders and OR gate. (10)  
(ii) Design a 3:8 decoder using NOR gates. (6)
13. (a) (i) Compare pipeline and multicore processors. (10)  
(ii) Explain the various instruction formats. (6)

Or

- (b) (i) Explain the instruction fetch – execute cycle with timing diagram. (10)  
(ii) Describe Von Neumann architecture. (6)
14. (a) (i) Explain paging. (8)  
(ii) Describe cache mapping. (8)

Or

- (b) (i) Explain the concept of virtual memory. (8)  
(ii) Explain LRU replacement strategy. (8)
15. (a) Compare  
(i) Programmed I/O and interrupt driven I/O. (10)  
(ii) Serial and Parallel data transfer. (6)

Or

- (b) Write notes on the following :  
(i) DMA (10)  
(ii) Polling. (6)
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