Towards an Efficient BCI Simulation and Development Platform

ATHENA

Yale NSF Duke

Shaan Yadav[1], Muhammed Ugur[2], Raghav Pothukuchi[2], Abhishek Bhattacharjee[2]

[1]Duke University; [2]Computer Systems Lab, Yale University shaan.yadav@duke.edu

Overview

Brain computer interfaces (BCIs) provide opportunities to treat neurological disorders, and understand how the brain functions. BCIs today are created as hyper specific ASICs treating a single disease. More general-purpose architectures such as SCALO [1] are needed to treat more diseases and provide more personalized treatment.

Traditonally, these systems have been difficult to develop due to the lack of infrastructure to solve such a high dimensional problem subject to strict constraints such as power and latency.

We aim to build a modular simulator that allows neuroengineers to develop and evaluate many different hardware compute options for next generation BCI chips, without needing to become expert hardware engineers themselves.

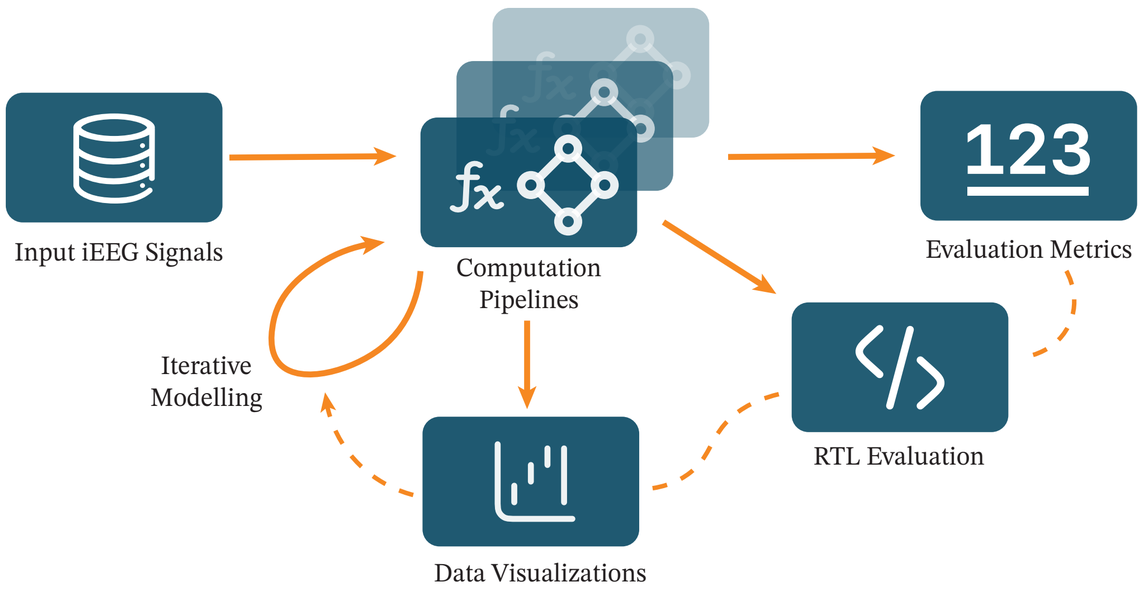

Figure 1: Neuroengineer workflow for the simulator

Pipelines

A *pipeline* is a directed graph of PEs, set up for a specific function. This creates a network of accelerators that can then be evaluated for validity and optimized for performance.

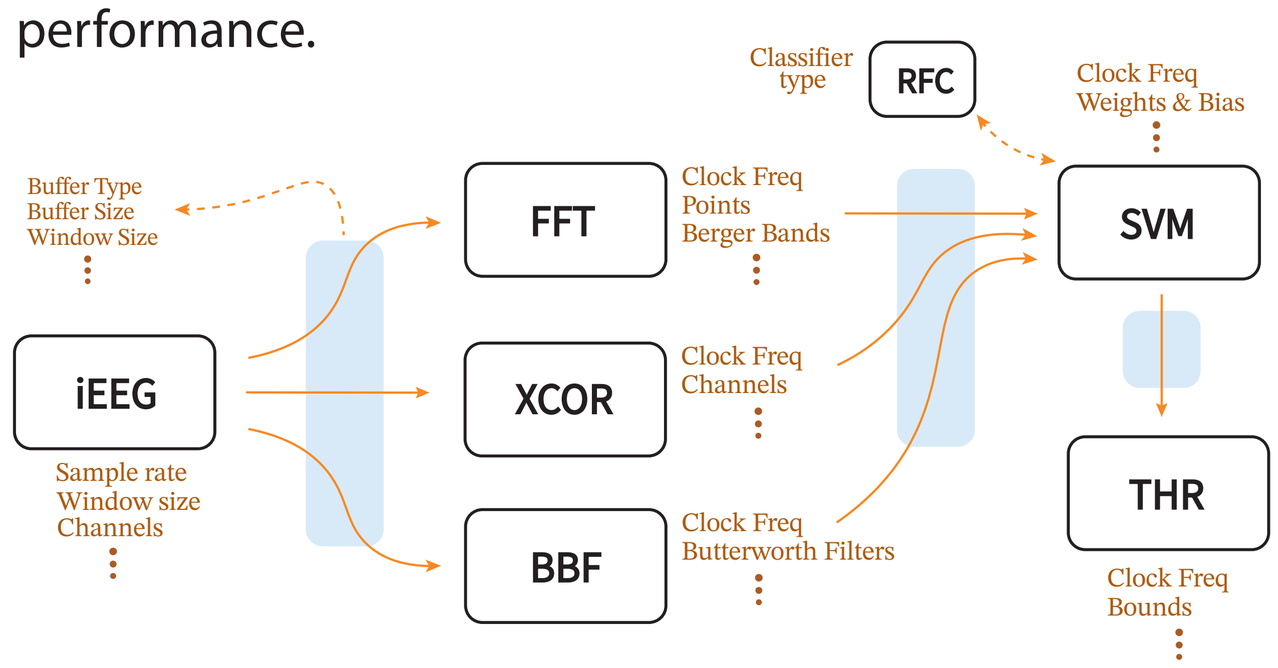

Figure 3: Shiao et al. [2] inspired pipeline for seizure detection with its component PEs and all the parameters that can affect the pipeline's performance; Our tool allows for the development of such pipelines without hardware expertise

Future Vision

- Open-source tool
- Expansive PE library
- Integrating multi-pipeline systems
- Automated pipeline optimization
- Accurate hardware estimations
- Verifying designs with animal/human testing

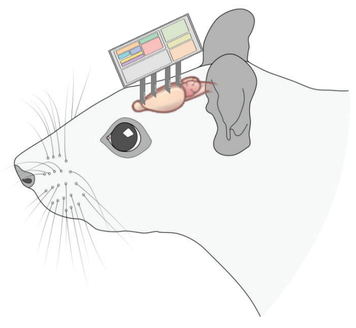

Figure 4: Lab Rat Testing of BCI designs

Processing Elements

Processing Elements (PEs) are hardware accelerators that are the main building block used in the simulator. Graphs of PEs are made to create specific applications for BCIs.

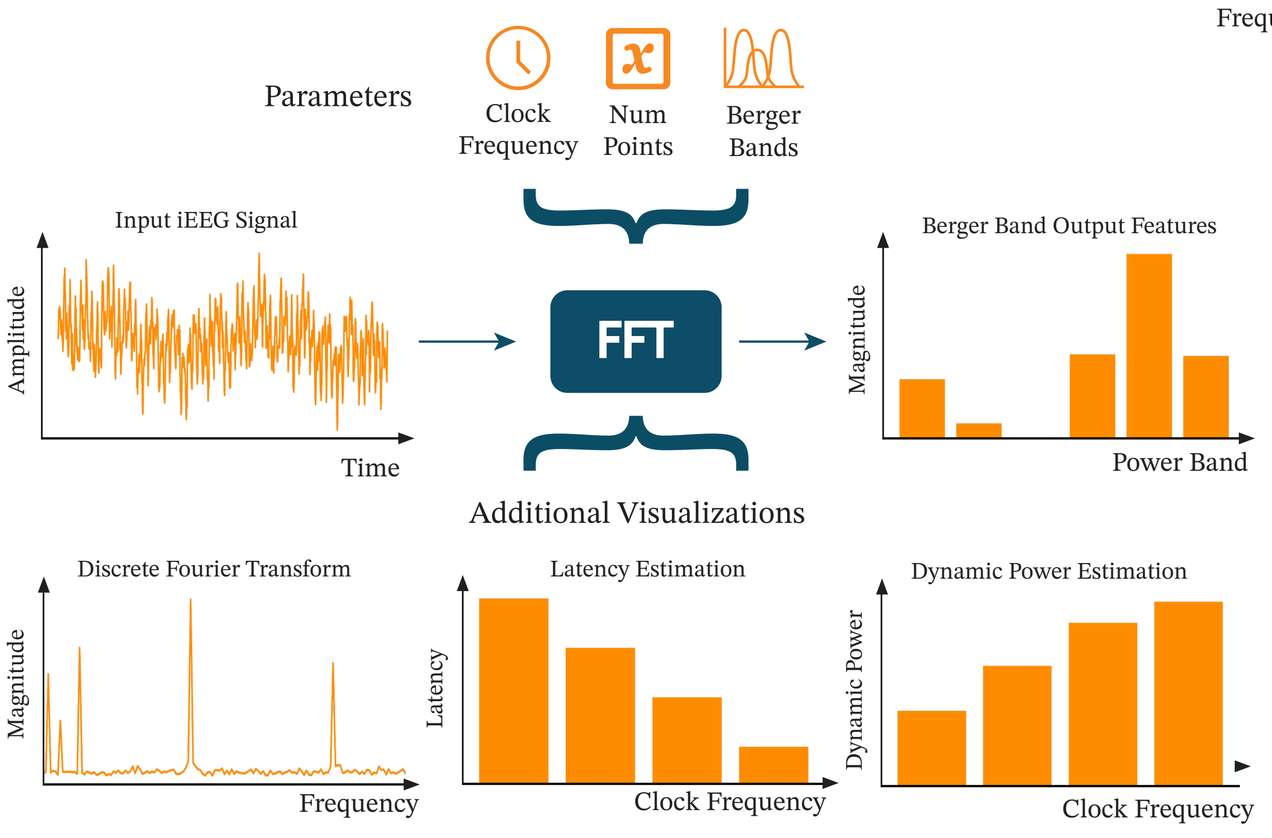

Figure 2: A Fast Fourier Transform Processing Element and a subset of the visualizations generated

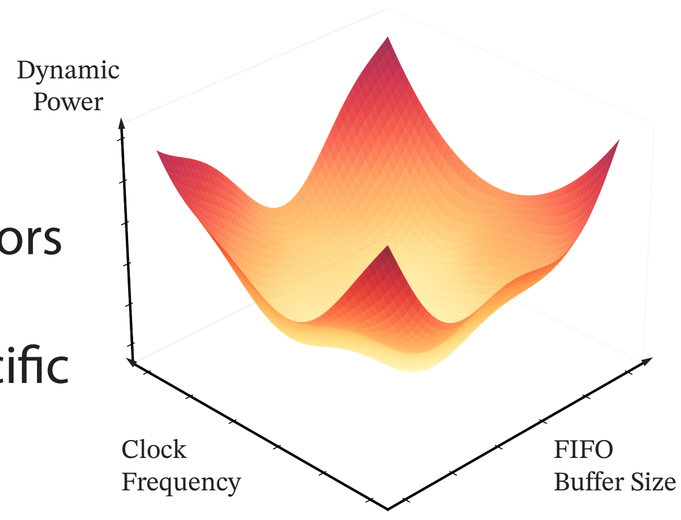

Figure 5: Automated optimization of pipeline systems

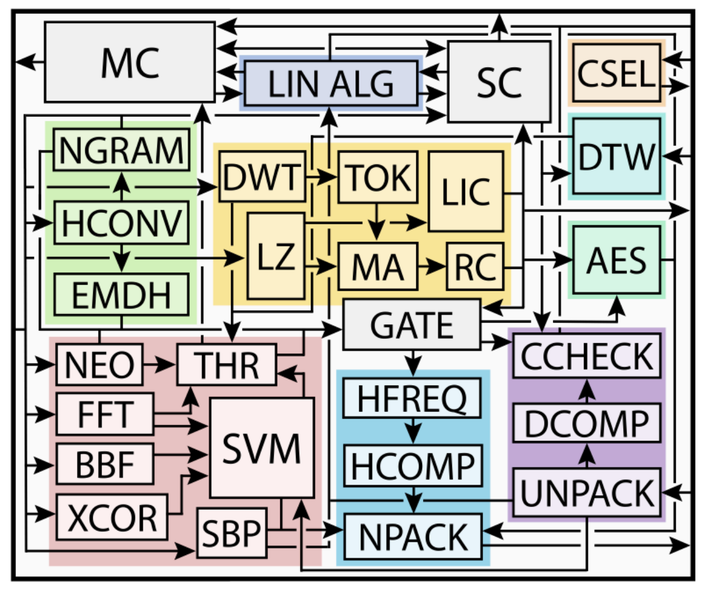

Figure 6: A diagram of the SCALO chip with its multi-pipeline system

References & Acknowledgements

Thank you to Muhammed Ugur, Raghav Pothukuchi and Abhishek Bhattacharjee for their guidance and support through this project, and to the Athena AI Institute for providing a platform for this research.

[1] Karthik Sriram, Raghavendra Pradyumna Pothukuchi, Michał Gerasimiuk, Muhammed Ugur, Oliver Ye, Rajit Manohar, Anurag Khandelwal, and Abhishek Bhattacharjee. SCALO: An Accelerator-Rich Distributed System for Scalable Brain-Computer Interfacing. ISCA '23. June 17–21, 2023

[2] Shiao HT, Cherkassky V, Lee J, Veber B, Patterson EE, Brinkmann BH, Worrell GA. SVM-Based System for Prediction of Epileptic Seizures From iEEG Signals. IEEE Trans Biomed Eng. 2017.