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Shaan (Aasmaan) Yadav

github & website:
github.com/shaan106
shaan106.github.io

Education

Duke University — Expected May 2026
BSE:** Double major in **Electrical and Computer Engineering & Computer Science — *Durham, NC, USA*
***4.0 GPA** | Dean's List with Distinction*

Eton College — September 2017 – June 2022
***4.0 GPA** (all A* grades) | Oppidan (Academic) Scholar | House Captain | President of Scientific Society* — *Windsor, Berkshire, UK*

Experience

BCI Architecture Researcher — May 2024 – Present
Yale Computer Systems Lab — *Yale University, CT, USA*

- Research under Prof. Abhishek Bhattacharjee on Brain Computer Interface chips
- Leading 4 person research project for creating a modular globally-asynchronous-locally-synchronous (GALS) hardware-level accelerator set simulator for BCI specific algorithms with built in accelerator optimization tools
- Implementing a custom Python-based RTL simulation framework using OpenSTA to enable verification and evaluation of hardware accelerators in a 130nm Skywater based process
- Paper being submitted to a Neuroengineering conference November, and a follow-up to a Systems conference in 2025

Computer Architecture Researcher — August 2024 – present
Hilton Lab — *Duke University, NC, USA*

- Research under Prof Andrew Hilton on a novel leading-trailing checker chip architecture to enable aggressive microarchitecture designs without compromising chip accuracy or reliability
- Microarchitecture modelling done using gem5, extending OOO CPU components in C++ and creating novel components (ie custom cache hierarchies, validation schemes and instruction commit paths) for TSV-based checker chip

Teaching Assistant — December 2023 – Present
Duke Electrical & Computer Engineering — *Duke University, NC, USA*

- Teaching Assistant for CS/ECE 350: Digital Systems, previously for Computer Architecture and Fundamentals of ECE
- Guiding students in FPGA and gtkwave demos, providing breadboard and circuitry training, solving and analyzing boolean theory, and mentoring final FPGA-based projects
- Leading office hours sessions for ∼300 students every week, help create and grade quizzes & exams, assist with lectures

Raiz Vertical Farms — June 2023 – August 2023
Engineering Intern — *Lisbon, Portugal*

- Built computational models using PyTorch and self-collected data to show optimal combination of liquid flow rate, temperature and luminosity for maximising yield, leading to an annual yield increase of about 0.2 kg per square meter

Relevant Courses & Skills

Courses – Digital Systems & FPGAs [A+], Computer Architecture [A+], Signals & Systems [A], Multivar Calc. [A], Advanced Comp. Architecture (Grad.) [Fall '24], Microelectronic Devices [Fall '24], Linear Algebra [A]

Languages – Python, Verilog, C/C++, Java, HTML/CSS, Matlab, Swift, Lua, Assembly

Frameworks – Gem5, OpenSTA, CUDA, Skywater-PDK, Linux, Shell, FPGAs, PyTorch, Git, HPCs

Relevant Projects

***more projects:** shaan106.github.io*

FPGA Boids — https://shaan106.github.io/projects.html#boids_fpga

- A highly efficient FPGA implementation of the boids algorithm (modelling flocking behaviour in multi-agent environments)
- Designed and implemented parallel "BPU" computation units, and a custom C to assembly compiler, and a double-buffered VGA display wrapper to maximize refresh rate
- Full, in depth documentation: github.com/Shaan106/Boids_FPGA/

5-stage pipelined bypassed CPU — https://shaan106.github.io/projects.html#verilog_mips_cpu

- Implemented a MIPS inspired processor built only using structural verilog on a Xilinx FPGA
- Design is a 32-bit 100MHz processor, fully Pipelined and Bypassed to maximize throughput. Design is hazard handling and includes custom arithmetic units such as a Wallace Tree multiplier, Restoring Division Divider and a CLA adder

Other Experiences

Palantir *(Data Science Intern, '22)*, **Jaipur Foot** *(Field Volunteer, '21)*, **TeensInAI** *(ML Theory Teacher, '20-'21)*, **BBC** *(Intern, '19)*, Rock Climbing *(since '22)*, Fencing *(since '18)*