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Department of Computer Science and Engineering
B. Sc. (Engineering) in Computer Science and Engineering
Special Repeat Examination 2018
Level 3 Semester I, Credit: 3.0
Course Code: CSE 309, Course Title: Computer Architecture

Time: 03 hours | Total Marks: 90

[N.B. The figure in the right margin indicates the marks allocated for respective question. Split answer of any question will not be accepted.]

SECTION-A

(Answer any three from the following questions.)

1. (a) Discuss computer architecture. Mention the importance of studying computer architecture in Computer Science and Engineering. 2+3

   (b) Draw the architecture of a modern computer. Describe major structural components of a computer system 2+3

   (c) Define: CPU time, clock cycle, clock period, MIPS, and Opcode. 5

2. (a) Define bus. Distinguish between single-bus system and multi-bus system. 1+4

   (b) What is CPU register? Describe the functionality of its different types. 1+4

   (c) What is pipelining? Describe the functions of each of the five pipelined stages. 1+4

3. (a) What are the main features of Booth's algorithm? Draw a flowchart for Unsigned Binary Division. 1+4

   (b) Consider *R1* as a processor register containing binary data of 10011010. Now, what will be output if the processor executes the following operations on *R1*? 1+2+2

   i. Logical left shift
   ii. Arithmetic right shift
   iii. Right rotate, if the MSB is treated as sign bit

   (c) What is machine instruction? Draw instruction cycle state diagram and describe in short. 1+4

4. (a) Why floating point number is more difficult to represent and process than integer in computer? Describe the difficulties faced during floating point arithmetic. 2+3

   (b) Consider the execution of a program which results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction Mix and the CPI for each instruction type are given below based on the result of a program trace experiment: 2+3

Instruction Type	CPI	Instruction Mix (%)
Arithmetic and logic	1	60
Load/store with cache hit	2	18
Branch	4	12
Memory reference with cache miss	8	10

   Calculate average CPI, and corresponding MIPS rate.

   (c) What is CISC and RISC architecture? Describe similarities and differences between them 2+3

SECTION-B

(Answer any three from the following questions.)

1. (a) What is Parallel Processing? Describe categories of a computer system proposed by Flynn. 1+4

   (b) Define PCI and SCSI bus. Mention their role(s) in computer architecture. 2+3

   (c) Mention some key benefits of clustering. Describe the impact of Moore's law on computer architecture. 2+3

2. (a) Discuss the basic performance measure equation of a computer. A processor with clock frequency of 1.25 GHz and that of for another processor is 1.05 GHz. Which is better in performance? Explain. 2+3

   (b) Draw and describe a typical DMA block diagram 2+3

   (c) What is cache memory? Describe cache read operation with necessary diagram. 1+4

3. (a) Draw the hardware architecture for performing addition and subtraction by the processor. Show the steps for multiplying -4 by -2 using Booth's algorithm. 2+3

   (b) What is addressing mode? How do addressing modes affect the instruction pipelining? 1+4

   (c) Distinguish between shared memory multiprocessor and message-passing multiprocessor. Draw the basic structure of a symmetric shared memory multiprocessor. 2+3

4. (a) What is the difference between random access and non-random access memory? Derive the equation for the time taken to read n bits for a non-random memory. 2+3

   (b) What is SSD? Assume a memory access to main memory on a cache "miss" takes 20 ns and a memory access to the cache on a cache "hit" takes 2 ns. If 75% of the processor's memory requests result in a cache "hit", what is the average memory access time? 1+4

   (c) Suppose you have a data file of size 512 MB, defend whether it is possible to store that file in a properly formatted disk of size 512 MB or not. Draw the basic block diagram of external devices for a computer system. 2+3