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Department of Computer Science & Engineering
B. Sc. in Electronics & Communication Engineering (B. Sc. ECE)
Semester Final Examination 2017 (Jan-Jun)
Level 3 Semester I, Course Code: CSE 317, Credit: 3.0
Course Title: Microprocessor and Embedded System Design

Time: 3 Hours **Total Marks: 90**

Figure on the right side indicates the mark for the respective question.
Split answer is not allowed.
Answer any three questions.

Section - A

1. (a)	Define Microprocessor and Instruction Set.		2.5x2 =5
(b)	Describe the instruction: **MVI A, 32H**. If this instruction is executed in 8085 with clock frequency of 2 MHz, calculate its execution time.		2+3= 5
(c)	Write an assembly subroutine to transfer 100 bytes of data that is stored in memory location starting from C000H to memory location starting from F000H.		5
2. (a)	Explain why the number of output ports in the peripheral-mapped I/O is restricted to 256 ports.		4
(b)	Explain the machine cycles with proper timing diagram of the instruction – **LXI B, FF00H**. The opcode is 01H.		5
(c)	Explain the following initialisation instructions of the 8259A Interrupt Controller.		3x2= 6
	i) MVI A, 74H	; ICW1	
	ii) MVI A, 20H	; ICW2	
3. (a)	Can the microprocessor be interrupted again before the completion of the ISR?		4
(b)	List the necessary conditions to generate INTR when port A of the 8255A PPI is set up as an output port in Mode 1. Support your answer with proper timing waveforms.		6
(c)	Write a BSR control word subroutine of 8255A PPI to set bits PC7 and PC3 and reset them after 10 ms. Assume that the control register address is 83H, and that a delay subroutine is available at location F001H to provide desired 10 ms delay.		5
4. (a)	What is Pending Interrupt? Describe the mechanism how you check if RST 6.5 is pending or not.		2+4= 6
(b)	Describe different priority modes of 8259A.		4
(c)	Given that maskable-vectored interrupts RST 5.5, 6.5, and 7.5 can be enabled/disabled individually, write proper assembly code to enable all interrupts in an 8085 system.		5

Section – B

Split answer is not allowed.

Answer any three questions.

1. (a) Why data bus and address bus in 8085 microprocessor are multiplexed. How this multiplexing is achieved? 2+4= 6

(b) Describe the steps of 8085 interrupt process to handle maskable non-vectored interrupt in INTR pin. 4

(c) Draw 8085 timing diagram of instruction: **OUT 01H**. 5

2. (a) Specify new features introduced to Intel 80386/80486 and Pentium™ processors. 2.5x2 =5

(b) Specify the Loading Format and Modes of 8155 timer. 3x2= 6

(c) Identify the mode 0 control word of 8255A to configure port A and port C_U as input ports and port B and port C_L as output ports. 4

3. (a) Write an assembly code to make a loop to count from FF down to zero. Calculate delay time of this loop if the clock frequency of 8085 is 3 MHz. 3x2= 6

(b) Given that 8237A DMA Controller has four channels and two 16-bit registers are associated with each channel. Specify the functions of these registers per channel. 5

(c) Distinguish between minimum mode and maximum mode of 8086 microprocessor. 4

4. (a) Define memory register M with proper assembly code example. 4

(b) Differentiate between JMP and CALL instructions. 5

(c) Given that 8085 instructions are not of same size. Identify different sized instructions with proper example. 6