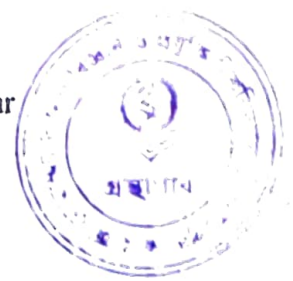


Hajee Mohammad Danesh Science and Technology University, Dinajpur
Department of Computer Science and Engineering
B. Sc. in CSE

Semester Final Examination 2016 (Jan-Jun)
Level 3 Semester I, Course Code: CSE 309, Credit: 3.0
Course Title: Computer Architecture (Theoretical)



Time: 3 Hours

Total Marks: 90

[N.B. The figure in the right margin indicates the marks allocated for respective question, all the portions of each question must be answered consecutively]

Section-A
Answer any THREE

1. a) What is computer architecture? Describe major structural components of a computer system. 1+4
b) Define: CPU time, clock cycle, clock period, CPI, MIPS, and Opcode. 6
c) What is CPU register? Describe the functionality of its different types. 1+3
2. a) What are the main features of Booth's algorithm? 3
b) Why floating point number is more difficult to represent and process than integer? Describe the difficulties faced when we use floating point arithmetic. 2+6
c) Draw a flowchart for Unsigned Binary Division. 4
3. a) What is machine instruction? Draw instruction cycle state diagram and describe in short. 1+4
b) What is the difference between an arithmetic shift and a logical shift? 3
c) What is CISC and RISC architecture? Describe similarities and differences between them. 2+5
4. a) What is Parallel Processing? Describe categories of a computer system proposed by Flynn. 1+4
b) Describe some of the key benefits of clustering. 3
c) What is instruction pipelining? 2
d) Describe the following terms: Dual-core, Core 2 Duo, Pentium D, Core i3, and Core i5. 5

Section-B

Answer any THREE

1. a) Distinguish between computer organization and computer architecture. 4
 b) What is the different memory types based on the method of accessing? Describe each of them. 2+6
 c) What is cache memory? Describe cache read operation with necessary diagram. 1+3
2. a) What is semiconductor memory? Describe its different types. 4
 b) Distinguish between SRAM and DRAM. 7
 c) Describe the procedure of i) data written onto a magnetic disk and ii) data read from a magnetic disk. 1+3
3. a) Define parallel processing. What are the steps required for a pipelined processor to process the instruction? 3
 b) How addressing modes affect the instruction pipelining? 3+3
 c) Distinguish between shared memory multiprocessor and message-passing multiprocessor. Draw the basic structure of a symmetric shared memory multiprocessor. 2
 d) What is multicore processor? How it works? 4
4. a) Consider the execution of a program which results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix (%)
Arithmetic and logic	1	60
Load/store with cache hit	2	18
Branch	4	12
Memory reference with cache miss	8	10

Calculate average CPI, and corresponding MIPS rate.

- b) What is Programmed and Interrupt-Driven I/O? Describe Drawbacks of them in short. 3+2
- c) Define interrupt service routine. 2
- d) Describe the role of interrupts in instruction cycle. How it transfers control among user program? 2+2