2EC501

VLSI DESIGN

"Design CMOS circuit for Boolean Expression"
(F = AB' + CD'A)

SPECIAL ASSIGNMENT REPORT

SUBMITTED BY

SHABBIR. M. AGLODIYA 21BEC006

ELECTRONICS & COMMUNICATION ENGINEERING DEPT.

NIRMA UNIVERSITY

PROBLEM: **F = AB' + CD'A using CMOS**

Assumption: All the transistors have been sized to give a worst-case output resistance of 20 K for the worst-case input pattern.

Introduction:

A Boolean expression is a logical statement that is either TRUE and FALSE. The logic symbols "0" and "1" being used to represent a digital input or output, we can also use them as constants for a permanently "Open" or "Closed" circuit or contact respectively.

A set of rules or laws of Boolean Algebra expressions have been invented to help reduce the number of logic gates needed to perform a particular logic operation resulting in a list of functions or theorems known commonly as the laws of Boolean Algebra.

Boolean Algebra is the mathematics we use to analyze digital gates and circuits. We can use these "Laws of Boolean" to both reduce and specify a complex Boolean expression in an attempt to reduce the number of logics based on logic that has its own set of rules or laws which are used to define and reduce Boolean expression.

The variables used in Boolean Algebra only have one of two possible values, a logic "0"and a logic "1" but an expression can have an infinite number of variables all labelled individually to represent inputs to the expression. Most of Boolean expression use AND, OR and NOT operator. A Boolean expression can consist of Boolean data, such as the following:

- Boolean values
- Boolean variables of formulas
- Functions that yield Boolean results
- Boolean values calculated by comparison operators

Optimized Boolean Equation:

F = AB'+ ACD'
F = A(B'+CD')

The above function requires total 5 logic gates.
2 NOT Gates, 2 AND Gates and 1 OR Gate.

Optimized gate level circuit diagram and transistor level:

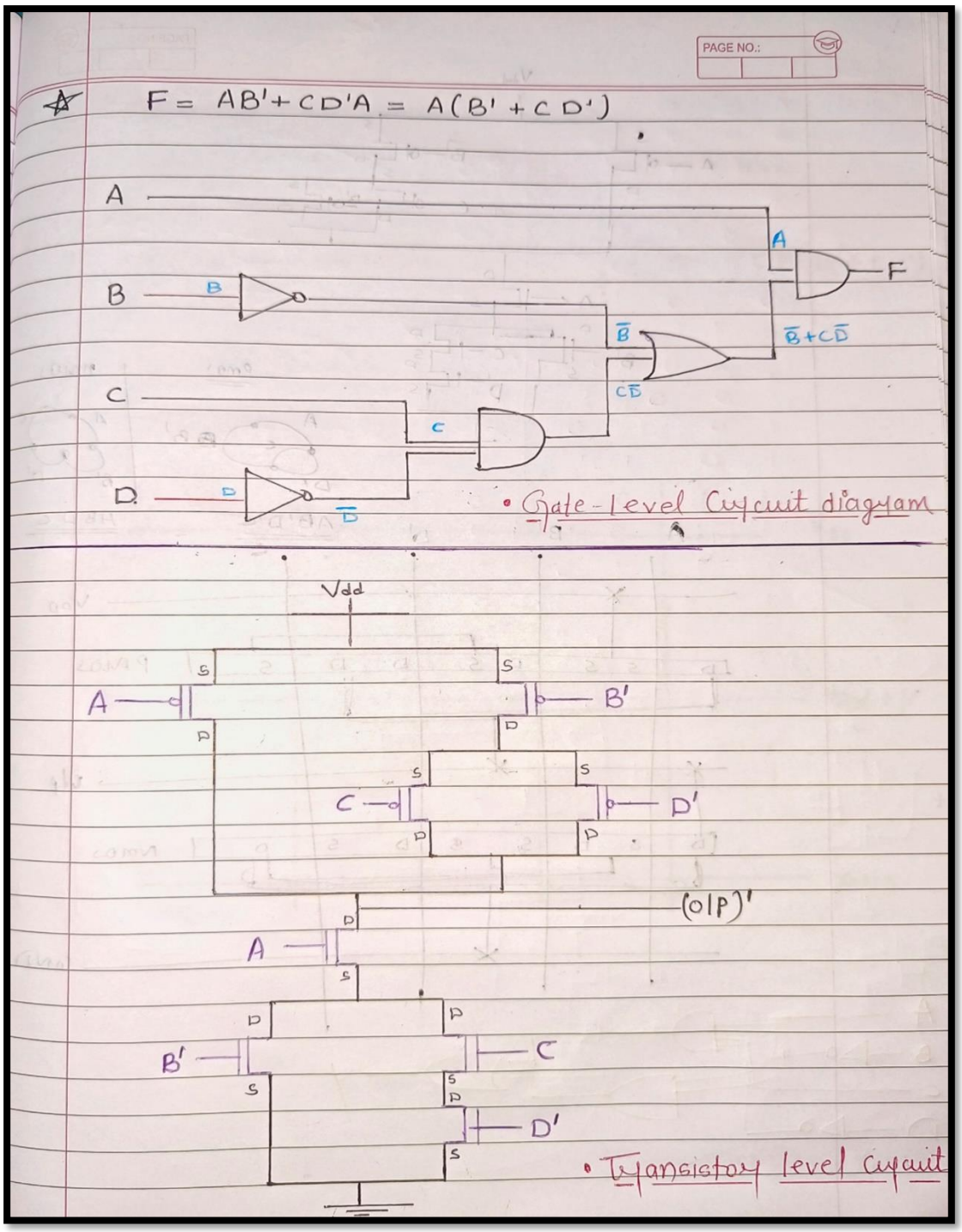


Figure 1 Gate level and Transistor level circuit

Truth Table:

A	B	C	D	B’	D’	CD’	B’ + CD’	A(B’+CD’)
0	0	0	0	1	1	0	1	0
0	0	0	1	1	0	0	1	0
0	0	1	0	1	1	1	1	0
0	0	1	1	1	0	0	1	0
0	1	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	0	1	1	1	0
0	1	1	1	0	0	0	0	0
1	0	0	0	1	1	0	1	1
1	0	0	1	1	0	0	1	1
1	0	1	0	1	1	1	1	1
1	0	1	1	1	0	0	1	1
1	1	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	0	0	1	1	1
1	1	1	1	0	0	0	0	0

Stick Diagram:

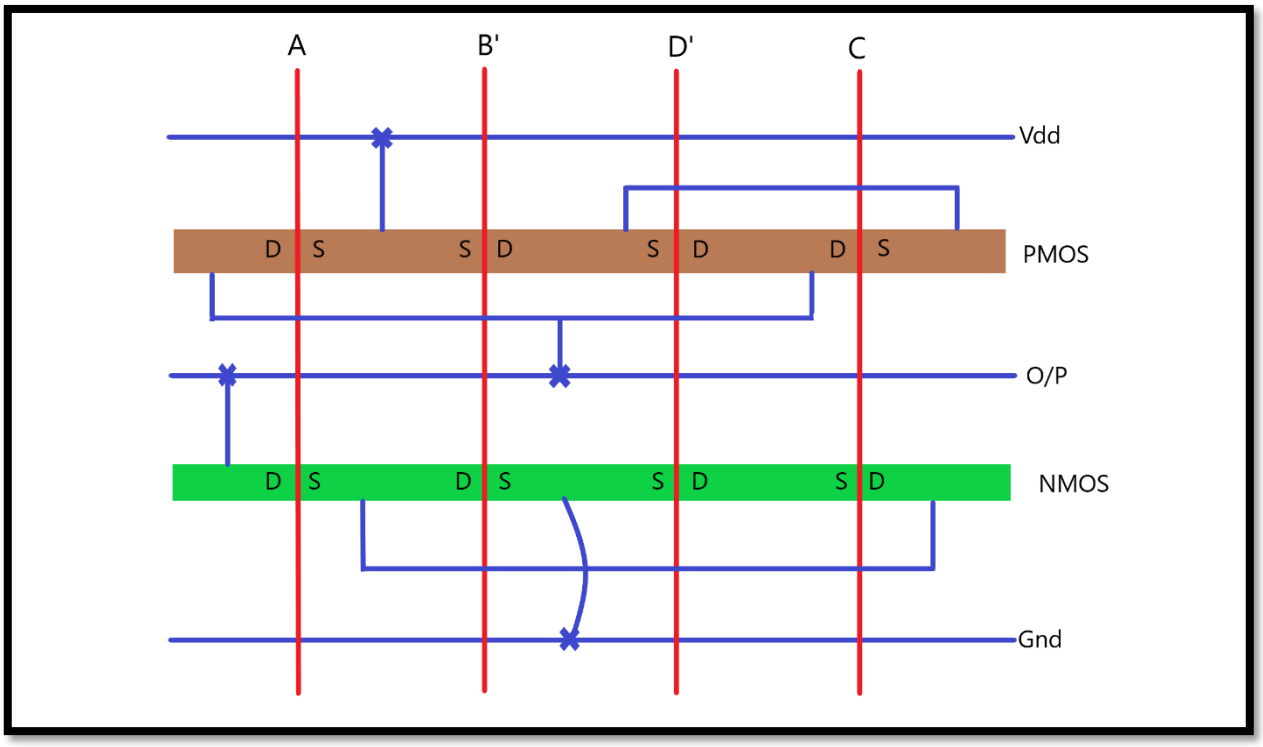


Figure 2 Stick diagram

Q) Various levels of VOL corresponding to various transistor statuses

The value of Vol is determined by nMOS. By analysing the various nMOS transistor statuses, there can be three different values of Vol depending on the three different paths available.

ON Transistors	Equivalent resistance	Different values of Vol
AB’	40K	Vol_1
ACD’	60K	Vol_2
AB’D’C	100/3K	Vol_3

Vol_1>Vol_2>Vol_3

Q) For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

ON Transistors	Equivalent resistance	Different values of Vol
AB’	40K	Vol_1
ACD’	60K	Vol_2
AB’D’C	100/3K	Vol_3

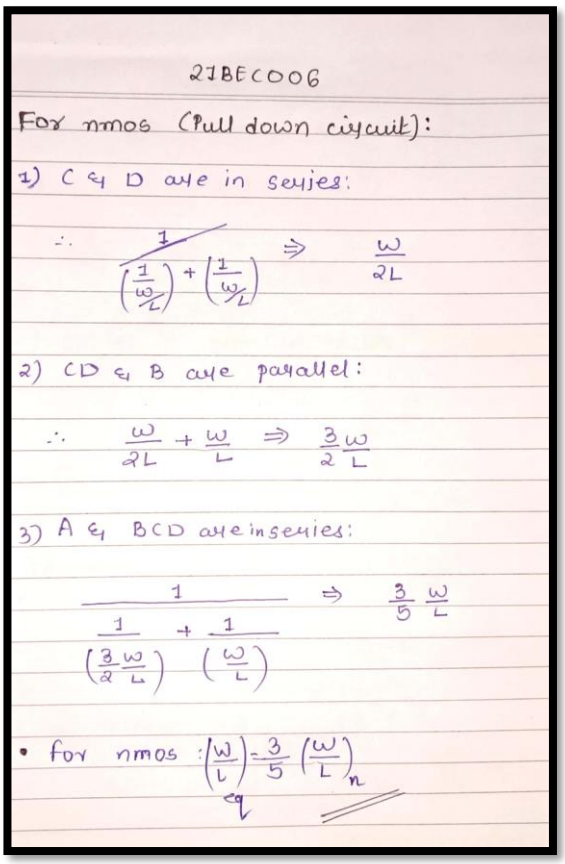
The NMOS determines the lowest output value of Vol. So, when the output is low, the lowest output resistance is found by considering the different transistor status. Here, the lowest output resistance is set at 100/3K.

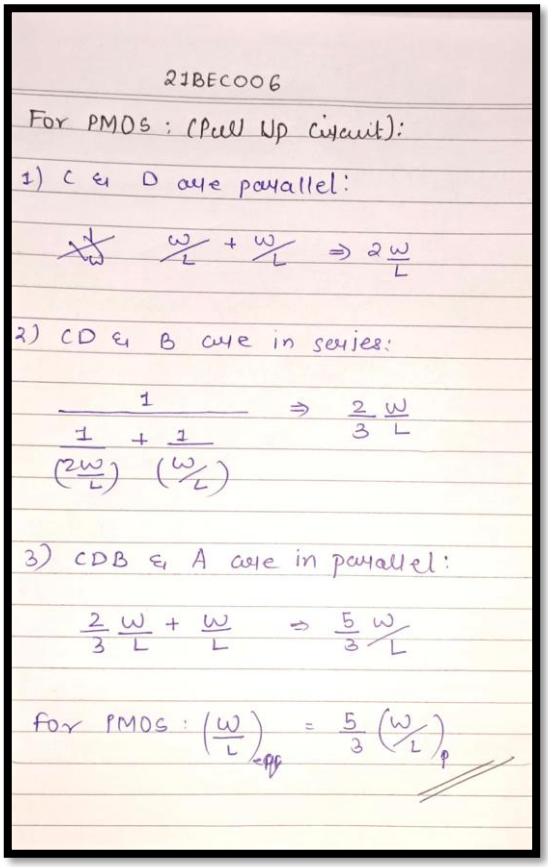
Q) For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

ON Transistors	Equivalent resistance	Different values of Voh
A	20K	Voh_1
B’D’ B’C	40K	Voh_2
AB’C AB’D’	40/3K	Voh_3
AB’CD’	60/5K	Voh_4

The highest output value i.e., VOH is decided by the PMOS. So, by considering the different statues of PMOS transistor, the lowest output resistance is obtained when all the PMOS are ON. The value of the lowest output resistance is 60/5K.

Equivalent Inverter Circuit:





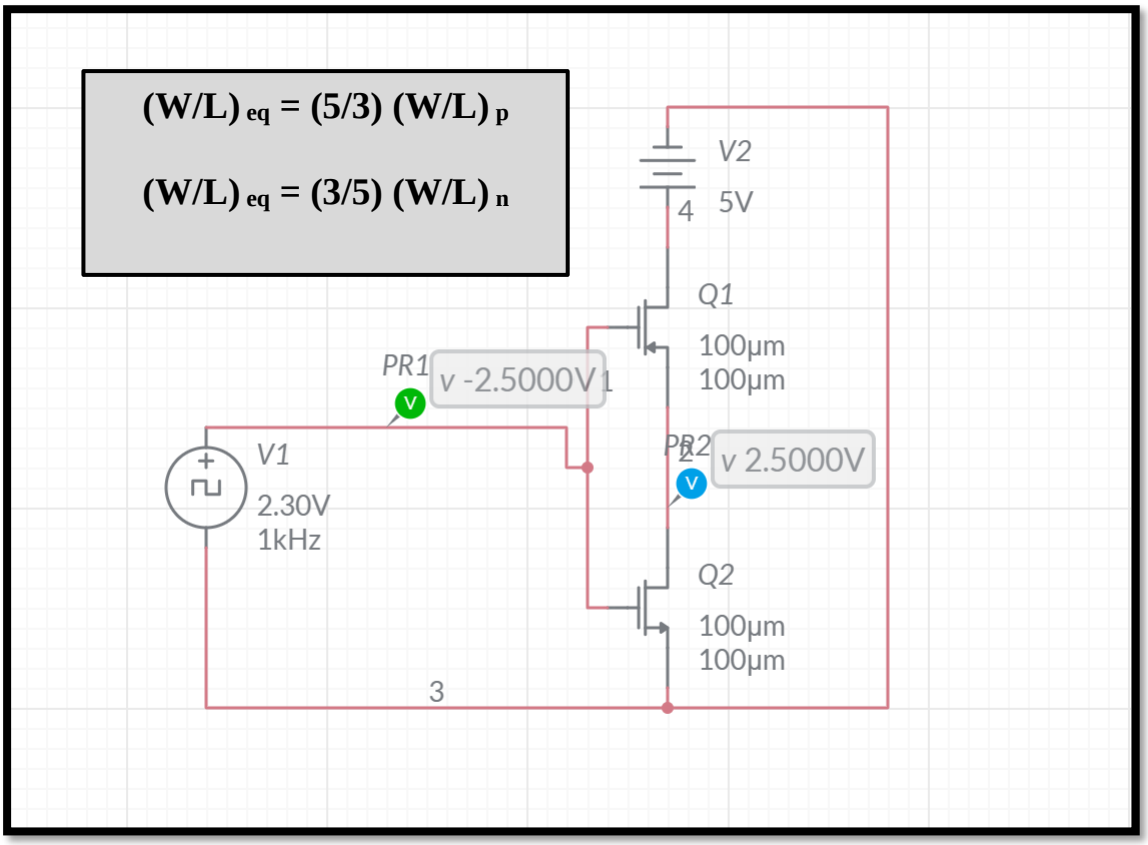
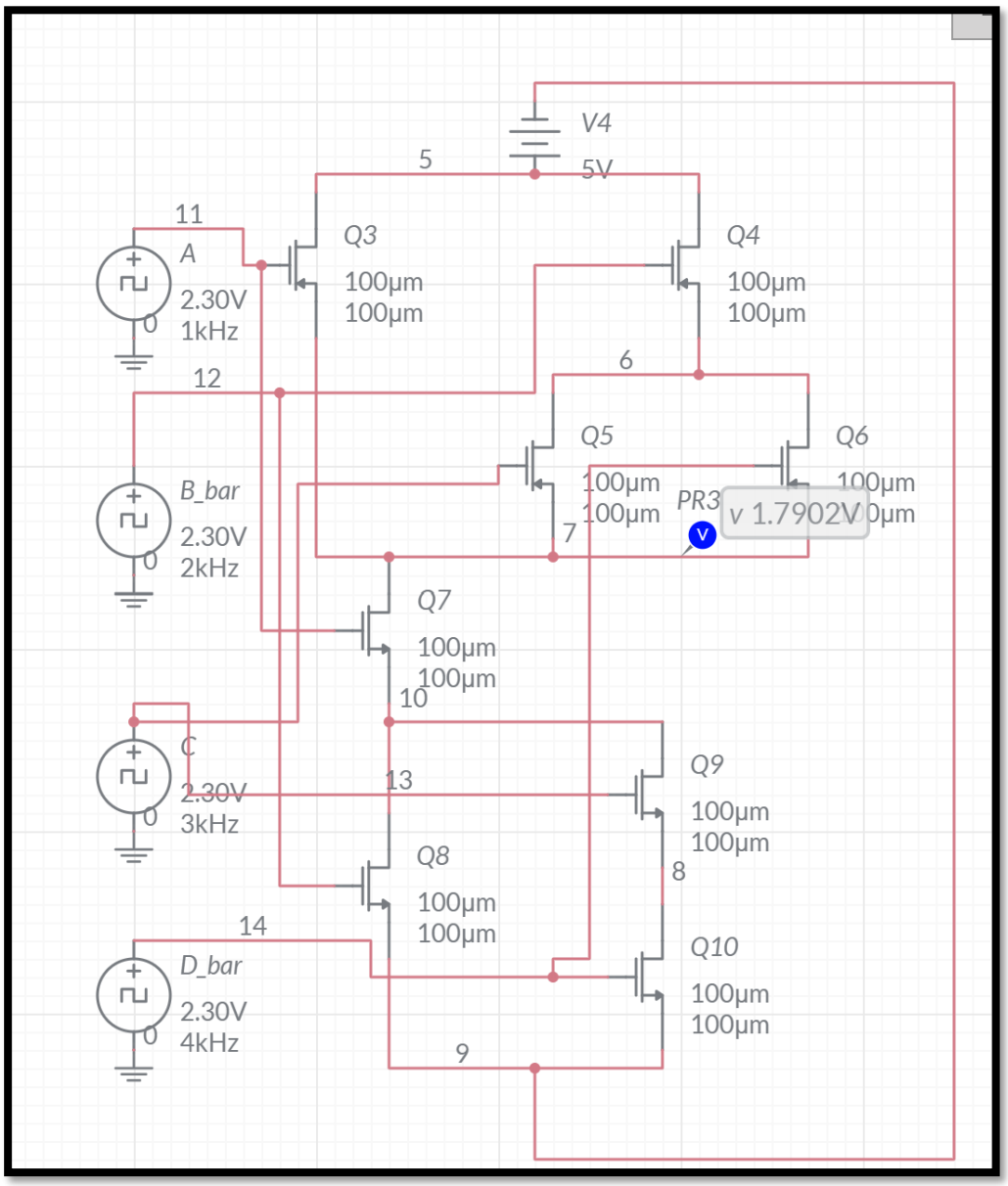


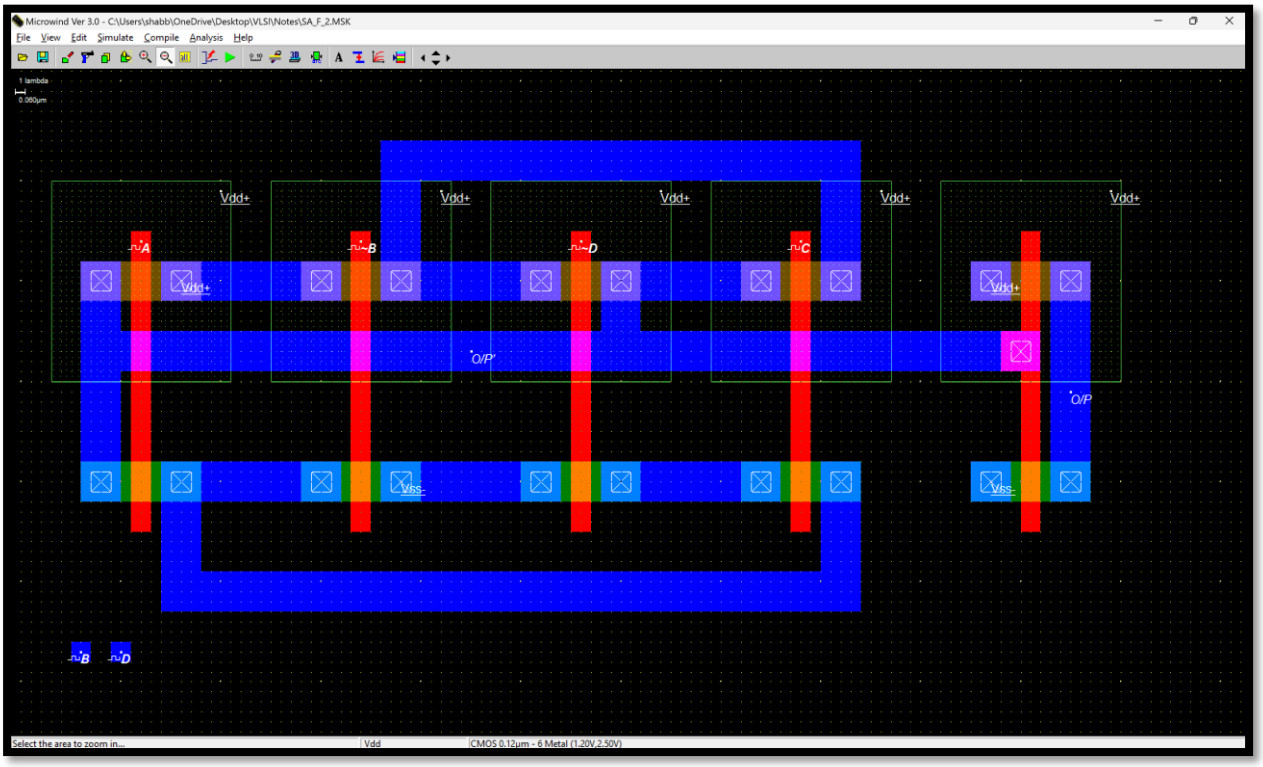
Figure 3 Equivalent Inverter Circuit

Circuit Diagram in Simulator:



Boolean Expression in Microwind Tool:

Without using readymade transistors:



Using readymade transistors:

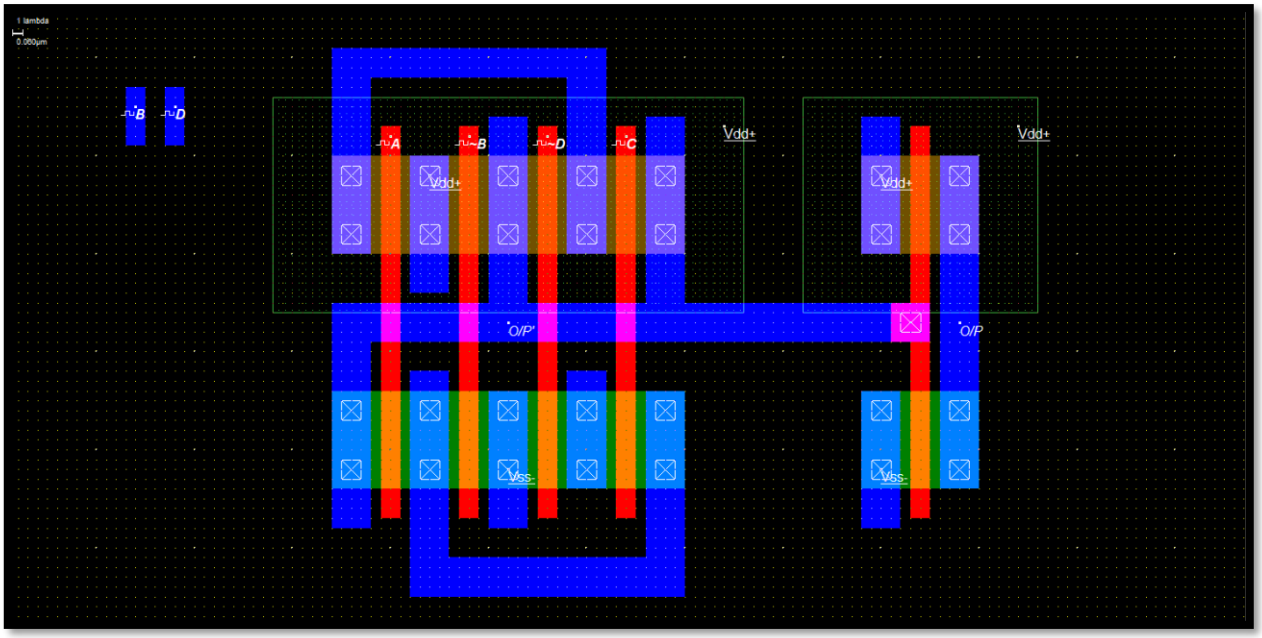
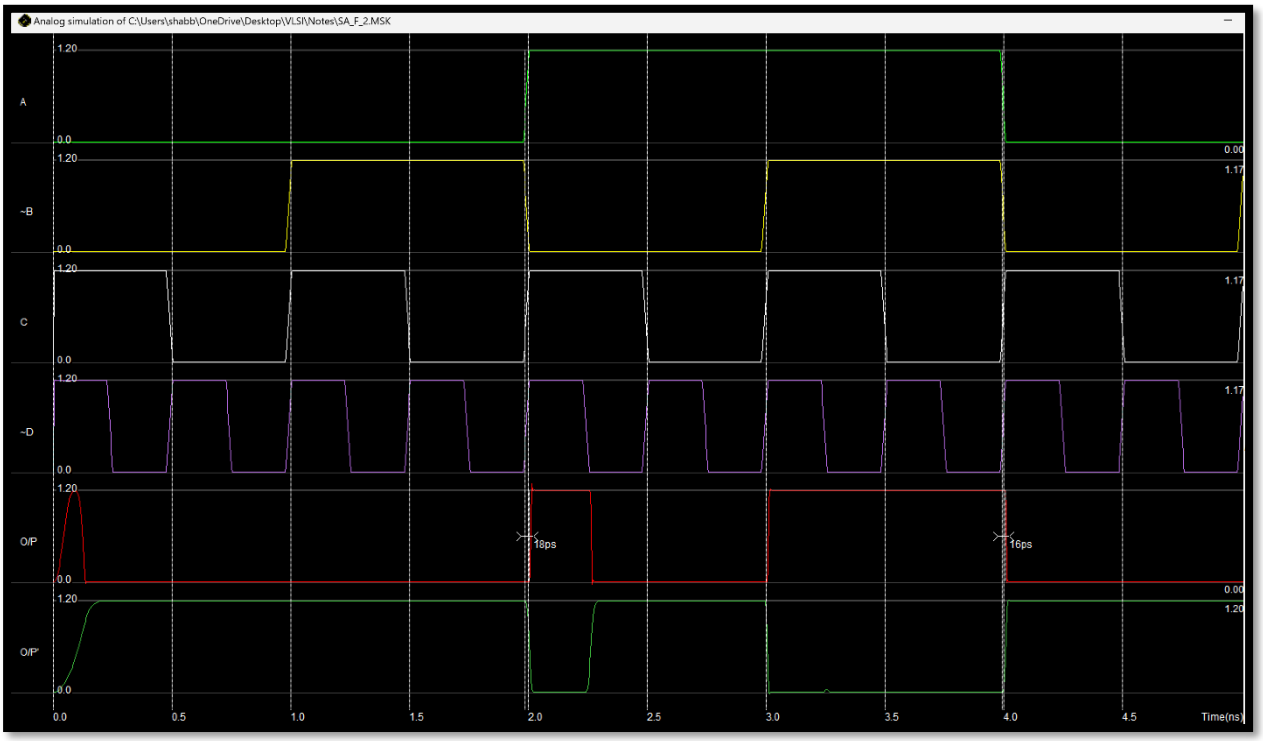


Figure 4 Layout in Microwind tool

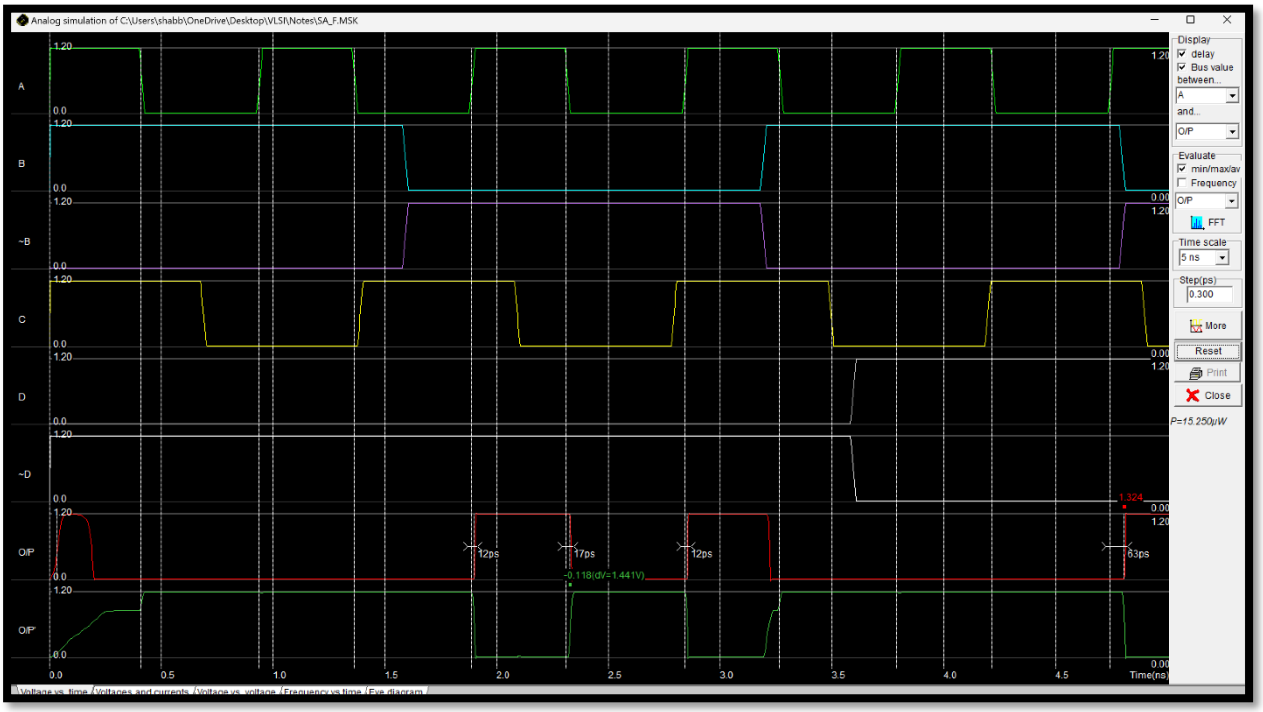
Simulation Results:

Voltage vs time:

i). Only A, B', C, D'

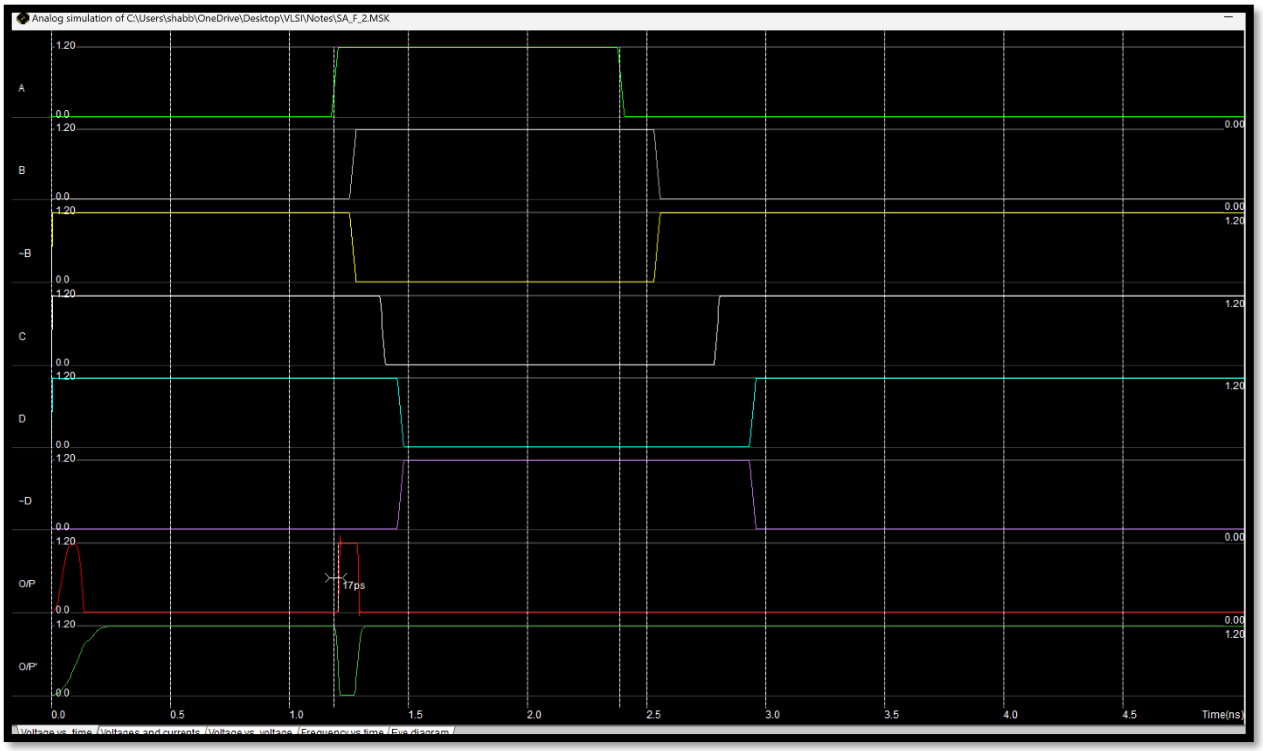


ii). A, B, C, D, B', D'

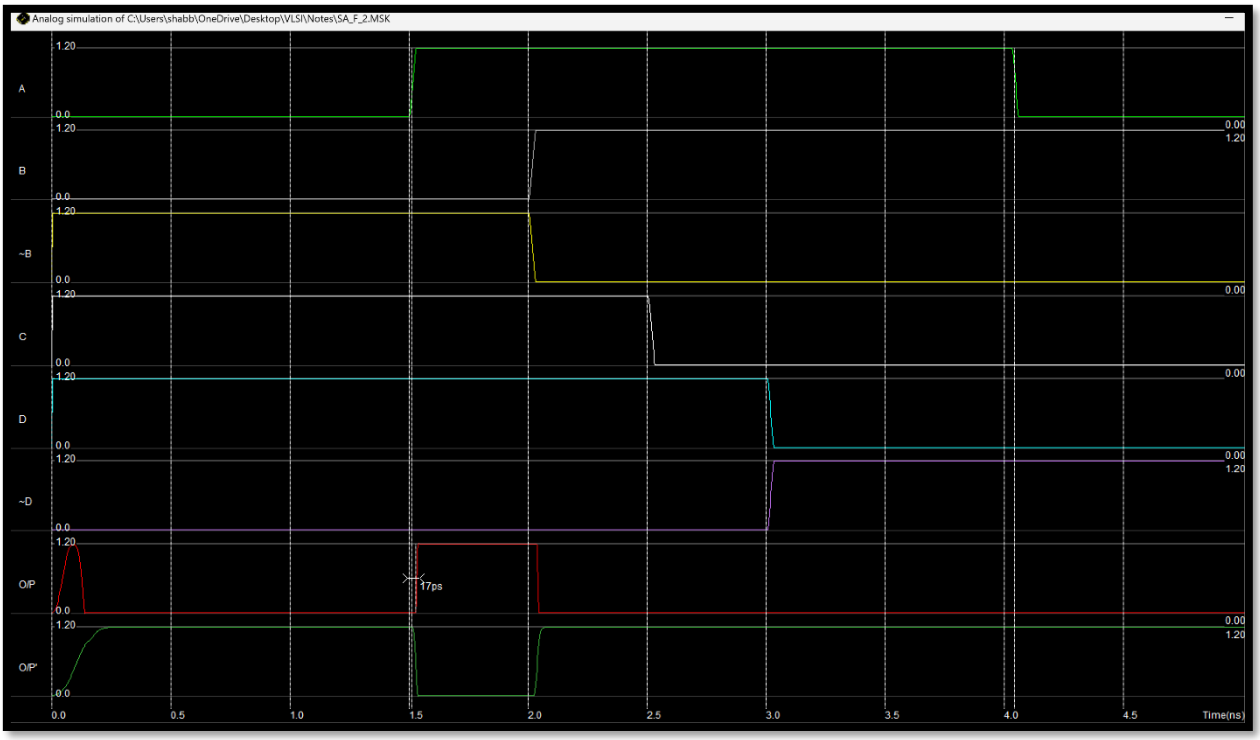


For Combination:

i. A=1, B=0, C=1, D=1 → O/P=1 & A=1, B=1, C=0, D=0 → O/P = 0



ii. A=1, B=1, C=1, D=1 → O/P=0 & A=1, B=0, C=1, D=1→ O/P = 1



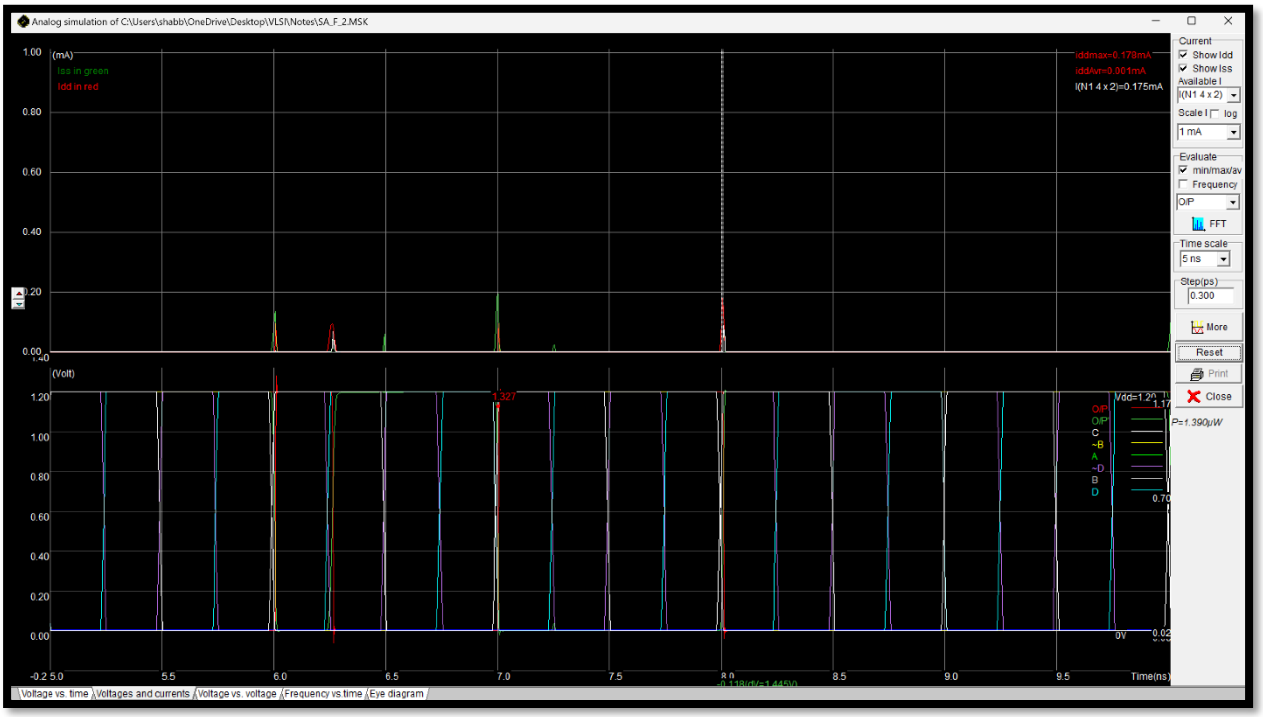
Input delay:

Rise Time	Fall Time
25ps	25ps

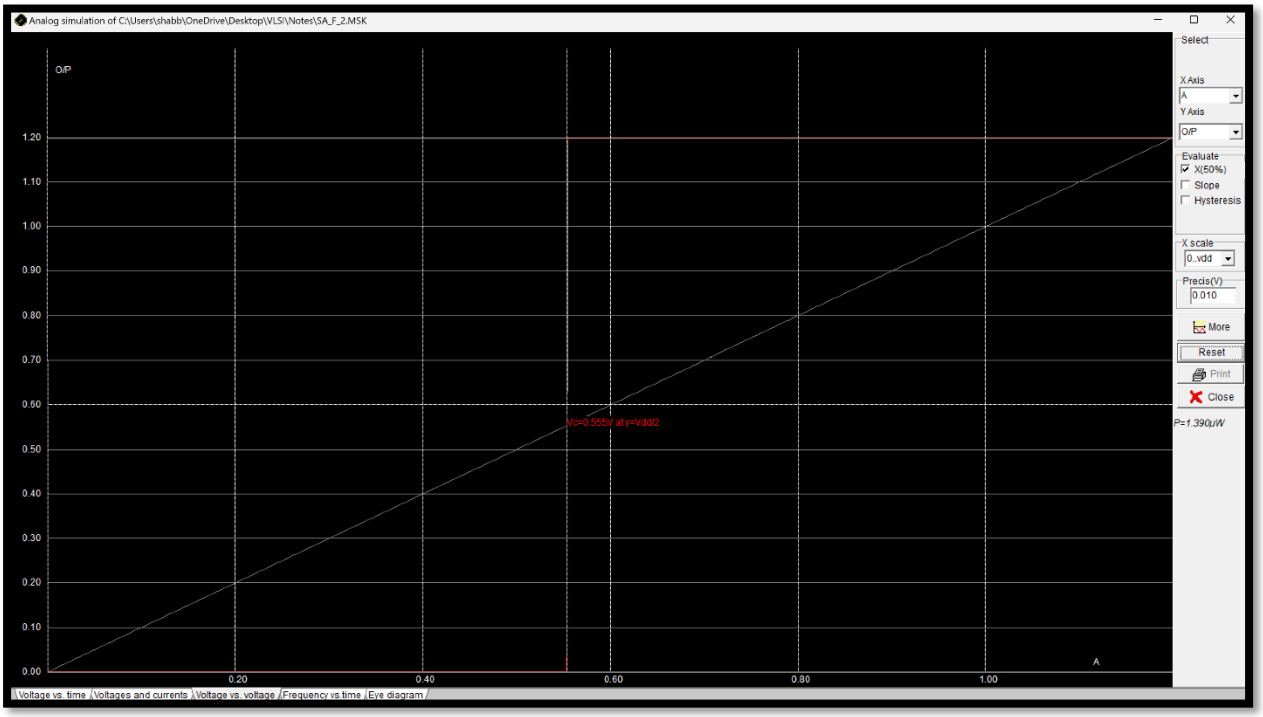
Output delay:

τ_{tplh}	τ_{tphl}	Propagation delay
18ps	16ps	17ps

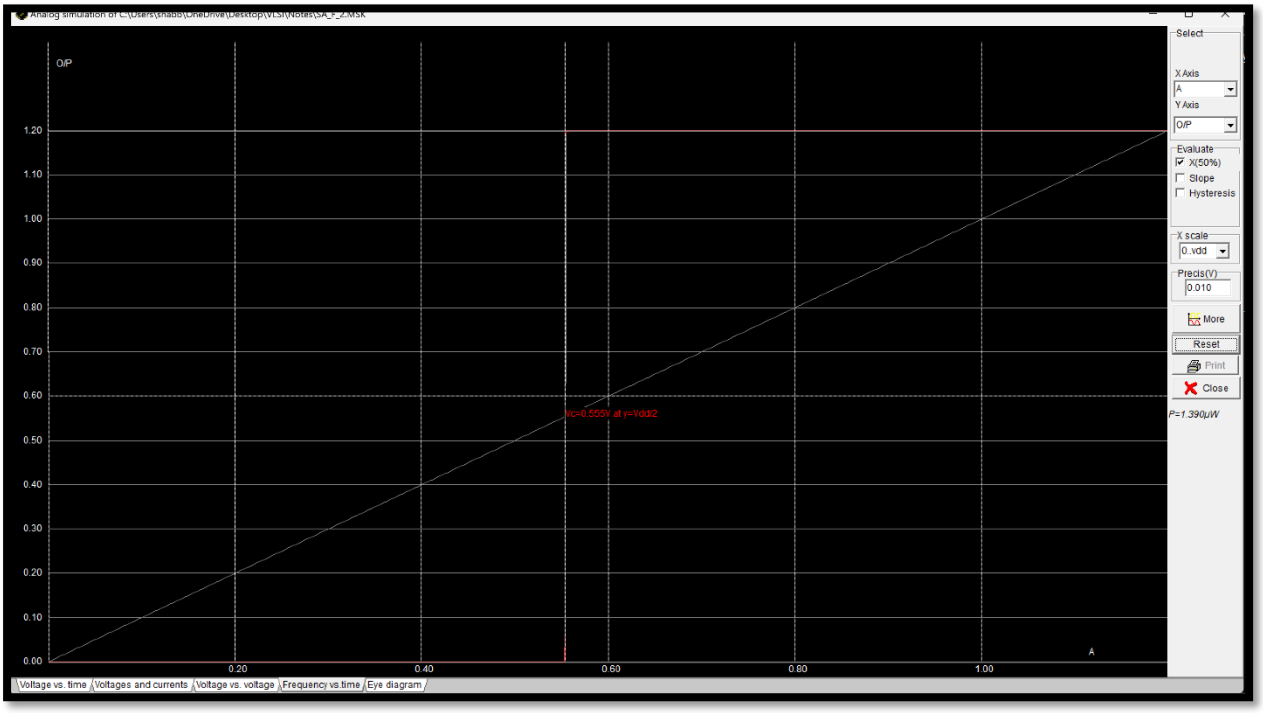
Voltage and current:



Voltage vs Voltage:



Frequency vs time:



Conclusion:

In this project, the Boolean expression $F = AB' + CD'A$ has been implemented using CMOS technology. The layout for transistor level circuit of the expression has been designed in Microwind Tool with different combinations of inputs. It has been observed that 3 distinct values of VOL and 4 distinct values of VOH are obtained by considering different status of the transistors. Their rise time, fall time and, propagation delays have been observed.