A Bootstrapped NMOS LDO Regulator for Low Supply Voltage and High PSRR

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***Abstract*—This work presents a bootstrapped NMOS low-dropout (LDO) regulator designed to operate effectively under low supply voltage conditions while maintaining high performance in terms of line regulation, load regulation, transient response, and power supply rejection ratio (PSRR). The proposed design leverages a bootstrap circuit to elevate the gate voltage of the NMOS pass transistor, enabling it to function efficiently even when the supply voltage is limited. Simulation results demonstrate that the bootstrapped NMOS LDO achieves a line regulation of 10.248 mV/V, a load regulation of 0.534 mV/mA, and a transient response figure of merit (FoM) as low as 25.65 fs under large load steps. Additionally, the design exhibits robust PSRR performance, making it suitable for applications requiring stable power delivery in low-voltage environments.**

***Index Terms*—Bootstrap switch, Low-dropout regulator, LDO, Power management**

I. Introduction

Low-dropout (LDO) regulators are widely used in modern electronic systems to provide stable and efficient power supply to various components. They are particularly favored for their simplicity, low noise, and fast transient response.

Among different types of LDOs, NMOS-based LDOs offer several advantages, including higher current handling capability and better thermal performance compared to their PMOS counterparts. However, they typically require a higher supply voltage to operate effectively, which can be a limitation in low-voltage applications.

NMOS LDOs face challenges in low supply voltage scenarios due to their threshold voltage requirements. As the supply voltage decreases, the headroom for the NMOS pass transistor becomes limited, leading to potential dropout issues and reduced output voltage accuracy.

To address these challenges, this work proposes a bootstrapped NMOS LDO. By utilizing a bootstrap capacitor and switch, the gate voltage of the NMOS transistor can be elevated above the supply voltage, allowing for improved performance in low-voltage applications without the need for a higher supply voltage.

II. Proposed Bootstrapped NMOS LDO

A conventional NMOS LDO architecture is illustrated in Fig. 1, where the NMOS pass transistor regulates the output voltage based on the feedback from the output node. The gate of the NMOS transistor is driven by an error amplifier that compares the output voltage with a reference voltage.

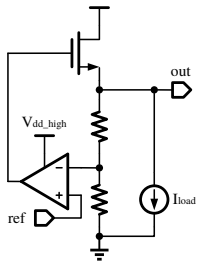

Fig. 1. Conventional NMOS LDO architecture

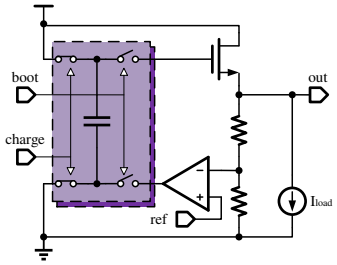

Fig. 2. A conceptual model of the proposed bootstrapped NMOS LDO

A major limitation of this architecture is the requirement for a higher gate voltage to ensure proper operation of the NMOS transistor. This is often challenging in low supply voltage scenarios.

Multiple techniques have been proposed to overcome this limitation, such as using charge pumps[1] or using a higher separate voltage supply. However, these approaches can introduce additional complexity, power consumption, and noise into the system.

The proposed bootstrapped NMOS LDO architecture, shown in Fig. 2, addresses these challenges by incorporating a bootstrap capacitor between the output of the error amplifier and the gate of the NMOS pass device.

The bootstrap circuit, highlighted in purple in Fig. 2, consists of a capacitor and 4 switches driven by non-overlapping clock signals `boot` and `charge`, whose waveform is shown in Fig. 3.

During the `boot` phase, the capacitor is placed between the output of the error amplifier and the gate of the NMOS transistor.

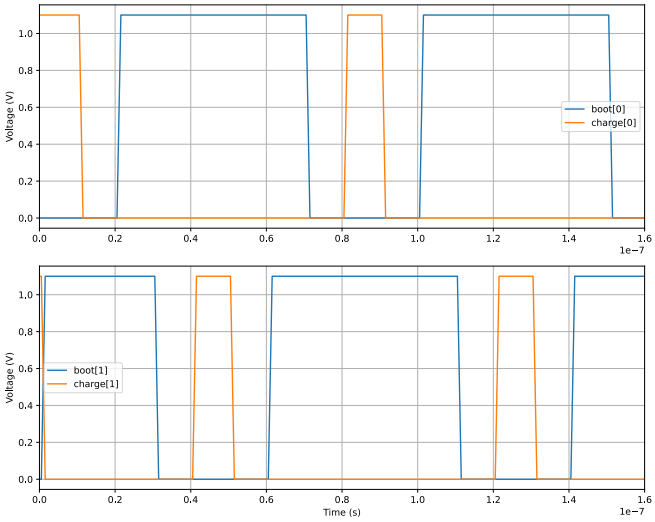

Fig. 3. Non-overlapping clock waveform for bootstrap circuit

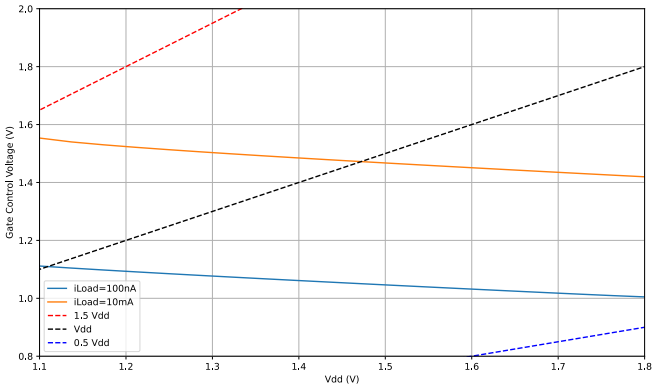

Fig. 4. Simulated proper NMOS gate control voltage range under varying V_{dd}

During the `charge` phase of the clock, the capacitor is charged to the output voltage. To avoid the gate being left floating during the `charge` phase, another bootstrap circuit with complementary clock phases, highlighted in dark purple in Fig. 2, is used to maintain the error amplifier's control on the gate voltage.

The bootstrap circuit elevates the gate voltage of the NMOS transistor above the supply voltage during operation, allowing for improved regulation performance even at low supply voltages. This approach maintains the simplicity of the LDO design while enhancing its capability to operate effectively in low-voltage environments.

III. Circuit Implementation

A. Bootstrap Circuit

Unfortunately, adding a V_{dd} to the output of the error amplifier to drive the gate of the NMOS pass transistor exceeds the proper operating voltage of the NMOS pass device when V_{dd} varies.

As shown in Fig. 4, the NMOS gate control voltage stays within $[0.5V_{\mathrm{dd}}, 1.5V_{\mathrm{dd}}]$, which means that the bootstrap circuit

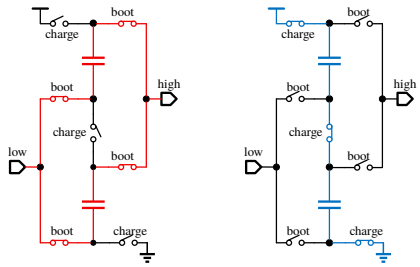

Fig. 5. Bootstrap circuit schematic. left: `boot` phase; right: `charge` phase

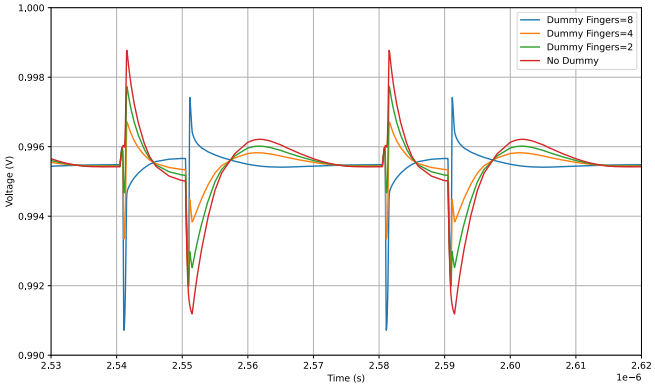

Fig. 6. Gate control voltage waveform under different dummy compensation

needs to provide a voltage boost of precisely $0.5V_{\mathrm{dd}}$ to ensure proper operation across the entire V_{dd} range.

In order to achieve this, a bootstrap circuit as shown in Fig. 5 is designed. During the `charge` phase, two identical capacitors share the V_{dd} voltage, charging each capacitor to approximately $0.5V_{\mathrm{dd}}$. During the `boot` phase, the capacitors are put in parallel, exhibiting the $0.5V_{\mathrm{dd}}$ voltage boost required.

Another important consideration in the bootstrap circuit design is the clock feedthrough and charge injection effect from the switches directly connected to the gate of the NMOS pass transistor. This effect can introduce unwanted voltage spikes on the gate, potentially disrupting the regulation performance. To mitigate this, dummy switches controlled by the complementary clock signals are added in parallel with the main switches.

The effectiveness of the dummy switches in reducing voltage spikes is demonstrated in Fig. 6, where the gate control voltage spikes where reduced from dozens of millivolts to around 10 millivolts.

The schematic of the complete bootstrap circuit with dummy switches is shown in Fig. 7.

B. Error Amplifier

The DC voltage gain from the supply voltage V_{dd} to the output voltage V_{out} can be expressed as:

$$A_{\mathrm{line}} = \frac{1}{\frac{1}{Z_{\mathrm{L}}} + 1 + g_{\mathrm{m}} r_{\mathrm{o}} + A \cdot g_{\mathrm{m}} r_{\mathrm{o}}} \approx \frac{1}{A \cdot g_{\mathrm{m}} r_{\mathrm{o}}} \tag{1}$$

When testing the LDO line regulation performance, the small signal parameters g_{m} and r_{o} of the pass transistor can

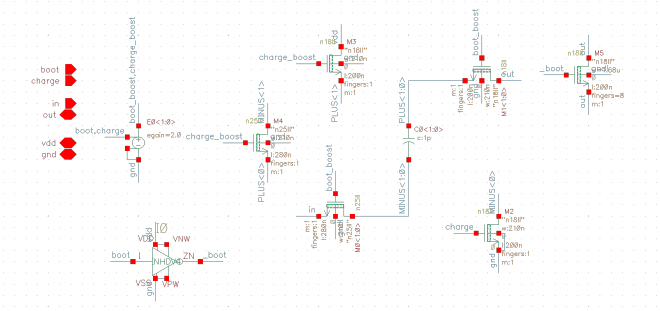

Fig. 7. Complete bootstrap circuit schematic with dummy switches

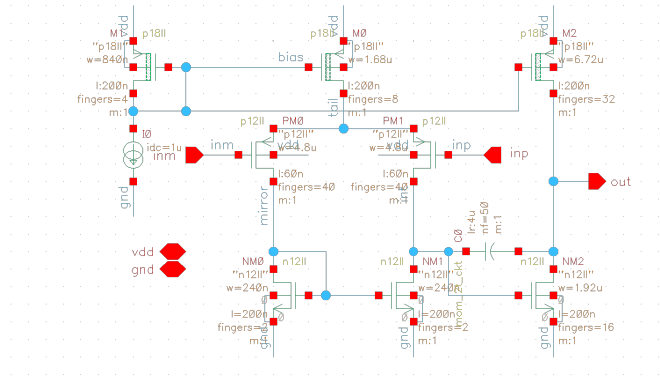

Fig. 8. Error amplifier schematic

be considered constant. Therefore, it's line performance can be estimated by (1).

Simulation shows that at high load current and low dropout voltage conditions, the r_o of the pass transistor degrades significantly due to channel length modulation, leading to an intrinsic gain $g_m r_o$ of only around 1. To ensure line regulation of less than 10 mV/V, the error amplifier is designed to have a high gain of around 40 dB.

The error amplifier schematic is shown in Fig. 8, which is a two-stage amplifier with Miller compensation. The first stage is a differential pair with current mirror load, providing high gain and common-mode rejection. The second stage is a common-source amplifier that further amplifies the signal before driving the bootstrap circuit. The current ratio between the two stages is set to 2 µA:8 µA to provide sufficient slew rate at the output.

IV. Simulation Results

The proposed bootstrapped NMOS LDO is implemented in a standard 65 nm CMOS process. The LDO receives a reference voltage V_{ref} of 0.6 V, resulting in a nominal output voltage V_{out} of 1 V. The 2-way non-overlapping bootstrap clock frequency is set to 12.5 MHz. The simulation testbench schematic is shown in Fig. 9.

A. Line Regulation

By sweeping the supply voltage V_{dd} from 1.1 V to 1.8 V at constant load currents of 100 nA and 10 mA, respectively, the averaged stable state output voltage is simulated and presented

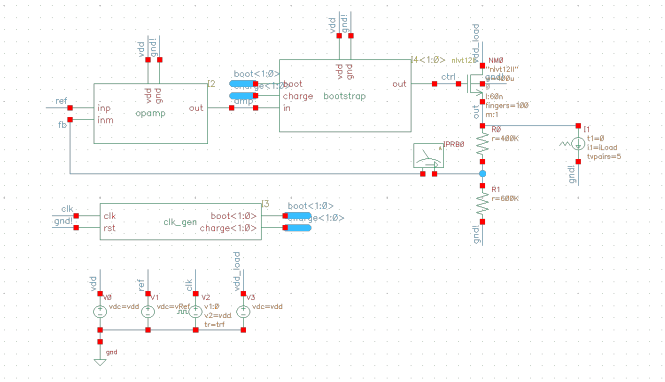

Fig. 9. Simulation testbench schematic

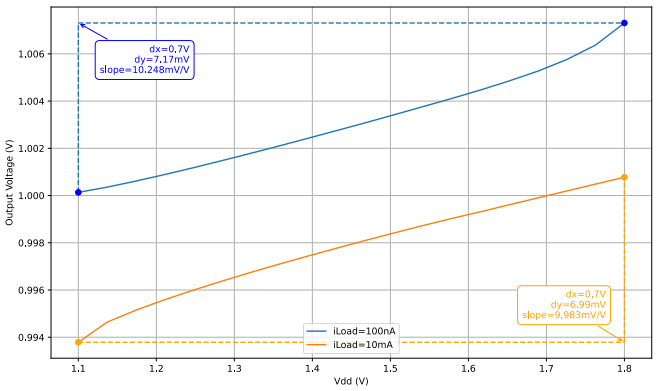

Fig. 10. Simulated line regulation performance

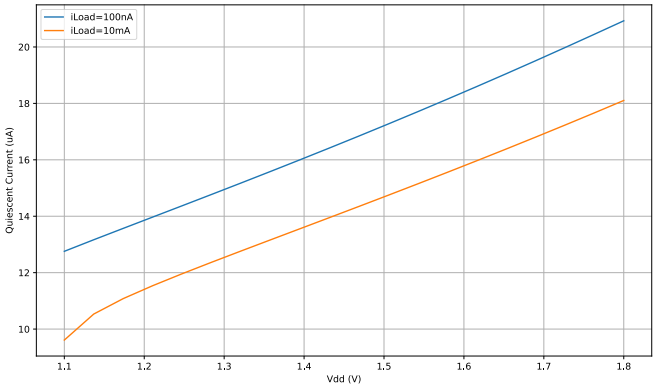

Fig. 11. Simulated quiescent current under varying V_{dd} and load conditions

in Fig. 10, which shows a line regulation of 10.248 mV/V across the entire supply voltage range.

B. Power Consumption

Based on the conditions of Section IV.A, the quiescent current is simulated and presented in Fig. 11. The quiescent current remains relatively constant at around 10 µA to 20 µA across the entire supply voltage range, demonstrating the efficiency of the proposed design.

C. Load Regulation

By sweeping the load current from 100 nA to 10 mA at a constant supply voltage of 1.2 V, the averaged stable state

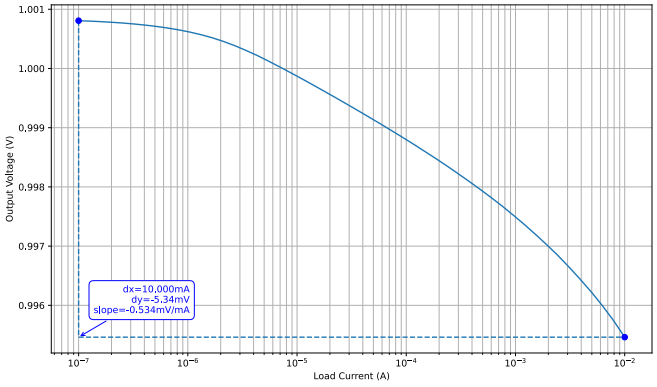

Fig. 12. Simulated load regulation performance

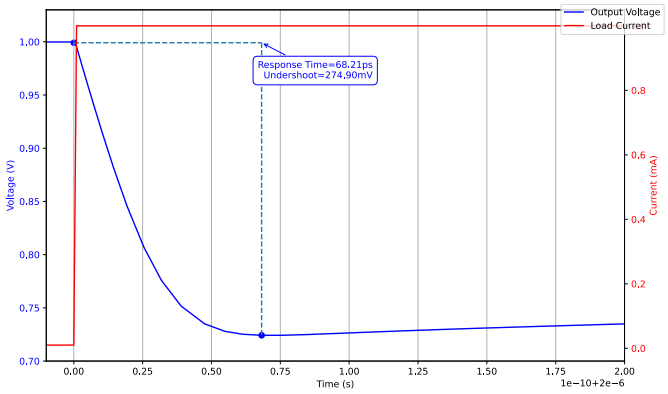

Fig. 14. Simulated transient response

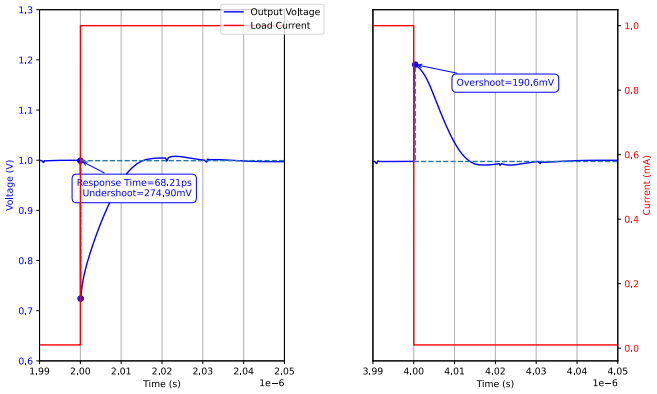

Fig. 13. Simulated transient response

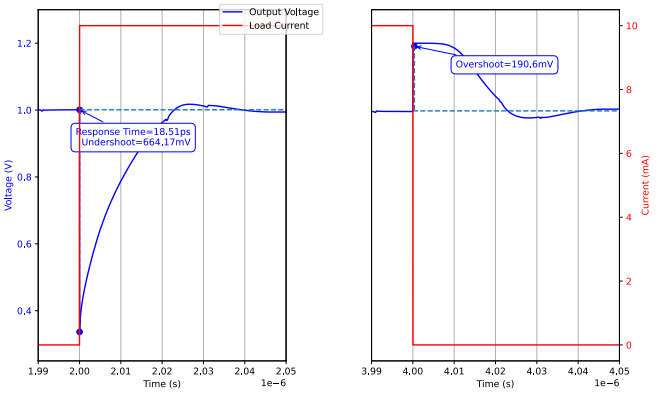

Fig. 15. Simulated transient response

output voltage is simulated and presented in Fig. 12, which shows a load regulation of $0.534\,\mathrm{mV/mA}$ across the entire load current range.

D. Transient Response

The transient response of the LDO is evaluated by applying a step load current and observing the output voltage response. The rise & fall time of the load current step is set to 1 ps for accurate FoM calculation.

a) *Small Step Load Change:*

The load current steps from $10\,\mu\mathrm{A}$ to $1\,\mathrm{mA}$ and back to $10\,\mu\mathrm{A}$. The results are presented in Fig. 13 and Fig. 14.

The output voltage exhibits an undershoot of $274.9\,\mathrm{mV}$ and an overshoot of $190.6\,\mathrm{mV}$ when the load current steps from $10\,\mu\mathrm{A}$ to $1\,\mathrm{mA}$ and back to $10\,\mu\mathrm{A}$, respectively. The settling time for both transitions is around 15 ns. The response time from the load step to the peak of the undershoot is around 68.21 ps.

The corresponding figure of merit (FoM) is:

$$\mathrm{FoM} = T_{\mathrm{R}} \frac{I_{\mathrm{Q}}}{I_{\max}} = 68.21\,\mathrm{ps} \cdot \frac{13.38\,\mu\mathrm{A}}{1\,\mathrm{mA}} = 912.6\,\mathrm{fs} \quad (2)$$

b) *Large Step Load Change:*

The load current steps from $100\,\mathrm{nA}$ to $10\,\mathrm{mA}$ and back to $100\,\mathrm{nA}$. The results are presented in Fig. 15 and Fig. 16.

The output voltage exhibits a much larger undershoot of $664.17\,\mathrm{mV}$ and overshoot of $109.6\,\mathrm{mV}$ under larger load current steps. The settling time for these transitions is around 23 ns. The response time from the load step to the peak of the undershoot is around 18.51 ps.

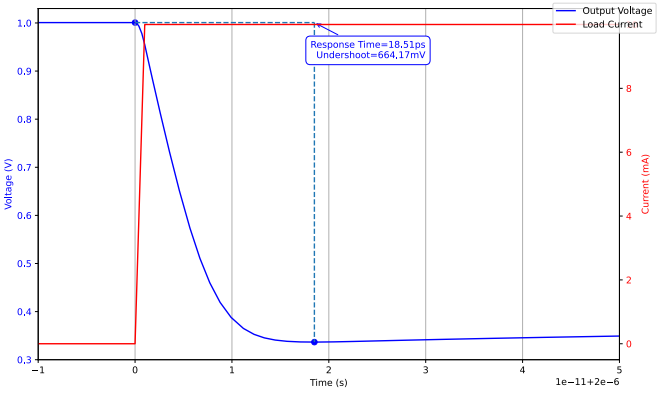

Fig. 16. Simulated transient response

The corresponding figure of merit (FoM) is:

$$\mathrm{FoM} = T_{\mathrm{R}} \frac{I_{\mathrm{Q}}}{I_{\max}} = 18.51\,\mathrm{ps} \cdot \frac{13.86\,\mu\mathrm{A}}{10\,\mathrm{mA}} = 25.65\,\mathrm{fs} \quad (3)$$

E. PSRR

Replacing the bootstrap circuit with a $V_{\mathrm{dd}}/2$ dc voltage source, the PSRR performance is simulated by applying a small-signal AC voltage source at the supply voltage node and measuring the output voltage AC response under multiple

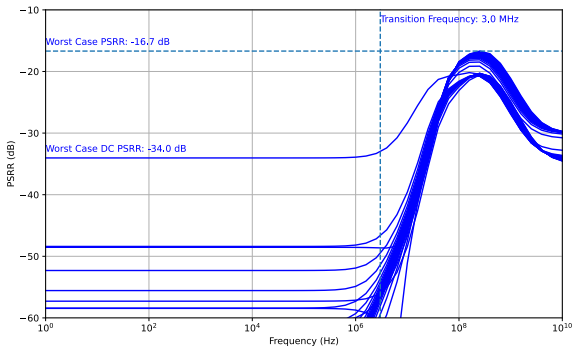

Fig. 17. Simulated PSRR performance

load & supply voltage conditions. The results are presented in Fig. 17.

The PSRR performance shows a higher attenuation of supply voltage variations than conventional PMOS LDOs, with a PSRR peaking of around $-16.7\,\mathrm{dB}$ at around $300\,\mathrm{MHz}$. The worst case PSRR across all load and supply voltage conditions at low frequencies is around $-34\,\mathrm{dB}$ under $3\,\mathrm{MHz}$, where the NMOS dropout gets too low and could not provide sufficient r_o. In most other conditions, the PSRR is less than $-50\,\mathrm{dB}$ under $3\,\mathrm{MHz}$.

V. Conclusion

This work presents a bootstrapped NMOS LDO regulator designed to operate effectively under low supply voltage conditions while maintaining high performance in terms of line regulation, load regulation, transient response, and PSRR. The proposed design leverages a bootstrap circuit to elevate the gate voltage of the NMOS pass transistor, enabling it to function efficiently even when the supply voltage is limited.

Simulation results demonstrate that the bootstrapped NMOS LDO achieves a line regulation of $10.248\,\mathrm{mV/V}$, a load regulation of $0.534\,\mathrm{mV/mA}$, and a transient response FoM as low as $25.65\,\mathrm{fs}$ under large load steps.

Additionally, the design exhibits robust PSRR performance, making it suitable for applications requiring stable power delivery in low-voltage environments. The proposed bootstrapped NMOS LDO thus represents a promising solution for modern low-power electronic systems.

A. Potential Improvements

Despite the fast transient response, Section IV.D shows significant undershoot and overshoot during load transients. For example, in Section IV.D.b, the $664.17\,\mathrm{mV}$ undershoot may cause the regulated circuit to malfunction at low supply voltages.

Conventionally, adding a decoupling capacitor at the output node can help reduce voltage spikes during load transients by providing a temporary energy reservoir. However, they consume significant chip area and worsen response time as well as the FoM. In the case of Section IV.D.b, a decoupling capacitor of around $2.3\,\mathrm{nF}$ is required to reduce the undershoot to less than $100\,\mathrm{mV}$, which is impractical for on-chip implementation.

References

[1] Y. Wang, T. Wu, and J. Guo, "A Charge Pump Based 1.5A NMOS LDO with 1.0~6.5V Input Range and 110mV Dropout Voltage," in *2022 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, 2022, pp. 188–189. doi: 10.1109/ICTA56932.2022.9963126.