1.)

Cache Configuration and Simulation

In this problem we will consider several cache designs for a processor implementing the MIPS ISA [Note that this has implications needed to answer the below questions]. Assume that the block offset is four bits and the index is four bits.

a) What is the cache block size in bytes? words? double words?
   1) 2^4 bytes → 16 bytes, 4 words (32 bits) or 2 double word (64 bits)

b) How many sets does this cache have? [Hint: note that both direct-mapped and fully-associative caches can be considered to have sets.]
   1) 2^4 = 16 sets

c) Record both the amount of data and meta-data (in bits) this cache holds if it is direct-mapped, two-way set associative, and four-way set associative.
   1) DM – Data - 16 byte blocks, 16 blocks, 256 bytes of data == 2048 bits
      Meta – Valid bit, tag, 25 bits * 16 blocks, 400 bits
   2) 2W - Data - 16 byte blocks, 32 blocks (2 per set), 4096 bits
      Meta – Valid bit, tag, 25 bits * 32 blocks, 800 bits
   3) 4W – Data – 16 byte blocks, 64 blocks (4 per set), 8192 bits
      Meta – Valid bit, tag, 25 bits* 64 blocks, 1600 bits

d) Simulate the direct-mapped and four-way set associative cache with respect to the following series of memory accesses. In the table below, indicate whether each memory access was a hit or a miss and provide the reason for each miss. Assume the caches have no valid entries to begin with and use a least-recently-used (LRU) replacement policy.

Direct-Mapped – Hit Rate 0/10

Memory Access	Tag	Set# (Index)	Offset	Hit
0x1001FEA0	1001FE	A	0	Miss
0x1001EFA4	1001EF	A	4	Miss
0x1001FEA8	1001FE	A	8	Miss
0x100100A0	100100	A	0	Miss
0x100100B0	100100	B	0	Miss
0x100100C0	100100	C	0	Miss
0x10011FA1	10011F	A	1	Miss
0x1001EEA2	1001EE	A	2	Miss
0x1001EFAF	1001EF	A	F	Miss
0x100100A2	100100	A	2	Miss

4-Way Set Associative – Hit Rate 2/10

Memory Access	Tag	Set# (Index)	Offset	Hit
0x1001FEA0	1001FE	A	0	Miss
0x1001EFA4	1001EF	A	4	Miss
0x1001FEA8	1001FE	A	8	Hit
0x100100A0	100100	A	0	Miss
0x100100B0	100100	B	0	Miss
0x100100C0	100100	C	0	Miss
0x10011FA1	10011F	A	1	Miss
0x1001EEA2	1001EE	A	2	Miss
0x1001EFAF	1001EF	A	F	Hit
0x100100A2	100100	A	2	Mis

2.)

For a cache structure with 8 bit index and stores 64 KiB of data, not including meta-data.
(64KiB == 65536 bytes)

a.) How many cache blocks are there in a direct mapped, 2 way set associative, 8 way set associative, and 16 way set associative caches?

DM – 2^8 == 256 sets, each has there own cache block so 256 cache blocks
2W – each set has 2 cache blocks so 512 cache blocks total
8W – 2048 cache blocks
16W- 4096 cache blocks

b.) How many bits are needed for offset in the same cache formats? How bytes are in each cache block?

DM – 65536 bytes / 256 blocks = 256 bytes per block,
8 bits needed for offset
2W - 65536 bytes / 512 blocks = 128 bytes per block,
7 bits needed for offset
8W - 65536 bytes / 2048 blocks = 32 bytes per block,
5 bits needed for offset
16W - 65536 bytes / 4096 blocks = 16 bytes per block,
4 bits needed for offset

c.) How much meta data is needed for each of the same cache formats if addresses are 32 bits in length?

Valid bit and Tag needed for each block

DM – 16 bit tag, 17 bits per block == 17 * 256 = 4352 bits
2W - 17 bit tag, 18 bits per block == 18 * 512 = 9216 bits
8W - 19 bit tag, 20 bits per block == 20 * 2048 = 40960 bits
16W – 20 bit tag, 21 bits per block == 21 * 4096 = 86016 bits