	Inst Mem		Reg File				ALU				MemToReg Mux			PCSrc Mux		
Cycle	Addr	Inst	Reg 1	Data 1	Write Reg	Write Data	A	B	Op	Result	1	0	S	1	0	S
1	0x00000010	lui	X	X	X	X	X	X	X	X	X	X	X	0xXXXXXXXX	0x00000014	0
2	0x00000014	addi	X	X	X	X	X	X	X	X	X	X	X	0xXXXXXXXX	0x00000018	0
3	0x00000018	sub	$0 / 0x00	0x00000000	X	X	X	0x00001001	lui	0x10010000	X	X	X	0xXXXXXXXX	0x0000001c	0
4	0x0000001c	xor	$a0 / 0x04	3	X	X	0	42	add	42	X	X	X	0x00004014	0x00000020	0
5	0x00000020	ori	$a0 / 0x06	1023	$s0 / 0x10	0x10010000	3	1024	sub	-1021	M[0x10010000]	0x10010000	0	0x000000BC	0x00000024	0
6	0x00000024	beq	$s0 / 0x10	0x1001000	$t0 / 0x08	42	0x000027E5	-1	xor	0xFFFFD81A	M[0x0000002A]	42	0	0x00120A0	0x00000028	0
7	0x00000028	addi	$t0 / 0x08	42	$t1 / 0x09	-1021	0x10010000	0x0040	or	0x10010040	M[0xFFFFFC03]	-1021	0	0xFFFF6084	0x0000002c	0
8	0x0000002c	sll	$0 / $0x00	0	$t2 / 0x0A	0xFFFFD81A	42	-1	beq	UNKNOWN	M[0xFFFFD81A]	0xFFFFD81A	0	0x00000120	0x00000030	0
9	0x00000030	sw	$0 / $0x00	0	$s0 / 0x10	0x10010040	0	0	add	0	M[0x10010040]	0x10010040	0	0x00000100	0x00000034	0
10			$s0 / 0x10	0x10010040	Write Disabled		0	0 – shamt	sll	0	UNKNOWN	UNKNOWN	DC	0x00000028	0x00000038	0
11					$t4 / 0x0c	0	0x10010040	0	add	0x10010040	M[0x00000000]	0	0	0x0000002c	0x0000003c	0
12					$0 / 0x00	0					M[0x00000000]	0	0	0x00000030	0x00000040	0
13					Write Disabled						M[0x10010040]	0x10010040	DC			