1.

View other file. Spreadsheet pdf.

2.

Find all data dependencies and RAW hazards in the code. How many stalls do you need to insert to solve RAW hazards?

7 stalls

Code	Dependencies	Hazards
Frodo:		
lw $t0, 0($a1)	addi $a1	Raw Hazard, +1 stall
add $t1, $t0, $a2	lw $t0, directly before	Raw Hazard, +2 stalls
lw $t0, 0($a0)	addi $a0	
add $t0, $t0, $t1	lw $t0 and add $t1	Raw Hazard, +2 stalls
sw $t0, 0($a0)	addi $a0 and add $t0	Raw Hazard, +2 stalls
sub $a3, $a3, 1	Read $a3 to write to $a3	
addi $a0, $a0, 4	Read $a0 to write to $a0	
addi $a1, $a1, 4	Read $a1 to write to $a1	
bne $a3, $0, Frodo	sub $a3	

3.) The implementation of a processor takes the following times for each operation type:

Register Ops:	**1ns**
ALU Ops:	**2ns**
Memory Ops:	**3ns**

a.) What is the minimum cycle time for single cycle, multi cycle, and 5 stage pipelined processor with this implementation and why?

Single – 3 + 1 + 2 + 3 + 1 = 10ns
Must be long enough to execute slowest instruction, LW, in one cycle. LW reads inst memory, reads registers, adds in ALU, reads from data memory, and writes back to register file.

Multi – 3ns
Pipeline – 3ns
One cycle must be long enough to account for the slowest sub-operation/micro-instruction. That is the memory read/write operations which take 3ns.
(Multi and Pipeline have same reasoning why.)

b.) How long would an R-type instruction take for each type of processor?

Single – 8ns

Multi – 3 + 3 + 3 +3 = 12ns
(Only needs 4 cycles – read inst, read reg, ALU, write reg)

Pipeline – 3 * 5 = 15ns

c.) What is the speed up for an R-type instruction if the implementations memory operations were improved to take only 2ns long?

Single – 8ns **SU = 10 / 8 = 5/4 = 1.25**

Multi – 2+2+2+2 = 8ns **SU = 12 / 8 = 3/2 = 1.5**

Pipeline – 2 * 5 = 10ns **SU = 15 / 10 = 3/2 = 1.5**