max10 on chip flash read/write in nios

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Altera_Forum
Honored Contributor II

06-01-2015 • 12:37 PM • 3,607 Views

hi everone, for two weeks i stuck in the max10 on chip flash read/write in nios.

in my project, it has a nios system and the clk frequency is 100mHz.

i want to use the internal configuration mode of max10(single compressed image with memory initialization), as well as read/write the chip flash UFM in nios.

i can read the UFM, but i can not write to it.

the following is my code, i run it in debug mode

flash_status_reg1=IORD_32DIRECT(ONCHIP_FLASH_0_CSR_BASE,0x0); // read the flash_status_reg, the result is 0xfffffc04,

flash_control_reg1=IORD_32DIRECT(ONCHIP_FLASH_0_CSR_BASE,0x4); // read the flash_control_reg, the result is 0x3fffffff,

flash_data_reg1=IORD_32DIRECT(ONCHIP_FLASH_0_DATA_BASE,0x0); // read the first 32 bit of UFM1,the result is 0x0,

while(1)

{

flash_status_reg1=IORD_32DIRECT(ONCHIP_FLASH_0_CSR_BASE,0x0);//read the flash_status_reg, the result is 0xfffffc04, it means read success

flash_status_reg1=flash_status_reg1&0x4;

if (flash_status_reg1== 0x4) break; // write success

}

// write to UFM1

IOWR_32DIRECT(ONCHIP_FLASH_0_CSR_BASE,0x4,0xff7fffff);// disable the write protection of UFM1

flash_control_reg1=IORD_32DIRECT(ONCHIP_FLASH_0_CSR_BASE,0x4);// read the flash_control_reg, the result is 0x3f7fffff,

IOWR_32DIRECT(ONCHIP_FLASH_0_DATA_BASE,0x0,0x12345678);// write to the first 32 bit of UFM1, then the debug stuck in here

can someone gives me some help?

i have found the reference desin for how to use the UFM in quartus without nios;

i also have found the reference desin for how to use the onchip internal configuration mode of max10 in nios system;

but i have not found a reference desin use nios, and the UFM

thanks!

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11 Replies

Altera_Forum
Honored Contributor II

06-02-2015 • 11:54 AM • 2,348 Views

Hi,

Have you try to erase before write? Typical CPLD and flash require erase operation before write. Thus you need to disable write protect and erase first before write to UFM1. Try setting CSR to 0x001fffff or 0xff1fffff to disable write protect and erase for UFM1.

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Altera_Forum
Honored Contributor II

06-03-2015 • 12:54 AM • 2,348 Views

thanks for your reply! i will try it.

does this mean that everytime i write to the flash, i should erase it at first?

by the way, the max10 user flash memory user guide.pdf do not tell me to erase the block before write.

have you write to the UFM in nios successfully?

can you show me your design?

thanks!

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Altera_Forum
Honored Contributor II

06-03-2015 • 01:53 AM • 2,348 Views

--- Quote Start ---

Hi,

Have you try to erase before write? Typical CPLD and flash require erase operation before write. Thus you need to disable write protect and erase first before write to UFM1. Try setting CSR to 0x001fffff or 0xff1fffff to disable write protect and erase for UFM1.

--- Quote End ---

thank you very much! i stuck in this problem for 2 weeks!

i erase the UFM1, then the wrie success.

then i repower the board, and write to the UFM1 without erase, and it success too.

so it seems like the UFM only should be eased at the first time,.

thanks!

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Altera_Forum
Honored Contributor II

06-03-2015 • 02:06 AM • 2,348 Views

I'm don't have any design with Nios as I'm not that familiar on Nios.

I heard that Altera is going to publish a reference design on accessing the CFM and UFM with Nios using the on chip flash and dual boot ip.

Yes, in CPLD (MAX II and MAX V too) you need to erase before write. Somewhere in the MAX 10 handbook should have stated on this.

Also, you need to set the write protect once complete write. This is stated from the UFM user guide.

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Altera_Forum
Honored Contributor II

06-04-2015 • 11:10 AM • 2,348 Views

check this out..

https://cloud.altera.com/devstore/platform/15.0.0/max10-remote-system-upgrade-rsu-over-uart-with-nios-ii-processor/

Altera just released the reference design with the documentation..yeayy!!!

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Altera_Forum
Honored Contributor II

06-24-2015 • 02:19 AM • 2,348 Views

--- Quote Start ---

thanks for your reply! i will try it.

does this mean that everytime i write to the flash, i should erase it at first?

by the way, the max10 user flash memory user guide.pdf do not tell me to erase the block before write.

have you write to the UFM in nios successfully?

can you show me your design?

thanks!

--- Quote End ---

Hi,

I came across the MAX 10 UFM user guide which did mentioned the need to erase before write. You can refer to page 2 from the MAX 10 UFM user guide in the link below:

https://www.altera.com/content/dam/altera-www/global/en_us/pdfs/literature/hb/max-10/ug_m10_ufm.pdf

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Altera_Forum
Honored Contributor II

06-24-2015 • 03:45 AM • 2,348 Views

thanks!

you give me the newest version(2015.05.04), in my version(2014.12.15), there is no charpter 3.2 in my user guide.

altera correct this user guide finally!

still thanks!

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Altera_Forum
Honored Contributor II

11-18-2015 • 02:39 AM • 2,348 Views

--- Quote Start ---

Hi,

Have you try to erase before write? Typical CPLD and flash require erase operation before write. Thus you need to disable write protect and erase first before write to UFM1. Try setting CSR to 0x001fffff or 0xff1fffff to disable write protect and erase for UFM1.

--- Quote End ---

Hello，where i can find write protect and erase register for MAX10. I have read user guide but i can not see anything about it.

Thank you!!

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Altera_Forum
Honored Contributor II

11-20-2015 • 01:39 AM • 2,348 Views

you should read " MAX10 User Flash Memory User Guide"

check the control register page 5-5 and 5-6

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so this this mean when ever we nee to use such flash, just do a first erase at the first place?

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Honored Contributor II

11-20-2015 • 04:50 AM • 2,348 Views

OK~ i have found it.

Thanks a lot.

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