Assignment 2

EEL318 – Digital Hardware Design

Date of Assignment: 22/02/2021 Submission Deadline: 28/01/2021

Question 1: Design a SRAM based FIFO for the following specifications:

1. The word size should be 8bit for the SRAM memory that means you are reading or writing 8bit of data from the SRAM
2. The number of address locations in your SRAM should be 1024
3. You should also keep the condition in consideration when the synchronizer fails for 1 cycle due to meta-stability condition.
4. Add adequate comments in your VHDL code for readability.