Name: MD. Mosthiur Rahman

ID: 2017-1-60-165

Course code: CSE442

Ans to the ans No: 1

a) Given that,

Memory location will start from => 08H

So, code:

```
MOV A, B
MOV 08H, A
MOV 09H, A
MOV 0AH, A
```

Ans to the Ques NO: 2

a) C9H → 1100 1001

2DH → 0010 1101

1111 0110

So, Here, OV = Overflow = 0

P = parity bit = 0

AC = Auxillary carry = 1

Cy = carry = 0

b) BEH → 1011 1110

IEH → 0000 1110

1101 1100

So, Here, OV = overblow = 0

P = parity = 1

AC = Auxiliary = 1

C = carry = 0

Ans:

Ans to the Ques NO: 3

Given that,

the pulse width is = '4X'

where X = last digit of the student ID

So, the pulse = 45 ms

As we know that,

XTAL = 11.059 kHz

So clock frequency = $\frac{11.059}{12}$ = 921.6 kHz

So, clock periods = 1/921.6 = 1.085 micro second.

So, The clocks amount = $\frac{(45 * 1000)}{1.085}$

= 41,474 clocks

So, the TH and TL value =>

=> 65536 - 41474 [FFFF = 65535]

[FFFFH + 1 = 65536]

=> 24,062

So, In hex the address is = 5D FEH

So, TH = 5D and TL = FE

Code :

```
        CLR   P1.5
        MOV   TMOD, #01
Here :  MOV   TL0, #FEH
        MOV   TH0, #5DH
        SETB  P1.5
        SETB  TR0
Again : JNB   TF0, Again
        CLR   P1.5
        CLR   TR0
        CLR   TF0
```

Ans to the Question NO: 4

Given that,

the student id: 165 Delay: 255

```
        org     0000H
Rept:   CPL     P1.0
        LCall   Delay
        SJump   Rept
        org     0100H
Delay:  MOV     R1, #2D
22:     MOV     R0, #64D
21:     DJNZ    R0, 21
        DJNZ    R1, 22
        Ret
        END
```

Ans to the Ques No: 5

An interrupt is a special condition that ~~arises~~ arises during the working period of micro-processor it is executing with ISR. A hardware interrupts process ~~occurs~~ occurs operating system signal on the external pins of the micro-processor 8086 has two pins to accept hardware interrupts. ~~There~~ There were NMI and INTR

1. NMI is non-maskable interrupt. It is high triggered and high priority interrupt. The microprocessor executes INT2 on receiving an interrupt.

2. INTR is maskable interrupt. It is levelled triggered and lower priority interrupt the micro processor Executes 2 INTA pulse on receiving an interrupt on INTR line.