North South University

Department of Electrical & Computer Engineering

CSE Project

Course Code: CSE231

Course Title: DIGITAL LOGIC DESIGN

Course Instructor: KMM

Project Name: Final Project (CSE-4-20)

Date of Submission: 07-01-2022

Section: 2

Group Number: 5

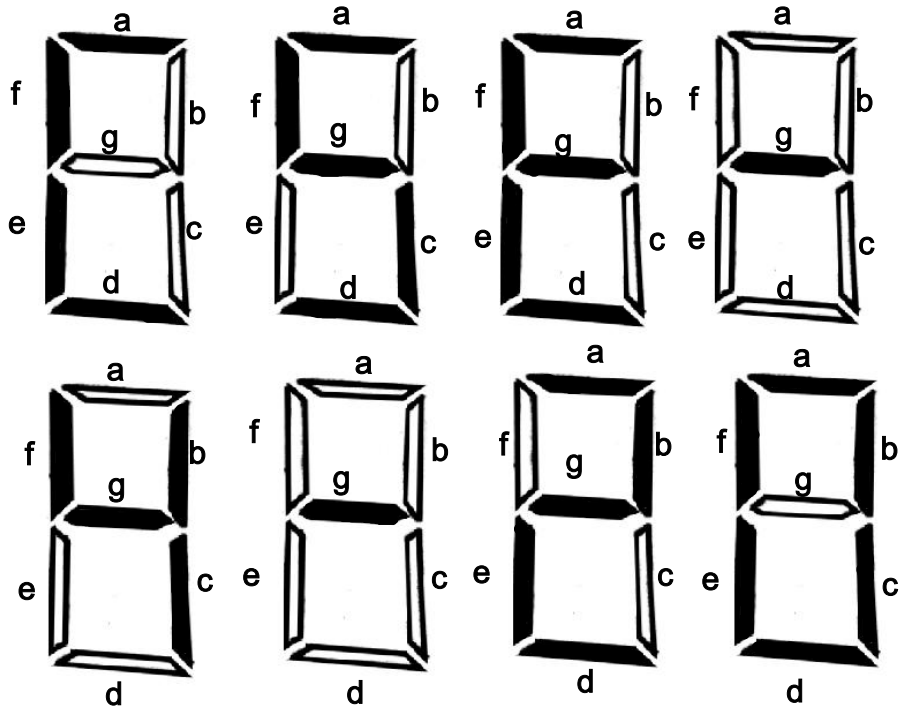
Submitted To: Dr Mohammad Monirujjaman Khan

Submitted By:	Scored:
Student Name and ID: 1. 2014172642 Shadman Sakib Ayan 2. 2012036642 Israt Jahan Meem 3. 2013130642 Rayan Ahmed 4. 2014160042 Md. Sabbir Hossain Soykat 5. 2012440642 Tanvir Rahman Navin	

On behalf of the group member

The Project Submitted by: Shadman Sakib Ayan

CSE-4-20



Group-4

CSE-4-20

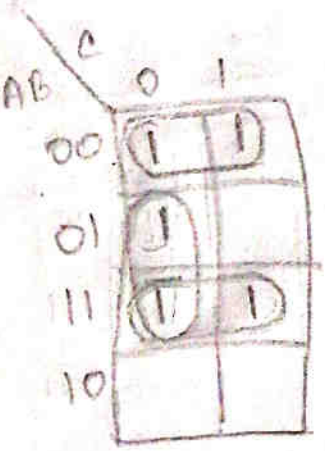
A	B	C	Output	a	b	c	d	e	f	g
0	0	0	[	1	0	0	1	1	1	0
0	0	1	⊏	1	0	1	1	0	1	1
0	1	0	⊏	1	0	0	1	1	1	1
0	1	1	–	0	0	0	0	0	0	1
1	0	0	⊔	0	1	1	0	0	1	1
1	0	1	–	0	0	0	0	0	0	1
1	1	0	⊏	1	1	0	1	1	0	1
1	1	1	⊓	1	1	1	1	1	1	0

For a:

$a = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC$.

000 001 010 110 111

K-map:



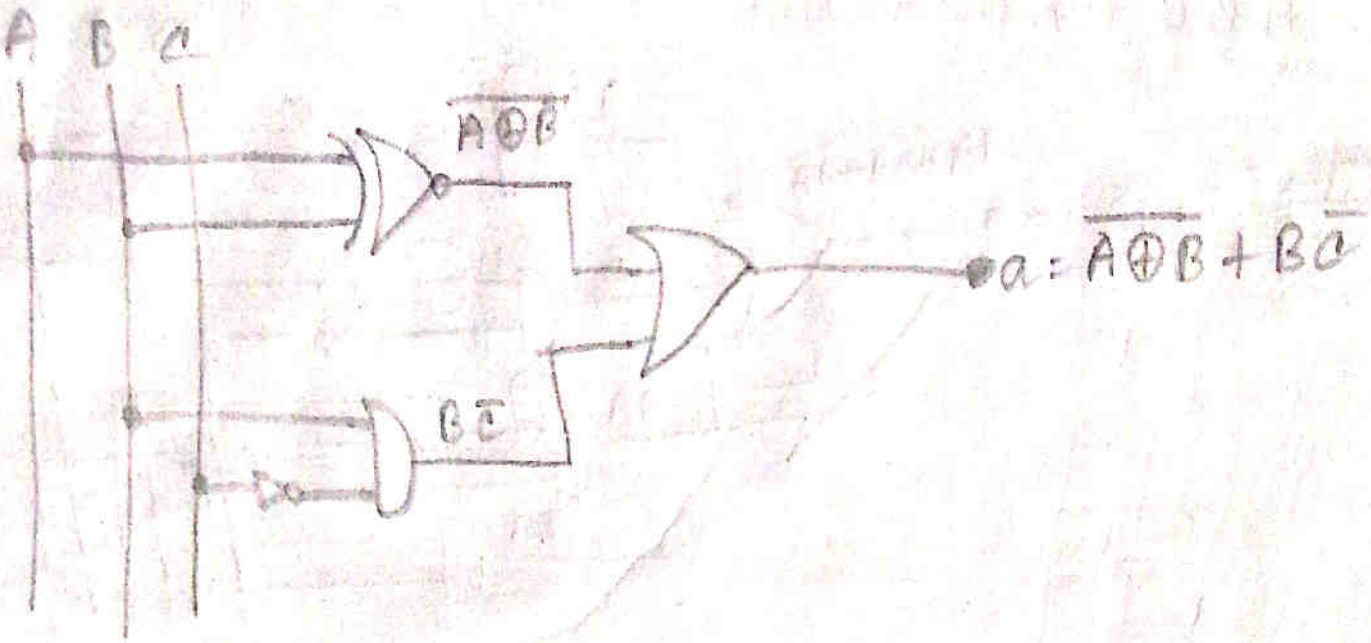
~~$a = \bar{A}\bar{B} + \bar{A}\bar{C} + B\bar{C} + AB$.~~

$\therefore a = \bar{A}\bar{B} + B\bar{C} + AB$.

$= \bar{A}\bar{B} + AB + B\bar{C}$

$= \overline{A \oplus B} + B\bar{C}$

Circuit for a:

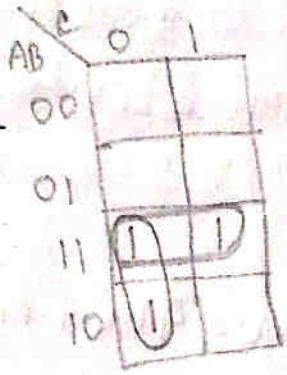


For b:

$b = A\bar{B}\bar{C} + AB\bar{C} + ABC$

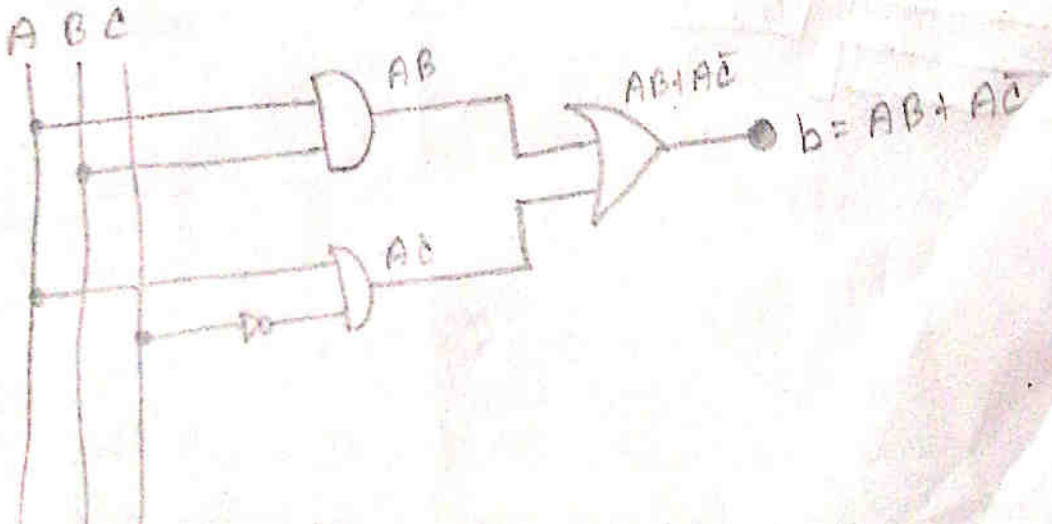
(1 0 0) (1 1 0) (1 1 1)

K-map:



$\therefore b = AB + A\bar{C}$.

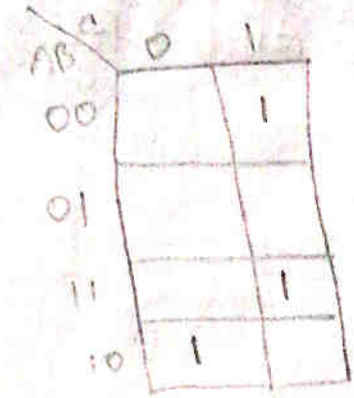
Circuit for b:



For C:

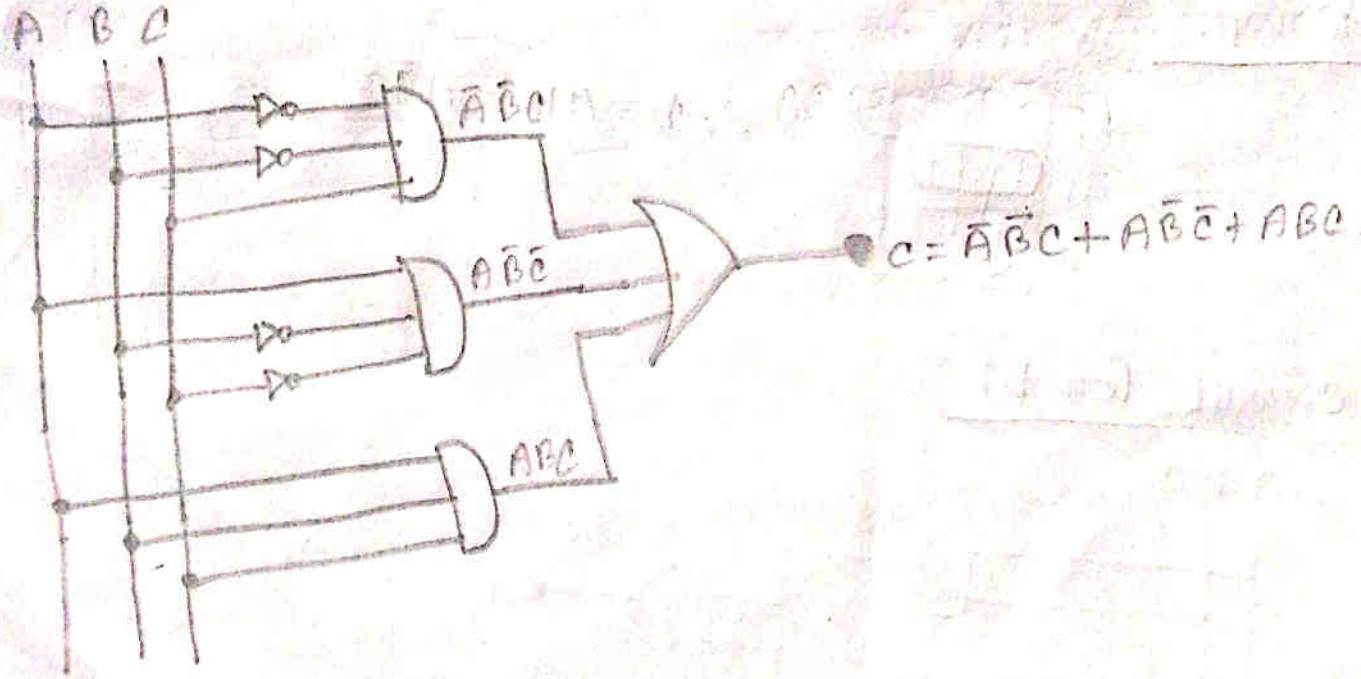
$C = \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$

K-map:



$\therefore C = \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$

Circuit for C:

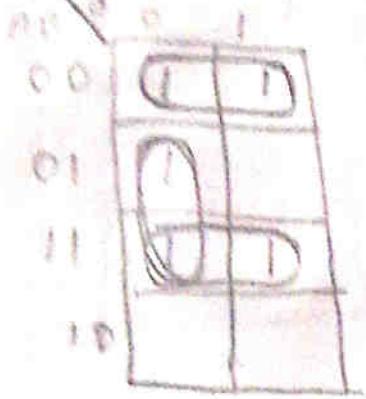


For d:

$d = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC.$

000 001 010 110 111

k-map:



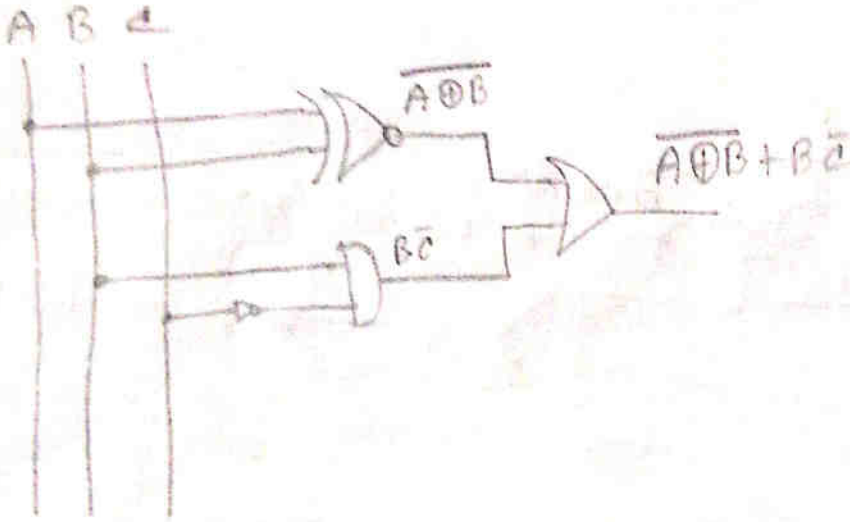
$\therefore d = \bar{A}\bar{B} + B\bar{C} + AB$

$= AB + \bar{A}\bar{B} + B\bar{C}.$

$= \overline{A \oplus B} + B\bar{C}.$

~~circuit~~

circuit:

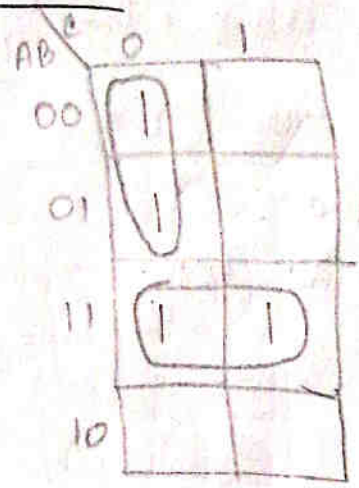


For e:

$e = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + ABC$.

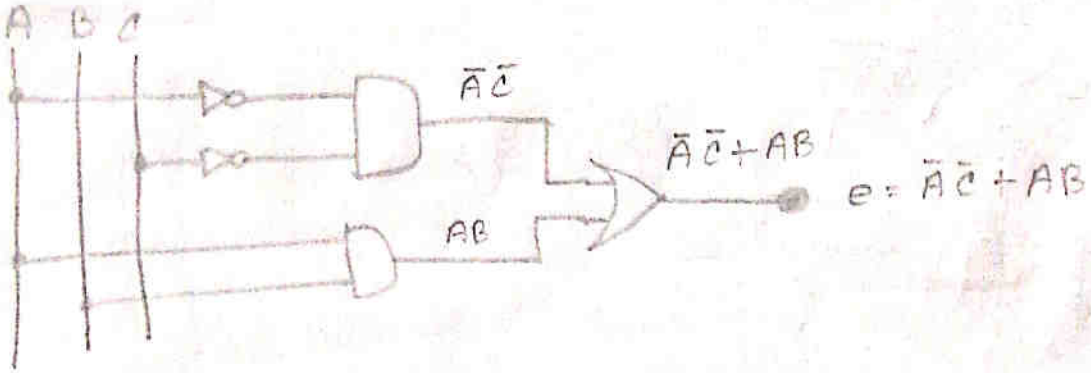
000 010 110 111

K-map:



$\therefore e = \bar{A}\bar{C} + AB$.

Circuit:

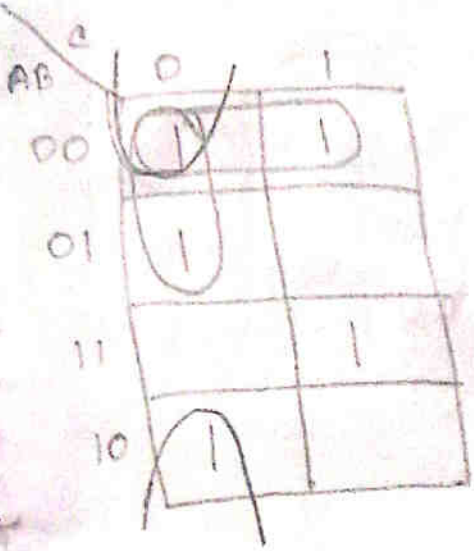


For f:

$f = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

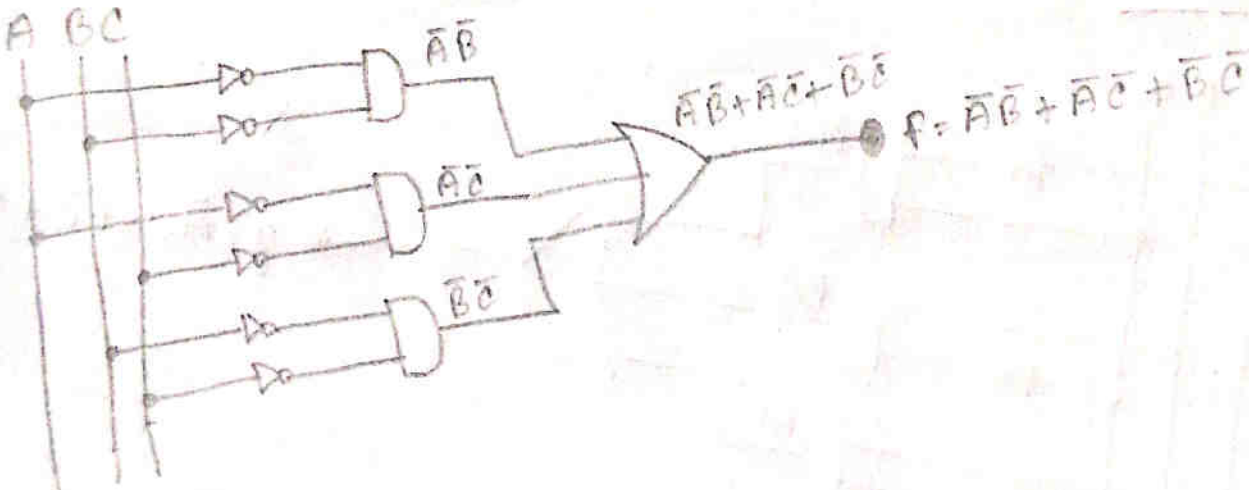
000 001 010 100 111

K-map:



$\therefore f = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$

Circuit:

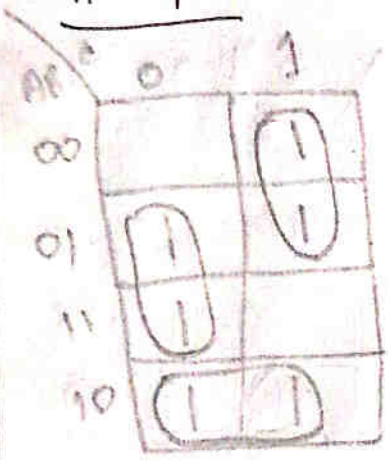


For g:

$$g = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$

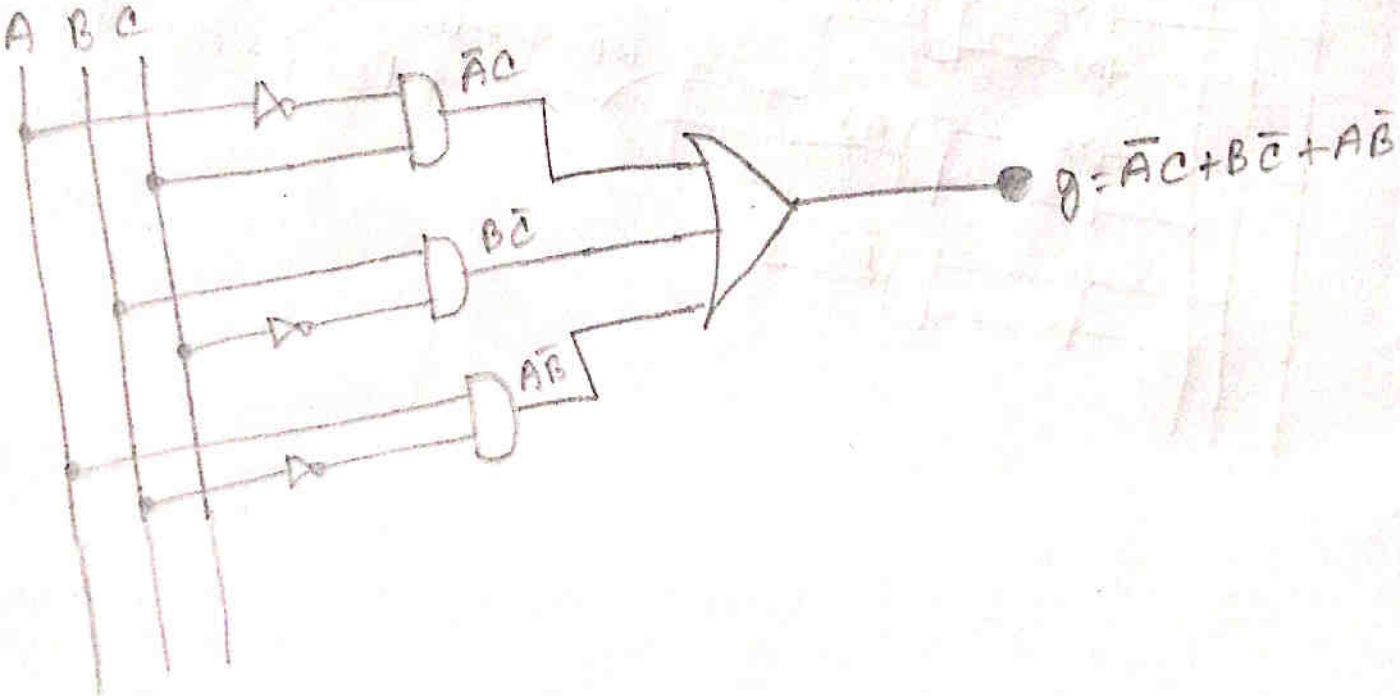
001 010 011 100 101 110

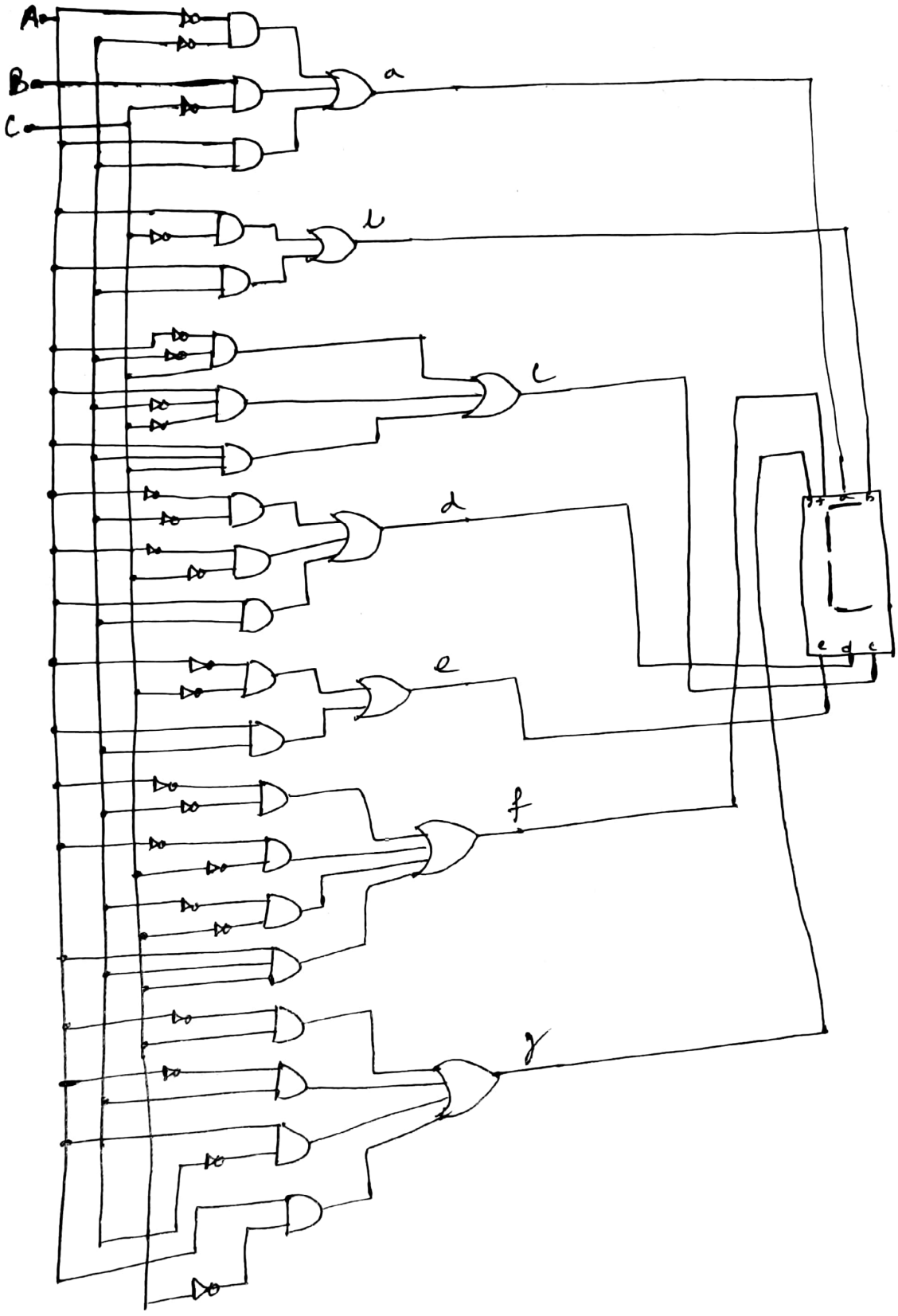
K-map:

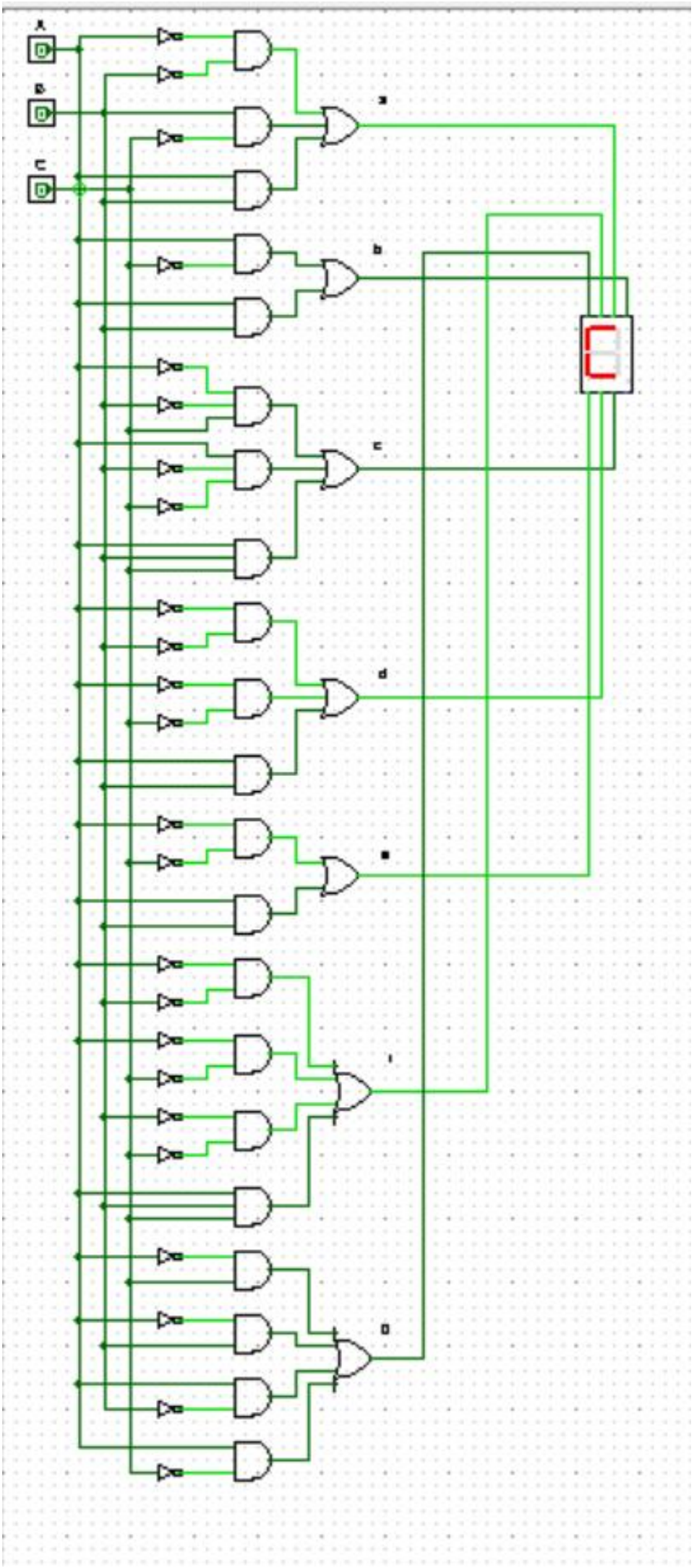


$\therefore g = \bar{A}C + B\bar{C} + A\bar{B}$

Circuit:






A
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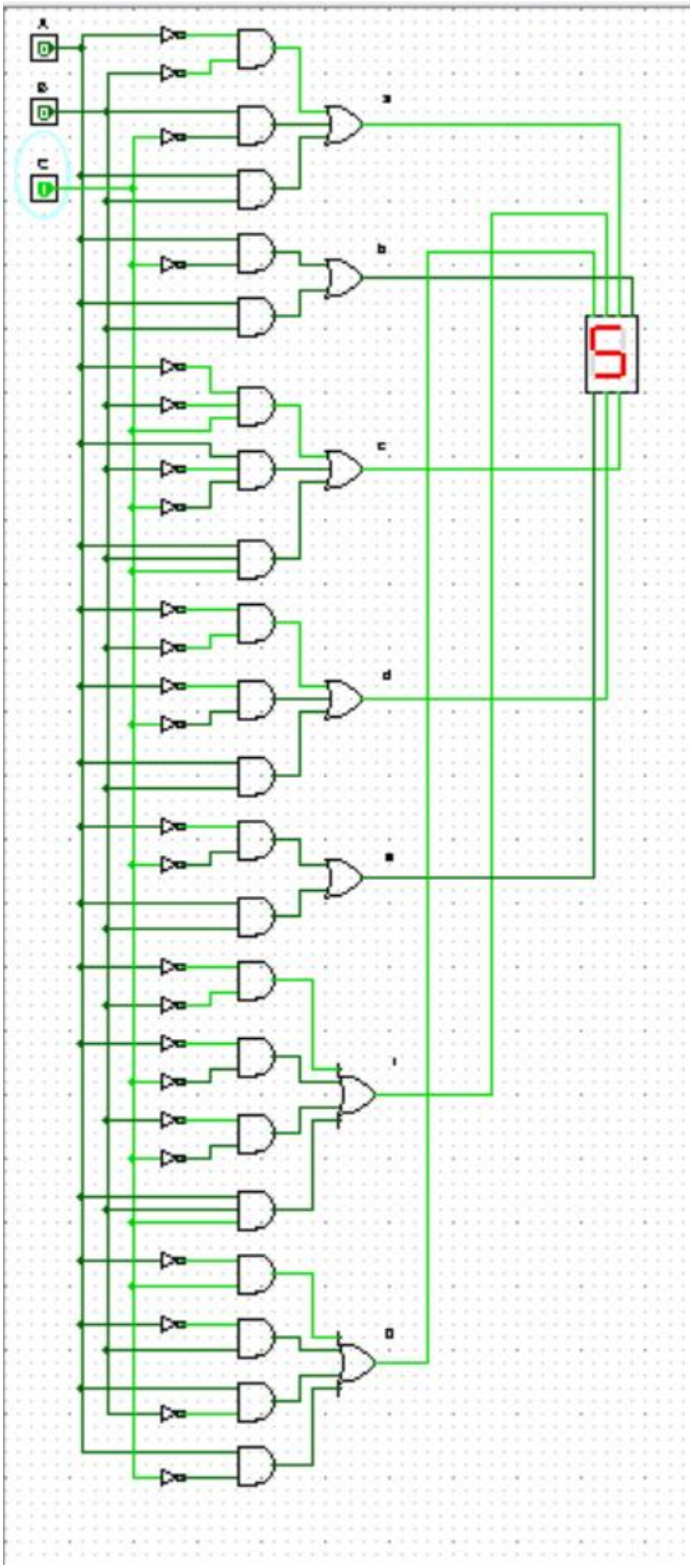
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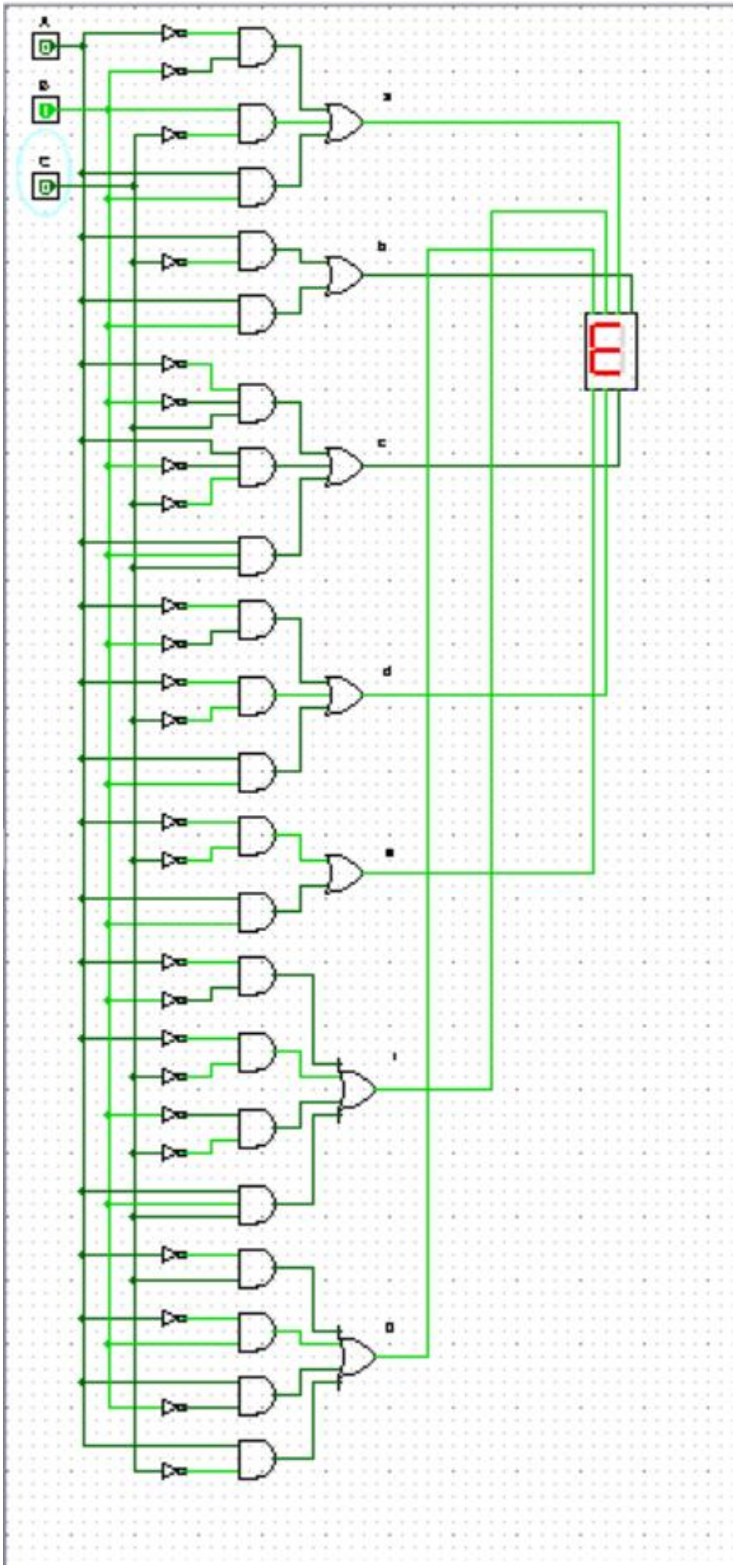
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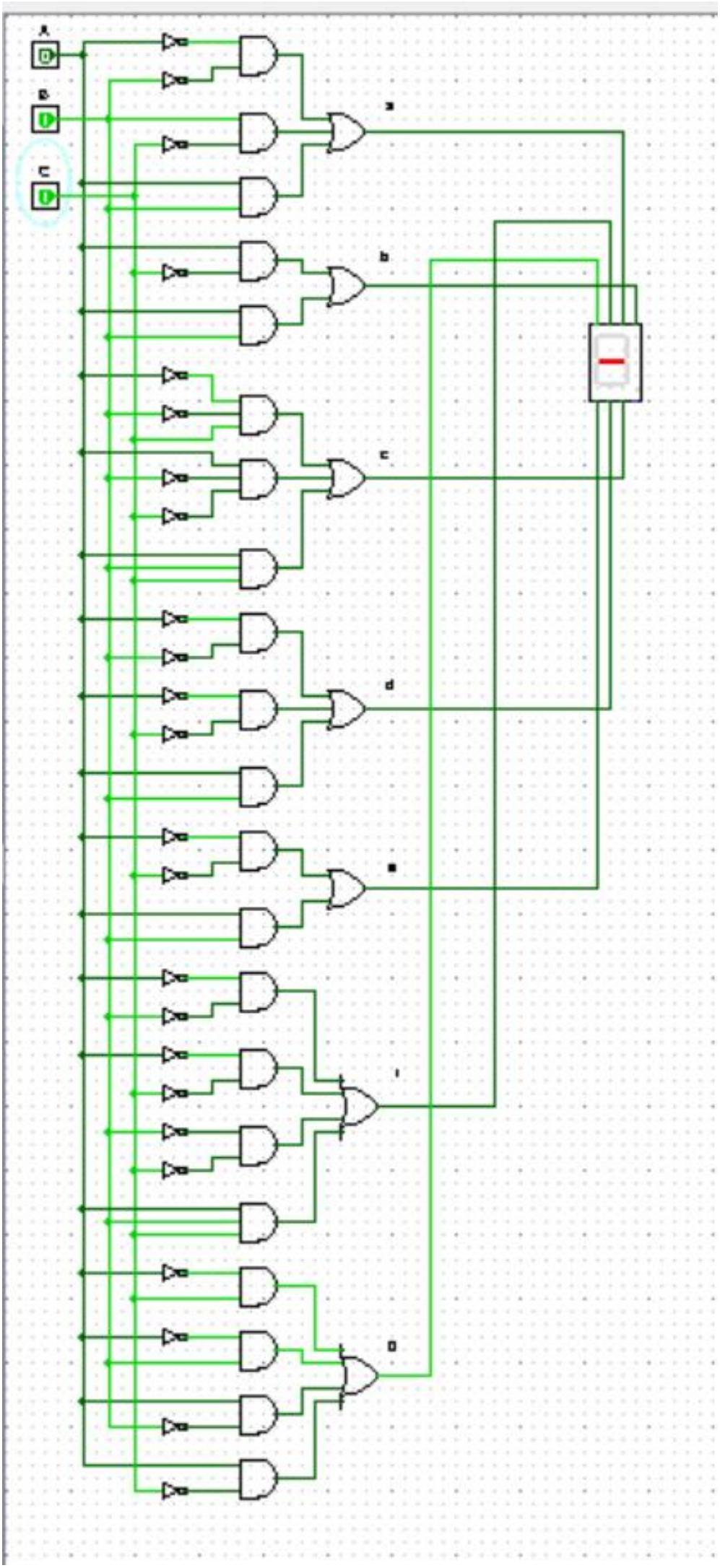
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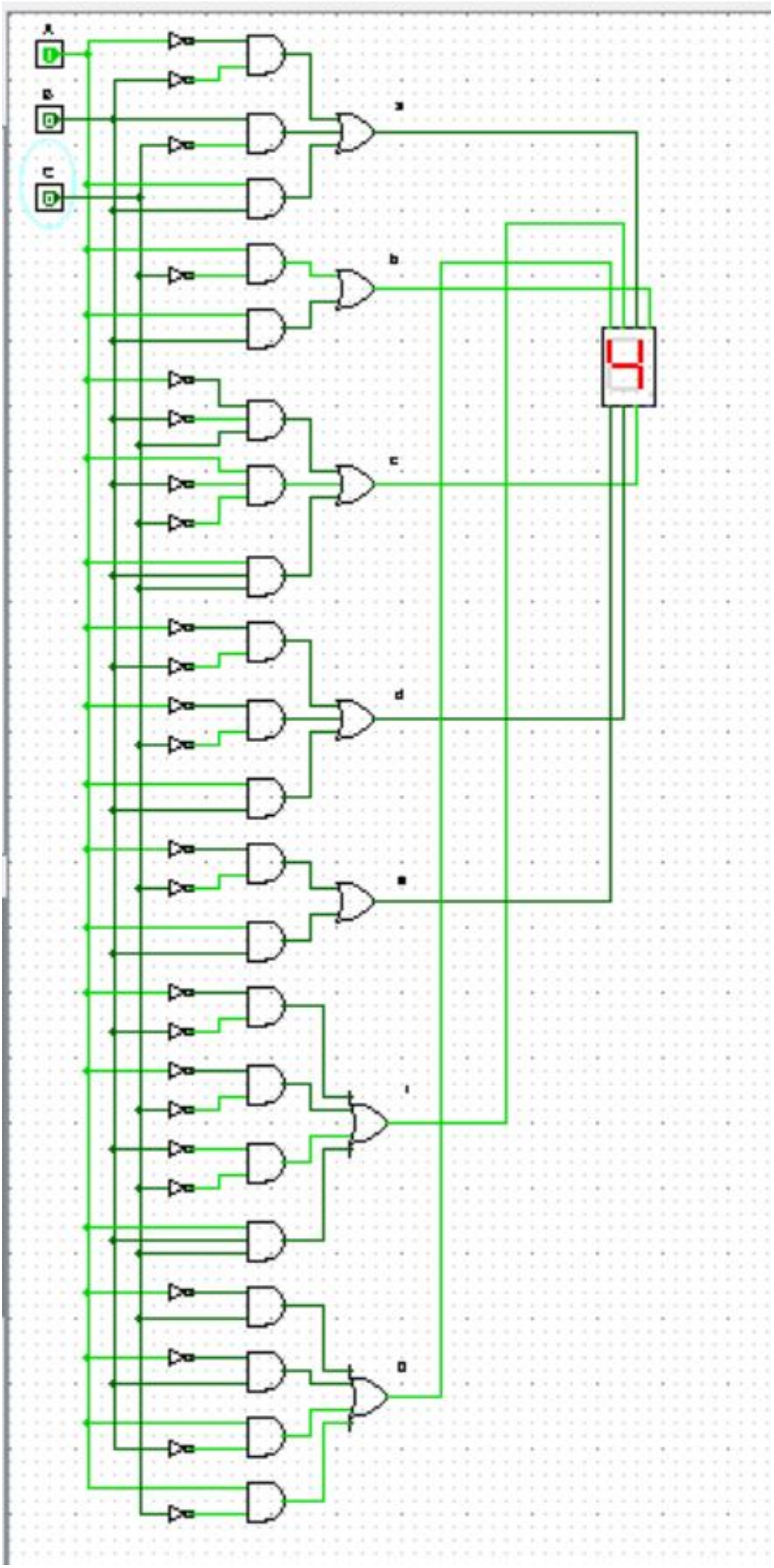
A
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C
0
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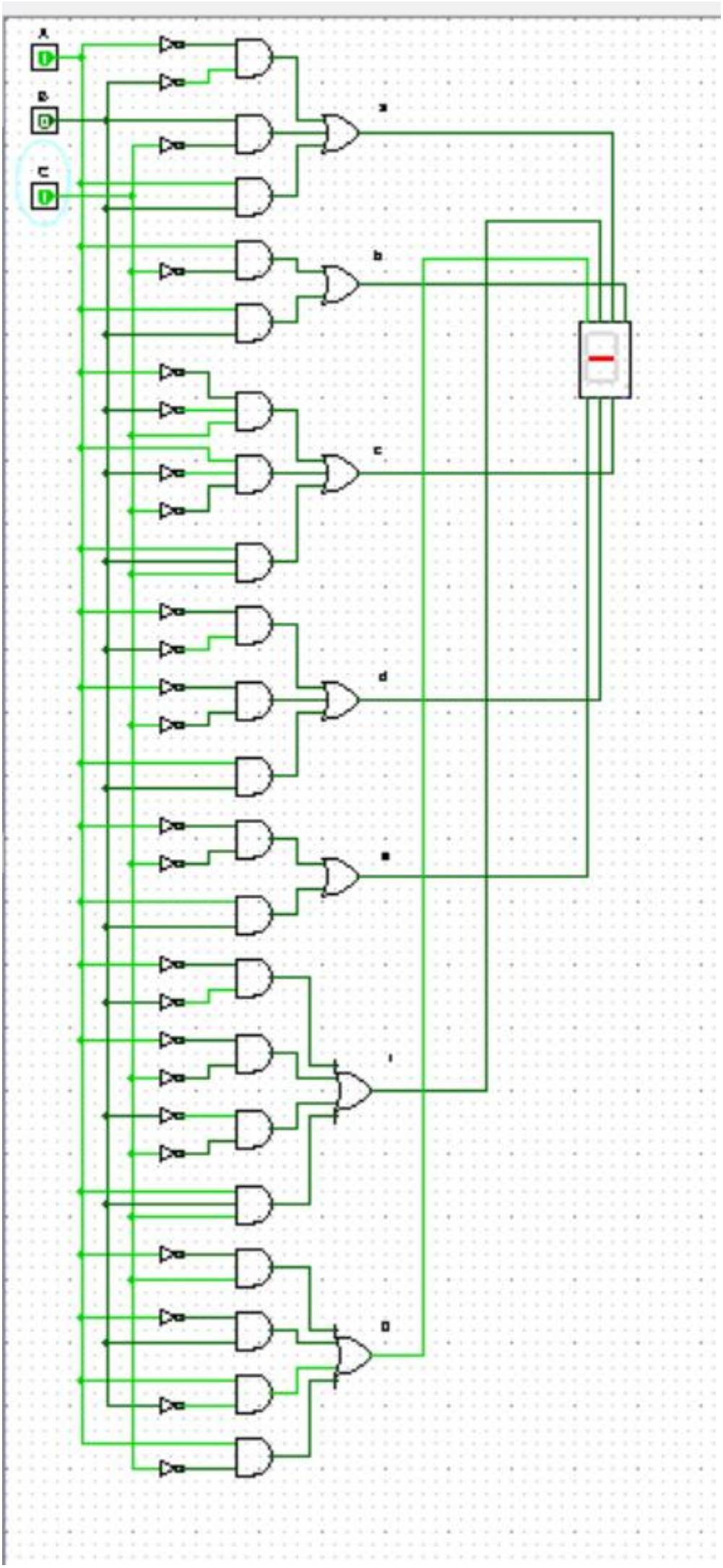
4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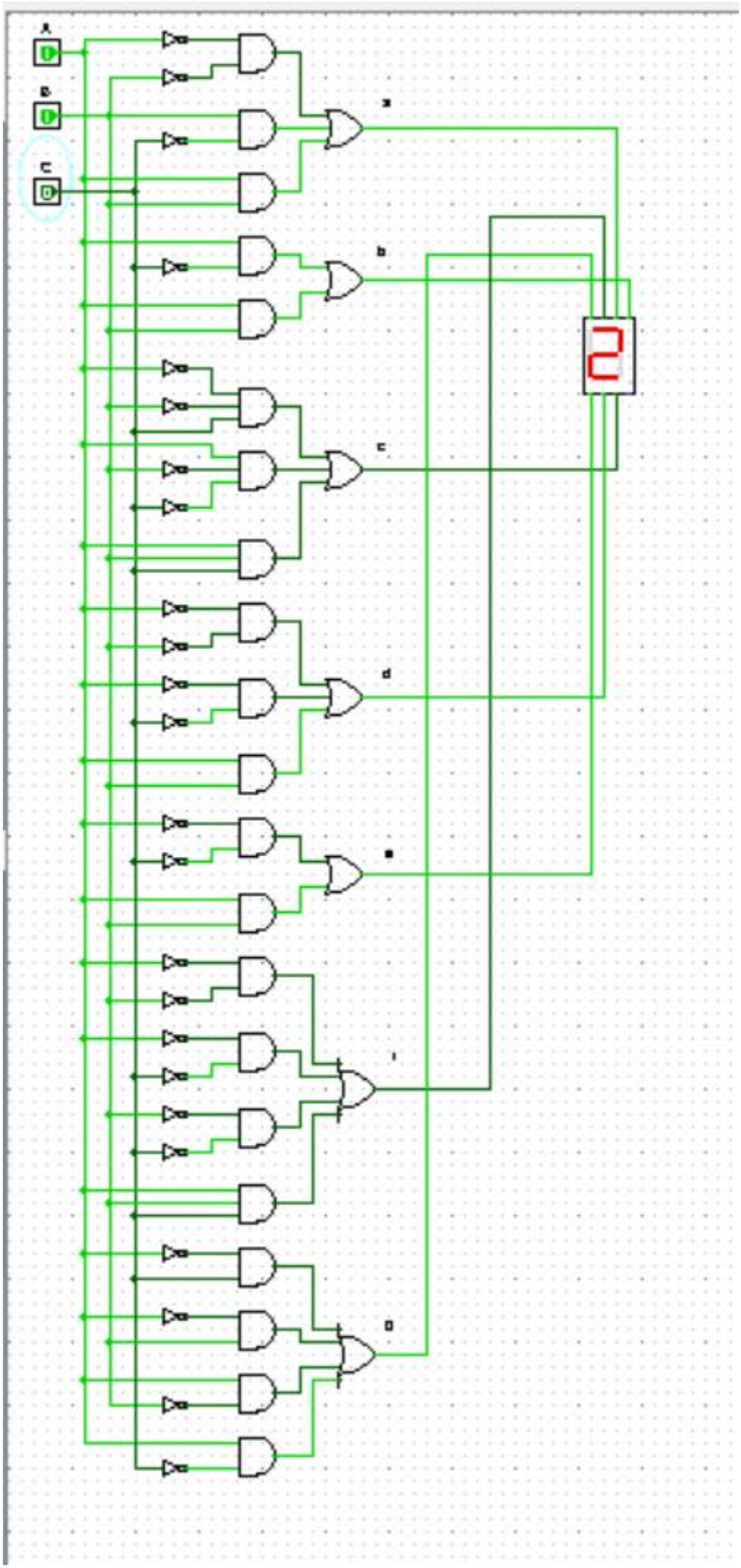
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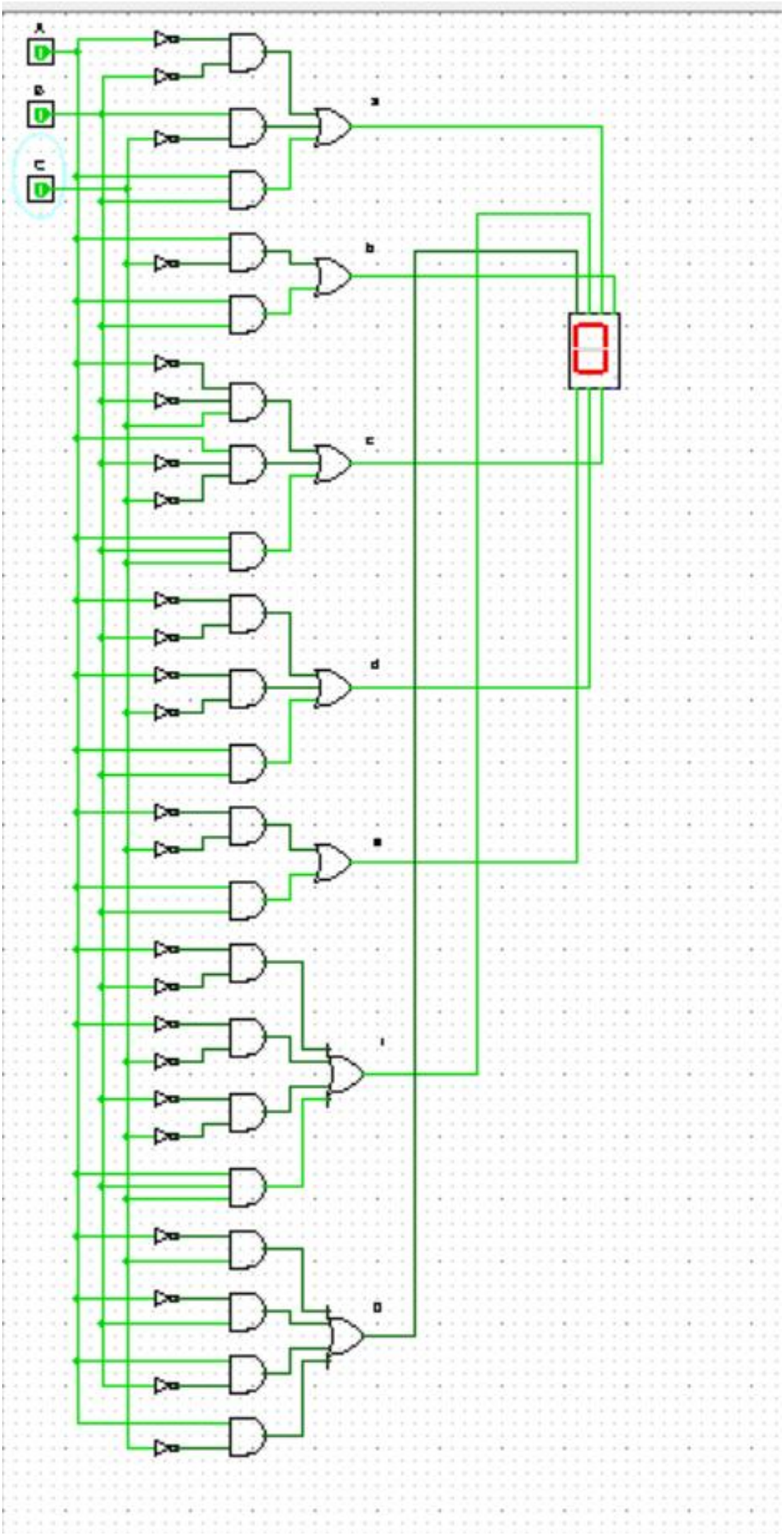
A
B
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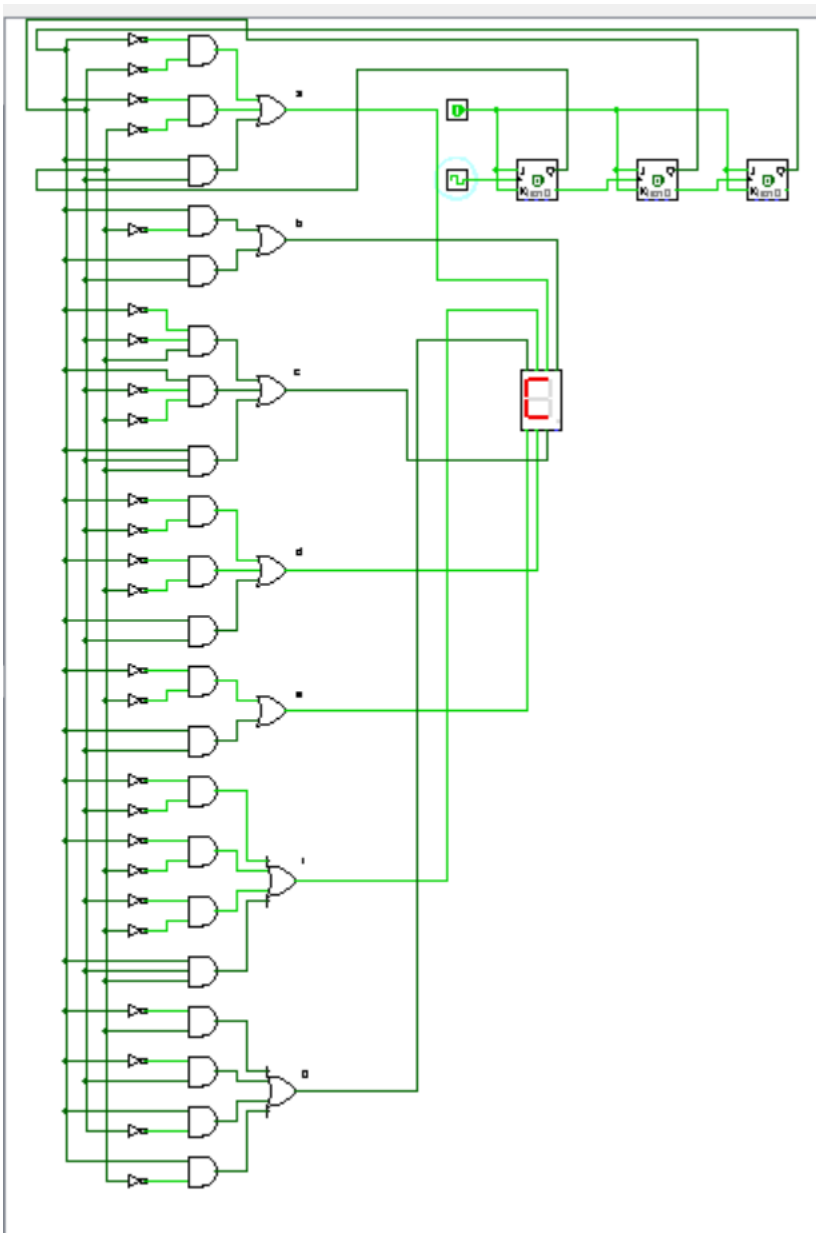
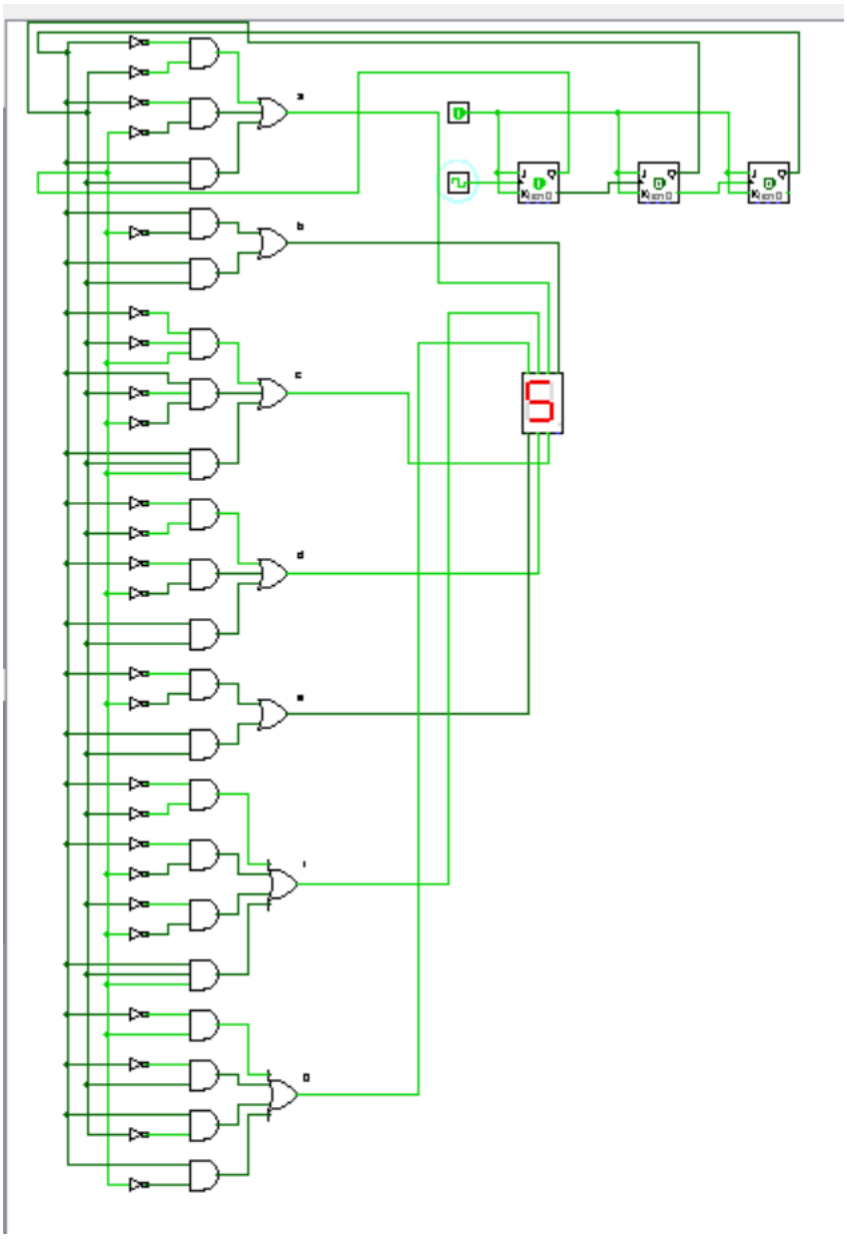
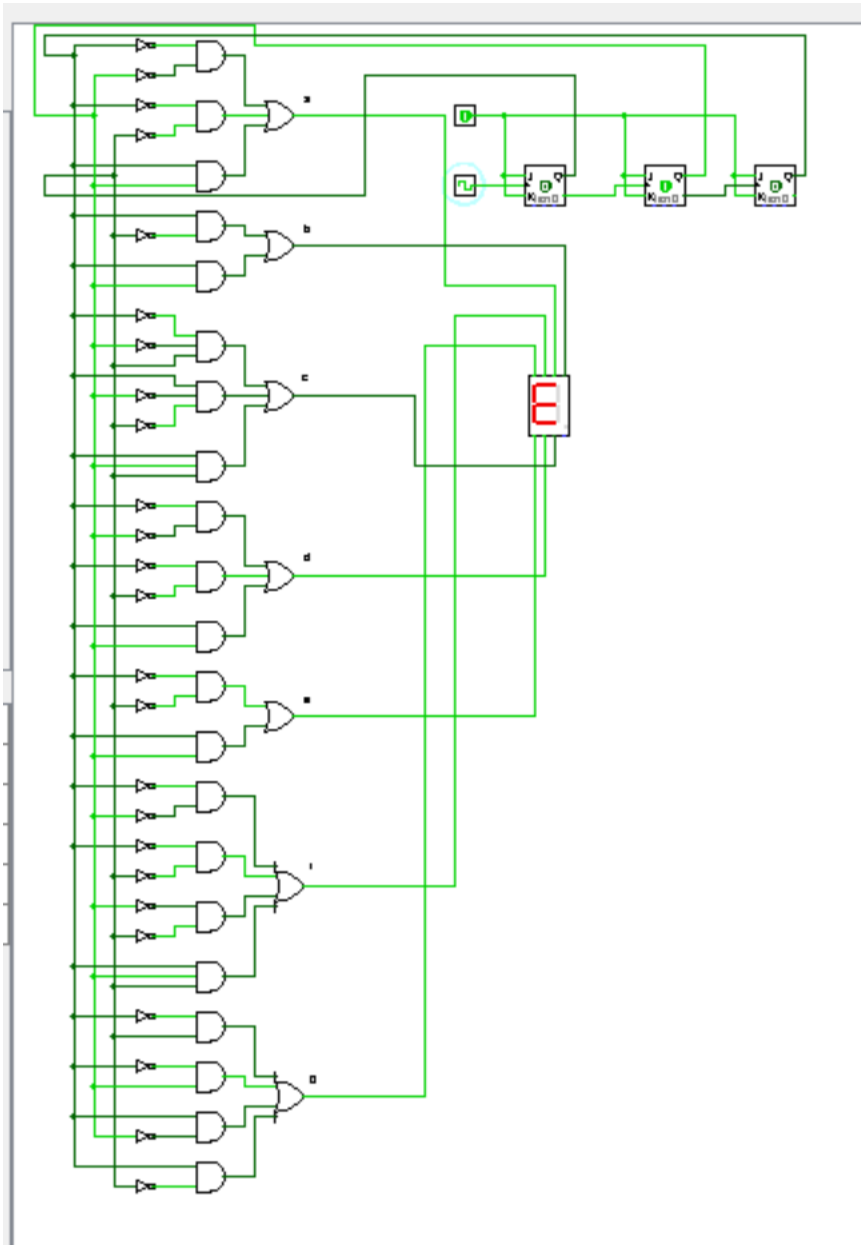
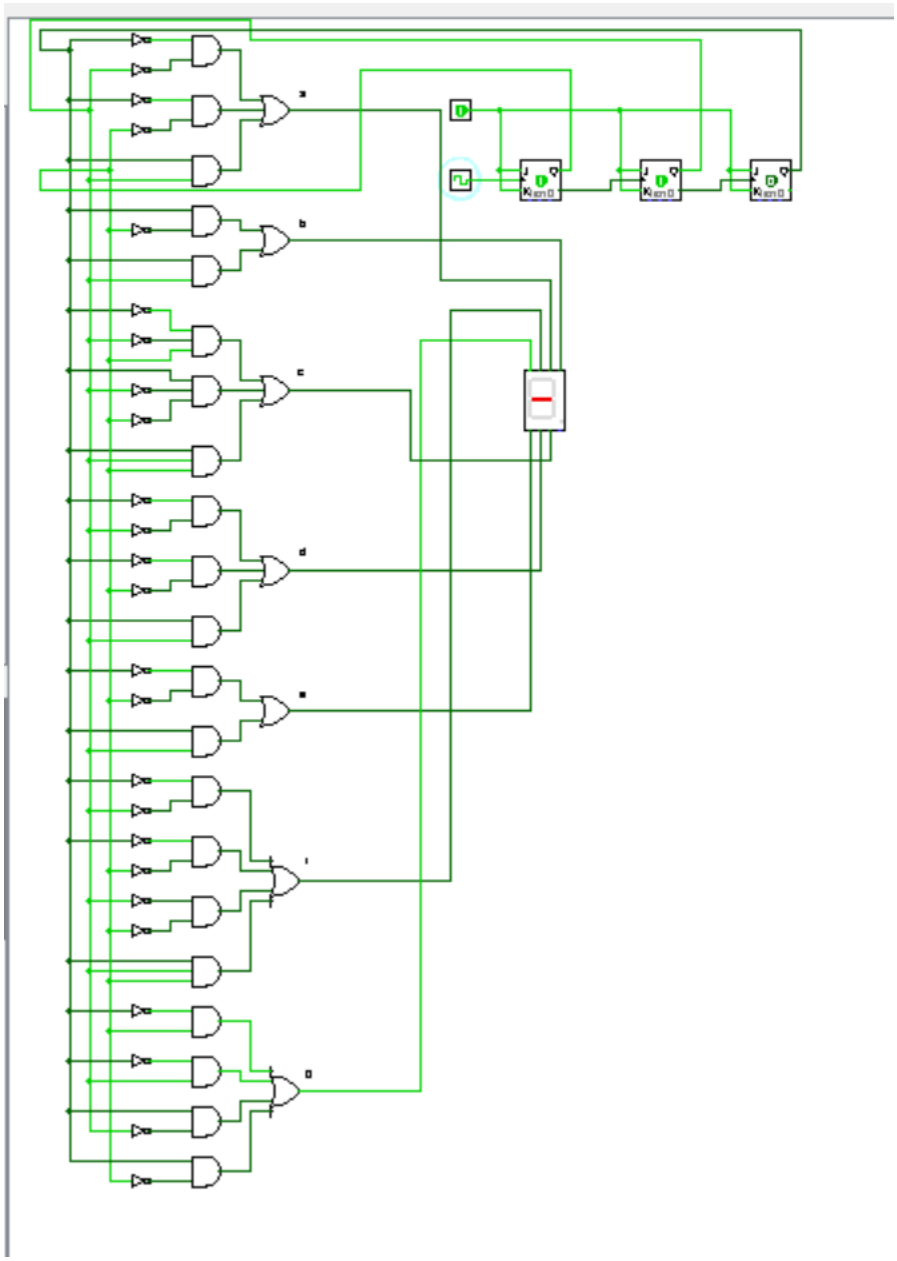
g

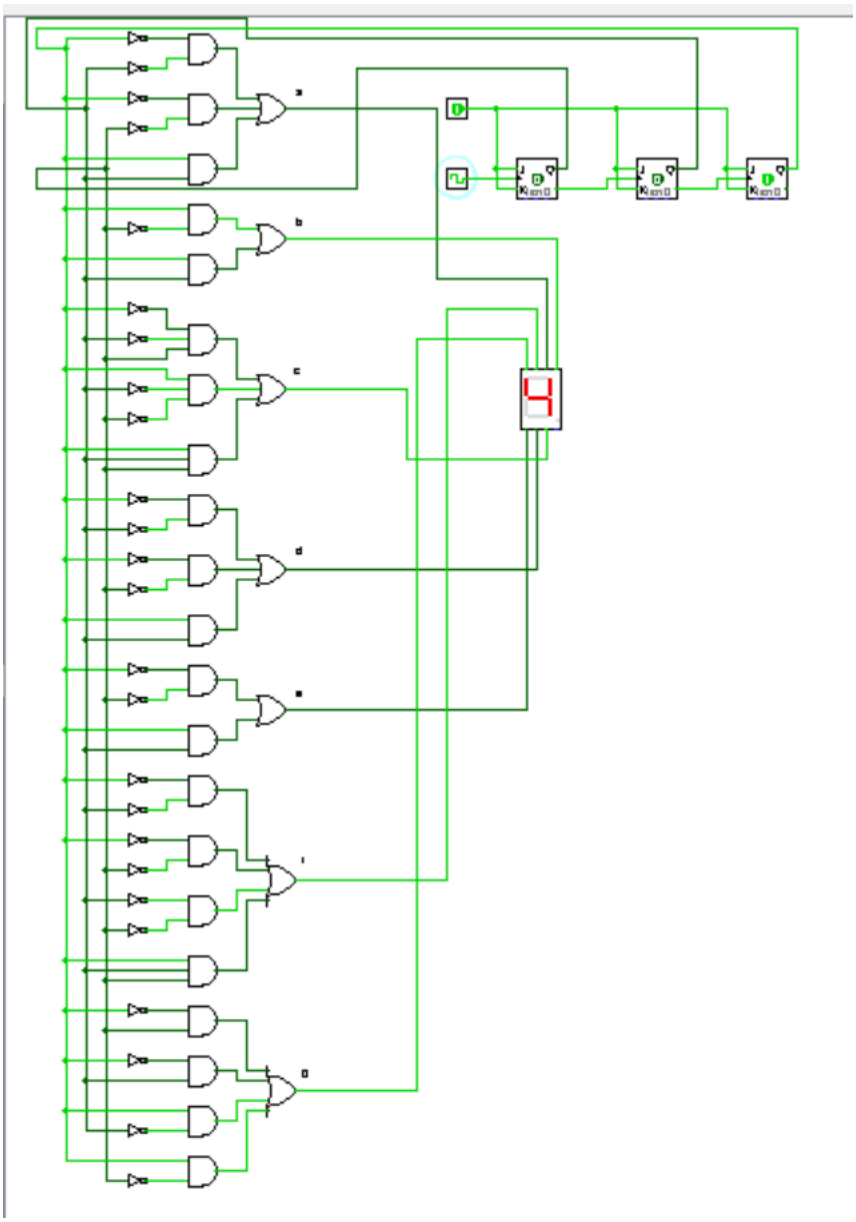
Sequential circuit (Truth Table, Circuit, logisim circuit)

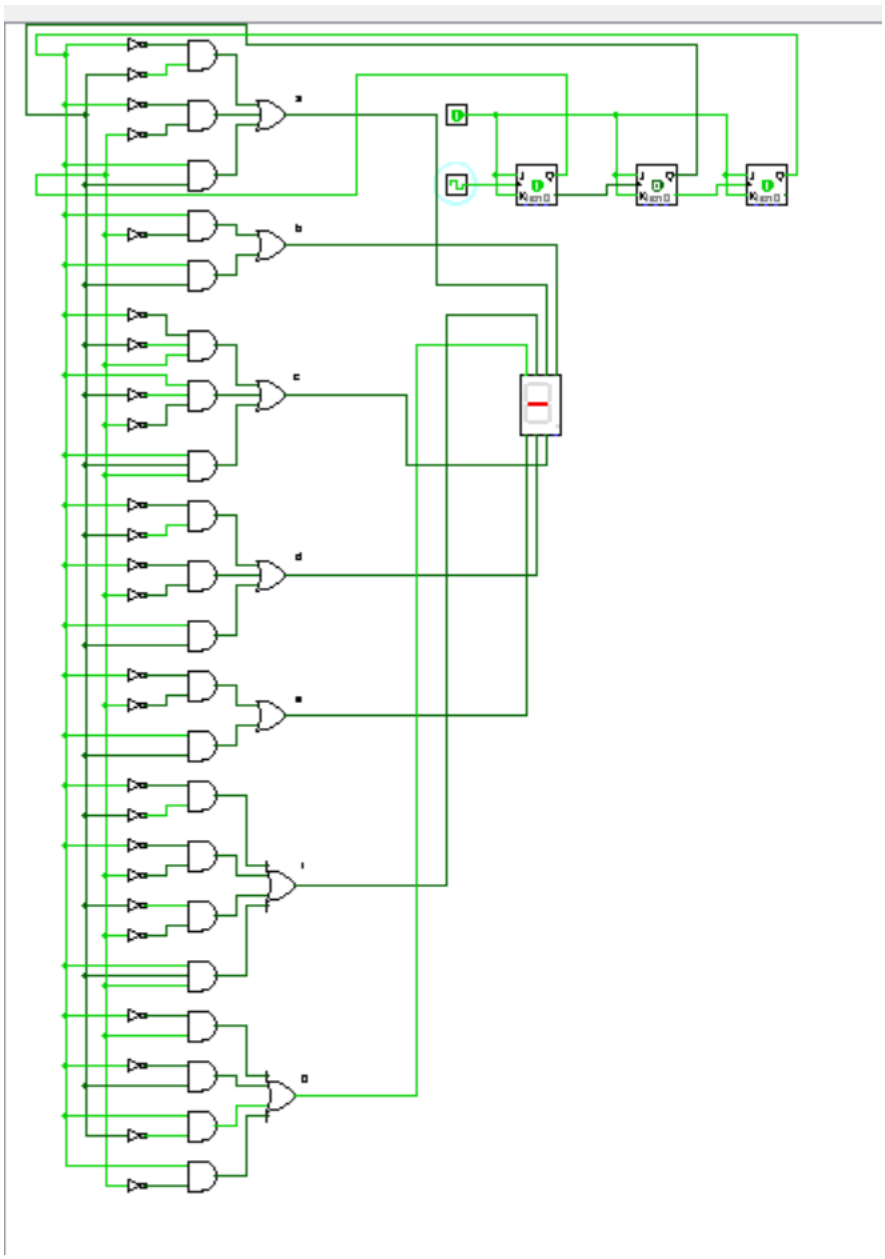


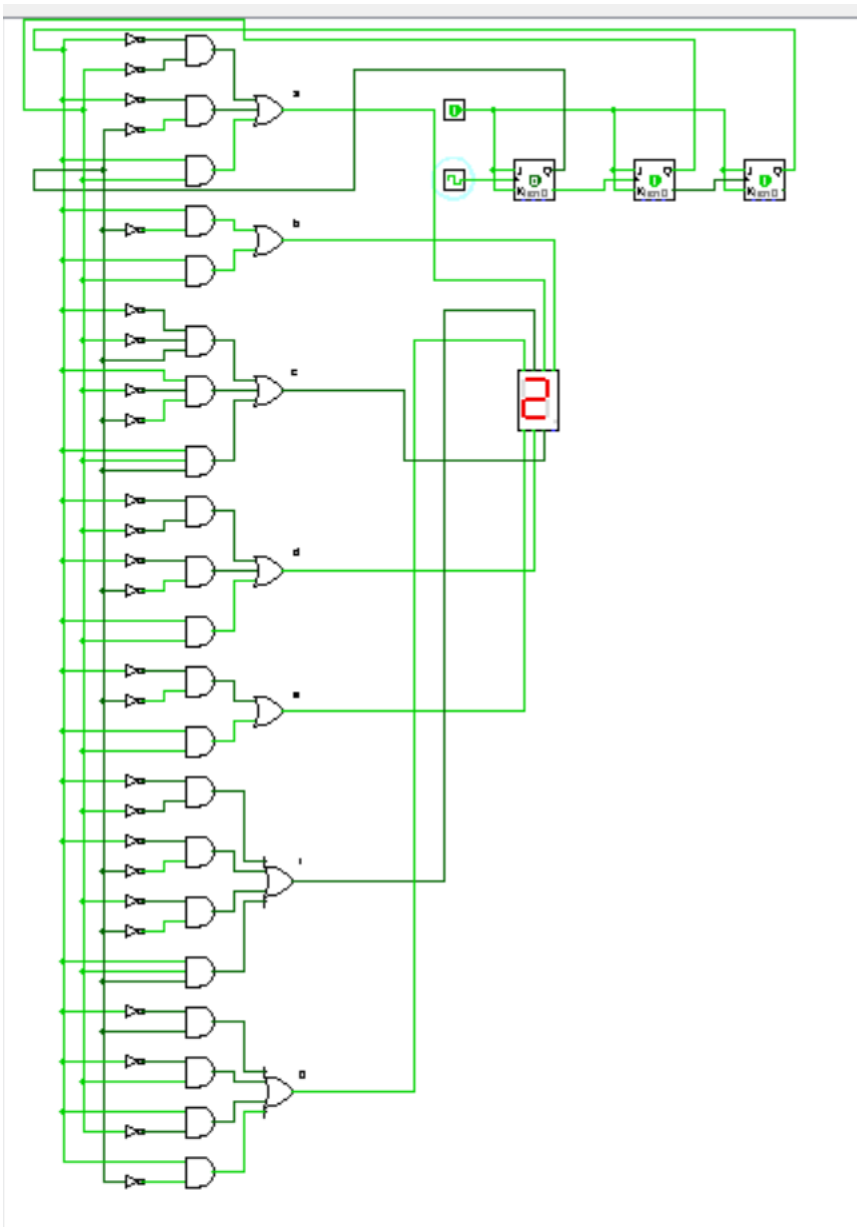


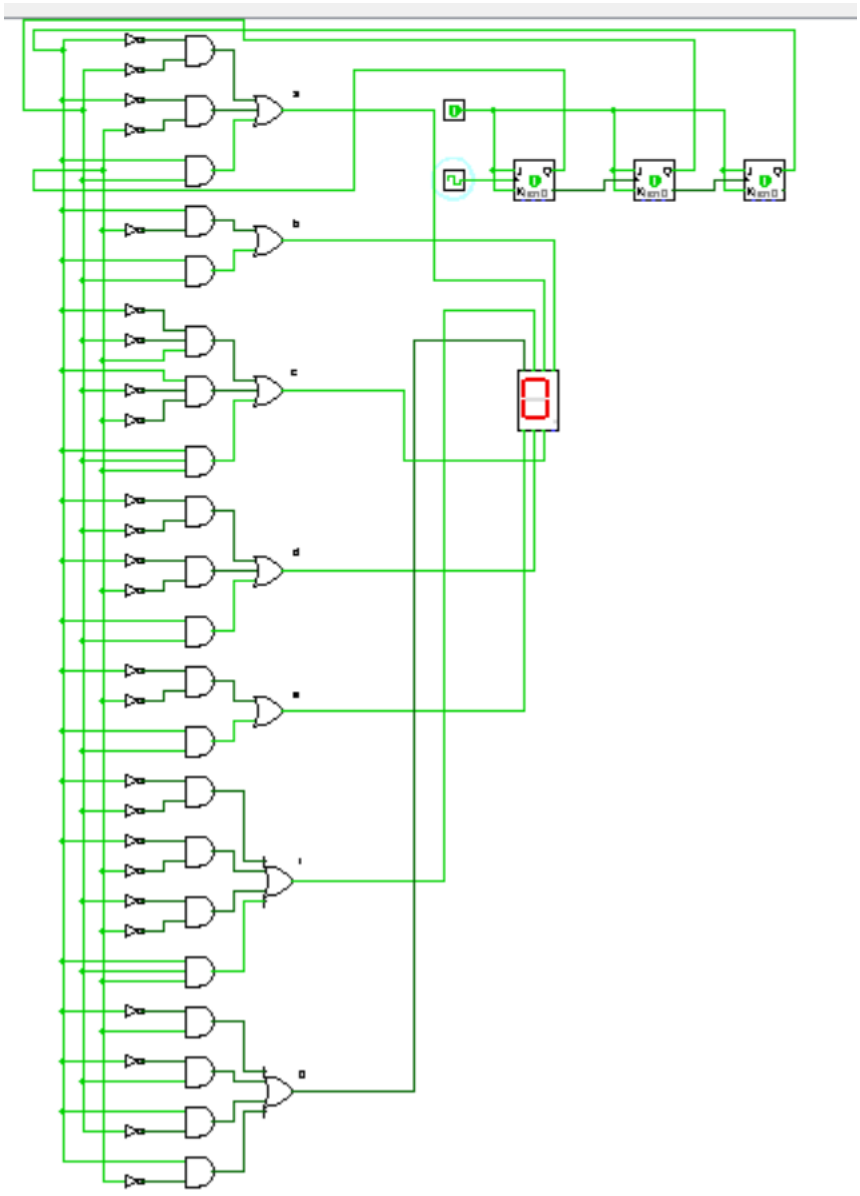












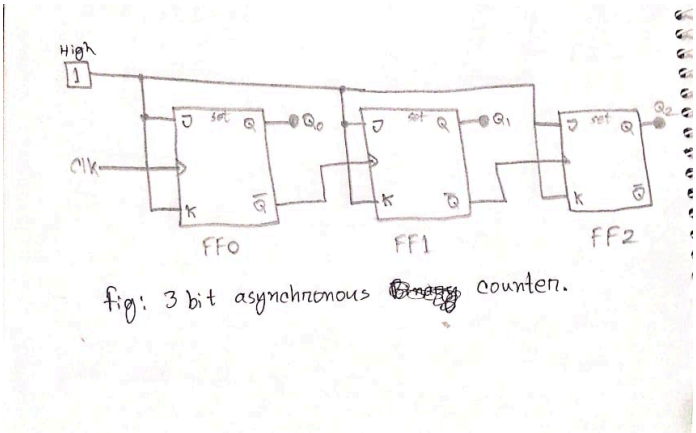
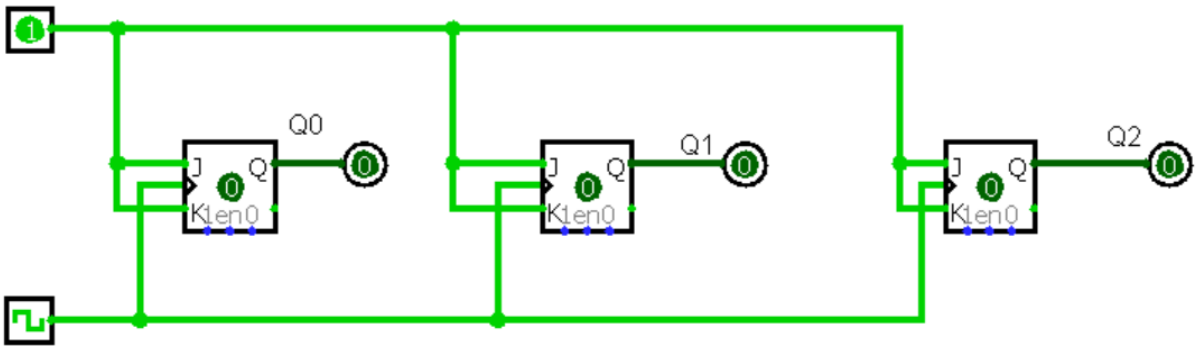


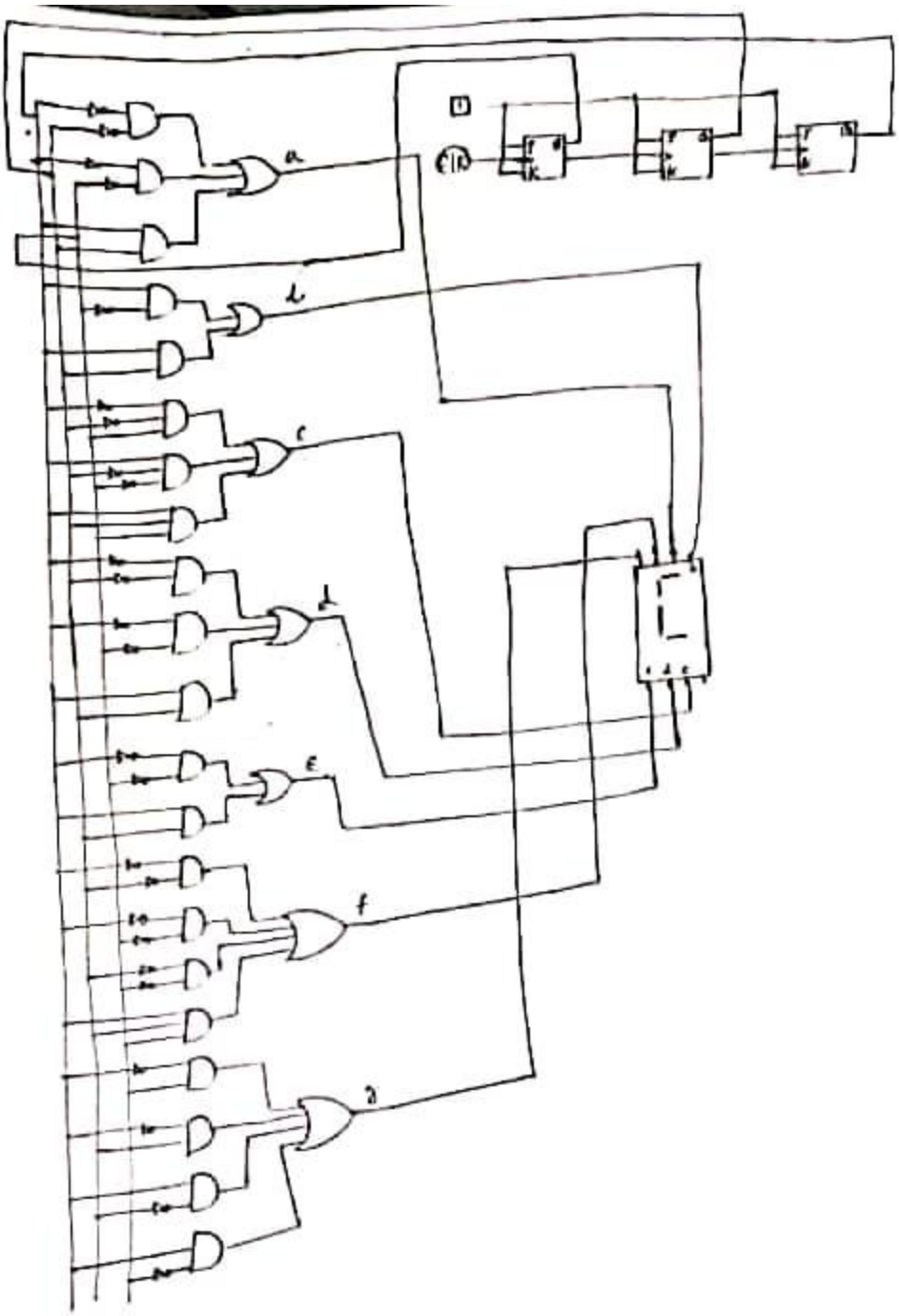
fig: 3 bit asynchronous counter.



3 Bit Asynchronos Counter

** 3 Bit Asynchronous Counter Truth Table:

Clk	Q_2	Q_1	Q_0	Decimal Eqv
Initially	0	0	0	0
1st	0	0	1	1
2nd	0	1	0	2
3rd	0	1	1	3
4th	1	0	0	4
5th	1	0	1	5
6th	1	1	0	6
7th	1	1	1	7
8th	0	0	0	0 (recycle)


a
b
c
d
e
f
g

The 555 timer IC is an integrated circuit used in a variety of timer, delay, pulse generation, and oscillator applications. The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a ~~single~~ string of stabilised waveforms of varying duty cycles from 50 to 100%.

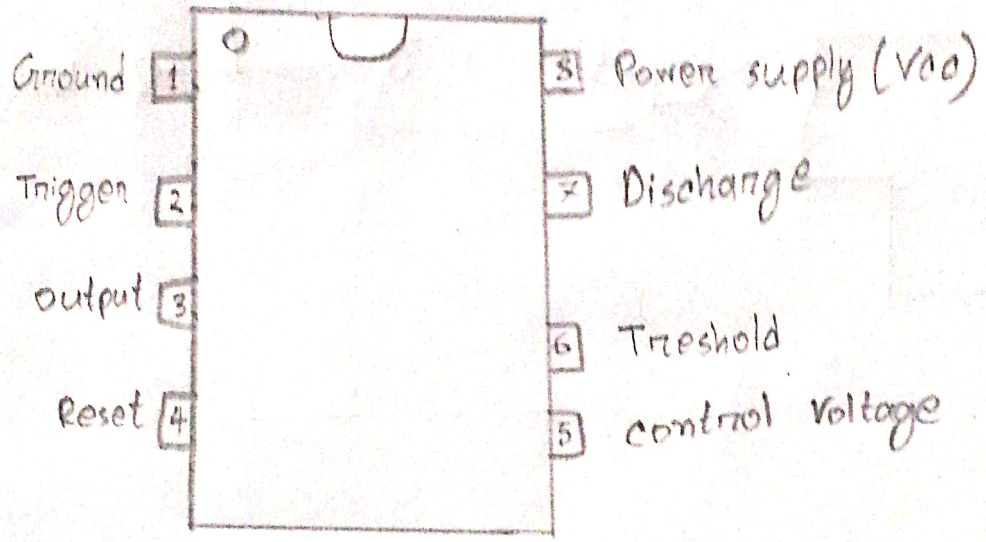


fig: 555 Timer IC.

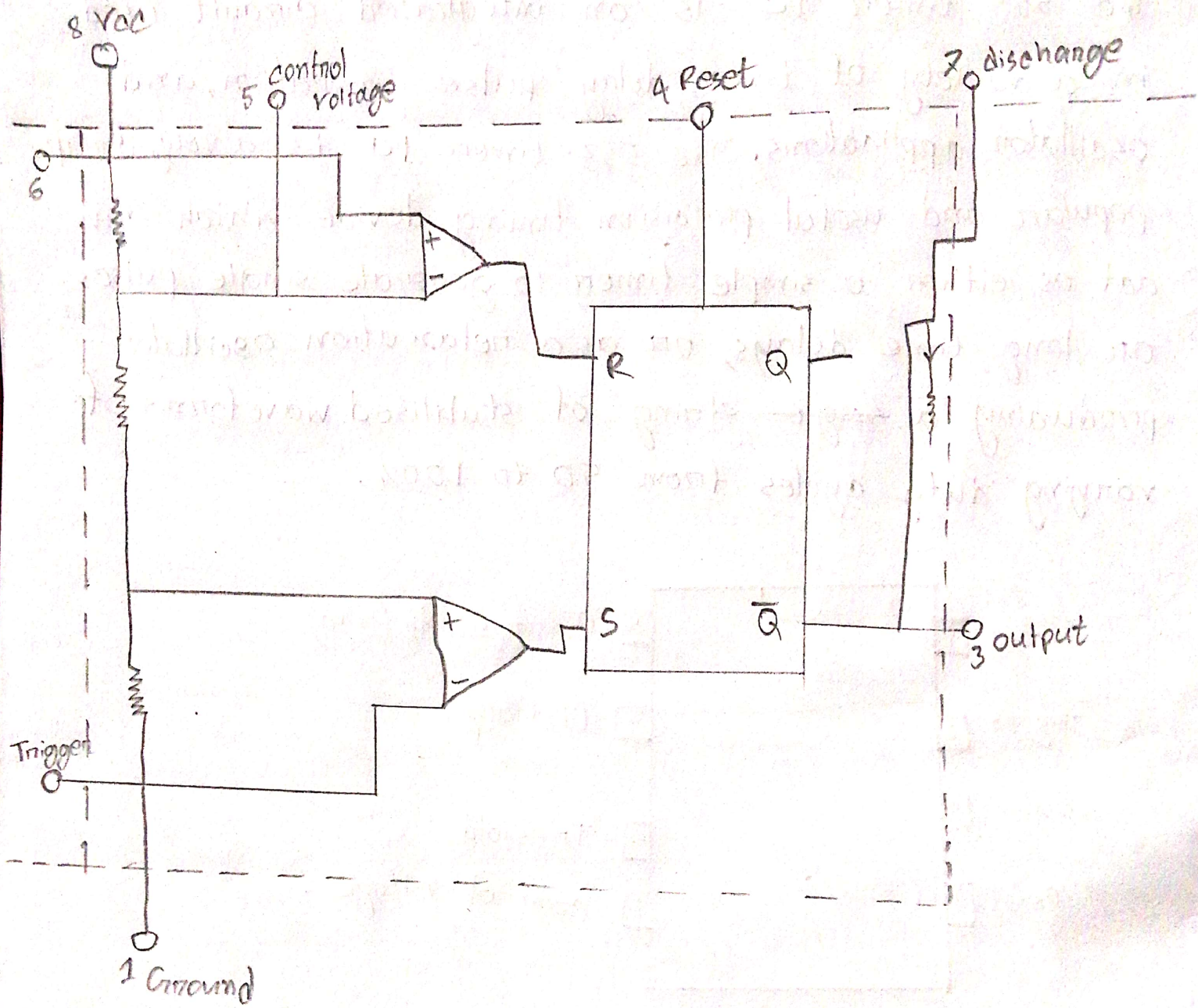


fig: Internal construction of 555 Timer IC Diagram.

Report

We are group 4. **Our project is 'CSE-4-20'.** For displaying **'CSE-4-20'** in the seven segment display we used SOP equation and circuit. we have used the process of converting BCD to seven segment decoder. At first, we filled the truth table such way so that we can display **'CSE-4-20'** in the seven segment display. Since there are total eight characters in **'CSE-4-20'**, so we need 3 BCD inputs A, B, and C and 7 outputs a, b, c, d, e, f, and g. These seven outputs of the decoder (a, b, c, d, e, f, and g) select the corresponding segments in the seven segment display. According to the value of inputs (A, B, C), the seven segment display will select the character for displaying **'CSE-4-20'.**

After filling the truth table, we derived SOP expressions from the truth table for output (a, b, c, d, e, f, g). Then by using K-MAP, we minimized expression. Then we have built a combinational logic circuit using basic gates (AND, OR, NOT) and then connected the all outputs of our combinational circuit (a, b, c, d, e, f, g) with the seven segment display. This is how we built the combinational logic circuit for displaying **'CSE-4-20'** in the seven segment display.

After creating the combinational logic circuit, we created the sequential circuit for displaying **'CSE-4-20'**. Here we used 3 JK flip flops. Because 3 FFs will count upto 8 - 000, 001, 010,011, 100, 101,110,111 - the last number is 7. Since we have 7 segment display and our inputs are 3, so we used 3 JK flip flops.

Using these 3 JK flip flops, we built and asynchronous counter and then we connected the asynchronous counter with our previous combinational circuit.

Finally, for generation continuous pulse into these JK flip flops, we used logisim default CLOCK which will do the job of both Clock and 555 timer IC. We know, 555 Timer IC is used to generate continuous clock pulse, generate time delay etc. This is why for providing continuous clock pulse to these JK flip flops, we used default clock of Logisim, which will continuously show **'CSE-4-20'** all characters one by one, after a certain time delay on the Logisim seven segment display.