[This question paper contains 4 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 1123 **I**

Unique Paper Code : 2222013503

Name of the Paper : Digital Electronics

Name of the Course : **B.Sc. Hons.–(Physics)_NEP: UGCF-2022**

Semester : V

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Attempt **five** questions in all.
3. Question No. **1** is compulsory.
4. **All** questions carry equal marks.

1. Attempt any **Six** parts (all parts carry equal marks) (3×6=18)

(a) Write three differences between synchronous and asynchronous counters.

(b) What are Passive and Active components in electronics? Explain giving appropriate examples.

(c) Why JK Master-Slave flip flop is preferred over level triggered JK latch?

(d) Explain the role of control voltage (pin 5) and reset (pin 4) in IC 555 timer.

(e) Subtract $(32)_{10}$ from $(12)_{10}$ using 2's complement method in 8-bit representation.

(f) Draw the circuit of a 5-bit even parity generator. Use the binary number 1100 and 0111 to generate the output.

(g) Realize a 2-input OR gate using diodes and resistors and briefly explain its working.

2. (a) A four variable truth table has high output when at least two input variables are in the high state. Draw the truth table and derive the minimized expression using Boolean algebra. Realize the logic circuit using 2-input NAND gates only.

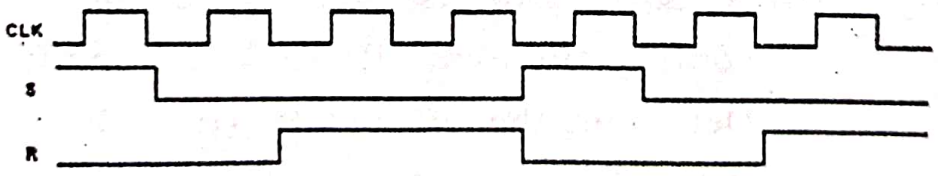
(b) Determine the minimized Boolean expression for the function: $F(A,B,C,D) = \sum m(0,8,9,10) + d(1,2,7)$ using K-map method and design the logic circuit using basic gates. (10,8)

3. (a) Implement and explain the working of a 4-bit binary addition and subtraction circuit that utilizes 2's

complement method for subtracting two numbers. Suppose the above circuit is used to subtract two binary numbers and generate carry 0 output and a sum output of 11001100. Explain how this circuit can be used to get the final answer.

(b) Implement a 16:1 Multiplexer using two 8:1 Multiplexers and explain briefly it's working. (Use only the simple block diagram of 8:1 multiplexer to implement the above). (10,8)

4. (a) Explain the working of a positive level triggered SR flip flop with the help of a circuit diagram and truth table. Explain why for S=1 and R=1 the Q output is unpredictable and lead to race condition. Draw the output waveform for the following conditions:



(b) Using the method of excitation table design the circuit of a JK flip flop using SR flip flop. Use block diagram of SR flip to draw the final circuit. (10,8)

5. (a) Design a synchronous self-correcting MOD-6 count down counter using the method of excitation table. Use negative edge triggered JK flip flop to design the counter. The initial state of the counter is 000.

(b) Explain the difference between Serial-in-serial-out (SISO) and Serial-in-parallel-out (SIPO) shift registers? Explain the working of a 4-bit SISO shift register with suitable waveform, if the binary number 1100_2 has to be shifted from the LSB side? (10,8)

6. (a) Draw circuit diagram of a monostable multivibrator using IC 555 timer and explain it's working. Derive the expression for pulse width during which it is in unstable state.

(b) IC 555 Timer is used to design a monostable configuration with R = 3.3 MΩ and C = 0.22 μF. Determine the pulse width (time for which output is high) of the output wave. Draw the waveforms across capacitor and at the output if the time period of the applied trigger input is half the above calculated pulse width. (10,8)