[This question paper contains 4 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 5568 **J**

Unique Paper Code : 2512013603

Name of the Paper : Semiconductor Device Technology

Name of the Course : **B.Sc. (H) Electronics (CORE)**

Semester : VI

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question 1 is compulsory.
3. Attempt total 5 questions in all.
4. Use of scientific calculators is allowed.

1. (a) Differentiate between single crystal, polycrystalline, and amorphous semiconductor materials. (3)

   (b) Explain heteroepitaxy. Give diagrams of lattice-matched, strained and relaxed heteroepitaxial structures. (3)

   (c) Compare wet and dry wafer cleaning techniques. Mention one chemical used in each. (3)

   (d) Compare thermal diffusion and ion implantation as methods for doping semiconductors. (3)

(e) In an optical lithography system, the wavelength of the light source is λ=248 nm and the numerical aperture (NA) of the lens system is 0.6. Assuming a process factor k_1=0.5, calculate the minimum resolvable feature size (critical dimension). (3)

(f) Compare CMOS and Bipolar technologies in terms of power consumption, speed and integration density. (3)

2. (a) Derive the expression for dopant concentration variation in the crystal during Czochralski (Cz) growth using the concept of effective segregation coefficient (k_e). (6)

(b) Describe the Float Zone (Fz) technique. How does it help to achieve high-purity crystals as compared with Cz technique? (6)

(c) Explain the concept of Encapsulation used to grow GaAs in Czochralski (Cz) method. (6)

3. (a) Explain in detail the process of Vapor-Phase Epitaxy (VPE). Discuss its mechanism, advantages and applications in semiconductor device fabrication. (6)

(b) Describe the Molecular Beam Epitaxy (MBE) technique. Discuss the process, equipment used, advantages and why MBE is preferred for low-volume high-performance applications. (6)

(c) Explain the process of etching in semiconductor fabrication. Differentiate between dry etching and wet etching in terms of mechanism, process control, materials used, and applications. (6)

4. (a) Discuss the Deal-Grove model of oxidation. Derive the equations used to describe oxide thickness growth over time. (6)

(b) A wet oxidation process at 1100°C has the following rate constants:

$B = 0.3\ \mu m^2/hr$

$B/A = 0.06\ \mu m/hr = 0.06$

Calculate the oxide thickness grown after 4 hours of oxidation on bare silicon. (6)

(c) Explain the effect of impurities on the oxidation process in semiconductor fabrication. How do different types of impurities (boron, phosphorus and arsenic) influence the oxidation rate of the oxide layer? (6)

5. (a) Explain the process of thermal diffusion in semiconductors. Derive the diffusion equation for a constant surface concentration and plot the resulting diffusion profile. (6)

(b) Explain the process of doping in semiconductors using ion implantation. Describe the process and discuss parameters such as implantation range and channeling effects. (6)

(c) What is a clean room and why is it essential for lithography processes? Describe the exposure methods in optical lithography with a diagram and discuss the role of photoresist. (6)

6. (a) Explain electron beam lithography in detail. Compare it with optical lithography in terms of resolution, throughput and applications. (6)

(b) Explain in detail the metallization processes used in IC fabrication. (6)

(c) Discuss various isolation techniques used in integrated circuits, including LOCOS (Local Oxidation of Silicon) and STI (Shallow Trench Isolation). (6)

7. (a) Describe the step-by-step fabrication process of an NPN bipolar junction transistor (BJT). (6)

(b) Explain the process of CMOS fabrication using twin-tub or n-well technology with the help of diagrams and describe how both NMOS and PMOS are integrated on the same substrate. (6)

(c) How are passive components like resistors and capacitors fabricated in monolithic ICs? (6)