DISCIPLINE SPECIFIC CORE COURSE – 15: Basic VLSI Design

CREDIT DISTRIBUTION, ELIGIBILITY AND PRE-REQUISITES OF THE COURSE

Course title & Code	Credits	Credit distribution of the course			Eligibility criteria	Pre-requisite of the course (if any)
		Lecture	Tutorial	Practical/ Practice		
Basic VLSI Design	4	3	-	1	Class XII passed with Physics + Mathematics/Applied Mathematics + Chemistry OR Physics + Mathematics/Applied Mathematics + Computer Science/Informatics Practices	Semiconductor Devices(DSC 3, Sem I), Digital Electronics(DSC 5, Sem II)

Learning Objectives

The Learning Objectives of this course are as follows:
This course introduces the student to basic principle of MOS Transistor operation, SPICE model, MOS transistor and Inverter layout, CMOS layout, Inverter design, CMOS inverter, inverter characteristics and specifications. Static and Sequential MOS Logic design, pass transistor logic, static & dynamic latches, flip flops, static & dynamic registers, Monostable sequential circuits. MOS memory design, RAM & ROM cells, Logic families performance.

Learning outcomes

The Learning Outcomes of this course are as follows:

- Understand the concept of models of MOS devices and their implementation in designing of CMOS inverter
- Measure the performance parameters like threshold voltage, noise margins, time delays etc.
- Familiarize with the techniques and components involved in combinational MOS circuit designs.
- Describe the various types of semiconductor memories and issues involved in them

SYLLABUS OF ELDSC-15 Total Hours- Theory: 45 Hours, Practicals: 30 Hours

UNIT – I (12 Hours)

Metal Oxide Semiconductor (MOS): Introduction to basic principle of MOS transistor, large signal MOS models (long channel) for digital design. MOS SPICE model, MOS Transistor layout(PMOS and NMOS)

UNIT – II (12 Hours)
MOS Inverter: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, Dynamic behaviour, Propagation Delay and Power Consumption.

UNIT – III (11 Hours)
Combinational MOS Logic Design: Static MOS design, Pass Transistor logic, complex logic circuits.
Sequential MOS Logic Design - Static latches, Flip flops & Registers, Dynamic Latches & Registers, Monostable sequential circuits.

UNIT – IV (10 Hours)
Memory Design: ROM & RAM cells design. Dynamic MOS design- Dynamic logic families and performances.
Design for testability: Introduction, Fault types and models, Controllability and observability, AdHoc Testable design techniques, Scan –based techniques.

Practical component (if any) – Basic VLSI Design
(PSpice/other Simulation Software)

Learning outcomes

The Learning Outcomes of this course are as follows:

- Reproduce the characteristics of digital circuits like inverter and other logic gates based on CMOS technology.
- Design the digital circuit components like latches, multiplexers etc.
- Perform experiments and the circuit design and collect and analyse the data
- Prepare the technical report on the experiments carried

LIST OF PRACTICALS (Total Practical Hours- 30 Hours)

1. To plot the (i) output characteristics & (ii) transfer characteristics of an n-channel and p-channel MOSFET.
2. To design and plot the static and dynamic characteristics of a digital CMOS inverter.
3. To design and plot the output characteristics of a 3-inverter ring oscillator.
4. To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.
5. To design and plot the characteristics of a 4x1 digital multiplexer using pass-transistor logic.
6. To design and plot the characteristics of a positive and negative latch/master-slave edge triggered registers based on multiplexers.

7. To prepare layout for given logic function and verify it with simulations.
   To measure propagation delay of a given CMOS Inverter circuit.

Note: Students shall sincerely work towards completing all the above listed practicals for this course. In any circumstance, the completed number of practicals shall not be less than six.

Essential/recommended readings

1. Weste and Eshraghian, —Principles of CMOS VLSI design, Addison-Wesley, 2002.
2. Basic VLSI design: Douglas A Pucknell, Kamran Eshraghian, PHI, 3rd edition

Suggestive readings

1. Kang & Leblebigi —CMOS Digital IC Circuit Analysis & Design- McGraw Hill, 2003.
2. Rabey, —Digital Integrated Circuits Design, Pearson Education, Second Edition, 2003.

Note: Examination scheme and mode shall be as prescribed by the Examination Branch, University of Delhi, from time to time.