1. (a) Explain the formation of a potential barrier across a PN junction and discuss how the width of this barrier varies with the applied voltage in forward and reverse-biased conditions.

- **Formation of a Potential Barrier:**
    - When a p-type semiconductor and an n-type semiconductor are joined together, a PN junction is formed.
    - Due to the concentration gradient, holes from the p-side diffuse to the n-side, and electrons from the n-side diffuse to the p-side.
    - As electrons move from the n-side to the p-side, they leave behind positively charged donor ions on the n-side.
    - Similarly, as holes move from the p-side to the n-side, they leave behind negatively charged acceptor ions on the p-side.
    - This region, depleted of mobile charge carriers, is called the depletion region or space-charge region.
    - The accumulated positive charges on the n-side and negative charges on the p-side create an electric field across the depletion region.
    - This electric field opposes further diffusion of charge carriers, establishing an equilibrium and forming a potential difference across the junction, known as the potential barrier or barrier voltage.
- **Variation of Barrier Width with Applied Voltage:**
    - **Forward-biased condition:**
        - When a positive voltage is applied to the p-side and a negative voltage to the n-side, the PN junction is forward-biased.
        - The applied voltage opposes the built-in potential barrier.

        - This reduces the effective potential barrier, allowing more majority carriers to cross the junction.
        - Consequently, the width of the depletion region decreases.
    - **Reverse-biased condition:**
        - When a negative voltage is applied to the p-side and a positive voltage to the n-side, the PN junction is reverse-biased.
        - The applied voltage adds to the built-in potential barrier.
        - This increases the effective potential barrier, making it more difficult for majority carriers to cross the junction.
        - Consequently, the width of the depletion region increases.

2. (b) Sketch the output of the given circuit in Fig. 1 with suitable explanations.

- As the circuit diagram for Fig. 1 is not provided, a sketch of the output and explanation cannot be given.

3. (c) Define current amplification factor β for common emitter transistor configuration. Establish a relation between α and β.

- **Current amplification factor β (Beta) for common emitter transistor configuration:**
    - The current amplification factor β (also known as h_{fe}) in a common emitter (CE) configuration is defined as the ratio of the change in collector current (ΔI_C) to the change in base current (ΔI_B), while the collector-emitter voltage (V_{CE}) is kept constant.
    - Mathematically, $\beta = \frac{\Delta I_C}{\Delta I_B}|_{V_{CE}=\text{constant}}$
- **Relation between α and β:**

- We know that in a transistor, the emitter current (I_E) is the sum of the collector current (I_C) and the base current (I_B): $I_E = I_C + I_B$
- Dividing by I_C, we get: $\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$
- We know that $\alpha = \frac{I_C}{I_E}$ (common base current gain) and $\beta = \frac{I_C}{I_B}$ (common emitter current gain).
- Therefore, $\frac{1}{\alpha} = 1 + \frac{1}{\beta}$
- Multiplying by $\alpha\beta$: $\beta = \alpha\beta + \alpha\ \beta(1 - \alpha) = \alpha\ \beta = \frac{\alpha}{1-\alpha}$
- Alternatively, we can express α in terms of β: $\frac{1}{\alpha} = \frac{\beta+1}{\beta}\ \alpha = \frac{\beta}{\beta+1}$

4. (d) Discuss the effect of bypass and coupling capacitors in a common emitter amplifier.

- **Effect of Bypass Capacitors:**
  - **Emitter Bypass Capacitor (C_E):**
    - It is connected in parallel with the emitter resistor (R_E).
    - Its primary function is to provide a low-reactance path for AC signals to bypass R_E.
    - Without C_E, the AC signal would flow through R_E, causing a voltage drop that would reduce the AC gain of the amplifier (negative feedback).
    - By bypassing R_E, C_E prevents this degeneration, thus increasing the AC voltage gain of the amplifier.
    - For DC biasing, C_E acts as an open circuit, allowing R_E to provide necessary DC bias stability.
  - **Power Supply Bypass Capacitor (C_B):**

- It is connected between the power supply line and ground.
- Its purpose is to filter out any AC ripples or noise present in the DC power supply, providing a smooth DC voltage to the amplifier.
- It also helps in preventing unwanted oscillations by providing a low impedance path to ground for high-frequency signals that might propagate through the power supply lines.

- **Effect of Coupling Capacitors:**
  - **Input Coupling Capacitor (C_{in}):**
    - It is connected between the input signal source and the base of the transistor.
    - Its main function is to block the DC component of the input signal from reaching the transistor's base, preventing any alteration of the DC bias point.
    - It allows the AC signal to pass through to the amplifier, acting as a short circuit for AC frequencies of interest.
  - **Output Coupling Capacitor (C_{out}):**
    - It is connected between the collector of the transistor and the load resistor.
    - Its main function is to block the DC component of the collector voltage from reaching the load, ensuring that the load only receives the amplified AC signal.
    - It also allows the AC output signal to pass through to the load, acting as a short circuit for AC frequencies of interest.

5. (e) A Zener diode has a nominal voltage of 5.6 V at 25°C with a temperature coefficient of -2 mV/°C. If the temperature increases to 85°C, calculate the new Zener voltage.

- Given:
    - Nominal Zener voltage (V_Z) at $T_1 = 25^\circ C = 5.6V$
    - Temperature coefficient (TC) = -2 mV/°C = -0.002 V/°C
    - New temperature (T_2) = $85^\circ C$
- Change in temperature (ΔT) = $T_2 - T_1 = 85^\circ C - 25^\circ C = 60^\circ C$
- Change in Zener voltage (ΔV_Z) = TC × ΔT
    - $\Delta V_Z = (-0.002 \text{ V/°C}) \times (60^\circ C)$
    - $\Delta V_Z = -0.12$ V
- New Zener voltage ($V_{Z,\text{new}}$) = $V_Z + \Delta V_Z$
    - $V_{Z,\text{new}} = 5.6 \text{ V} + (-0.12 \text{ V})$
    - $V_{Z,\text{new}} = 5.48$ V
- The new Zener voltage is 5.48 V.

6. (f) Calculate the frequency of oscillations in Colpitt's oscillator if C1 = C2 = 3nF, L = 200µH.

- Given:
    - $C_1 = 3$ nF $= 3 \times 10^{-9}$ F
    - $C_2 = 3$ nF $= 3 \times 10^{-9}$ F
    - $L = 200\mu$H $= 200 \times 10^{-6}$ H
- In a Colpitt's oscillator, the equivalent capacitance (C_{eq}) is given by the series combination of C_1 and C_2:

- $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$
- $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$
- Since $C_1 = C_2 = 3$ nF:
  - $C_{eq} = \frac{(3\times10^{-9})\times(3\times10^{-9})}{(3\times10^{-9})+(3\times10^{-9})}$
  - $C_{eq} = \frac{9\times10^{-18}}{6\times10^{-9}}$
  - $C_{eq} = 1.5 \times 10^{-9}$ F $= 1.5$ nF

- The frequency of oscillation (f) for a Colpitt's oscillator is given by the formula:
  - $f = \frac{1}{2\pi\sqrt{LC_{eq}}}$
  - $f = \frac{1}{2\pi\sqrt{(200\times10^{-6}\ \text{H})\times(1.5\times10^{-9}\ \text{F})}}$
  - $f = \frac{1}{2\pi\sqrt{300\times10^{-15}}}$
  - $f = \frac{1}{2\pi\sqrt{0.3\times10^{-12}}}$
  - $f = \frac{1}{2\pi\times0.5477\times10^{-6}}$
  - $f = \frac{1}{3.441\times10^{-6}}$
  - $f \approx 290.6 \times 10^3$ Hz
  - $f \approx 290.6$ kHz
- The frequency of oscillations is approximately 290.6 kHz.

2. (a) Derive the expression for ripple factor and efficiency of the Half-wave rectifier.

- **Ripple Factor (γ) for a Half-wave Rectifier:**

- The ripple factor is a measure of the effectiveness of a rectifier circuit in converting AC to DC. It is defined as the ratio of the RMS value of the AC component of the output voltage to the DC (average) component of the output voltage.
- $\gamma = \frac{V_{rms,AC}}{V_{DC}}$
- We know that $V_{rms}^2 = V_{DC}^2 + V_{rms,AC}^2$
- So, $V_{rms,AC} = \sqrt{V_{rms}^2 - V_{DC}^2}$
- Therefore, $\gamma = \frac{\sqrt{V_{rms}^2 - V_{DC}^2}}{V_{DC}} = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$
- For a half-wave rectifier, assuming an ideal diode:
  - Peak output voltage V_m (where V_m is the peak of the input AC voltage).
  - DC output voltage (V_{DC}) = $\frac{V_m}{\pi}$
  - RMS output voltage (V_{rms}) = $\frac{V_m}{2}$
- Substitute these values into the ripple factor formula:
  - $\gamma = \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1}$
  - $\gamma = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$
  - $\gamma = \sqrt{(1.57)^2 - 1}$
  - $\gamma = \sqrt{2.4649 - 1}$
  - $\gamma = \sqrt{1.4649}$
  - $\gamma \approx 1.21$ or 121%

- The ripple factor for a half-wave rectifier is approximately 1.21.

- **Efficiency (η) for a Half-wave Rectifier:**
  - Efficiency is defined as the ratio of the DC output power to the AC input power.
  - $\eta = \frac{P_{DC}}{P_{AC}} \times 100\%$
  - $P_{DC} = V_{DC} I_{DC} = I_{DC}^2 R_L = \frac{V_{DC}^2}{R_L}$
  - $P_{AC} = V_{rms} I_{rms} = I_{rms}^2 (R_L + R_f)$ (where R_f is the forward resistance of the diode)
  - For an ideal diode, $R_f = 0$. So, $P_{AC} = I_{rms}^2 R_L = \frac{V_{rms}^2}{R_L}$
  - We know that $V_{DC} = \frac{V_m}{\pi}$ and $V_{rms} = \frac{V_m}{2}$.
  - $I_{DC} = \frac{V_{DC}}{R_L} = \frac{V_m}{\pi R_L}$
  - $I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{2R_L}$
  - $P_{DC} = (\frac{V_m}{\pi R_L})^2 R_L = \frac{V_m^2}{\pi^2 R_L}$
  - $P_{AC} = (\frac{V_m}{2R_L})^2 R_L = \frac{V_m^2}{4R_L}$
  - $\eta = \frac{V_m^2/(\pi^2 R_L)}{V_m^2/(4R_L)} = \frac{4}{\pi^2}$
  - $\eta = \frac{4}{(3.14159)^2} = \frac{4}{9.8696} \approx 0.406$
  - $\eta = 0.406 \times 100\% = 40.6\%$
  - The maximum efficiency of a half-wave rectifier is 40.6%.

3. (b) Draw the output waveform for the clamper circuit in Fig. 2 with a suitable explanation.

- As the circuit diagram for Fig. 2 is not provided, a sketch of the output waveform and explanation cannot be given.

4. (c) A full-wave rectifier circuit has an input AC voltage of 12 V (RMS) and a load resistance (R_L) of 1 kΩ. Calculate: (i) The DC output voltage (V_{DC}). (ii) The ripple factor (r). (iii) The efficiency (η) of the rectifier.

- Given:
    - Input AC voltage (RMS) = $V_{in,rms} = 12$ V
    - Load resistance (R_L) = 1 kΩ $= 1000\Omega$
- First, calculate the peak input voltage (V_m):
    - $V_m = V_{in,rms} \times \sqrt{2} = 12 \text{ V} \times \sqrt{2} \approx 12 \times 1.414 = 16.97 \text{ V}$
- **(i) The DC output voltage (V_{DC}):**
    - For a full-wave rectifier (ideal), the DC output voltage is given by:
        - $V_{DC} = \frac{2V_m}{\pi}$
        - $V_{DC} = \frac{2 \times 16.97 \text{ V}}{\pi} = \frac{33.94}{\pi} \text{ V} \approx 10.8 \text{ V}$
- **(ii) The ripple factor (r):**
    - For an ideal full-wave rectifier, the theoretical ripple factor is approximately 0.482.
    - Using the formula $r = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$
    - For a full-wave rectifier, $V_{rms} = \frac{V_m}{\sqrt{2}} = 12$ V (this is the RMS value of the output, which is generally not used for the formula here, instead, the RMS value of the rectified waveform is used, which for a full-wave rectifier is $\frac{V_m}{\sqrt{2}}$ as input RMS if ideal output).

- Let's use the standard values derived for a full-wave rectifier for ideal diodes:
  - $V_{DC} = \frac{2V_m}{\pi}$
  - $V_{rms} = \frac{V_m}{\sqrt{2}}$ (This is for the AC input. For the rectified output, the RMS value is also $\frac{V_m}{\sqrt{2}}$ assuming ideal full-wave rectification).
  - Let's re-evaluate. The RMS value of the rectified output voltage of a full-wave rectifier is $V_{orms} = \frac{V_m}{\sqrt{2}}$.
  - So, $r = \sqrt{\left(\frac{V_{orms}}{V_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1}$
  - $r = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = \sqrt{\left(\frac{3.14159}{2\times 1.414}\right)^2 - 1}$
  - $r = \sqrt{\left(\frac{3.14159}{2.828}\right)^2 - 1} = \sqrt{(1.111)^2 - 1}$
  - $r = \sqrt{1.234 - 1} = \sqrt{0.234} \approx 0.4837$
- The ripple factor for the full-wave rectifier is approximately 0.484.

- **(iii) The efficiency (η) of the rectifier:**
  - For an ideal full-wave rectifier, the theoretical maximum efficiency is 81.2%.
  - $\eta = \frac{P_{DC}}{P_{AC}} \times 100\%$
  - $P_{DC} = V_{DC} I_{DC} = V_{DC}^2 / R_L = (10.8\ \text{V})^2 / 1000\Omega = 116.64/1000 = 0.11664\ \text{W}$
  - $P_{AC} = V_{orms}^2 / R_L = (12\ \text{V})^2 / 1000\Omega = 144/1000 = 0.144\ \text{W}$

- $\eta = \frac{0.11664\ \text{W}}{0.144\ \text{W}} \times 100\% \approx 81\%$
- The efficiency of the full-wave rectifier is approximately 81%.

3. (a) Draw and explain the input and output characteristics curve for the transistor in common emitter configuration.

- **Input Characteristics Curve (Common Emitter Configuration):**
  - **Drawing:**
    - Plot I_B (Base Current) on the y-axis against V_{BE} (Base-Emitter Voltage) on the x-axis.
    - A family of curves will be obtained for different constant values of V_{CE} (Collector-Emitter Voltage).
  - **Explanation:**
    - The input characteristic curve of a CE configuration is similar to the forward characteristics of a diode.
    - Initially, for small values of V_{BE}, the base current I_B is very small. This is due to the potential barrier of the base-emitter junction.
    - As V_{BE} increases and crosses the cut-in voltage (approximately 0.7 V for silicon transistors), the base current I_B starts to increase rapidly.
    - The curves shift slightly to the right with increasing V_{CE}. This is because as V_{CE} increases, the depletion region width at the collector-base junction increases, causing the effective base width to decrease (Early effect). This, in turn, slightly reduces the potential barrier for a given V_{BE}, leading to a small increase in I_B. However, this effect is often negligible for practical purposes, and the curves are often shown close to each other.

- **Output Characteristics Curve (Common Emitter Configuration):**
    - **Drawing:**
        - Plot I_C (Collector Current) on the y-axis against V_{CE} (Collector-Emitter Voltage) on the x-axis.
        - A family of curves will be obtained for different constant values of I_B (Base Current).
    - **Explanation:**
        - The output characteristics are divided into three main regions:
            - **Active Region:** This is the most important region for amplifier operation. In this region, the collector-base junction is reverse-biased, and the base-emitter junction is forward-biased. The collector current I_C is approximately proportional to the base current I_B and is relatively independent of V_{CE}. The curves are nearly horizontal and evenly spaced for equal increments of I_B. This region is where the transistor acts as an amplifier.
            - **Saturation Region:** In this region, both the base-emitter and collector-base junctions are forward-biased. V_{CE} is very small (typically less than 0.2 V for silicon), and I_C is limited by the external circuit. The transistor acts like a closed switch. Small changes in V_{CE} cause significant changes in I_C. The curves crowd together in this region.
            - **Cut-off Region:** In this region, both the base-emitter and collector-base junctions are reverse-biased. The base current I_B is zero or very small. The collector current I_C is also very small, typically equal to the reverse leakage current (I_{CEO}). The

transistor acts like an open switch. The region below $I_B = 0$ is the cut-off region.

4. (b) Draw the Hybrid-π model of BJT in a common base configuration and explain the significance of each parameter.

- As per the user's instructions, I will not draw diagrams. However, I can explain the parameters of the Hybrid-π model for a BJT in common base configuration.

- **Hybrid-π Model of BJT (Common Base Configuration) - Parameters and Significance:**

    - The Hybrid-π model is a high-frequency equivalent circuit for a BJT, useful for analyzing its AC performance, especially at higher frequencies. For the common base configuration, the model is based on small-signal parameters.

    - r_e **(Emitter resistance or dynamic resistance of the emitter-base junction):**

        - Significance: Represents the dynamic resistance of the forward-biased emitter-base junction. It is a key parameter influencing the input impedance and voltage gain of the amplifier. It decreases with increasing emitter current.

    - $r_{b'}$ **(Base spreading resistance):**

        - Significance: Represents the ohmic resistance of the base region between the base terminal and the active region under the emitter. It accounts for the voltage drop across the base region.

    - $r_{c'}$ **(Collector resistance or output resistance):**

        - Significance: Represents the resistance of the collector region. It is typically very large, indicating that the

collector current is relatively independent of the collector-base voltage in the active region.

- C_{eb} **or** C_{π} **(Base-Emitter diffusion capacitance):**
  - Significance: This capacitance models the charge storage effects in the forward-biased emitter-base junction due to the diffusion of minority carriers. It is dominant at higher frequencies and influences the upper cut-off frequency of the amplifier.
- C_{cb} **or** C_{μ} **(Collector-Base transition capacitance or depletion capacitance):**
  - Significance: This capacitance models the charge storage effects in the reverse-biased collector-base junction. It is due to the depletion region and is generally smaller than C_{eb}. It plays a significant role in the Miller effect, affecting the input capacitance and high-frequency performance.
- $g_m V_{eb}$ **(Transconductance dependent current source):**
  - Significance: This represents the voltage-controlled current source that models the transistor's amplifying action. g_m is the transconductance, defined as the change in collector current with respect to the change in emitter-base voltage (at constant collector-base voltage). It shows how the input voltage across the emitter-base junction controls the output current. $g_m = \frac{I_C}{V_T}$, where V_T is the thermal voltage.
- r_o **(Output resistance due to Early effect):**
  - Significance: Represents the finite output resistance due to the Early effect (base-width modulation). As V_{CB} increases, the effective base width decreases, leading to a slight increase in collector current. This slope in the output characteristics is modeled by r_o. It is typically large.

5. (c) The reverse leakage current of the transistor when connected in the CB configuration is 0.2 mA and it is 18μA when the same transistor is connected in the CE configuration. Determine α_{dc} & β_{dc} of the transistor. Assume $I_B = 30mA$.

- Given:
    - Reverse leakage current in CB configuration, $I_{CBO} = 0.2$ mA $= 0.2 \times 10^{-3}$ A
    - Reverse leakage current in CE configuration, $I_{CEO} = 18\mu$A $= 18 \times 10^{-6}$ A
    - Base current, $I_B = 30$ mA $= 30 \times 10^{-3}$ A
- We know the relation between I_{CEO} and I_{CBO}:
    - $I_{CEO} = (\beta_{dc} + 1)I_{CBO}$
    - We can find β_{dc} from this relation:
        - $\beta_{dc} + 1 = \frac{I_{CEO}}{I_{CBO}}$
        - $\beta_{dc} + 1 = \frac{18\times10^{-6}\text{ A}}{0.2\times10^{-3}\text{ A}} = \frac{18\times10^{-6}}{200\times10^{-6}} = \frac{18}{200} = 0.09$
        - This result for $\beta_{dc} + 1$ is less than 1, which implies β_{dc} is negative, which is incorrect for a typical transistor.
        - **Rechecking the given values:** It is highly probable that the values for leakage currents are swapped or there is a misunderstanding of the typical values. I_{CEO} is usually much larger than I_{CBO} because $I_{CEO} = (\beta + 1)I_{CBO}$.
        - Assuming the values are correctly given and there might be an unusual scenario or a typo in the question's values. If I_{CEO} is significantly smaller than I_{CBO}, then the initial premise of the formula connecting them needs to be re-evaluated, or the values are non-typical.

    - However, proceeding with the provided numbers:
    - $\beta_{dc} + 1 = 0.09 \Longrightarrow \beta_{dc} = 0.09 - 1 = -0.91$. This is not a practical value for β_{dc}.

- **Let's assume there was a typo and $I_{CBO} = 18\mu A$ and $I_{CEO} = 0.2mA$ (which is more typical values):**
    - $I_{CBO} = 18\mu\text{A} = 18 \times 10^{-6}$ A
    - $I_{CEO} = 0.2$ mA $= 200 \times 10^{-6}$ A
    - $\beta_{dc} + 1 = \frac{I_{CEO}}{I_{CBO}} = \frac{200\times10^{-6}\text{ A}}{18\times10^{-6}\text{ A}} = \frac{200}{18} \approx 11.11$
    - $\beta_{dc} = 11.11 - 1 = 10.11$
- Now, calculate α_{dc} using the relation $\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc}+1}$:
    - $\alpha_{dc} = \frac{10.11}{10.11+1} = \frac{10.11}{11.11} \approx 0.91$
- **If we strictly use the given values as written in the question, even if they are atypical:**
    - Given $I_{CBO} = 0.2$ mA and $I_{CEO} = 18\mu$A. This implies $I_{CEO} < I_{CBO}$. This is fundamentally impossible for a transistor as $I_{CEO} = (\beta + 1)I_{CBO}$ and β is a positive quantity.
    - Therefore, there must be a typo in the problem statement regarding the values of I_{CBO} and I_{CEO}.
- **If the question implies that the value of I_B is for another calculation not directly related to finding α_{dc} and β_{dc} from leakage currents, and we are simply asked to determine α_{dc} and β_{dc} given a collector current and base current. However, only I_B is given, not I_C or I_E.**
- **Conclusion based on given leakage currents:** With the given values ($I_{CBO} = 0.2$ mA and $I_{CEO} = 18\mu$A), it is not possible to

determine a meaningful positive β_{dc} or α_{dc} using the standard relation $I_{CEO} = (\beta_{dc} + 1)I_{CBO}$. This suggests an error in the problem statement's given values.

- **Assuming a common convention, let's consider the current amplification factors directly.**
    - If we were given I_C and I_B, we could calculate $\beta_{dc} = I_C/I_B$.
    - If we were given I_C and I_E, we could calculate $\alpha_{dc} = I_C/I_E$.
    - Since I_B is given as 30 mA, it is highly likely that a corresponding I_C value is implicitly expected or missing to calculate β_{dc} directly.
    - **Without an I_C or I_E value, and with inconsistent leakage currents, a definitive answer for α_{dc} and β_{dc} cannot be obtained from the provided information.**
- **Assuming the intent was to find α_{dc} and β_{dc} if I_{CBO} was $18\mu A$ and I_{CEO} was $0.2mA$ (more typical):**
    - $\beta_{dc} \approx 10.11$
    - $\alpha_{dc} \approx 0.91$

4. (a) Explain the selection of the Q point for a transistor bias circuit and discuss the limitations on the output voltage swing.

- **Selection of the Q-point (Quiescent Point):**
    - The Q-point, also known as the operating point, is the DC bias point of a transistor. It represents the collector current (I_C) and collector-emitter voltage (V_{CE}) of the transistor when no AC signal is applied.
    - **Purpose:** The Q-point is chosen to ensure that the transistor operates in the active region for the entire range of the input AC signal. This allows for faithful amplification without distortion.

- **Factors influencing selection:**
    - **Minimizing Distortion:** The Q-point should be chosen near the center of the load line in the active region. This allows for maximum peak-to-peak swing of the output voltage and current without entering the saturation or cut-off regions, which would cause clipping and distortion.
    - **Transistor Characteristics:** The specific characteristics of the transistor (e.g., maximum power dissipation, maximum I_C, maximum V_{CE}) must be considered to prevent damage and ensure reliable operation. The Q-point should be well within the safe operating area (SOA).
    - **Temperature Stability:** The biasing circuit should be designed such that the Q-point is stable against variations in temperature and transistor parameters (like β). This is achieved through proper selection of biasing resistors (e.g., using voltage divider bias).
    - **Power Dissipation:** The power dissipated by the transistor at the Q-point ($P_D = V_{CEQ} \times I_{CQ}$) should be less than the maximum power dissipation rating of the transistor.
    - **Voltage Gain Requirement:** The chosen Q-point affects the transconductance (g_m) of the transistor, which in turn influences the voltage gain of the amplifier.
    - **Input Impedance:** The Q-point also influences the input impedance of the amplifier.

- **Limitations on the Output Voltage Swing:**
    - The maximum possible peak-to-peak output voltage swing of a common emitter amplifier is limited by the boundaries of the active region, specifically the cut-off and saturation regions.
    - **Saturation Limitation:**

- When the instantaneous collector-emitter voltage V_{CE} drops to its saturation value ($V_{CE,sat}$), which is typically very small (e.g., 0.1 V to 0.3 V for silicon), the transistor enters the saturation region.
- At this point, the collector current reaches its maximum possible value, limited by the load line and $V_{CE,sat}$.
- Any further increase in input signal that would attempt to decrease V_{CE} below $V_{CE,sat}$ will result in the output voltage being clipped at $V_{CE,sat}$.

- **Cut-off Limitation:**
  - When the instantaneous collector current I_C drops to near zero (or I_{CEO}), the transistor enters the cut-off region.
  - At this point, the collector-emitter voltage reaches its maximum possible value, which is approximately equal to the supply voltage V_{CC} (assuming the load resistance drops negligible voltage due to leakage current).
  - Any further decrease in input signal that would attempt to reduce I_C below zero will result in the output voltage being clipped at V_{CC}.
- **Optimal Swing:** For undistorted output, the Q-point should be chosen such that the positive and negative swings of the output voltage are symmetrical, avoiding both saturation and cut-off clipping. Ideally, the Q-point (V_{CEQ}) should be midway between $V_{CE,sat}$ and V_{CC}.

5. (b) Find the operating point and draw the load line of a fixed bias circuit using an NPN transistor for β=300, V_{cc}=15 V, R_b=200 KΩ, and R_c=1 KΩ.

- Given:
  - $\beta = 300$

- $V_{CC} = 15$ V
- $R_b = 200\ \text{k}\Omega = 200 \times 10^3 \Omega$
- $R_c = 1\ \text{k}\Omega = 1 \times 10^3 \Omega$
- Assume $V_{BE} = 0.7$ V for an NPN silicon transistor.

- **Operating Point (Q-point) Calculation:**
  - **1. Calculate Base Current (I_B):**
    - For a fixed bias circuit, $I_B = \frac{V_{CC} - V_{BE}}{R_b}$
    - $I_B = \frac{15\ \text{V} - 0.7\ \text{V}}{200 \times 10^3 \Omega} = \frac{14.3\ \text{V}}{200 \times 10^3 \Omega}$
    - $I_B = 0.0715 \times 10^{-3}\ \text{A} = 0.0715\ \text{mA}$
  - **2. Calculate Collector Current (I_C):**
    - $I_C = \beta I_B$
    - $I_C = 300 \times 0.0715\ \text{mA}$
    - $I_C = 21.45\ \text{mA}$
  - **3. Calculate Collector-Emitter Voltage (V_{CE}):**
    - $V_{CE} = V_{CC} - I_C R_c$
    - $V_{CE} = 15\ \text{V} - (21.45 \times 10^{-3}\ \text{A}) \times (1 \times 10^3 \Omega)$
    - $V_{CE} = 15\ \text{V} - 21.45\ \text{V}$
    - $V_{CE} = -6.45\ \text{V}$
  - **Analysis of Result:** A negative V_{CE} indicates that the transistor is heavily driven into saturation, and the assumptions for the active region (like $V_{CE} = V_{CC} - I_C R_C$) are no longer valid. In saturation, V_{CE} would be approximately $V_{CE,sat}$ (around 0.2V). This means the chosen R_b is too small for the given β and R_c,

causing too much base current, pushing the transistor deep into saturation.

- Therefore, the operating point (I_C, V_{CE}) would be in the saturation region.
- In saturation, $V_{CE} \approx V_{CE,sat}$ (typically 0.2V).
- Then, I_C would be approximately $\frac{V_{CC}-V_{CE,sat}}{R_C} = \frac{15-0.2}{1\text{k}\Omega} = \frac{14.8}{1\text{k}\Omega} = 14.8$ mA.
- So, the calculated Q-point ($I_C = 21.45$ mA, $V_{CE} = -6.45$ V) is not physically achievable in the active region. The transistor is saturated. The actual Q-point would be approximately $(14.8\text{ mA}, 0.2\text{ V})$.

- **Load Line Drawing:**
  - The DC load line is a straight line drawn on the output characteristics (I_C vs. V_{CE}) of the transistor. It represents all possible DC operating points of the transistor for a given circuit.
  - **X-intercept (Cut-off point):** When $I_C = 0$, $V_{CE} = V_{CC}$.
    - $V_{CE,\text{cut-off}} = 15$ V
    - Point: $(15\text{ V}, 0\text{ mA})$
  - **Y-intercept (Saturation point):** When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_c}$.
    - $I_{C,\text{saturation}} = \frac{15\text{ V}}{1\text{ k}\Omega} = 15$ mA
    - Point: $(0\text{ V}, 15\text{ mA})$
  - **Plotting the Load Line:** Draw a straight line connecting the two points $(15\text{ V}, 0\text{ mA})$ and $(0\text{ V}, 15\text{ mA})$ on the $V_{CE} - I_C$ graph.
  - **Plotting the Q-point:** Based on our calculation, the calculated Q-point $(21.45\text{ mA}, -6.45\text{ V})$ falls outside the load line. The

actual operating point will be at the intersection of the load line and the I_B curve corresponding to 0.0715 mA. Since $I_{C,saturation}$ is 15 mA, and our calculated I_C (based on βI_B) is 21.45 mA, this confirms the transistor is operating in saturation. The actual Q-point will be approximately at $(0.2$ V$, 14.8$ mA$)$ on the load line, very close to the Y-intercept.

6. (c) For the CE two port hybrid circuit, determine the voltage gain, input impedance, and output impedance, given $h_{ie} = 1100\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25\mu S$.

- Given h-parameters for CE configuration:
    - $h_{ie} = 1100\Omega$ (Input impedance with output shorted)
    - $h_{re} = 2.5 \times 10^{-4}$ (Reverse voltage ratio with input open)
    - $h_{fe} = 50$ (Forward current transfer ratio with output shorted, i.e., β_{ac})
    - $h_{oe} = 25\mu S = 25 \times 10^{-6}$ S (Output admittance with input open)
- To determine the voltage gain, input impedance, and output impedance, we usually need the source resistance (R_s) and load resistance (R_L). Since they are not given, we will determine the intrinsic (ideal) values without considering external resistors, or provide formulas based on R_L.
- **Assuming no external source resistance (ideal voltage source at input) and considering a load resistance R_L (which is typically external to the h-parameter model).**
- **1. Voltage Gain (A_V):**
    - The voltage gain for a CE amplifier with a load resistor R_L is given by:
        - $A_V = \frac{-h_{fe}R_L}{h_{ie}+(h_{ie}h_{oe}-h_{fe}h_{re})R_L}$

- If R_L is not specified, we can't get a numerical value.
- However, if we are asked for the open-circuit voltage gain ($R_L \to \infty$), the formula simplifies, but usually, a practical R_L is implied.
- Often, for simplicity, if h_{re} and h_{oe} are small, $A_V \approx \frac{-h_{fe}R_L}{h_{ie}}$.
- Let's assume a typical R_L for a small signal amplifier, say $R_L = 5\ \text{k}\Omega = 5000\Omega$. (This is an assumption for calculation purposes as R_L is missing).
  - $h_{ie}h_{oe} = 1100 \times 25 \times 10^{-6} = 0.0275$
  - $h_{fe}h_{re} = 50 \times 2.5 \times 10^{-4} = 0.0125$
  - $h_{ie}h_{oe} - h_{fe}h_{re} = 0.0275 - 0.0125 = 0.015$
  - $A_V = \frac{-50\times5000}{1100+(0.015)\times5000} = \frac{-250000}{1100+75} = \frac{-250000}{1175} \approx -212.77$
- If the question implies the voltage gain of the transistor itself without external load (which is less common for "voltage gain"), then the output is typically considered to be across h_{oe} or $1/h_{oe}$. However, voltage gain requires an output voltage, which means a current flowing through some resistance.

- **2. Input Impedance (Z_{in}):**
  - The input impedance for a CE amplifier with a load resistor R_L is given by:
    - $Z_{in} = h_{ie} - \frac{h_{re}h_{fe}}{h_{oe}+\frac{1}{R_L}}$
    - This can be rewritten as: $Z_{in} = h_{ie} - \frac{h_{re}h_{fe}R_L}{1+h_{oe}R_L}$
  - Using the assumed $R_L = 5\ \text{k}\Omega$:
    - $Z_{in} = 1100 - \frac{2.5\times10^{-4}\times50\times5000}{1+25\times10^{-6}\times5000}$

- $Z_{in} = 1100 - \frac{62.5}{1+0.125} = 1100 - \frac{62.5}{1.125}$
- $Z_{in} = 1100 - 55.56 \approx 1044.44\Omega$

- If R_L is not given and ideal conditions are assumed (e.g., $R_L \to \infty$ or $h_{re} = 0, h_{oe} = 0$), then $Z_{in} \approx h_{ie}$. In this case, $Z_{in} = 1100\Omega$.

- **3. Output Impedance (Z_{out}):**
  - The output impedance for a CE amplifier with a source resistance R_s is given by:
    - $Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}+R_s}}$
  - If R_s is not specified, we can't get a numerical value.
  - Often, if R_s is very small (ideal voltage source), $Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}}} = \frac{1}{25\times10^{-6} - \frac{50\times2.5\times10^{-4}}{1100}}$
    - $Z_{out} = \frac{1}{25\times10^{-6} - \frac{0.0125}{1100}} = \frac{1}{25\times10^{-6} - 11.36\times10^{-6}}$
    - $Z_{out} = \frac{1}{13.64\times10^{-6}} \approx 73313\Omega \approx 73.3\ \text{k}\Omega$
  - If the question implies the output impedance of the transistor itself without external source resistance, and $h_{re} = 0$, then $Z_{out} \approx 1/h_{oe}$. In this case, $Z_{out} = 1/(25 \times 10^{-6}\ \text{S}) = 40000\Omega = 40\ \text{k}\Omega$.

- **Summary (with assumption $R_L = 5\ \text{k}\Omega$ and $R_s = 0$ for numerical results):**
  - Voltage Gain (A_V) ≈ -212.77
  - Input Impedance (Z_{in}) $\approx 1044.44\Omega$
  - Output Impedance (Z_{out}) $\approx 73.3\ \text{k}\Omega$

- **Without R_L and R_s, the answers would be expressions:**
  - $A_V = \frac{-h_{fe}R_L}{h_{ie}+(h_{ie}h_{oe}-h_{fe}h_{re})R_L}$
  - $Z_{in} = h_{ie} - \frac{h_{re}h_{fe}R_L}{1+h_{oe}R_L}$
  - $Z_{out} = \frac{1}{h_{oe}-\frac{h_{fe}h_{re}}{h_{ie}+R_S}}$

5. (a) Evaluate the effect of negative feedback on input and output impedances of voltage series feedback amplifiers.

- **Effect of Negative Feedback on Voltage Series Feedback Amplifiers:**
  - In voltage series feedback, a fraction of the output voltage is sampled and fed back in series with the input voltage. This type of feedback is characterized by:
    - **Sampling:** Voltage (output is in parallel with the sampling network).
    - **Mixing:** Series (feedback signal is in series with the input signal).

- **Effect on Input Impedance (Z_{inF}):**
  - Negative series feedback increases the input impedance of the amplifier.
  - **Explanation:** When the feedback voltage (V_f) is in series with the input signal (V_s), the effective input voltage ($V_i = V_s - V_f$) to the amplifier stage is reduced. For a given input current, this implies that a larger overall input voltage (V_s) is required.
  - Since $Z_{inF} = \frac{V_s}{I_i}$, and V_s increases for a given I_i due to the opposing feedback voltage, the input impedance effectively increases.

- The input impedance with feedback (Z_{inF}) is given by: $Z_{inF} = Z_{in}(1 + A_v\beta)$, where Z_{in} is the input impedance without feedback, A_v is the open-loop voltage gain, and β is the feedback factor. Since $A_v\beta$ is positive for negative feedback, $Z_{inF} > Z_{in}$.

- **Effect on Output Impedance (Z_{outF}):**
  - Negative voltage feedback (regardless of series or shunt mixing at input) decreases the output impedance of the amplifier.
  - **Explanation:** When the output voltage tries to change due to a change in load or internal conditions, the feedback network senses this change. The feedback signal then modifies the input to the amplifier in such a way as to oppose this change in output voltage. This effectively makes the amplifier appear to have a lower internal resistance (output impedance) because it can maintain its output voltage more consistently despite load variations.
  - The output impedance with feedback (Z_{outF}) is given by: $Z_{outF} = \frac{Z_{out}}{1+A_v\beta}$, where Z_{out} is the output impedance without feedback, A_v is the open-loop voltage gain, and β is the feedback factor. Since $1 + A_v\beta > 1$, $Z_{outF} < Z_{out}$.

6. (b) Prove that the negative feedback in amplifiers increases the Bandwidth.

- **Proof of Bandwidth Increase with Negative Feedback:**
  - Let A_v be the open-loop gain of an amplifier and A_{vF} be the closed-loop gain with negative feedback.
  - The closed-loop gain is given by: $A_{vF} = \frac{A_v}{1+\beta A_v}$, where β is the feedback factor.

- Now, consider the frequency response. The gain of an amplifier typically falls off at high frequencies. Let the open-loop gain at any frequency f be represented by:
  - $A_v(f) = \frac{A_{v0}}{1+j(f/f_H)}$ (for a single-pole low-pass response, where A_{v0} is the mid-band gain and f_H is the upper 3dB cut-off frequency).
- Substitute this into the closed-loop gain formula:
  - $A_{vF}(f) = \frac{\frac{A_{v0}}{1+j(f/f_H)}}{1+\beta\frac{A_{v0}}{1+j(f/f_H)}}$
  - $A_{vF}(f) = \frac{A_{v0}}{1+j(f/f_H)+\beta A_{v0}}$
  - $A_{vF}(f) = \frac{A_{v0}}{(1+\beta A_{v0})+j(f/f_H)}$
  - $A_{vF}(f) = \frac{\frac{A_{v0}}{1+\beta A_{v0}}}{1+j\frac{f}{f_H(1+\beta A_{v0})}}$
- Let $A_{vF0} = \frac{A_{v0}}{1+\beta A_{v0}}$ be the mid-band closed-loop gain.
- Let $f_{HF} = f_H(1 + \beta A_{v0})$ be the new upper 3dB cut-off frequency with feedback.
- From the equation for $A_{vF}(f)$, it is clear that the new upper cut-off frequency f_{HF} is increased by a factor of $(1 + \beta A_{v0})$ compared to the original open-loop cut-off frequency f_H.
- Similarly, for the lower cut-off frequency (f_L), the closed-loop lower cut-off frequency f_{LF} becomes $f_{LF} = \frac{f_L}{1+\beta A_{v0}}$. This means the lower cut-off frequency is reduced.
- Since Bandwidth (BW) = $f_H - f_L$, and with feedback, $BW_F = f_{HF} - f_{LF}$.

- As f_{HF} increases and f_{LF} decreases (or f_{LF} is usually negligible for mid-band analysis), the overall bandwidth of the amplifier increases with negative feedback.
- **Conclusion:** Negative feedback effectively "trades" gain for bandwidth. While the mid-band gain is reduced by a factor of $(1 + \beta A_{v0})$, the bandwidth is increased by the same factor. This maintains the gain-bandwidth product constant ($A_{v0} f_H = A_{vF0} f_{HF}$).

7. (c) Why the LC oscillators are not suitable for low-frequency applications? In a Transistor Colpitts oscillator L = 15 μH, $C_1 = 0.001\mu F$, $C_2 = 0.01\mu F$. Find (a) operating frequency (b) Feedback fraction.

- **Why LC Oscillators are not suitable for low-frequency applications:**
  - **Large Component Size:** For very low frequencies (e.g., in the Hz or a few kHz range), the required values of inductance (L) and capacitance (C) become extremely large.
    - Large inductors are physically bulky, heavy, and expensive. They also introduce significant parasitic resistance, which can reduce the Q-factor of the tank circuit and make it difficult to sustain oscillations.
    - Large capacitors, while more manageable than large inductors, still become physically large and expensive at very low frequencies, especially if they need to be of high quality (low ESR, good stability).
  - **Practical Limitations:** It becomes impractical to build and implement stable and efficient LC oscillators for low frequencies due to these large component requirements.
  - **Alternative for Low Frequencies:** For low-frequency applications (below approximately 100 kHz), RC oscillators (like

Wien bridge or phase shift oscillators) are generally preferred because they can achieve low frequencies with reasonable-sized resistors and capacitors.

- **Colpitts Oscillator Calculations:**
  - Given:
    - $L = 15\mu\text{H} = 15 \times 10^{-6}$ H
    - $C_1 = 0.001\mu\text{F} = 0.001 \times 10^{-6}$ F $= 1 \times 10^{-9}$ F
    - $C_2 = 0.01\mu\text{F} = 0.01 \times 10^{-6}$ F $= 10 \times 10^{-9}$ F
  - **(a) Operating Frequency (f):**
    - First, calculate the equivalent capacitance (C_{eq}) for the series combination of C_1 and C_2:
      - $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} = \frac{1}{1\times10^{-9}} + \frac{1}{10\times10^{-9}}$
      - $\frac{1}{C_{eq}} = (1 \times 10^9) + (0.1 \times 10^9) = 1.1 \times 10^9$
      - $C_{eq} = \frac{1}{1.1\times10^9} = 0.909 \times 10^{-9}$ F $= 0.909$ nF
    - The frequency of oscillation (f) for a Colpitts oscillator is:
      - $f = \frac{1}{2\pi\sqrt{LC_{eq}}}$
      - $f = \frac{1}{2\pi\sqrt{(15\times10^{-6}\text{ H})\times(0.909\times10^{-9}\text{ F})}}$
      - $f = \frac{1}{2\pi\sqrt{13.635\times10^{-15}}}$
      - $f = \frac{1}{2\pi\times\sqrt{13.635}\times10^{-7.5}}$
      - $f = \frac{1}{2\pi\times3.692\times10^{-7.5}}$
      - $f = \frac{1}{2\pi\times3.692\times10^{-7.5}} = \frac{1}{2.32\times10^{-6}}$

- $f \approx 431.03 \times 10^3$ Hz $= 431.03$ kHz

- **(b) Feedback Fraction (β):**
  - In a Colpitts oscillator, the feedback fraction is given by the ratio of the voltage across C_1 to the voltage across C_2. However, typically the feedback fraction is taken as the ratio of the feedback voltage to the output voltage.
  - For a Colpitts oscillator, the feedback network consists of C_1, C_2, and L. The voltage across C_1 is fed back to the input, and the output is taken across C_2.
  - The feedback fraction is usually $\beta = \frac{C_1}{C_2}$. (This is for the common collector configuration version, or for understanding the voltage division).
  - More generally, the feedback factor in Colpitts is often considered as C_1/C_2 (ratio of reactive components that determine the feedback voltage).
  - $\beta = \frac{C_1}{C_2} = \frac{1\times10^{-9}\ \text{F}}{10\times10^{-9}\ \text{F}} = \frac{1}{10} = 0.1$

- **The operating frequency is approximately 431.03 kHz.**
- **The feedback fraction is 0.1.**

6. (a) Show that the transformer coupled class A amplifier maximum efficiency is 50%.

- **Derivation of Maximum Efficiency for Transformer Coupled Class A Amplifier:**
  - **Assumptions:**
    - Ideal transformer (no losses).
    - Transistor is ideal (no $V_{CE,sat}$, no power dissipation in the transistor itself beyond the load).

- No power loss in the quiescent collector resistance of the primary winding.

- **DC Power Input (P_{DC}):**
  - The DC power drawn from the supply V_{CC} is given by:
    - $P_{DC} = V_{CC} I_{CQ}$
    - Where I_{CQ} is the quiescent collector current.
- **AC Power Output (P_{AC}):**
  - The AC power delivered to the load is given by:
    - $P_{AC} = \frac{(V_{CE,peak-to-peak}/2)^2}{2R_{L'}} = \frac{V_{CE,max}^2}{2R_{L'}}$
    - Where $R_{L'}$ is the reflected load resistance seen by the primary winding of the transformer.
    - The peak AC voltage across the primary is $V_{CE,peak} = V_{CC}$ (assuming ideal swing from V_{CC} to 0V).
    - The peak AC current is $I_{C,peak} = I_{CQ}$ (assuming ideal swing from $2I_{CQ}$ to 0A).
    - So, $P_{AC} = \frac{V_{CE,peak} I_{C,peak}}{2}$ (for sinusoidal signal).
    - In an ideal Class A amplifier, the peak AC voltage swing can be from $V_{CE,Q}$ up to V_{CC} and down to 0 V. For maximum swing, $V_{CE,Q} = V_{CC}/2$. In a transformer-coupled amplifier, the maximum peak AC voltage can be V_{CC} (swing from V_{CC} to 0V and then V_{CC} above V_{CC} not possible for output transistor). Let's use the voltage and current swing from the Q-point.

- The maximum peak AC voltage swing is $V_m = V_{CEQ}$ (voltage from Q-point to cutoff, or Q-point to saturation). For ideal case, $V_m = V_{CC}$.
- The maximum peak AC current swing is $I_m = I_{CQ}$.
- Thus, $P_{AC} = \frac{V_m I_m}{2}$. For maximum efficiency, $V_m = V_{CC}$ (peak voltage swing across primary) and $I_m = I_{CQ}$ (peak current swing through primary).
- So, $P_{AC} = \frac{V_{CC} I_{CQ}}{2}$

- **Efficiency (η):**
  - $\eta = \frac{P_{AC}}{P_{DC}} \times 100\%$
  - $\eta = \frac{V_{CC} I_{CQ}/2}{V_{CC} I_{CQ}} \times 100\%$
  - $\eta = \frac{1}{2} \times 100\%$
  - $\eta = 50\%$

- **Explanation for Maximum 50% Efficiency:**
  - In a transformer-coupled Class A amplifier, the transformer prevents DC current from flowing through the load, only coupling the AC signal. This allows the Q-point V_{CEQ} to be set at V_{CC} (or very close to it with small primary DC resistance), which maximizes the voltage swing across the primary winding.
  - For maximum undistorted output (Class A operation), the transistor must remain in the active region. This means the collector current can swing from 0 to $2I_{CQ}$, and the collector-emitter voltage can swing from 0 to $2V_{CEQ}$.
  - For maximum efficiency, the Q-point is chosen such that $V_{CEQ} = V_{CC}$. In this ideal case, the AC voltage swing can be from 0 to

$2V_{CC}$ (but the transistor can only go down to 0 and up to V_{CC} from V_{CC}, thus a peak swing of V_{CC}). The peak current swing is I_{CQ}.

- The DC power consumed is always $V_{CC}I_{CQ}$.
- The maximum AC power that can be delivered to the load is $\frac{1}{2}V_{peak}I_{peak} = \frac{1}{2}V_{CC}I_{CQ}$.
- Thus, the maximum efficiency is $\frac{P_{AC,max}}{P_{DC}} = \frac{0.5V_{CC}I_{CQ}}{V_{CC}I_{CQ}} = 0.5 = 50\%$.
- The remaining 50% of the input power is dissipated as heat in the transistor itself due to its quiescent current and voltage drop.

7. (b) Determine the range of values of V_L that will maintain the Zener diode shown in Fig. 3 in the "ON" state. Given R=220 Ω, V_z=20V, I_{zm}=60 mA and R_L=1.2kΩ.

- As the circuit diagram for Fig. 3 is not provided, I will assume a standard Zener shunt regulator circuit, which typically has an input voltage V_S (or V_{in}), a series resistor R, the Zener diode, and a parallel load resistor R_L.
- The question asks for the range of V_L that keeps the Zener in the "ON" state. For a Zener diode to be "ON" (in breakdown region), two conditions must be met:
  a. The voltage across the Zener diode must be at least V_Z.
  b. The current through the Zener diode (I_Z) must be greater than or equal to the minimum Zener current (I_{ZK}, which is not given, but usually much smaller than I_{ZM}) and less than or equal to the maximum Zener current (I_{ZM}).
- Given:
  - $R = 220\Omega$

- $V_Z = 20$ V (Nominal Zener voltage)
- $I_{ZM} = 60$ mA $= 0.06$ A (Maximum Zener current)
- $R_L = 1.2$ kΩ $= 1200\Omega$
- Let's assume the question implies the range of *input voltage* (V_{in} or V_S) that maintains the Zener in the ON state, as V_L (load voltage) is ideally fixed at V_Z when the Zener is "ON". If V_L itself varies, then the Zener is likely not fully regulating.
- However, if "range of values of V_L" implies the permissible range of Zener voltage due to tolerances or operation conditions, it is not directly calculable without more info.
- Let's interpret this as the range of *input voltage* that keeps the Zener in regulation.

- **Calculations to keep Zener in "ON" state:**
  - When the Zener is "ON", $V_L = V_Z = 20$ V.
  - Current through the load (I_L) = $\frac{V_L}{R_L} = \frac{20\text{ V}}{1200\Omega} = 0.01667$ A $=$ 16.67 mA
  - **Case 1: Minimum Input Voltage ($V_{in,min}$)**
    - The Zener diode turns "ON" when the voltage across it reaches V_Z. At this point, the current through the Zener diode is at its minimum value, I_{ZK}. If I_{ZK} is not given, we often assume a very small current, or the lower limit of Zener operation is reached when $I_Z = 0$ (just at the edge of regulation).
    - Let's consider the minimum current through the series resistor R ($I_R = I_Z + I_L$) when the Zener just begins to conduct or is at its minimum stable current.

- The minimum current through the Zener diode needed to keep it in breakdown is usually I_{ZK}. Let's assume a typical I_{ZK} is around 1 mA (often not provided, but essential for defining the lower boundary). If no I_{ZK} is given, we might consider the case where $I_Z \approx 0$.
- **Scenario A: Assuming the lower limit of Zener operation is when I_Z is very small, approaching 0.**
  - $I_R = I_L = 16.67$ mA
  - $V_{in,min} = I_R R + V_L = (0.01667\ \text{A}) \times (220\Omega) + 20\ \text{V}$
  - $V_{in,min} = 3.6674\ \text{V} + 20\ \text{V} = 23.6674\ \text{V}$
- **Scenario B: Assuming a specified minimum Zener current I_{ZK} (e.g., $I_{ZK} = 1$ mA if provided):**
  - $I_R = I_{ZK} + I_L = 1\ \text{mA} + 16.67\ \text{mA} = 17.67\ \text{mA}$
  - $V_{in,min} = (0.01767\ \text{A}) \times (220\Omega) + 20\ \text{V}$
  - $V_{in,min} = 3.8874\ \text{V} + 20\ \text{V} = 23.8874\ \text{V}$
- Without I_{ZK}, the minimum input voltage is found when the Zener voltage is V_Z and the current is just enough to maintain breakdown.

- **Case 2: Maximum Input Voltage ($V_{in,max}$)**
  - The maximum input voltage occurs when the Zener current reaches its maximum permissible value, I_{ZM}.
  - $I_Z = I_{ZM} = 60$ mA
  - $I_R = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA} = 76.67\ \text{mA}$
  - $V_{in,max} = I_R R + V_L = (0.07667\ \text{A}) \times (220\Omega) + 20\ \text{V}$
  - $V_{in,max} = 16.8674\ \text{V} + 20\ \text{V} = 36.8674\ \text{V}$

- **Range of Input Voltage:**
    - The range of input voltage (V_{in}) that will maintain the Zener diode in the "ON" state (regulating) is approximately 23.67 V to 36.87 V (assuming $I_Z \approx 0$ for min input). If I_{ZK} is provided, use that.
- **Regarding the question's phrasing "range of values of V_L":**
    - If the Zener diode is "ON" and performing its regulating function, V_L is ideally maintained constant at $V_Z = 20$ V.
    - The only way V_L would vary while the Zener is still considered "ON" or "in state of regulation" would be due to the Zener's dynamic resistance (r_z) or temperature effects. Since r_z is not given, we assume an ideal Zener for the range of V_L that is V_Z.
    - However, if "ON" implies simply forward biased or having voltage across it, then it is a different case.
    - Assuming the question means the range of *input voltage* that keeps $V_L = V_Z$, then the answer is the range calculated above for V_{in}. If it strictly means V_L, then for regulation, V_L is essentially fixed at V_Z.
- **Most common interpretation:** The question is asking for the range of input voltage (V_{in}) for which the Zener acts as a regulator.
    - Therefore, the input voltage V_{in} must be in the range of approximately 23.67 V to 36.87 V. Within this range, V_L is maintained at 20 V.

8. (c) Calculate the closed loop gain for the negative feedback amplifier when open loop gain $A_V = 100{,}000$ and $\beta = 1/100$. Also, calculate closed loop gain when A_V is increased by 50%.

- **Given:**
    - Open loop gain (A_V) = $100{,}000$

- Feedback factor (β) = $1/100 = 0.01$

- **1. Calculate Closed Loop Gain (A_{VF}) for initial A_V:**
  - The formula for closed loop gain of a negative feedback amplifier is:
    - $A_{VF} = \frac{A_V}{1+\beta A_V}$
  - $A_{VF} = \frac{100{,}000}{1+(0.01\times 100{,}000)}$
  - $A_{VF} = \frac{100{,}000}{1+1000}$
  - $A_{VF} = \frac{100{,}000}{1001} \approx 99.9$

- **2. Calculate Closed Loop Gain when A_V is increased by 50%:**
  - New open loop gain ($A_{V'}$) = $A_V + (0.50 \times A_V) = 100{,}000 + (0.50 \times 100{,}000) = 100{,}000 + 50{,}000 = 150{,}000$
  - Calculate the new closed loop gain ($A_{VF'}$) with $A_{V'} = 150{,}000$ and $\beta = 0.01$:
    - $A_{VF'} = \frac{A_{V'}}{1+\beta A_{V'}}$
    - $A_{VF'} = \frac{150{,}000}{1+(0.01\times 150{,}000)}$
    - $A_{VF'} = \frac{150{,}000}{1+1500}$
    - $A_{VF'} = \frac{150{,}000}{1501} \approx 99.93$

- **Results:**
  - Initial Closed Loop Gain ≈ 99.9
  - Closed Loop Gain when A_V is increased by 50% ≈ 99.93

- **Observation:** This demonstrates one of the key benefits of negative feedback: it makes the closed-loop gain much less sensitive to variations in the open-loop gain, as long as the loop gain (βA_V) is much greater than 1.

7. (a) Derive the expression for the frequency of oscillations of a phase shift oscillator using three RC networks.

- **Derivation of Oscillation Frequency for a Three-Stage RC Phase Shift Oscillator:**
    - **Circuit Overview:** A typical RC phase shift oscillator consists of an amplifier (usually a BJT in common emitter or an Op-Amp) and a feedback network made of three identical RC stages. Each RC stage provides a phase shift, and the total phase shift provided by the three stages at the oscillation frequency is $180°$. The amplifier typically provides the other $180°$ phase shift (for common emitter BJT) to meet Barkhausen's criterion for sustained oscillations ($A_v\beta = 1$ and total phase shift $= 360°$ or $0°$).
    - **Assumptions:**
        - The amplifier has very high input impedance and very low output impedance, so it doesn't load the RC network.
        - The RC stages are identical (each with resistance R and capacitance C).
    - **Analysis of a Single RC Stage:**
        - Consider one RC stage (R in series, C in parallel to ground). The phase shift ϕ introduced by a single RC lead network is $\phi = \arctan(\omega RC)$.
        - For three identical stages, the total phase shift is $3\phi = 3\arctan(\omega RC)$.

- For oscillation, the phase shift provided by the feedback network must be 180° (π radians).
- $3\arctan(\omega RC) = 180^\circ$
- $\arctan(\omega RC) = 60^\circ$
- $\omega RC = \tan(60^\circ) = \sqrt{3}$
- $\omega = \frac{\sqrt{3}}{RC}$
- Since $\omega = 2\pi f$,
- $f = \frac{\sqrt{3}}{2\pi RC}$

- **More Rigorous Derivation (considering loading effects and gain requirement):**
  - When a more accurate analysis is performed, considering the loading of each RC section on the previous one, and the amplifier's input impedance, the phase shift condition for sustained oscillation with exactly 180° phase shift from the RC network (and 180° from amplifier) is achieved when:
  - $\omega = \frac{1}{\sqrt{6}RC}$
  - Therefore, the frequency of oscillation (f) is:
    - $f = \frac{1}{2\pi\sqrt{6}RC}$
  - And for sustained oscillations, the amplifier's voltage gain (A_v) must compensate for the attenuation of the feedback network. The attenuation factor ($\frac{V_f}{V_{out}}$) for a three-stage RC network is typically $\frac{1}{29}$ when each stage loads the previous one.

    - Thus, the minimum gain required from the amplifier for sustained oscillation is $A_v \geq 29$.

- **Summary of Frequency Expression:**
    - The expression for the frequency of oscillations of a phase shift oscillator using three RC networks is:
        - $f = \frac{1}{2\pi\sqrt{6}RC}$
    - Where R is the resistance and C is the capacitance of each identical RC stage.

8. (b) Draw the block diagram of the regulated power supply and explain significance of C filter.

- As per the user's instructions, I will not draw diagrams.
- **Block Diagram of a Regulated Power Supply (Explanation):**
    - A regulated power supply typically consists of the following functional blocks:
        i. **Transformer:** Takes the AC mains voltage and steps it down to a lower, more manageable AC voltage suitable for the electronic circuit. It also provides electrical isolation.
        ii. **Rectifier:** Converts the stepped-down AC voltage into a pulsating DC voltage. Common types include half-wave, full-wave (center-tapped), and bridge rectifiers.
        iii. **Filter (Capacitor Filter):** Smooths out the pulsating DC voltage from the rectifier into a relatively smooth, but still rippled, DC voltage.
        iv. **Voltage Regulator:** Takes the unregulated (rippled) DC voltage from the filter and produces a stable, constant DC output voltage, regardless of variations in the input voltage or load current.

v. **Load:** The electronic circuit or device that receives power from the regulated power supply.

- **Significance of the Capacitor Filter (C Filter):**
  - The capacitor filter (typically a large electrolytic capacitor) is connected in parallel with the output of the rectifier. Its significance lies in its ability to smooth the pulsating DC voltage from the rectifier.
  - **How it Works:**
    - During the positive half-cycle (or both half-cycles for full-wave rectification) when the rectifier output voltage rises, the capacitor charges up to the peak value of the rectified voltage.
    - When the rectifier output voltage starts to fall (after reaching its peak and moving towards zero), the capacitor, being charged, begins to discharge through the load resistance.
    - Since the capacitor discharges relatively slowly compared to the rate at which the rectified voltage drops, it maintains a nearly constant voltage across the load, thus smoothing out the pulsations.
    - When the rectifier output voltage again rises and exceeds the capacitor voltage, the diode conducts, and the capacitor recharges.
  - **Benefits:**
    - **Reduces Ripple:** The most significant effect is the reduction of the AC ripple component in the rectified output. A larger capacitance generally results in less ripple.

- **Provides a Smoother DC Voltage:** By reducing ripple, the filter produces a DC voltage that is much closer to a pure DC level, which is essential for the proper operation of sensitive electronic circuits.
- **Improves Regulator Performance:** A smoother DC input to the voltage regulator allows the regulator to operate more efficiently and effectively, as it has to deal with smaller input variations. Without a filter, the regulator would have to dissipate more power and might struggle to maintain a stable output.
- **Acts as an Energy Storage Element:** The capacitor stores energy during the peaks of the rectified voltage and releases it during the valleys, effectively bridging the gaps between the rectified voltage pulses.

9. (c) For a phase shift oscillator, the feedback network uses R=6 KΩ and C=1500 pF. The transistorized amplifier used has a collector resistance of 18 KΩ. Calculate the frequency of oscillation and minimum value of h_{fe} of the transistor.

- **Given for Phase Shift Oscillator:**
  - $R = 6\ \text{k}\Omega = 6 \times 10^3 \Omega$
  - $C = 1500\ \text{pF} = 1500 \times 10^{-12}\ \text{F} = 1.5 \times 10^{-9}\ \text{F}$
  - Collector resistance $R_C = 18\ \text{k}\Omega = 18 \times 10^3 \Omega$
- **1. Calculate the Frequency of Oscillation (f):**
  - For a three-stage RC phase shift oscillator, the frequency of oscillation is given by:
    - $f = \frac{1}{2\pi\sqrt{6}RC}$
  - $f = \frac{1}{2\pi\sqrt{6}\times(6\times10^3\Omega)\times(1.5\times10^{-9}\ \text{F})}$

- $f = \frac{1}{2\pi \times 2.449 \times (9 \times 10^{-6})}$
- $f = \frac{1}{2\pi \times 2.449 \times 9 \times 10^{-6}}$
- $f = \frac{1}{138.45 \times 10^{-6}}$
- $f \approx 7222$ Hz $= 7.222$ kHz

- **2. Calculate the Minimum Value of h_{fe} (or β) of the Transistor:**
  - For sustained oscillations, the Barkhausen criterion states that the loop gain ($A_v \beta_{feedback}$) must be at least 1.
  - For a phase shift oscillator with three identical RC stages, the minimum voltage gain (A_v) required from the amplifier is 29. (This is derived from the analysis of the feedback network's attenuation).
  - For a common emitter amplifier, the voltage gain A_v is approximately given by $A_v \approx \frac{h_{fe} R_{L'}}{h_{ie}}$, where $R_{L'}$ is the effective AC load resistance and h_{ie} is the input impedance of the transistor ($h_{ie} \approx \beta r_e$).
  - In a typical BJT phase shift oscillator, the collector resistance R_C acts as the load for the amplifier. However, the input impedance of the RC feedback network also loads the amplifier. The effective load seen by the transistor is approximately $R_C || Z_{in,feedback}$, where $Z_{in,feedback}$ is the input impedance of the first RC stage.
  - However, for the minimum h_{fe} condition, considering an ideal amplifier driving the RC network, the gain of the amplifier must be at least 29.

- For a common emitter amplifier, the voltage gain is approximately $A_v = \frac{R_C}{R_{in}}$, where R_{in} is the equivalent input resistance of the transistor and the phase shift network.
- More accurately, for a transistor amplifier with R_C as collector resistance and with the loading from the first RC section, the minimum h_{fe} for oscillation is approximately given by:
  - $h_{fe,min} = 29 + \frac{29R}{R_C} + \frac{R_C}{R}$ (This formula applies when the phase shift network R is loaded by the amplifier's input resistance).
  - However, a simpler, more common formula derived for $h_{fe,min}$ where the amplifier provides a gain of 29 and the input impedance of the feedback network is neglected, or absorbed into the design:
    - $h_{fe,min} = 29$ (This is when the amplifier gain magnitude is $|A_V| = 29$).
  - A more precise formula for the minimum h_{fe} that takes into account the loading effect of the feedback network:
    - $h_{fe,min} = \left(29 + \frac{3R}{R_C}\right)$ or often simplified to $h_{fe,min} \approx 29 + \frac{R_C}{R}$ in some contexts. Let's use the most widely accepted one from common derivations.
    - For the three-stage RC phase shift oscillator using a BJT amplifier where the RC network loads the output of the amplifier:
      - The feedback factor $\beta_{feedback} = \frac{1}{29}$
      - The minimum gain of the amplifier for oscillation (A_v) must be 29.

  - The voltage gain of a CE amplifier is given by $A_v = \frac{-h_{fe}R_C}{h_{ie}}$ (approximately, neglecting h_{re}, h_{oe}).
  - For $A_v = 29$, $29 = \frac{h_{fe}R_C}{h_{ie}}$
  - Also, $h_{ie} = h_{fe}r_e = h_{fe}\frac{V_T}{I_E}$ (where r_e is emitter AC resistance).
  - This relationship implies that $h_{fe,min}$ is actually derived from the loop gain condition.

- Let's use the standard result that for a transistor phase shift oscillator, the minimum h_{fe} is approximately 29 when the amplifier's output impedance is low and input impedance is high. However, if the resistance of the RC network also affects the biasing, a more precise formula is needed.

- The typical formula for minimum h_{fe} considering the loading of the RC network and collector resistor is:
  - $h_{fe,min} = 23 + \frac{29R}{R_C}$
  - This formula can also be given as $h_{fe,min} = 29 + \frac{4R}{R_C}$ for certain assumptions.
  - A very common approximation is $h_{fe,min} = 29$.
  - Let's use a more complete one: $h_{fe,min} = \frac{1}{\beta_{feedback}}$. The attenuation of the RC network is $1/29$. So, $h_{fe,min} = 29$.

- Let's use the common formula: $h_{fe,min} \approx 29$. If we are to consider the specific loading due to R_C and R:
    - A more accurate formula for $h_{fe,min}$ in a BJT phase shift oscillator, considering R_C and the individual R of the RC network, is $h_{fe,min} = (23 + \frac{29R}{R_C} + \frac{R_C}{R})$ in some texts, or $h_{fe,min} = (23 + 4\frac{R}{R_C})$ assuming the current gain is h_{fe} and voltage gain is derived from that.
    - The simplest interpretation is that the amplifier must provide a voltage gain of 29.
    - If we use $h_{fe,min} = 29 + \frac{4R}{R_C}$:
        - $h_{fe,min} = 29 + \frac{4\times(6\times10^3\Omega)}{(18\times10^3\Omega)}$
        - $h_{fe,min} = 29 + \frac{24}{18} = 29 + 1.33 = 30.33$
    - If we use $h_{fe,min} = 23 + \frac{29R}{R_C}$:
        - $h_{fe,min} = 23 + \frac{29\times(6\times10^3\Omega)}{(18\times10^3\Omega)}$
        - $h_{fe,min} = 23 + \frac{174}{18} = 23 + 9.67 = 32.67$

- **Considering the widely accepted minimum gain is 29, let's stick to that.**
    - The minimum voltage gain required from the amplifier is $A_V = 29$.
    - For a common emitter amplifier, $A_V \approx h_{fe}\frac{R_C}{h_{ie}}$ or for simpler analysis $A_V \approx \frac{I_C R_C}{V_T}$.

- However, the requirement for sustained oscillation is that the current gain of the transistor must be sufficient to overcome the losses in the feedback network. The widely quoted condition for minimum h_{fe} for a BJT phase shift oscillator is approximately 29.
- **Therefore, the minimum value of h_{fe} for the transistor is 29.** (Using the most common and simplest assumption for the condition of oscillation).

- **Final Results:**
  - Frequency of oscillation ≈ 7.222 kHz
  - Minimum value of h_{fe} of the transistor ≈ 29 (or 32.67 or 30.33 depending on the formula used, 29 is the most standard without detailed circuit specifics of how R and R_C interact with h_{fe}).