[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 1362 **I**

Unique Paper Code : 2512041101

Name of the Paper : Analog Electronics

Name of the Course : **B.Sc. (H) Instrumentation (CORE)**

Semester : I (Under NEP UGCF Mode)

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. There are seven questions in all, out of which you have to attempt any **five** questions
3. Question no. **1** is compulsory
4. **All** questions carry equal marks
5. Use of non-programmable scientific calculator is allowed.

P.T.O.

1. (a) Explain the formation of a potential barrier across a PN junction and discuss how the width of this barrier varies with the applied voltage in forward and reverse- biased conditions. (3)

(b) Sketch the output of the given circuit in Fig. 1 with suitable explanations. (3)

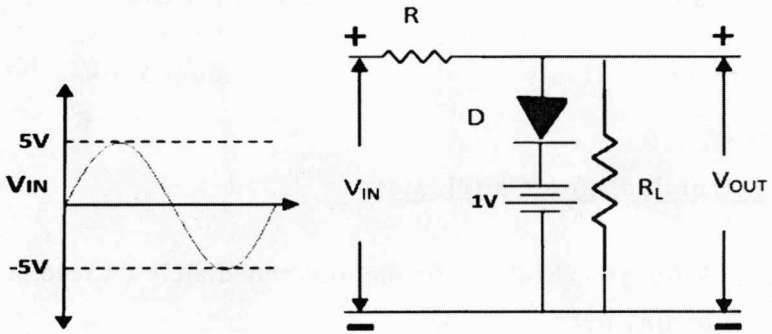

Fig. 1

(c) Define current amplification factor β for common emitter transistor configuration. Establish a relation between α and β. (3)

(d) Discuss the effect of bypass and coupling capacitors in a common emitter amplifier. (3)

(e) A Zener diode has a nominal voltage of 5.6 V at 25°C with a temperature coefficient of -2 mV/°C. If the temperature increases to 85°C, calculate the new Zener voltage. (3)

(f) Calculate the frequency of oscillations in Colpitt's oscillator if C1 = C2 = 3nF, L = 200μH. (3)

2. (a) Derive the expression of ripple factor and efficiency of the Half-wave rectifier. (7)

(b) Draw the output waveform for the clamper circuit in Fig. 2 with a suitable explanation. (7)

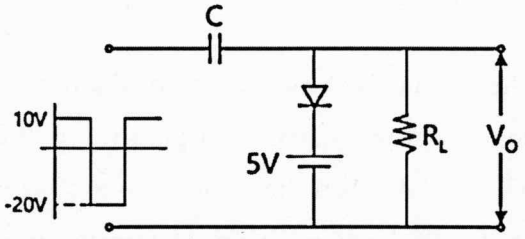

Fig. 2

P.T.O.

(c) A full-wave rectifier circuit has an input AC voltage of 12 V (RMS) and a load resistance (R_L) of 1 kΩ. Calculate : (4)

(i) The DC output voltage (V_{DC}).

(ii) The ripple factor (r).

(iii) The efficiency (η) of the rectifier.

3. (a) Draw and explain the input and output characteristics curve for the transistor in common emitter configuration. (7)

(b) Draw the Hybrid-π model of BJT in a common base configuration and explain the significance of each parameter. (7)

(c) The reverse leakage current of the transistor when connected in the CB configuration is 0.2 mA and it is 18μ,A when the same transistor is connected in the CE configuration. Determine α_{dc} & β_{dc} of the transistor. Assume $I_B = 30$ mA. (4)

4. (a) Explain the selection of the Q point for a transistor bias circuit and discuss the limitations on the output voltage swing. (6)

(b) Find the operating point and draw the load line of a fixed bias circuit using an NPN transistor for $\beta=300$, $V_{cc}=15$ V, $R_b=200$ KΩ, and $R_c=1$ KΩ. (6)

(c) For the CE two port hybrid circuit, determine the voltage gain, input impedance, and output impedance, given $h_{ie} = 1100\ \Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25\mu S$. (6)

5. (a) Evaluate the effect of negative feedback on input and output impedances of voltage series feedback amplifiers. (7)

(b) Prove that the negative feedback in amplifiers increases the Bandwidth. (7)

(c) Why the LC oscillators are not suitable for low-frequency applications? In a Transistor Colpitts oscillator L = 15 μH, C_1 = 0.001 μF, C_2 = 0.01 μF.

Find (a) operating frequency (b) Feedback fraction. (4)

6. (a) Show that the transformer coupled class A amplifier maximum efficiency is 50%. (7)

(b) Determine the range of values of V_i that will maintain the Zener diode shown in Fig. 3 in the "ON" state. Given R=220 Ω, V_z=20V, I_{zm}=60 mA and R_L=1.2kΩ. (7)

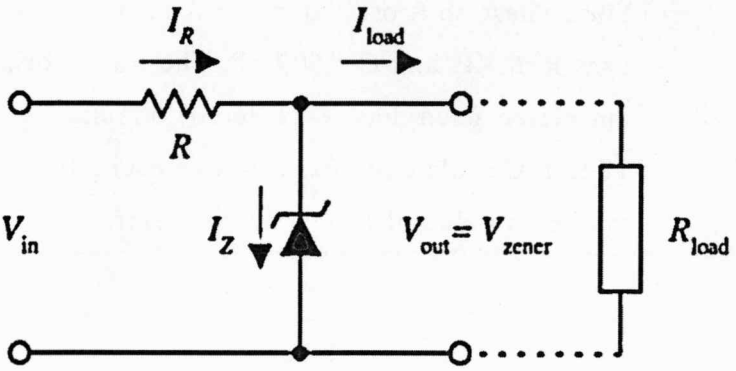

Fig. 3

(c) Calculate the closed loop gain for the negative feedback amplifier when open loop gain $A_v = 100,000$ and $\beta = 1/100$. Also, calculate closed loop gain when A_v is increased by 50%. (4)

7. (a) Derive the expression for the frequency of oscillations of a phase shift oscillator using three RC networks. (8)

(b) Draw the block diagram of the regulated power supply and explain significance of C filter. (5)

(c) For a phase shift oscillator, the feedback network uses R=6 KΩ and C=1500 pF. The transistorized amplifier used has a collector resistance of 18 KΩ. Calculate the frequency of oscillation and minimum value of h_{fe} of the transistor. (5)