Course- B.Tech
Course Code-CSET105
Session-2024-2025
Date- March 2025

Type- Core
Course Name- Digital Design
Semester-Even
Batch- ALL

Lab Assignment 7_Monday

Practical title: Implementation of Boolean expressions using logic gates

Name	CO1	CO2	CO3
	✓		✓

In this Lab, we will be able to determine the truth table of any given Boolean expression and then implement the expression with logic gates. Also, we will learn to implement an expression in Verilog-HDL.

1. How does a 4-to-2 Encoder function? Provide a truth table and explain.
2. What is the difference between Decoder and Demultiplexer?
3. Implement a 2-to-4 decoder using Verilog.
4. What is priority encoder? Write Verilog code for an 8-to-3 priority encoder.
5. Write a Verilog code to implement the following Boolean function using a decoder.

$$F(A,B,C)=\Sigma m(1,2,5,7)$$

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
    5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment2.pdf)**.
    6. Submit your file on LMS **within the deadline**.

- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.
- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.