Course- B.Tech
Course Code-CSET-105
Session-2024 - 25
Date- April-25

Type- Core
Course Name- Digital Design
Semester-Even
Batch- ALL

Lab Assignment 8_Set 1

Practical title: Implementation of various flip flops

In this Lab, we will understand concept of flip flops and implement various types of flip flops.

1. What is a flip-flop, and how is it different from a latch?

2. Explain the role of an SR flip-flop in digital circuits. Discuss its working with a truth table, logic diagram, and output waveform. Also, implement its functionality using Verilog and validate it with a test bench.

3. Explain the working of a JK Flip-Flop with a neat diagram. Provide its truth table and discuss its operations in detail. Design a JK Flip-Flop circuit and write a testbench code to verify its functionality. Also, include the expected waveform for the testbench simulation.

4. What is a D flip-flop, and how does it work? Can a JK flip-flop be converted into a D flip-flop? If yes, explain the conversion with a logic circuit and implement it using Verilog, including a testbench to verify its functionality.

5. Implement a T Flip-Flop, including its explanation, truth table, design, testbench, and waveform generation using a VCD file.

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
    5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment3.pdf)**.
    6. Submit your file on LMS **within the deadline**.
- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.
- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.