Course- B.Tech
Course Code-CSET-105
Session-2024 - 25
Date- 21 April 2025

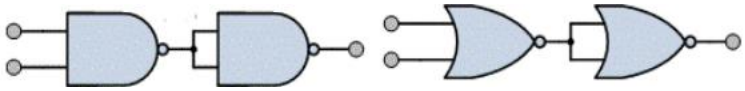
Type- Core
Course Name- Digital Design
Semester-Even
Batch- ALL

Assignment_Buffer_Lab_1_Monday

Practical title: Implementation of Boolean expressions using logic gates

Name	CO1	CO2	CO3
	✓	✓	✓

1. Find out the truth table of the below circuits and identify the gate that matches to their operation. Also implement them using Verilog-HDL and verify the results with that of its truth table.



2. Implement a half adder using NOR gates. Write a testbench to test all input combinations. Observe waveforms and verify the output.

3. Write verilog code to implement 2:1 Multiplexer.

4. Implement a 2-to-4 decoder using Verilog.

5. Design a 4-bit parallel-in-parallel-out (PIPO) register using Verilog.

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
    5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment3.pdf)**.
    6. Submit your file on LMS **within the deadline**.

- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.

- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.