**Name – Aryan Gahlot**

**Roll No- S24CSEU0701**

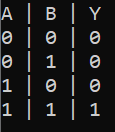
**Assignment Test**

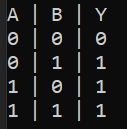
**Ans 1)** The gates shown in the t question are:

AND Gate using NAND Gate

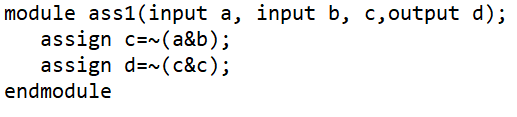
OR Gate using NOR Gate

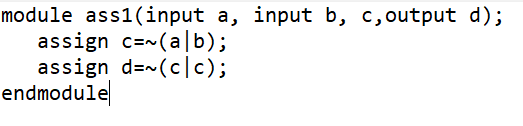
TRUTH TABLES:

 for AND Gate

for OR Gate

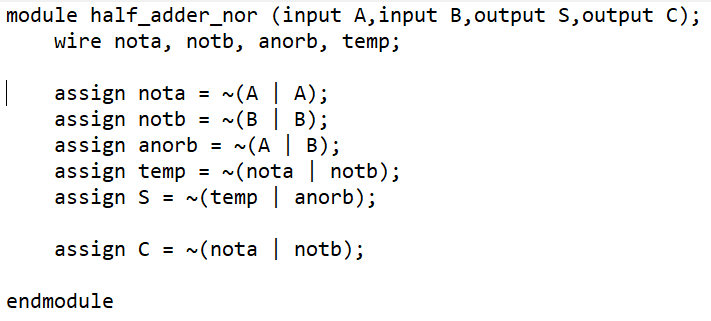
VERILOG CODES:

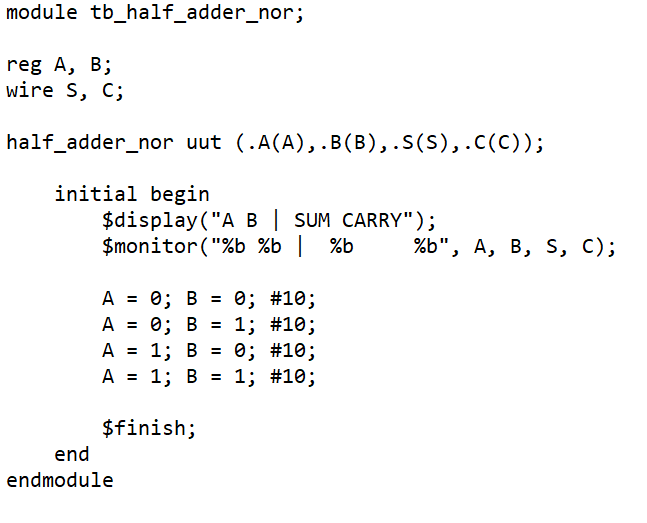
for AND Gate

for OR Gate

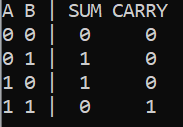
**ANS 2)**

VERILOG CODE AND TESTBENCH:

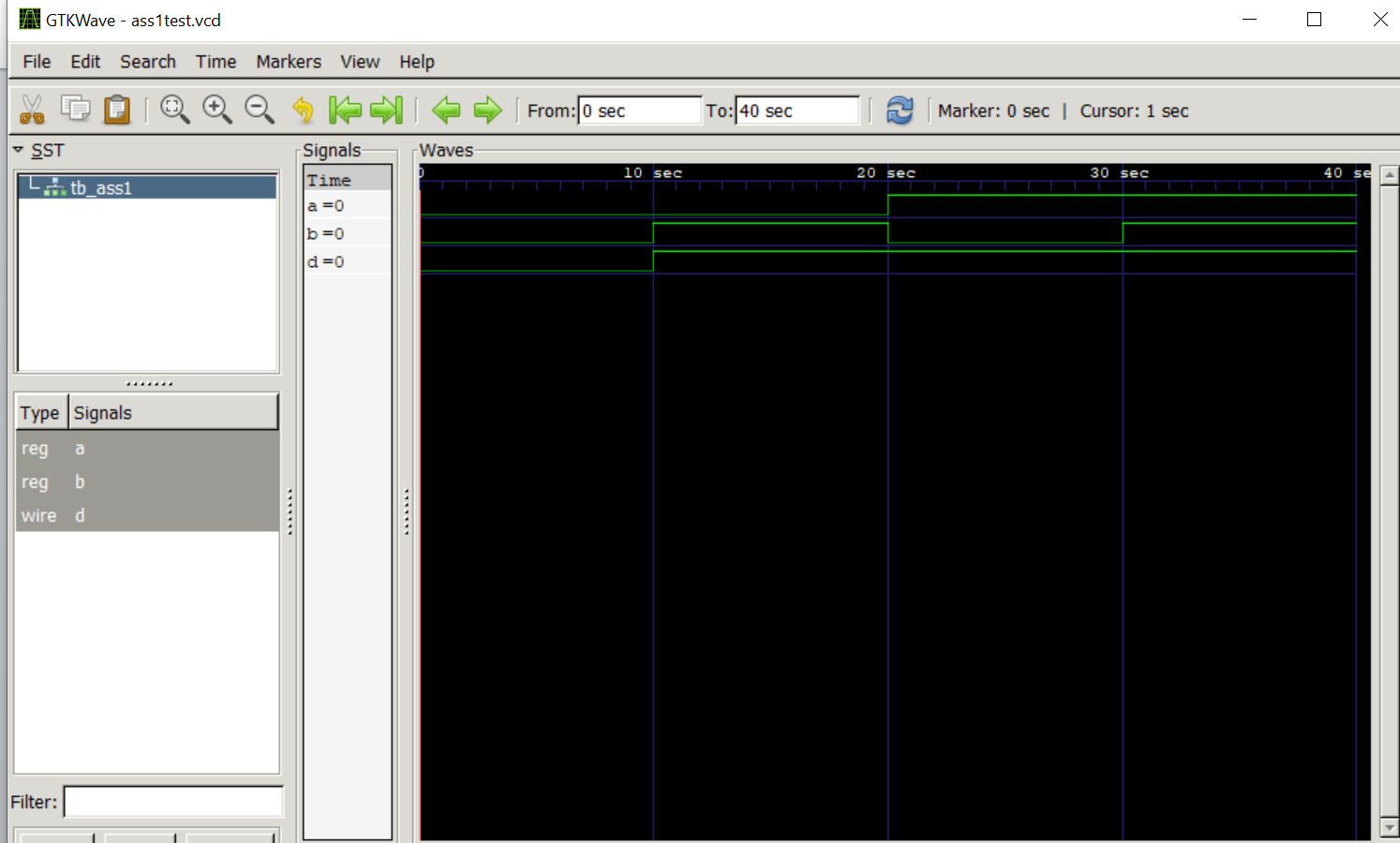




TRUTH TABLE:

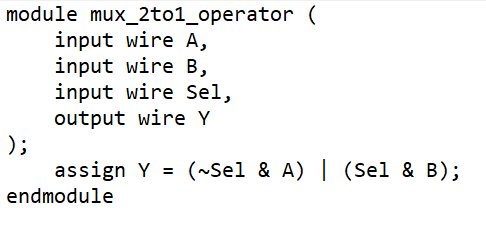


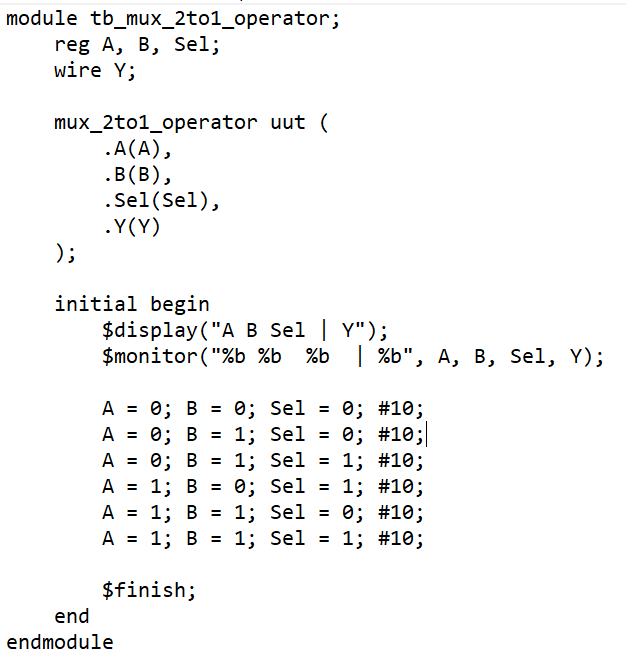
GTKWAVE:



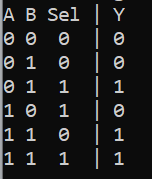
**ANS 3)**

VERILOG CODE AND TESTBENCH:

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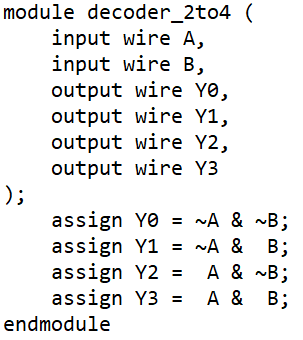
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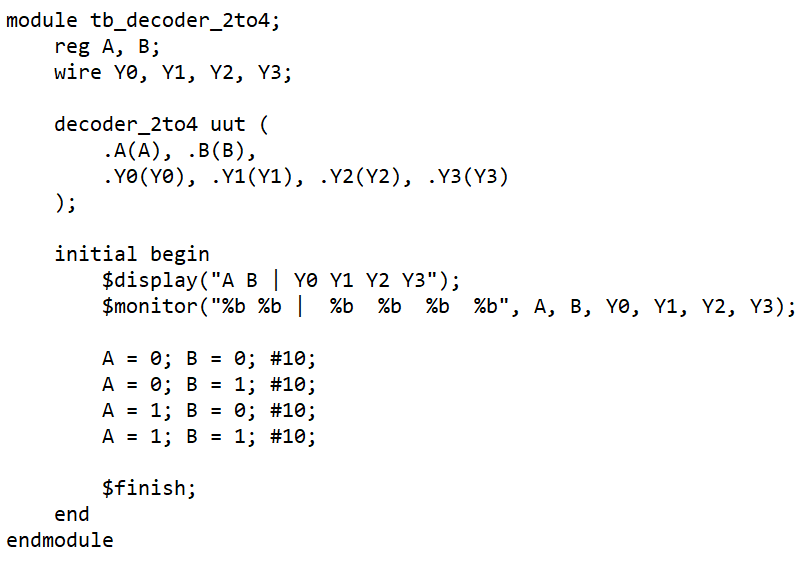
TRUTH TABLE:

****

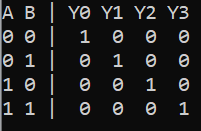
**ANS 4)**

VERILOG CODE AND TESTBENCH:

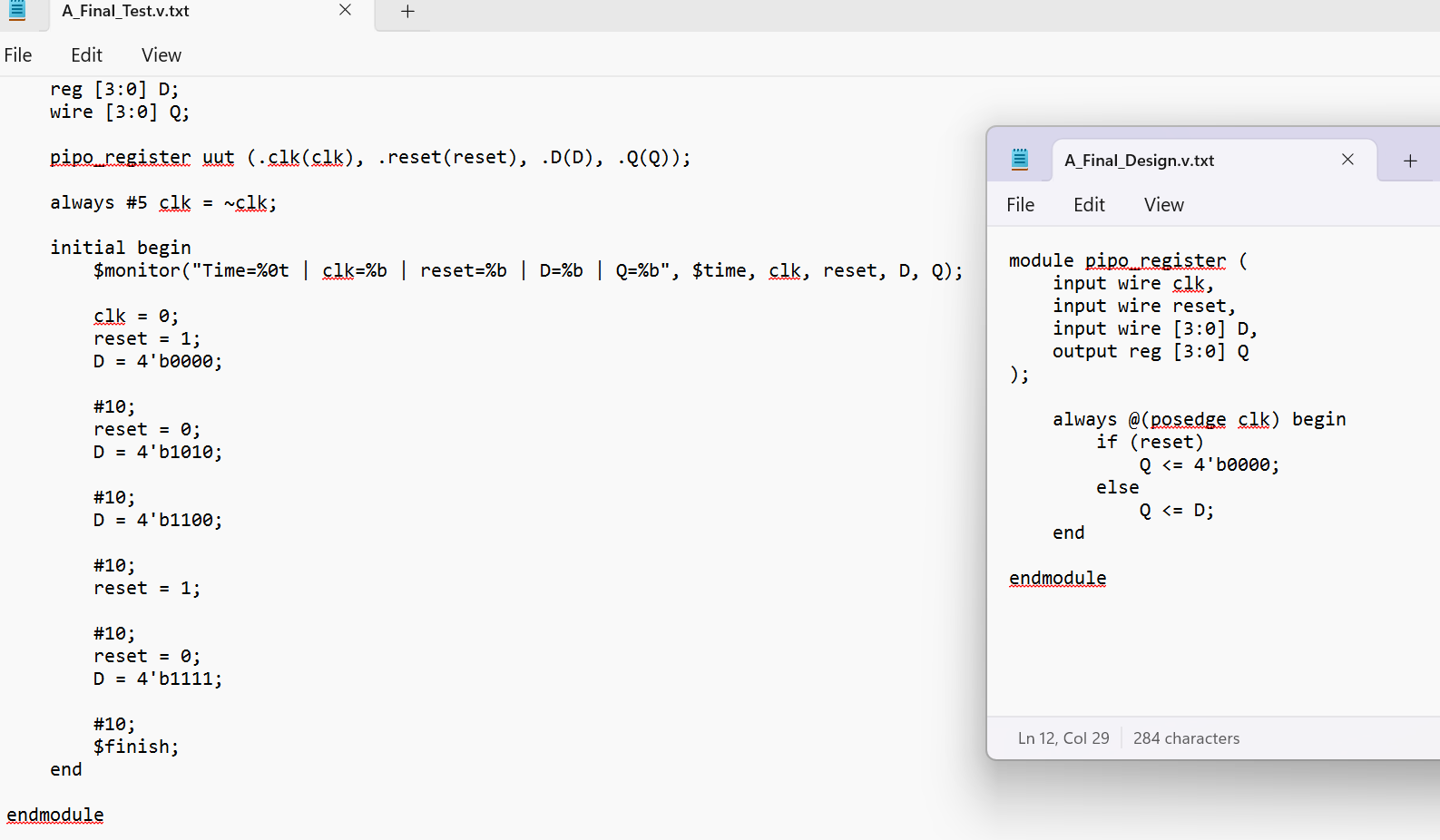
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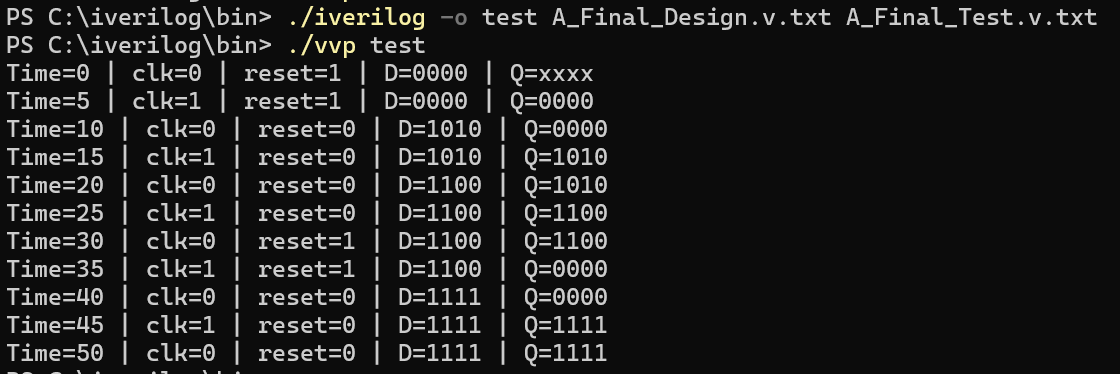
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TRUTH TABLE:

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**ANS 5)**

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