AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Electrical and Electronic Engineering

PROJECT REPORT

Project Title: SOC Design of 16-bit CPU following SIMD Processor Architecture

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SOC Design of 16-bit CPU following SIMD Processor Architecture

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***Abstract* - The SIMD processor architecture is a cutting-edge design in modern computing, allowing a single instruction to be executed on multiple data elements simultaneously. This approach leverages parallelism, executing the same operation on different data pieces simultaneously. The key idea is to have a central control unit that sends the same instruction to multiple processing units, which then operate in sync. This synchronization enables efficient processing of tasks involving repetitive operations on large data sets. The result is faster and more efficient computation, particularly for tasks that can be broken down into smaller, identical steps. In this project, we implemented a simple CPU with SIMD (Single Instruction, Multiple Data) capabilities defining a finite state machine (FSM) to execute instructions, including various arithmetic, logical, and data manipulation operations. This FSM module also incorporates multiple data registers and control registers to manage its operations.**

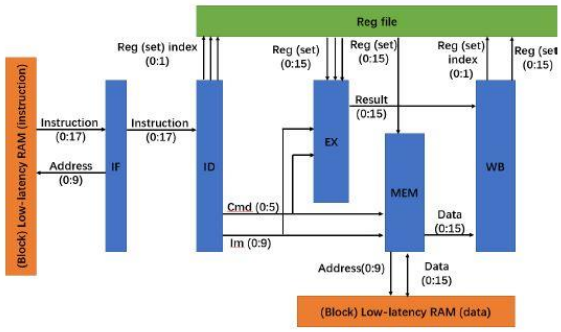


Figure 1: Simple SIMD Processor Architecture

METHODOLOGY

The Cadence Design Place and Route (PnR) process begins with creating a hardware description in Verilog code, followed by synthesis using a clock of MHz frequency to generate a gate-level netlist via a scripted command (synthesis_cmd.tcl). Moving from Genus to Encounter, the Design Import interface configures crucial settings such as library sets, RC corners, delay corners, and constraints. The floorplan then establishes initial chip cell placement and power distribution networks are defined for power integrity. Attention to clock distribution and signal routing optimizes timing, minimizes congestion, and ensures signal fidelity. This comprehensive methodology harmonizes circuit design, synthesis, and layout to produce a functional integrated circuit design, meeting performance, power, and area requirements while adhering to design constraints. The synthesis parameters employed for the specific operation of this project are presented in the table below:

Parameters for Group-03	Initial Clock Frequency (MHz)	Maximum Transition (ns)	Driving Cell	Operating Conditions	Input Delay (ns)	Output Delay (ns)	Max Fanout
	205	0.9	BUFX8	slow	2.86	2.38	8

The operational methodology of a SIMD processor unfolds as a symphony of simultaneous execution, wherein a singular command harmonizes the orchestration of parallel data processing. The pivotal modules driving operations within this SIMD CPU are delineated herein, and categorized based on their sequential functionality-

i. **CPU Finite State Machine:** Embedded within this module is a Finite State Machine (FSM) that orchestrates instruction execution through distinct stages, encompassing IDLE, IF (Instruction Fetch), ID (Instruction Decode), EX (Execute), MEM (Memory Access), and WB (Write-Back).

ii. **Pipelined Instruction Processing**: The CPU employs a pipelined approach to handle instructions, wherein each instruction undergoes sequential processing stages—fetching, decoding, execution, memory access, and eventual write-back.

iii. **Instruction Categorization and Encoding:** The CPU identifies diverse instruction types based on their opcodes, encompassing arithmetic (addition, subtraction, multiplication), accumulation, logical shifts, bitwise logical operations, bitwise NOT, memory load, and store operations.

iv. **Diverse Data and Control Registers:** Employing H, O, and Q sets, the module accommodates storage for varying data widths—16-bit, 8-bit, and 4-bit.

v. **Dynamic Register Selection:** Depending on instruction encoding, the CPU flexibly selects registers (R0, R1, R2, R3) to cater to specific operations.

vi. **Operation Execution:** Capitalizing on instruction opcodes and encodings, the CPU executes a spectrum of arithmetic, logical, and data manipulation operations.

vii. **Loop Management:** Facilitating loop control, the module introduces a CMD_loopjump instruction, affording modification of the program counter (PC) to enable looping constructs.

viii. **Temporal Result Registers:** To temporarily store operation outcomes prior to their commitment to data registers, the module maintains dedicated result registers.

ix. **Streamlined Data Access:** Ensuring efficient memory interaction, the module integrates logic to enable seamless read and write actions, guided by the ongoing instruction and its classification.

x. **Debugging Insights:** Augmented with display statements ($display), the module offers debugging insights—disclosing CPU status, executed instructions, and the contents of data and control registers.

xi. **Connecting Interface:** Facilitating integration, the CPU module interfaces with signals including CLK (clock), rst (reset), instruction_in (instruction input), data_in (data input), and produces outputs encompassing data_out (output data), instruction_address (fetched instruction address), data_address (data access address), data_R (read data enable), data_W (write data enable), and done (completion indicator).

RESULT ANALYSIS

The subsequent table provides a concise overview of the project outcome and violations-

Total Number of Instances	3414
Density after time Design analysis	0.855%
Number of Glitch Violations	0
Density after Optimizing design	0.850%
Routing Overflow	0.00%H & 0.00%V
DRC Violation	103(without wpad module), 9 (with wpad module)
Connectivity Violation	53 (Dangling wire violation)
Geometry Violation	124 (Short violation)
Other Occured Errors	Incomplete nano-routing, Global & Special Routing missing error

CONCLUSION

During this project, we have faced several difficulties like DRC and connectivity Violations- dangling wire and via violations, the software could not compile the memory instructions with success sometimes due to unknown error. The Pad Cells were placed effectively along with the VDD and VSS connection with pad cells from global net connections. We faced issues several times connecting pad cells with global nets though later we did face DRC violations due to this connection issue.

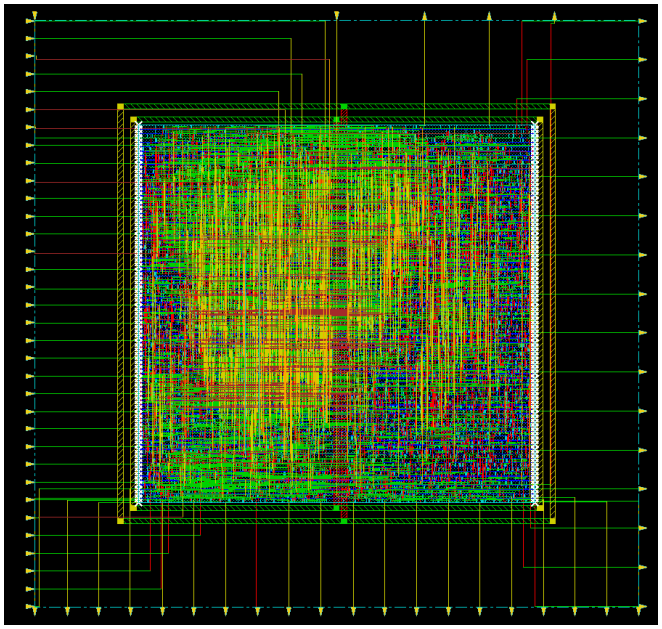


Figure: Pin Connection Placement view

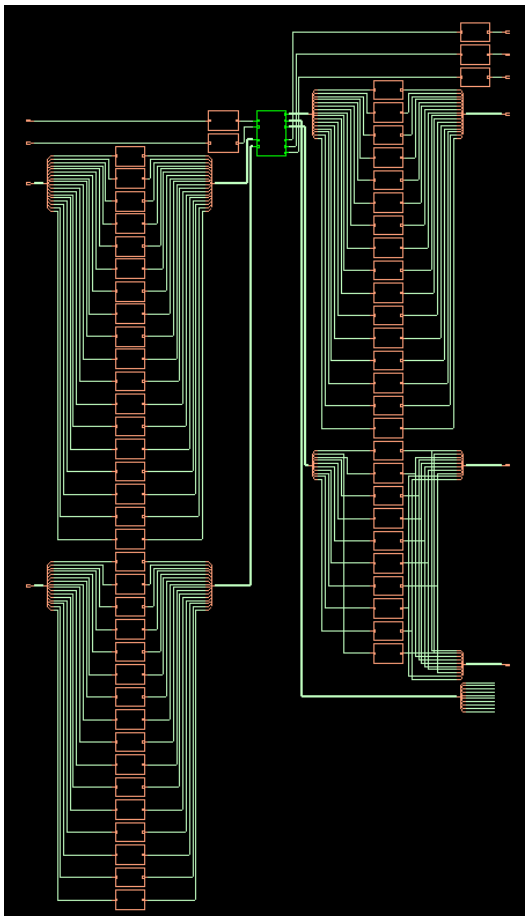


Figure: Gui_show view from Cadence

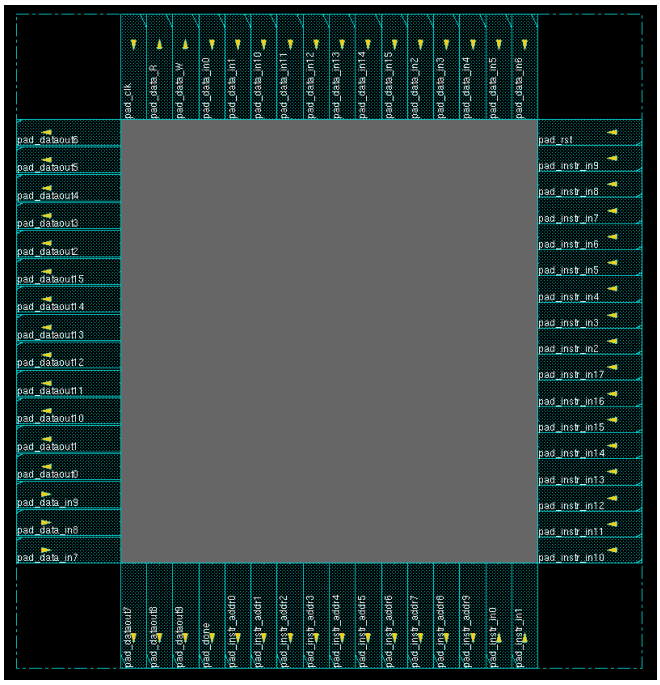


Figure: Placement Design with pad cell

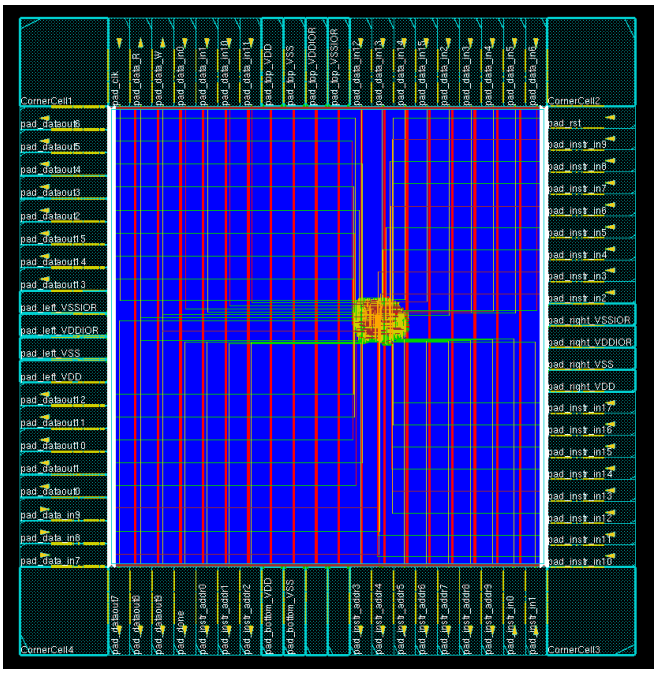


Figure: Placement Design with corner cell

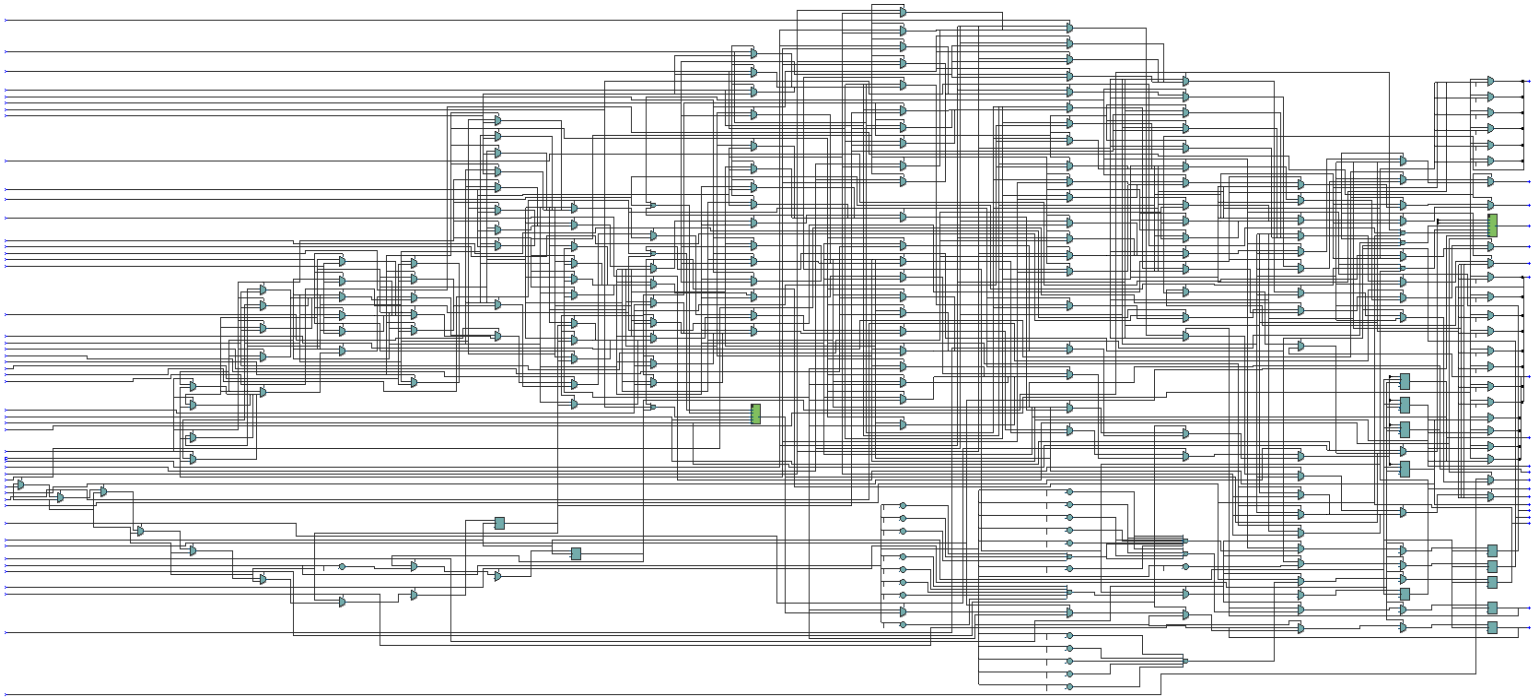
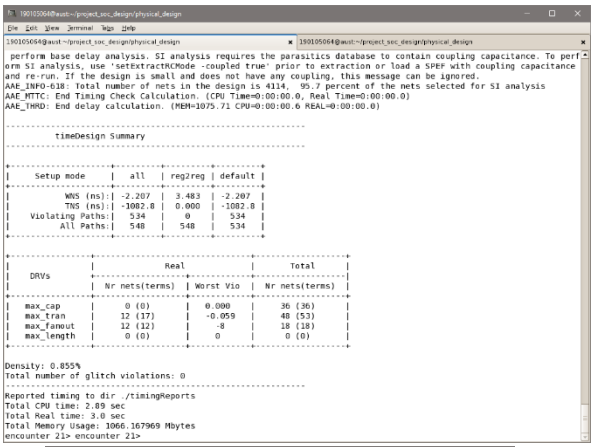


Figure: RTL Design view from Quartus Prime

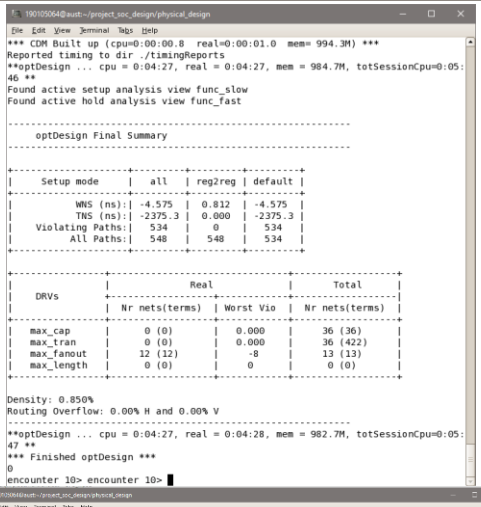
Screenshots of Analysis view:

Type	Instances	Area	Area %
timing_model	65	936000.000	99.0
sequential	387	2619.378	0.3
inverter	395	405.612	0.0
buffer	204	463.752	0.0
logic	2363	6275.016	0.7
total	3414	945763.758	100.0

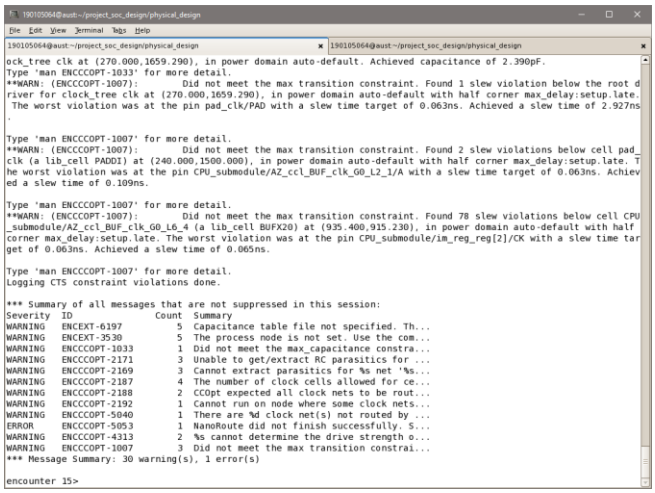
```
          Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
         plc_st         0  (        0 /        0 )  0.00
       plc_star         0  (        0 /        0 )  0.00
       drc_bufs         0  (        0 /        0 )  0.00
       drc_fopt         0  (        0 /        0 )  0.00
       drc_bufb         0  (        0 /        0 )  0.00
            dup         0  (        0 /        0 )  0.00
      crit_dnsz         0  (        0 /        0 )  0.00
      crit_upsz         0  (        0 /        0 )  0.00

 init_area              950228        0         0    157856    69714        0
 rem_inv_qb             950224        0         0    157856    69714        0
 gate_comp              950186        0         0    157856    69714        0
 glob_area              950088        0         0    157856    69714        0
 area_down              950075        0         0    157856    69714        0

          Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
          undup         2  (        0 /        0 )  0.01
        rem_buf       200  (        0 /        0 )  0.34
        rem_inv        58  (        0 /        2 )  0.13
       merge_bi        76  (        0 /        1 )  0.16
     rem_inv_qb        21  (        1 /        1 )  0.05
       io_phase        15  (        0 /        0 )  0.04
      gate_comp       236  (       13 /       13 )  0.88
      gcomp_mog        11  (        0 /        0 )  0.18
      glob_area        43  (       13 /       43 )  0.94
      area_down       291  (       13 /       17 )  1.37
 gate_deco_area         0  (        0 /        0 )  0.00

Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'CPU_wpad'.
Finished SDC export (command execution time mm:ss (real) = 00:00).
genus@design:CPU_wpad>
```



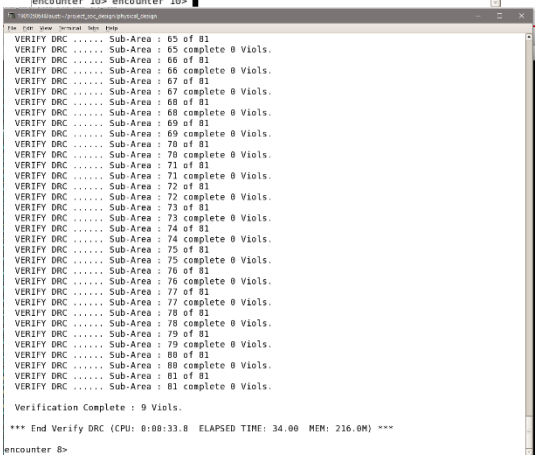
```
perform base delay analysis. SI analysis requires the parasitics database to contain coupling capacitance. To perform SI analysis, use 'setExtractRCMode -coupled true' prior to extraction or load a SPEF with coupling capacitance and re-run. If the design is small and does not have any coupling, this message can be ignored.
AAE_INFO-618: Total number of nets in the design is 4114,  95.7 percent of the nets selected for SI analysis
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=1075.71 CPU=0:00:00.6 REAL=0:00:00.0)

------------------------------------------------------------
        timeDesign Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Setup mode     |  all   | reg2reg | default |
+--------------------+--------+---------+---------+
|          WNS (ns):| -2.207 |  3.483  | -2.207  |
|          TNS (ns):| -1082.8 |  0.000  | -1082.8 |
|    Violating Paths:|  534   |    0    |   534   |
|         All Paths:|  548   |   548   |   534   |
+--------------------+--------+---------+---------+

+----------------+----------------------------------+------------------+
|                |               Real               |       Total      |
|    DRVs        +----------------+-----------------+------------------+
|                | Nr nets(terms) | Worst Vio       | Nr nets(terms)   |
+----------------+----------------+-----------------+------------------+
|   max_cap      |      0 (0)     |   0.000         |     36 (36)      |
|   max_tran     |     12 (17)    |  -0.059         |     48 (53)      |
|   max_fanout   |     12 (12)    |    -8           |     18 (18)      |
|   max_length   |      0 (0)     |     0           |      0 (0)       |
+----------------+----------------+-----------------+------------------+

Density: 0.855%
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 2.89 sec
Total Real time: 3.0 sec
Total Memory Usage: 1066.167969 Mbytes
encounter 21> encounter 21>
```



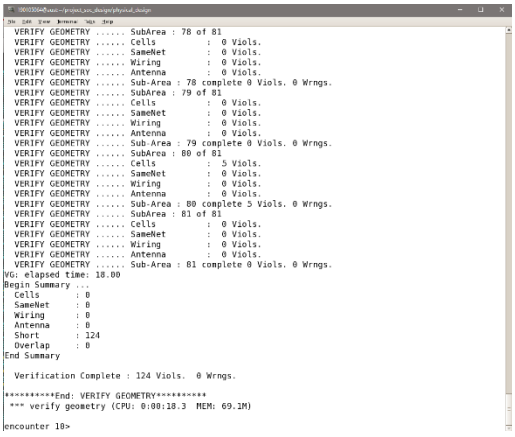
```
*** CDM Built up (cpu=0:00:00.8  real=0:00:01.0  mem= 994.3M) ***
Reported timing to dir ./timingReports
**optDesign ... cpu = 0:04:27, real = 0:04:27, mem = 984.7M, totSessionCpu=0:05:46 **
Found active setup analysis view func_slow
Found active hold analysis view func_fast

------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Setup mode     |  all   | reg2reg | default |
+--------------------+--------+---------+---------+
|          WNS (ns):| -4.575 |  0.812  | -4.575  |
|          TNS (ns):| -2375.3 |  0.000  | -2375.3 |
|    Violating Paths:|  534   |    0    |   534   |
|         All Paths:|  548   |   548   |   534   |
+--------------------+--------+---------+---------+

+----------------+----------------------------------+------------------+
|                |               Real               |       Total      |
|    DRVs        +----------------+-----------------+------------------+
|                | Nr nets(terms) | Worst Vio       | Nr nets(terms)   |
+----------------+----------------+-----------------+------------------+
|   max_cap      |      0 (0)     |   0.000         |     36 (36)      |
|   max_tran     |      0 (0)     |   0.000         |     36 (422)     |
|   max_fanout   |     12 (12)    |    -8           |     13 (13)      |
|   max_length   |      0 (0)     |     0           |      0 (0)       |
+----------------+----------------+-----------------+------------------+

Density: 0.850%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
**optDesign ... cpu = 0:04:27, real = 0:04:28, mem = 982.7M, totSessionCpu=0:05:47 **
*** Finished optDesign ***
0
encounter 10> encounter 10>
```



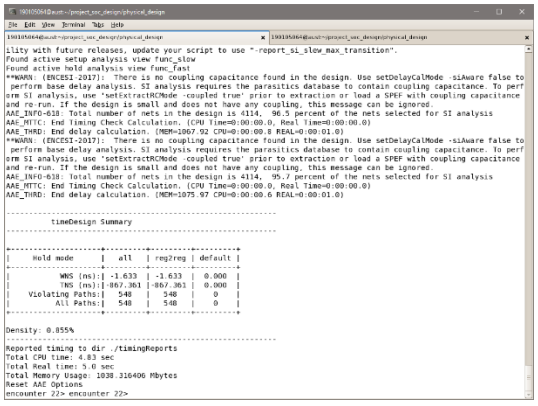
```
ock_tree clk at (270.000,1659.290), in power domain auto-default. Achieved capacitance of 2.390pF.
Type 'man ENCCCOPT-1033' for more detail.
**WARN: (ENCCCOPT-1007):        Did not meet the max transition constraint. Found 1 slew violation below the root driver for clock_tree clk at (270.000,1659.290), in power domain auto-default with half corner max_delay:setup.late. The worst violation was at the pin pad_clk/PAD with a slew time target of 0.063ns. Achieved a slew time of 2.927ns.

Type 'man ENCCCOPT-1007' for more detail.
**WARN: (ENCCCOPT-1007):        Did not meet the max transition constraint. Found 2 slew violations below cell pad_clk (a lib_cell PADDI) at (240.000,1500.000), in power domain auto-default with half corner max_delay:setup.late. The worst violation was at the pin CPU_submodule/AZ_ccl_BUF_clk_G0_L2_1/A with a slew time target of 0.063ns. Achieved a slew time of 0.109ns.

Type 'man ENCCCOPT-1007' for more detail.
**WARN: (ENCCCOPT-1007):        Did not meet the max transition constraint. Found 78 slew violations below cell CPU_submodule/AZ_ccl_BUF_clk_G0_L6_4 (a lib_cell BUFX20) at (935.400,915.230), in power domain auto-default with half corner max_delay:setup.late. The worst violation was at the pin CPU_submodule/im_reg_reg[2]/CK with a slew time target of 0.063ns. Achieved a slew time of 0.065ns.

Type 'man ENCCCOPT-1007' for more detail.
Logging CTS constraint violations done.

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   ENCEXT-6197          5  Capacitance table file not specified. Th...
WARNING   ENCEXT-3530          5  The process node is not set. Use the com...
WARNING   ENCCCOPT-1033        1  Did not meet the max_capacitance constra...
WARNING   ENCCCOPT-2171        3  Unable to get/extract RC parasitics for ...
WARNING   ENCCCOPT-2169        3  Cannot extract parasitics for %s net '%s...
WARNING   ENCCCOPT-2187        4  The number of clock cells allowed for ce...
WARNING   ENCCCOPT-2188        2  CCOpt expected all clock nets to be rout...
WARNING   ENCCCOPT-2192        1  Cannot run on node where some clock nets...
WARNING   ENCCCOPT-5040        1  There are %d clock net(s) not routed by ...
ERROR     ENCCCOPT-5053        1  NanoRoute did not finish successfully. S...
WARNING   ENCCCOPT-4313        2  %s cannot determine the drive strength o...
WARNING   ENCCCOPT-1007        3  Did not meet the max transition constrai...
*** Message Summary: 30 warning(s), 1 error(s)

encounter 15>
```



```
  VERIFY DRC ..... Sub-Area : 65 of 81
  VERIFY DRC ..... Sub-Area : 65 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 66 of 81
  VERIFY DRC ..... Sub-Area : 66 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 67 of 81
  VERIFY DRC ..... Sub-Area : 67 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 68 of 81
  VERIFY DRC ..... Sub-Area : 68 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 69 of 81
  VERIFY DRC ..... Sub-Area : 69 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 70 of 81
  VERIFY DRC ..... Sub-Area : 70 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 71 of 81
  VERIFY DRC ..... Sub-Area : 71 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 72 of 81
  VERIFY DRC ..... Sub-Area : 72 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 73 of 81
  VERIFY DRC ..... Sub-Area : 73 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 74 of 81
  VERIFY DRC ..... Sub-Area : 74 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 75 of 81
  VERIFY DRC ..... Sub-Area : 75 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 76 of 81
  VERIFY DRC ..... Sub-Area : 76 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 77 of 81
  VERIFY DRC ..... Sub-Area : 77 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 78 of 81
  VERIFY DRC ..... Sub-Area : 78 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 79 of 81
  VERIFY DRC ..... Sub-Area : 79 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 80 of 81
  VERIFY DRC ..... Sub-Area : 80 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 81 of 81
  VERIFY DRC ..... Sub-Area : 81 complete 0 Viols.

  Verification Complete : 9 Viols.

*** End Verify DRC (CPU: 0:00:33.8  ELAPSED TIME: 34.00  MEM: 216.0M) ***

encounter 8>
```



```
  VERIFY GEOMETRY ..... SubArea : 78 of 81
  VERIFY GEOMETRY ..... Cells         :  0 Viols.
  VERIFY GEOMETRY ..... SameNet       :  0 Viols.
  VERIFY GEOMETRY ..... Wiring        :  0 Viols.
  VERIFY GEOMETRY ..... Antenna       :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 78 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 79 of 81
  VERIFY GEOMETRY ..... Cells         :  0 Viols.
  VERIFY GEOMETRY ..... SameNet       :  0 Viols.
  VERIFY GEOMETRY ..... Wiring        :  0 Viols.
  VERIFY GEOMETRY ..... Antenna       :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 79 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 80 of 81
  VERIFY GEOMETRY ..... Cells         :  5 Viols.
  VERIFY GEOMETRY ..... SameNet       :  0 Viols.
  VERIFY GEOMETRY ..... Wiring        :  0 Viols.
  VERIFY GEOMETRY ..... Antenna       :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 80 complete 5 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 81 of 81
  VERIFY GEOMETRY ..... Cells         :  0 Viols.
  VERIFY GEOMETRY ..... SameNet       :  0 Viols.
  VERIFY GEOMETRY ..... Wiring        :  0 Viols.
  VERIFY GEOMETRY ..... Antenna       :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 81 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 18.00
Begin Summary ...
  Cells     : 0
  SameNet   : 0
  Wiring    : 0
  Antenna   : 0
  Short     : 124
  Overlap   : 0
End Summary

  Verification Complete : 124 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:18.3  MEM: 69.1M)

encounter 10>
```



```
ility with future releases, update your script to use "-report_si_slew_max_transition".
Found active setup analysis view func_slow
Found active hold analysis view func_fast
**WARN: (ENCESI-2017):  There is no coupling capacitance found in the design. Use setDelayCalMode -siAware false to perform base delay analysis. SI analysis requires the parasitics database to contain coupling capacitance. To perform SI analysis, use 'setExtractRCMode -coupled true' prior to extraction or load a SPEF with coupling capacitance and re-run. If the design is small and does not have any coupling, this message can be ignored.
AAE_INFO-618: Total number of nets in the design is 4114,  96.5 percent of the nets selected for SI analysis
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=1067.92 CPU=0:00:00.8 REAL=0:00:01.0)
**WARN: (ENCESI-2017):  There is no coupling capacitance found in the design. Use setDelayCalMode -siAware false to perform base delay analysis. SI analysis requires the parasitics database to contain coupling capacitance. To perform SI analysis, use 'setExtractRCMode -coupled true' prior to extraction or load a SPEF with coupling capacitance and re-run. If the design is small and does not have any coupling, this message can be ignored.
AAE_INFO-618: Total number of nets in the design is 4114,  95.7 percent of the nets selected for SI analysis
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=1075.97 CPU=0:00:00.6 REAL=0:00:01.0)

------------------------------------------------------------
        timeDesign Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Hold mode      |  all   | reg2reg | default |
+--------------------+--------+---------+---------+
|          WNS (ns):| -1.633 | -1.633  |  0.000  |
|          TNS (ns):| -867.361 | -867.361 |  0.000  |
|    Violating Paths:|  548   |   548   |    0    |
|         All Paths:|  548   |   548   |    0    |
+--------------------+--------+---------+---------+

Density: 0.855%
------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 4.83 sec
Total Real time: 5.0 sec
Total Memory Usage: 1038.316406 Mbytes
Reset AAE Options
encounter 22> encounter 22>
```