

# SHAGUFTA ZAINAB

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## Education

**S.A. Engineering College, Chennai**

*Bachelor of Engineering in Electronics & Communication*

**2022 - 2026**

*CGPA: 8.94*

**Smt. Chandabai Pagariya Jain Mat. Hr. Sec. School**

*Science Stream (Computer Science with Maths)*

**Grad. 2022**

*85.00%*

## Skills

**Networking:** TCP/IP, IP addressing, subnetting, routing (static, dynamic, default), switching (L2/L3), VLANs, DHCP, DNS basics, network troubleshooting, hands-on practice using Cisco Packet Tracer (CCNA Training)

**Testing & Tools:** Network simulation, topology validation, test case execution (Packet Tracer labs), documentation, Microsoft Office

**Programming:** Working knowledge of Java (Intermediate) & Python (Basic)

**Other Tools:** Arduino IDE, Xilinx Vivado

**Interpersonal:** Analytical problem-solving, technical documentation, Clear technical communication, Time Management, Leadership, Team Management, Critical Thinking

**Languages:** English, Hindi, Tamil, Urdu

## Experience

**Simpson & Co Pvt Ltd, Intern** ([Certificate](#))

**June 2025 – August 2025**

- Worked with SAP to manage and maintain enterprise digital data, ensuring accuracy and consistency across records.
- Identified discrepancies and resolved data issues through structured analysis and documentation.
- Collaborated across teams to improve reporting accuracy and workflow efficiency, strengthening problem-solving and cross-functional communication.

## Projects

**Network Simulation & Routing Labs (CCNA Practice)**

**2026**

- Built and tested multiple network topologies using Cisco Packet Tracer.
- Configured VLANs, routing protocols, IP addressing, and switching scenarios.
- Performed connectivity validation and troubleshooting across simulated enterprise networks.

**High-Performance ALU Design for 32-bit RISC-V Processor**

**2025 - 2026**

- Designed a 32-bit ALU for a single-cycle RISC-V processor in Verilog HDL using Xilinx Vivado, replacing RCA and array multiplier with Brent-Kung adder and Vedic multiplier.
- Achieved 7.8 ns ALU delay and improved dynamic power efficiency (0.592 W vs 0.606 W) through parallel prefix carry computation and parallel partial-product generation.

**Smart Cradle System**

**2025**

- Engineered an automated cradle using NodeMCU ESP8266, PIR sensor, and DHT11 module, featuring buzzer alerts and temperature monitoring for enhanced safety.

## Certifications

- Cisco Networking Academy — **CCNA** (Modules 1–3) — In Progress
- Python—Dynamic CAD
- Enhancing Soft Skills and Personality—NPTEL (Top 5 % scorer)
- IoT and IIoT—Techknots Academy LLP
- RFID and NFC Technologies—Techknots Academy LLP.

## Achievements & Activities

**Department Topper**

- Awarded Department Topper twice during the B.E. program by maintaining exceptional academic performance and ranking highest in the department.

**Intercollegiate Hackathon Participation – HackAIThon 2025**

- Contributed by ideating the solution approach and debugging code using AI tools during the HackAIThon intercollegiate competition at Stella Maris College, collaborating in a fast-paced problem-solving environment.