NIRMA UNIVERSITY
INSTITUTE OF TECHNOLOGY
B.Tech.

OPEN ELECTIVE

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Course Code	2ECOE07
Course Name	FPGA based VLSI Design

Course Outcomes (COs):

At the end of the course, the students will be able to –

1. Design different combinational and sequential design circuits.
2. Classify and Compare the architecture of programmable logic devices.
3. Implement digital circuits on reconfigurable hardware using Verilog.
4. Apply the concepts of finite state machines for the design of Synchronous Digital Circuits.

Syllabus: **Teaching Hours: 30**

UNIT I: Basics of Digital System Design **02**

Introduction to Digital Systems, Digital System Design Flow, Areas under Digital Design

UNIT II: Simple Programmable Logic Devices **05**

Read-Only Memory (ROM) and variants, Programmable Array Logic, Programmable Logic Arrays

UNIT III: Complex Programmable Logic Devices **05**

CPLD Architectures, FPGA Architectures, FPGA Programming Methods

UNIT IV: Hardware Description Language **02**

Requirements of HDL, HDL properties, Types of HDL and supported CPLDs, Lexical conventions, data types, system tasks, compiler directives, Modules and Ports, Module definition, port declaration, connecting ports, hierarchical name

UNIT V: Gate Level and Data Flow Style of Modelling **03**

Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays, Continuous assignments, delay specification, expressions, operators, operands, operator types.

UNIT VI: Behavioral and Structural Modelling **09**

Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate a statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks

UNIT VII: Finite State Machine and Implementation **04**

Melay Machine, Moore Machine, Overlapped, and Non overlapped sequence detectors, FSM based design on FPGA

Self-Study:
The self-study content will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:
Laboratory work will be based on the above syllabus with minimum 10 experiments to be incorporated.

Suggested Readings:

1. Charles Routh, Lizy Kurian, Beyong Kil Lee, "Digital Systems Design Using Verilog", Cengage Learning
2. Stephen Brown, Zvonkoc Vranesic, "Fundamentals of Digital Logic with Verilog Design", Tata McGraw Hill
3. Sunggu Lee, "Digital Logic Design using Verilog, State Machine & Synthesis for FPGA," Cengage Learning
4. Advanced Digital Design with Verilog HDL – Michel D. Ciletti, PHI
5. Verilog HDL – Samir Palnitkar, Pearson Education

L = Lecture, T = Tutorial, P = Practical, C = Credit