**RS14100 WiSeMCUTM Family**

**User Manual**

**Version 1.4**

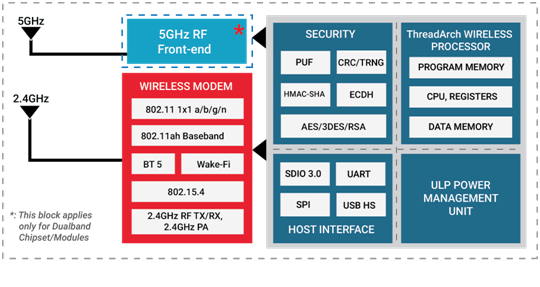
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# RS14100 WiSeMCU System Overview

Redpine Signals' RS14100 WiSeMCU™ family of chips and modules device is the industry's first Wireless Secure MCU family with a comprehensive multi-protocol wireless sub-system. It has an integrated ultra-low-power microcontroller, a built-in wireless subsystem, advanced security, high performance mixed-signal peripherals and integrated power-management.



**Solution Highlights**

* Efficient on-chip application processor based on ARM® Cortex®-M4F with up to 180 MHz performance, up to 4 MB dedicated flash
* Co-existence of multiple wireless protocols including 802.11a/b/g/n (2.4 GHz and 5 GHz), dual-mode Bluetooth 5 and 802.15.4 (capable of running Thread or ZigBee)
* Ultra-low power consumption with multiple power modes to reduce the system energy consumption
* Multiple levels of security including PUF (Physically Unclonable Function), Crypto HW accelerators, Secure Bootloader and Secure Zone to create a highly secure system
* Fully integrated and wireless certified modules with multiple sizes as small as 4.63 mm x 7.9 mm
* Integrated networking and wireless stacks for ease of integration
* Leading edge RF performance providing long range and higher throughputs
* Unique peripherals like ULP sub-system, voice activity detection (VAD) and up to 8 capacitive touch sensor inputs

**Features**

**Microcontroller**

* ARM Cortex-M4 core with up to 180 MHz
* Integrated FPU, MPU and NVIC
* SWD and JTAG debug options
* Internal and external oscillators with PLLs
* Flash In-Application Programming (IAP), In-System Programming (ISP) and Over-the-Air Wireless Firmware Upgrade
* Power-On Reset (POR), Brown-Out and Black-out Detect (BOD) with separate thresholds

**Memory**

* Up to 4 MB integrated Quad-SPI flash with inline AES engine and XIP
* Up to 400 KB SRAM
* 4-way set-associative 16 KB I-Cache

**Security**

* HW device identity and key storage with PUF
* Trusted Execution Environment with Secure Boot loader
* Accelerators: AES128/256, Accelerators: AES128/256, SHA256/384/512, RSA, ECC, ECDH, RNG, CRC

**Digital Peripherals**

* USB HS OTG with integrated HS transceiver
* 10/100 Mbps Ethernet MAC with RMII
* SDIO 3.0 host and slave, SD/eMMC
* 3x USART, 4x SPI, 3x I2C, 2x I2S, SIO, CAN 2.0B
* Timers: 5x 32-bit, 1x 16/32-bit, 1x 24-bit, WWDT, RTC, RIT, QEI
* Up to 85 GPIOs with GPIO multiplexer

**Analog Peripherals**

* 12-bit 16-ch, 5 Msps ADC, 10-bit DAC
* 3x op-amps, 2x Comparators and Temperature Sensor
* 8 capacitive touch sensor inputs
* Voice Activity Detection (VAD)

**Wi-Fi**

* Compliant to single-spatial stream IEEE 802.11 a/b/g/n with dual band (2.4 and 5 GHz) support
* Support for 20 MHz and 40 MHz channel bandwidths
* Transmit power up to +20dBm1 with integrated PA
* Receive sensitivity as low as -97 dBm1
* Application data throughput up to 40 Mbps1 in TCP mode

**Bluetooth**

* Compliant to dual-mode Bluetooth 5
* Transmit power up to +20 dBm1 with integrated PA
* Receive sensitivity as low as -104 dBm1
* <5 mA1 transmit current in BT 5 mode, 0 dBm output power, 2 Mbps data rate
* Data rates: 125 kbps, 500 kbps, 1 Mbps, 2Mbps, 3 Mbps

**802.15.42**

* Compliant to IEEE 802.15.4, 2.4 GHz
* Transmit power up to +20 dBm1 with integrated PA
* Receive sensitivity of -102 dBm1

**RF Features**

* Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun, T/R switch and flash memory
* Dual external antenna (diversity supported)

**Wake-FiTM [[1]](#footnote-1)**

* Ultra-low power wake-up receiver with secure wakeup pattern to prevent battery drain attack.

**Embedded Wi-Fi Stack Features**

* Support for Embedded Wi-Fi Client mode, Wi-Fi Access point mode, Wi-Fi Direct and Enterprise Security
* Supports advanced Wi-Fi security features: WPA/WPA2-Personal and Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP, EAP-LEAP, PEAP-MSCHAP-V2)
* Integrated TCP/IP stack (IPV4/IPV6), HTTP/HTTPS, DHCP, ICMP, SSL/TLS, Web sockets, IGMP, DNS, DNS-SD, SNMP, FTP Client
* Wi-Fi firmware upgrade and provisioning
* Support for concurrent Wi-Fi, dual-mode Bluetooth 5 and 802.15.42

**Embedded Bluetooth Stack**

* EDR+2.1, 4.0, 4.1, 4.2 and 5.0
* BT LE 1 Mbps, 2 Mbps and Long Range modes
* Piconet and scatternet
* BT profile support1 for SPP, A2DP, AVRCP, HFP, PBAP, IAP, GAP, SDP, L2CAP, RFCOMM, GATT, IAP1, IAP2

**Embedded Zigbee Stack**

* ZigBee PRO and Thread stack embedded
* Supported modes: ZigBee Coordinator, Router1, End device
* Supported profiles: Zigbee Light Link (ZLL), Home Automation (HA) and Smart Energy (SEP)

**MCU Sub-system Power Consumption**

* Active current as low as 15uA/MHz1 in low power mode
* Deep sleep mode current: ~400nA1
* Dynamic Voltage & Frequency Scaling
* Deep sleep mode with only timer active – with and without RAM retention

**Wireless Sub-system Power Consumption**

* Wi-Fi standby associated current of <50 uA1 (2.4GHz)
* Wi-Fi tx current = 220 mA1, rx current of 40 mA1 (2.4GHz)

**Software and Regulatory Certification**

* Wi-Fi Alliance
* ZigBee Certification2, Bluetooth Qualification2
* Regulatory certifications (FCC, IC, CE, ETSI, TELEC)2

**Operating Conditions**

* Single supply: 2.1 to 3.6V or 1.85V
* Operating temperature: -40ºC to +85ºC (Industrial grade)

**Packages**

* Modules with and without integrated antenna
* Chipset packages - WLCSP, QFN and BGA

**Evaluation Kit**

* WiSeMCU Single Band EVK: RS14100-SB-EVK1
* WiSeMCU Dual Band EVK: RS14100-DB-EVK1

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# Related Resources

Documentation, Software Packages, and more are available on Redpine’s document portal (<https://www.redpinenetworks.us>) after signing Redpine NDA. Contact the local Redpine Sales office or visit <http://www.redpinesignals.com/Contact_Us/Contact_Form.php> to obtain the NDA and instructions to login.

Please use the Redpine document portal as the latest and authoritative source for all information.

|  |  |
| --- | --- |
| **Name** | **Location on Redpine Document Portal** |
| **RS14100 WiSeMCU Family Common Documents** | |
| **RS14100 WiSeMCU Module Family Datasheet** | */RS14100 WiSeMCU/Datasheets, Manuals, and Guides/* |
| **RS9116 EVK User Guide** | */RS14100 WiSeMCU/EVK/* |
| **Module Integration Guide** | */RS14100 WiSeMCU/Datasheets, Manuals, and Guides/* |
| **Regulatory and Compliance Certificates** | |
| **FCC compliance certificates** | */ RS14100 WiSeMCU /Certifications and Declarations/* |
| **CE compliance certificates** | */ RS14100 WiSeMCU /Certifications and Declarations/* |
| **IC compliance certificates** | */ RS14100 WiSeMCU /Certifications and Declarations/* |
| **RS14100 WiSeMCU Documents** | |
| **WiSeMCU Getting** **Started Guide** | */Application Notes/* |
| **WiSeMCU Software Package including examples** | */RS14100 WiSeMCU/Firmware/* |
| **WiSeMCU SAPI Guide** | */RS14100 WiSeMCU/Firmware/* |
| **WiSeMCU SAPI Porting Guide** | */RS14100 WiSeMCU/Firmware/* |
| **Miscellaneous Resources** | |
| **3D Models** | */RS14100 WiSeMCU/CAD Files/* |
| **IBIS Models** | */RS14100 WiSeMCU/CAD Files/* |
| **Application Notes** | */Application Notes/* |
| **3D Models** | */RS14100 WiSeMCU/CAD Files/* |

Table 1: RS14100 WiSeMCU Related Resources

# Wireless Features

The table below lists the salient wireless features of the RS14100 based family of products.

All features marked in \* are not supported in current software release but planned for the future releases. Contact Redpine Sales ([sales@](mailto:sales@redpinesignals.com)[redpinesignals.com) for the software releases roadmap.](http://redpinesignals.com)

| **Feature** | **Description** |
| --- | --- |
| Wireless Protocols | IEEE 802.11b, 802.11g, 802.11n, 802.11a  Bluetooth 5 (2.1+EDR, LE, LE 2 Mbps, Long Range (125/500 Kbps), AoA/AoD)  ZigBee/Thread on 802.15.4 |
| Operational Modes Supported  (For other co-existence modes not listed here, please contact Redpine for custom offerings.) | Wi-Fi Access Point with support for upto 8 clients  Wi-Fi Client  Wi-Fi DirectTM  Wi-Fi Client + Bluetooth Classic (EDR v 2.1)  Wi-Fi Client + Bluetooth Low Energy  Wi-Fi Client + ZigBee End Device  ZigBee Router\*  ZigBee Coordinator\* |
| WLAN Bandwidth | 20 MHz, 40 MHz |
| WLAN Data Rates | 802.11b: 1, 2, 5.5, 11 Mbps  802.11g/a: 6, 9, 12, 18, 24, 36, 48, 54 Mbps  802.11n: MCS0 to MCS7 with and without Short GI and MCS32 |
| WLAN Operating Frequency Range | 2412 MHz – 2484 MHz  4.9 GHz – 5.975 GHz |
| WLAN Modulation | OFDM with BPSK, QPSK, 16-QAM, and 64-QAM  802.11b with CCK and DSSS |
| Maximum WLAN Transmit Power | 20 dBm |
| Minimum WLAN Receive Sensitivity | -97 dBm |
| Bluetooth Data Rates | 1, 2, 3 Mbps, 125 Kbps and 500 Kbps |
| Bluetooth Operating Frequency | 2.402 GHz - 2.480 GHz |
| Bluetooth Channel Spacing | BR, EDR, LE 1 Mbps, LR - 1 MHz  LE 2 Mbps - 2 MHz |
| Bluetooth Modulation | GFSK, DQPSK, 8DPSK |
| Maximum Bluetooth Transmit Power | 20 dBm (Class-1) |
| Minimum Bluetooth Receive Sensitivity | LE: -96 dBm, LR 125 Kbps: -104 dBm |
| ZigBee Data Rate | 250 Kbps |
| ZigBee Frequency Band | 2.402 GHz - 2.480 GHz |
| ZigBee Modulation | DSSS |
| Maximum ZigBee Transmit Power | 20 dBm |
| Minimum ZigBee Receive Sensitivity | -102 dBm |
| Software Architecture | Embedded Architecture (WiSeConnect) which includes all network related features, including WLAN, Bluetooth, ZigBee stacks, feature-rich TCP-IP stack embedded in the WiSeMCU SoC. Option to bypass the TCP-IP stack and include only the Wireless protocol stacks |
| Wireless Security Features | WPA/WPA2-Personal  WPA/WPA2 Enterprise for Client  EAP-TLS  EAP-FAST  EAP-TTLS  PEAP-MSCHAP-v2  (embedded in the WiSeConnect) |
| Advanced Security Features | PUF Based Security  AES 128/256 bit  RSA  SHA, SHA256, SHA384 |
| Application throughputs | Upto 50 Mbps (As measured in ideal environment. Note that throughput degrades in the presence of interference and reduce with range) |
| Operating Temperature Range | -40oC to +85o / 105º C |
| Supply Voltages | Option 1: Direct battery, 2.1-3.6V  Option 2: External 1.85V from system LDO |
| WLAN Features | Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics  Hardware accelerators for WEP 64/128-bit, TKIP, AES and WPS  Support for WMM  Support for AMPDU Aggregation/De-aggregation and AMSDU De-aggregation  Support for IEEE 802.11d/e/I, 802.11w/k/v/r/h\* |
| TCP/IP Features | TCP/IP Stack with IPV4, IPV6  HTTP Server/Client  Static and Dynamic Webpages with JSON Objects (for HTML Server)  DHCP Server/Client for IPV4/IPV6  HTTPS Server/Client  ICMP  SSL 3.0/TLS 1.2  Websockets  DNS Client  IGMP  FTP Client, mDNS Client, DNS-SD Client, SNMP\* |
| Bluetooth Features | Supports EDR+2.1, 4.0, 4.1, 4.2 and 5.0.  Supports LE 1 Mbps and 2 Mbps and Long Range modes.  Supports AoA, AoD  Supports Classic mode piconet with seven active slaves\* (two slaves in current release)  Supports Low Energy mode with eight active slaves  Supports scatternet with two slave roles or one master role and one slave role while being visible \*  Proprietary Mode to support 15 active slaves by using the “reserved” bit  Bluetooth security features: Authentication, Pairing and Encryption.  Supports low power connection states such as sniff (with selectable sniff intervals) and hold\* (only sniff in current release)  Adaptive Frequency Hopping (AFH), Interlaced scanning, Channel Quality Driven Data Rate\*, Quality of Service  Channel assessment algorithm provides fast and accurate determination of occupied channels for use in adaptive frequency hopping mode \*  Proprietary FEC for DQPSK and 8-PSK modes  Provides finer granularity of range vs. throughput control  BR/EDR secure connections, Train Nudging, Generalized interlaced scan, Low duty cycle directed adverting, Piconet clock adjustment, WMS coexistence, Slot availability mask (SAM)  Dual mode support, 32-bit UUID in LE, LE privacy, LE ping, LE L2CAP connection oriented channel, Connectionless slave broadcast, Fast advertising interval, LE data packet extension, LE secure connections, Link layer privacy, LE advertising extensions, LE channel selection algorithm2, high duty cycle non-connectable advertising. |
| Bluetooth Profiles (Contact Redpine Sales for other profiles) | GAP, GATT, SPP, SDP, SMP, L2CAP, RFCOMM |
| ZigBee Features | **MAC:**  Supported modes: ZigBee Coordinator, Router\*, End device  PHY features: Beacon\*, Non-Beacon, CCM Security  Promiscuous mode  Power saving using End Device Sleep, network periodic sleep  Supports CCM Security levels 1-7  Supports Active scan, channel selection, Association and Disassociation, Orphan scanning, and coordinator realignment  **Network:**  Network Discovery, Energy Detection Scan, Network Formation, Permit Joining, Network Join, Network Rejoin, Stochastic Addressing, Network Leave, Network Reset, Routing (Symmetric), Address Conflict, PANID Conflict, Network Status Updates, Link Status Commands, Data Transmission (Unicast and Broadcast), NIB Management, Many-to-one and source routing, Multicast relaying and route discovery  **APS:**  APSDE Data primitives, APSME Group Services, APSME Binding Services, APSME Fragmentation Service, Reliable Transport, Duplicate Rejection, APS Layer Security  **ZDO/ZDP**  Device Discovery, Service Discovery, Security Manager, Node Manager, Network Manager, Binding Manager, Group Manager, Startup Attributes Set |
| Power Save Modes | Dynamic Clock Gating  Ultra Low Power (ULP) Mode – Most of the WiSeMCU SoC powered off except for a small portion running a timer. Host interface is inactive. Entry and exit of sleep mode can be through packet or GPIO based handshake  Refer to MCU Programmers manual for detailed description of Power save modes and usage |
| Miscellaneous Features | Wireless Firmware Upgrade  Wireless Configuration |

Table 2: RS14100 Connectivity Wireless Features

# RS14100 System Block Diagram

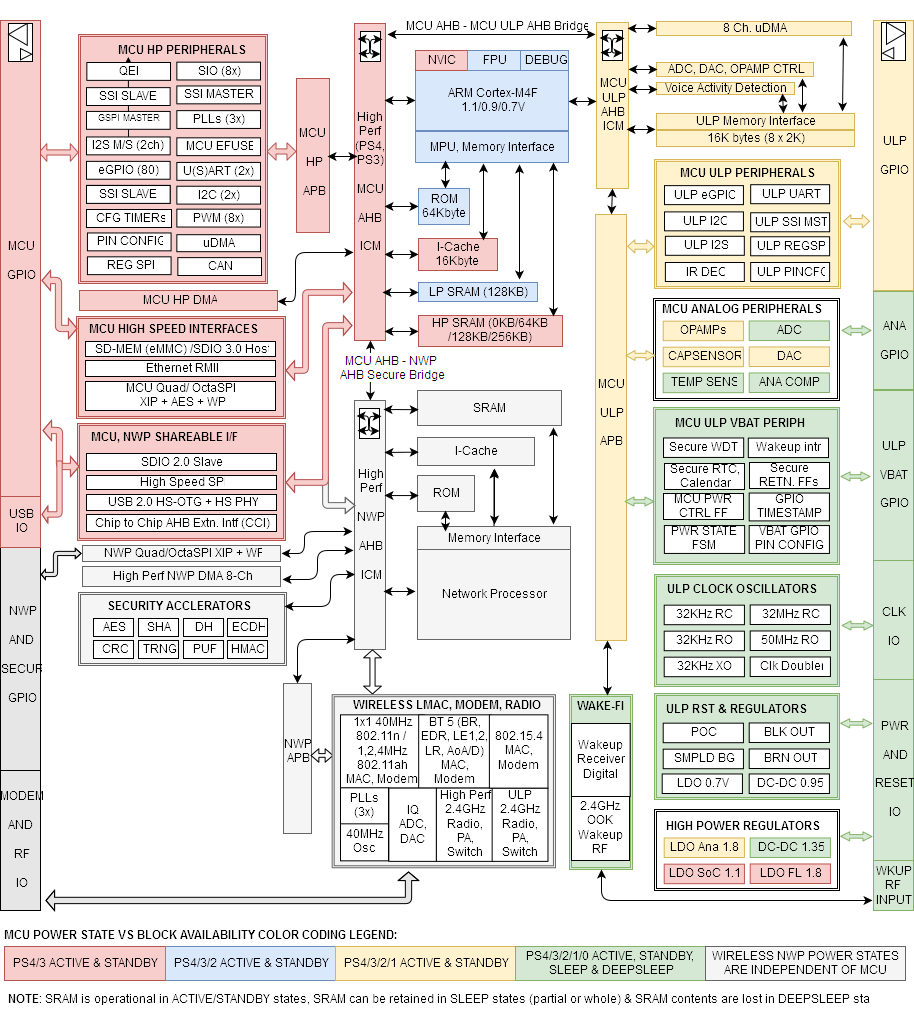


Figure 1: RS14100 System Block Diagram

# Block Descriptions

RS9116 includes two processors. An ARM Cortex-M4F running up to 180MHz and Redpine's ThreadArch 4-Threaded processor running up to 160MHz. The Cortex-M4 is dedicated for peripheral and application related processing whereas all the networking and wireless stacks run on independent threads of the ThreadArch. In addition, in adherence to the Trusted Execution Environment architecture - the ThreadArch subsystem also acts as the secure processing domain and takes care of secure boot, secures firmware upgrade and provides access to security accelerators and secure peripherals through pre-defined APIs. The bus matrices of Cortex-M4 and ThreadArch are separate and asynchronous. Though the two processors are present in a single chip - it is ensured that the ThreadArch based "Networking, Security and Wireless subsystem" is completely separated from the ARM Cortex-M4F based "Application subsystem". Thus, these two processors have separate power, separate clocks/PLLs, separate bus-matrices and independent memory. This provides two key advantages - programming, operating and power-state independence between the two processors and enhanced security by restricting access to the ThreadArch subsystem.

## ARM Cortex M4F

The ARM Cortex-M4F is the main application processor in RS9116. It is a high performance 32-bit processor designed by ARM for the micro-controller market. It is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division. The Cortex M4F microcontroller integrated in RS9116 supports the following features:

* MPU (Memory Protection Unit) with 8 memory regions, FPU (Floating Point Unit) and NVIC with 64 levels of interrupt priority.
* Debug port with both JTAG as well as Serial Wire interface. Comprehensive debug functionality including data matching for watch-point generation. Trace with ITM, TPIU, ETM and DWT triggers and counters. (Embedded Trace Buffer and HTM port not present.)
* To provide optimal power vs performance tradeoff, unique gear-shifting is available for the M4 that enables optimal power consumption based on the required performance. The available power-states are PS4 (at 1.1V): max 180MHz, PS3 (at 0.9V): max 100MHz, PS2 (at 0.7V): max 32MHz. More details are provided in the power-architecture section
* Architectural clock gates are included to minimize dynamic power dissipation.
* ThreadArch and M4 communicate through thread to thread interrupting and memory.
* On-chip SRAM of 144K/208K/272K/400Kbytes based on the RS9116 chip configuration
* Out of the above SRAM, 16Kbytes is present in the Ultra-low-power peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like VAD, FIM, ULP I2S, etc.
* 64Kbytes of ROM which holds the M4F peripheral drivers.
* 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with external quad/octa SPI SDR/DDR flashes.
* Based on the RS9116 package configuration up to 4MBytes of "in-package" Quad SPI flash is available for the M4
* eFuse of 64 bytes (available for customer applications)
* The ThreadArch processor has following memory:
* On-chip SRAM of 384K/256K/192K/128Kbytes based on RS9116 chip configuration
* 512Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
* 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with external quad/octa SPI SDR/DDR flashes.
* Based on the RS9116 package configuration up to 4MBytes of "in-package" Quad SPI flash is available for the ThreadArch
* eFuse of 512 bytes (used to store primary boot configuration, security and calibration parameters)
* No-Flash: Flash is not needed in devices where there is a host processor in the system that runs the network stack and wireless drivers.
* Single Flash used by M4: This is possible for non-Wi-Fi wireless MCUs (e.g., Wireless M4F MCU with BT 5)
* Single Flash used by TA: This is possible for Wireless MCUs where the MCU application code size is lesser than 128Kbytes (e.g., Wi-Fi + BT5 Sensor hub Wireless MCU)
* Two independent Flashes - one each for M4 and TA: This is needed for Wireless MCUs where Wi-Fi is needed and with MCU code size larger than 128KB.

## Interconnect

The following are the buses and bridges that form the interconnect in RS9116

* High Performance MCU AHB Interconnect Matrix (ICM)
* MCU AHB to APB dual bridge
* MCU AHB to ULP MCU AHB bridge
* ULP MCU AHB ICM
* ULP MCU AHB to APB bridge
* MCU AHB - NWP AHB bridge
* High Performance NWP AHB ICM
* NWP AHB to APB dual bridge
* High Performance MCU AHB Interconnect Matrix (ICM)
* The High Performance MCU AHB ICM is a multilayer interconnect implementation of the AHB protocol designed for higher performance and higher frequency systems. A 14 Master x 13 Slave AHB ICM is used. The next section shows the masters and slaves and the one after that shows the interconnect configuration / connections possible between masters and slaves. For further details like address mapping, please refer to the Hardware reference manual.

## Power

RS9116 achieves ultra low power without compromising on features that have been traditionally considered "power-hungry". Hierarchical partitioning and numerous system and circuit level innovations have been used to achieve ultra low power while retaining high performance capability. Unlike in GHz micro-processors, majority (>75%) of power consumption in traditional microcontrollers occurs outside the processor - typically in the bus-matrix, memory, PLLs, regulators and peripherals. On first look it would seem to be possible to have two processor cores (typically M4 and M0+) in an SoC to get power savings similar to those in microprocessors. But - without careful design, the gains in system power consumption would be incremental since the power is reduced in the processor alone. Additionally, software and development complexity is introduced with two cores due to inter-core communication, limitations in the instruction set of the smaller core and resulting code incompatibility and code redundancy. It is necessary in many applications to have the same code run in an ultra-low-power mode until the need for speed occurs. Also, it should be noted that "gear shifting" approach through dynamic voltage and frequency scaling (DVFS) alone doesn't achieve significant power savings. Through DVFS "and" careful optimization and hierarchical design for "all" components of the SoC, RS9116 achieves better power consumption using Cortex-M4F than typical off-the-shelf M0+ implementations. RS9116 can gear shift from 180MHz @ 36uA/MHz\*\* in PS4 down to 32MHz @ 12uA/MHz\*\* in PS2.

* Two integrated buck switching regulators (High performance and ULP) to enable efficient Dynamic Voltage Scaling across wide operating mode currents ranging from <1uA to 300mA
* High performance and ultra-low-power MCU peripheral subsystems and buses.
* Multiple voltage domains with Independent voltage scaling of each domain
* Fine grained power-gating including buses and pads.

## Digital and Analog Peripherals and Interfaces

In addition to the wireless interfaces, RS9116 provides a rich set of peripherals and interfaces - both digital and analog - thus enabling varied systems and applications. The following are the categories of the peripherals and interfaces, description of each category and list of the peripherals in that category:

### I2C

* Three speeds: Standard mode (100 Kb/s); Fast mode (400 Kb/s); High-speed mode (3.4 Mb/s)
* Clock synchronization
* Supports Master or slave I2C operation through software configuration
* 7- or 10-bit addressing
* 7- or 10-bit combined format transfers
* Bulk transmit mode
* Transmit and receive buffers
* Interrupt or polled-mode operation
* Handles Bit and Byte waiting at all bus speeds
* DMA handshaking interface
* Supports APB interface for programming and accessing data.

### UART

* Programmer interface compatible with the 16550A
* 5,6,7 and 8 bit character encoding
* even, odd and no parity
* 1, 1.5 (only with 5 bit character encoding) and 2 stop bits
* Auto flow control (RTS/CTS) as specified in 16750 standard
* Support for maximum FIFO depth of 16
* Programmable FIFO thresholds
* DMA handshake
* IrDA 1.0 SIR mode support with up to 115.2 K baud data rate and a pulse duration (width) as follows: width = 3/16 × bit period as specified in the IrDA physical layer specification (only for UART 2)
* IrDA 1.0 SIR low-power reception capabilities (only for UART 2)
* Use of two clocks (pclk,i.e. SoC clk and sclk-serial clk) instead of one (pclk)
* Support for dynamic clock gating on PCLK and SCLK
* Support from disabling dynamic clock gating
* Support for asynchronous clocking on UART side
* FIFO disable support
* Loopback mode that enables greater testing of Modem Control and Auto Flow Control features (Loopback support in IrDA SIR mode is available)
* Programmable baud rate as calculated by the following: baud rate = (serial clock frequency)/(16× divisor)

### USART

* Support both Synchronous and Asynchronous modes.
* Supports Full duplex and half duplex (single wire) mode of communication.
* Support all the baud rates available.
* Supports data buffering using FIFO implementation.
* Supports DMA and ADMA flow control.
* Supports apb interface for programming.
* Supports generation of interrupt for different events.

### I2S

* Philips Inter-IC sound Bus specifications compliant
* Support for one stereo channel in transmitter and one stereo channel in receiver
* Support asynchronous clocking of APB bus and I2S bus
* Supports master and slave Modes (configurable)
* Programmable resolution support(12 ,16, 20 and 24 bit resolutions)
* Support for FIFO(depth 8, one for each channel, four FIFOs are present)
* Programmable FIFO thresholds
* DMA handshake
* Programmable clock polarity and phases
* Static clock gating
* Multiple interrupts for transmit, receive data requests and for detecting error conditions
* Audio sampling rates supported are 8, 11.025, 16, 22.05, 24, 32 and 44.1kHz

### PCM

* The PCM interface works in slave mode which can transmit and receive serial data to and from an off-chip PCM master.
* Supports full-duplex data transfer with a PCM master.
* Supports 12, 16, 20 and 24-bit frame sizes.
* Data is driven at the rising edge of clock and sampled at the falling edge of clock.
* Maximum operating frequency is 24MHz.
* PCM Master/slave mode can be configured

### Quadrature Encoder Interface (QEI)

* Supports APB interface for programming.
* Tracks encoder wheel position.
* Increments/decrements depending on direction
* Programmable for 1x or 2x or 4x position counting
* Velocity capture using built-in timer
* Velocity compare function with "less than" interrupt
* Uses two 32-bit up/down position counters and one velocity counter
* Position compare registers with interrupts
* Supports position counter reset rollover/underflow or Index pulse
* Index counter for revolution counting
* Index compare register and with interrupts
* Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement
* Programmable synchronization logic on input signals
* Three input pins for two phase and one index pulse signals
* Logically swap A and B inputs
* Count error status bit
* Velocity capture using built-in timer.
* Velocity compare function with "less than" interrupt
* Accept decoded signal inputs (clock and direction) in timer mode

### SSI Slave

* The SSI slave can connect to any serial-master peripheral using one of the three interfaces: Motorola Serial Peripheral Interface (SPI), Texas Instruments Serial Protocol (SSP), National Semiconductor Microwire.
* DMA capable
* Independent masking of interrupts - Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow.
* Data Item size (4 to 16 bits) – Item size of each data transfer under the control of the programmer.
* Supported FIFO depth is 16 (Independent TX and RX fifos are present)
* Combined interrupt line for all interrupts
* APB clock and SSI serial clock are identical. SSI slave peripheral clock (ssi\_clk) should follow Fssi\_clk <= 4 × (maximum Fsclk\_in)

### SSI Master

* Supports 4 slaves
* Supports Motorola SPI, TI SSP and National semiconductors Micro wire protocols. Motorola SPI support directly available after reset
* DMA capable
* Clock polarity and phase zero immediately after reset
* Programmable receive sampling delay
* Slave select does not toggle in between data frames when programmed clock phase is zero.
* Supported FIFO depth is 16(Independent TX and RX FIFOs are present)
* Independent masking of interrupts - Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow.
* Combined interrupt line for all interrupts
* APB clock and SSI serial clock are asynchronous and independent
* Programmable division factor. Frequency of serial clock out = Frequency of ssi\_clk /divison factor. Where division factor = 0 to 65534.
* The max frequency of serial output clock is half the frequency of ssi\_clk.
* Supports single/dual/Quad mode

### SIO

* + Can be used to implement UART, I2C, I2S, SPI and CAN protocols.
  + Performs serial to parallel and parallel to serial conversion
  + Performs 1,2,4 and 8 bit shifts at desired edges
  + Performs edge and level detection on a single GPIO pin
  + Data \_in[0] is monitored
  + Rise and fall edges detected
  + Level 0 and level 1 detected
  + Generates a shift clock from 14-bit shift counter. The maximum frequency of the clock that can be generated is ½ of the input clock.
  + Generates directed and inverted versions of clock
  + Maintains a 32-bit shift register for shifting data
  + Maintains an buffer for buffering additional data
  + Shifts the data out and captures the input data at rising/falling edge of shift clock.
  + Clock used for shift operations can be internal counter clock or external clock coming in.
  + Clocks from 2 SIOs(4,5) can act as external clocks to other SIOs (except SIOs 4 and 5)
  + Clocks from 4 gpios(4,5,6,7) can act as external clocks to all SIOs.
  + The outputs of few SIOs(4,5,12,13) can act as qualifiers for other SIOs.
  + A few gpios(4,5,6,7) can act as qualifier for other SIOs.
  + SIOs can be concatenated to increase buffer size.
  + A few SIOs(6,7) provide OEN for other SIOs.
  + Maintains 8-bit position counter for tracking shift operations.
  + The number of bits pending in the shift register is determined by the position counter.
  + Position counter decrements with every shift edge and reaches zero subsequently
  + When the position counter reaches zero, data in the shift register is exchanged with the data in buffer.
  + Performs the operations based on qualifier-
  + Data shift operations are performed only when the qualifier is present
  + Qualifies clock with qualifier optionally
  + Detects a 32-bit pattern on the input pins
  + Provides DMA flow controls signals
  + Generates interrupts on shift, swap (position counter reaching zero), pattern match (supported by 0,1st ,2nd slices only), GPIO edge/level detection and underun/overrun.
  + Supports flow control mode in which operations and clock would be paused if data not available.
  + Delays the shift operation by one shift clock period if first data has to stay on the bus for a longer duration.
  + Supports loading and reading of shift data in reverse order. This feature is required for peripherals which transmit/receive MSB first.
  + Data position counter and shift counter can be read from the APB interface.
  + Data in shift registers will be repeated transferred to the stream(Self Loop Mechanism).
  + It supports APB interface to read and write the registers.
  + Provides the following programmability:
* Pin detection mode(EDGE/LEVEL detection)
* Number of bits to shift
* Posedge/Negedge clock selection for shifting
* Internal/External clock for shifting
* DMA flow control signal generation.
* Flow Control
* Delaying first shift by 1 clock edge
* Option to send inverted clock
* Option to qualify clock
* Option to use direct and inverted versions of qualifier for shift operations
* Pattern matching
* Programmable clock division factors(for loading to 14-bit shift counter)
* Programmable position counter (Initial value can be programmed different from the reload value. Useful for applications where different number of bits have to be shifted out during the initial phase and a fixed pattern later)
* Default value of clock out pin before initiating the shift operations
* Loading/reading the data in reverse order

### Capacitive Touch

* Capsensor has 8 input channels, 1 cap input and 1 resistor input. All the input channels are shared with GPIOs.
* Capacitive input and resistor input are connected to two GPIOs each.
* Has an option to use external reference instead of internal programmable reference.
* Programmable input clock source from the multiple available clocks in the chip
* Controls the rate of scanning for all sensors with configurable inter sensor scan ON time
* Supports both samples streaming and cumulative average mode
* Uses PWM for generating a measurement window for counting the raw sample counts
* Has 8 to 16 bit PWM resolution
* Has clock divider, which supports up to 256 division factor
* Has asynchronous FIFO size 64x16, with an interrupt raised after FIFO occupancy crosses the configurable threshold value
* DMA capable
* 8,16 and 32-bit pseudo-random number for generating two non overlapping streams with configurable delay
* Programmable polynomial and seed values for pseudo-random number generator
* Provides Wake up indication after capacitive touch sensing

### CAN

* Conforms to Bosch CAN 2.0B specification.
* 11 and 29 bit wide message identifiers
* Data rate up to 1Mbps
* Hardware message filtering (dual/single filters)
* 64-byte receive FIFO. 16-byte transmit buffer
* Overload frame is generated on FIFO overflow
* Normal & Listen Only modes supported
* Single Shot transmission
* Ability to abort transmission
* Readable error counters
* Last Error Code
* Programmable clock frequency

# RS14100 Pinout and Pin Description

## Module Packages

| **Pin Name** | **Pin # in**  **B00** | **Pin # in**  **CA0** | **Pin # in**  **CA1** | **Pin # in**  **CC0** | **Pin # in**  **CC1** | **Type** | **Description** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **RF and Control** |  |  |  |  |  |  |  |
| RESET\_N | TBD | K2 | 33 | K2 | 33 | AI | Active-low asynchronous reset signal. |
| TRST | TBD | H5 | NA | H5 | NA |  |  |
| RF\_OUT\_2 | TBD | N14 | NA | N14 | NA | RIO | Default Antenna port. |
| RF\_OUT\_1 | TBD | N12 | NA | N12 | NA | RIO | Second antenna port, if unused leave NC |
| POC\_IN | TBD | H1 | 30 | H1 | 30 | P | Power On Control Input. Connected to external POC for bypass. |
| POC\_OUT | TBD | J2 | 84 | J2 | 84 | P | Power On Control Output |
| **Power and Ground** | | | | | | | |
| MOD\_VDD | TBD | A1 | 21 | A1 | 21 | P | Module power supply |
| AVDD | TBD | NA | TBD | NA | TBD | P | Analog power supply |
| SDIO\_IO\_VDD | TBD | B9 | 8 | B9 | 8 | P | SDIO power supply |
| VBATT | TBD | NA | NA | NA | NA | P | Battery power supply. |
| UULP\_VBATT | TBD | D5 | NA | D5 | NA | P | Battery power supply. |
| UULP\_VBATT\_2 | TBD | D4 | NA | D4 | NA | P | Battery power supply. |
| UULP\_VOUTSCDC | TBD | D3 | 79 | D3 | 79 | P |  |
| RF\_VDD | TBD | E9 | NA | E9 | NA | P | 3.3V RF Analog power supply |
| BTTX\_VDD | TBD | NA | TBD | NA | TBD | NA | NA |
| VDD | TBD | B4 | 71 | B4 | 71 | P | RF Digital power supply |
| ANA1\_VDD | TBD | NA | TBD | NA | TBD | P | USB Mode: Connect to USB\_AVDD\_1P1 |
| NC | Other Modes: Reserved – leave  unconnected. |
| USB\_AVDD | TBD | B7 | 66 | B7 | 66 | P | USB Mode: Power Supply. |
| NC | Other Modes: Reserved – leave  unconnected. |
| USB1P1\_AVDD | TBD | A5 | 11 | A5 | 11 | P | USB Mode: Connect to ANA1V1 |
| GND | Other Modes: Connect to Ground. |
| GND | TBD | B1, B13, C4, D8, F2, F6, F10, F11, F12, F13, G8, G10, G11, G12, G13, G14, H6, H9, H11, H12, H13, H14, J4, J6, J8, J9, J10, J11, J12, J13, J14, K1, K4, K5, K6, K8, K9, K10, K11, K12, L1, L2, L3, L4, L6, L9, L10, L11, L12, L13, M1, M2, M3, M9, M10, M11, M12, M13, N1, N2, N11, N13 | 12, 36, 41, 49, 50, 51, 52, 53, 54, 55, 56, 13, 57, 68, 69, 70, 72, 73, 87, 88, 89, 93, 14, 97, 99, 100, 101, 102, 103, 104, 105, 106, 107, 15, 112, 113, 114, 115, 120, 121, 122, 123, 1, 127, 74, 128, 129, 130, 131, 136, 137, 138, 139, 144, 145, 17, 146, 147, 153, 154, 155, 19, 34, 35 | B1, B13, C4, D8, F2, F6, F10, F11, F12, F13, G8, G10, G11, G12, G13, G14, H6, H9, H11, H12, H13, H14, J4, J6, J8, J9, J10, J11, J12, J13, J14, K1, K4, K5, K6, K8, K9, K10, K11, K12, L1, L2, L3, L4, L6, L9, L10, L11, L12, L13, M1, M2, M3, M9, M10, M11, M12, M13, N1, N2, N11, N13 | 12, 36, 41, 49, 50, 51, 52, 53, 54, 55, 56, 13, 57, 68, 69, 70, 72, 73, 87, 88, 89, 93, 14, 97, 99, 100, 101, 102, 103, 104, 105, 106, 107, 15, 112, 113, 114, 115, 120, 121, 122, 123, 1, 127, 74, 128, 129, 130, 131, 136, 137, 138, 139, 144, 145, 17, 146, 147, 153, 154, 155, 19, 34, 35 | GND | Common Ground |
| C1P1\_VDD | TBD | NA | NA | NA | NA | P | 1.1V Power to Digital Core |
| RF\_AGND | TBD | NA | NA | NA | NA | GND | RF and AFE Ground |
| IO\_VDD\_1 | TBD | NA | NA | NA | NA | P | IO Supply for GPIOs. |
| IO\_VDD\_2 | TBD | NA | NA | NA | NA | P | IO Supply for GPIOs. (1.8-3.6V) |
| IO\_VDD\_3 | TBD | NA | NA | NA | NA | P |  |
| RF\_VBATT | TBD | F7 | NA | F7 | NA | P | VBAT Power Supply to RF and AFE (1.8-3.6V) |
| AFELDO\_VOUT\_BTTX | TBD | H10 | 48 | H10 | 48 |  |  |
| AFELDO\_VOUT | TBD | H8 | 98 | H8 | 98 |  |  |
| RFLDO\_AVDD\_OUT | TBD | G7 | 46 | G7 | 46 | P |  |
| DGND | TBD | NA | TBD | NA | TBD | GND |  |
| RF\_AVDD | TBD | D10 | NA | D10 | TBD | P |  |
| RF\_AVDD1 | TBD | K3 | 86 | K3 | 86 | P |  |
| BCK\_VIN | TBD | NA | NA | NA | TBD | P | Buck Input (1.8-3.6V) |
| SOC\_LDO\_VOUT | TBD | A3 | 16 | A3 | 16 | P | LDO SoC Output (1.1V) |
| SOC\_LDO\_VIN | TBD | A4 | NA | A4 | NA | P | Power Supply for LDO SoC |
| BCK\_VOUT | TBD | C5 | TBD | C5 | TBD | P | Buck Output 1.35V |
| PMU\_AGND | TBD | NA | NA | NA | NA | GND |  |
| RF\_LDO\_VOUT | TBD | NA | NA | NA | NA | P | LDO RF Output (1.8-3.6V) |
| BCK\_GND | TBD | NA | NA | NA | NA | GND | Buck Ground |
|  | TBD |  |  |  |  |  |  |
| PLL\_AVDD | TBD | NA | NA | NA | NA | P | PLL Power Supply input |
| PMU\_AVDD | TBD | NA | NA | NA | NA | P | PMU Power Supply input |
| QSPI\_IO\_VDD | TBD | NA | NA | NA | NA | P | IO Supply for QSPI GPIOs. (1.8-3.6V) |
| ULP\_IO\_VDD | TBD | B6 | 116 | B6 | 116 | P |  |
| RF\_LDO\_VDD | TBD | NA | NA | NA | NA | P | Power Supply for LDO RF (1.8-3.6V) |
| **ULP GPIOs** | | | | | | | |
| ULP\_GPIO\_0 | TBD | D1 | 25 | D1 | 25 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_1 | TBD | B2 | 76 | B2 | 76 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_11 | TBD | J1 | 31 | J1 | 31 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_2 | TBD | E4 | 23 | E4 | 23 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_3 | TBD | E3 | 22 | E3 | 22 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_4 | TBD | F1 | 26 | F1 | 26 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_5 | TBD | H4 | 90 | H4 | 90 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_6 | TBD | E6 | 20 | E6 | 20 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_7 | TBD | F3 | 24 | F3 | 24 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_8 | TBD | E2 | 80 | E2 | 80 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_9 | TBD | E5 | 91 | E5 | 91 | DIO | Ultra Low Power General Purpose I/O |
| ULP\_GPIO\_10 | TBD | G3 | 42 | G3 | 42 | DIO | Ultra Low Power General Purpose I/O |
| UULP\_VBATT\_GPIO\_0 | TBD | H2 | 83 | H2 | 83 | DIO | Ultra Low Power General Purpose I/O |
| UULP\_VBATT\_GPIO\_2 | TBD | H3 | 92 | H3 | 92 | DIO | Ultra Low Power General Purpose I/O |
| UULP\_VBATT\_GPIO\_3 | TBD | E10 | 43 | E10 | 43 | DIO | Ultra Low Power General Purpose I/O |
| UULP\_VBATT\_GPIO\_4 | TBD | F14 | 152 | F14 | 152 | DIO | Ultra Low Power General Purpose I/O |
| **Miscellaneous** | | | | | | | |
| WURX | TBD | C3 | 18 | C3 | 18 | RF | 2.4GHz Wakeup receiver RF input |
| XTAL\_32KHZ\_N | TBD | C7 | 117 | C7 | 117 | OSC | XTAL 32KHz N |
| XTAL\_32KHZ\_P | TBD | C8 | 125 | C8 | 125 | OSC | XTAL32KHz P |
| XTAL\_IN | TBD | NA | NA | NA | NA | OSC | XTAL P |
| XTAL\_OUT | TBD | NA | NA | NA | NA | OSC | XTAL N |
| TCK | TBD | G4 | 29 | G4 | 29 | DI | Reserved – connect a 4.7 k pull-down resistor. |
| TMS | TBD | G5 | 111 | G5 | 111 | DIO | Reserved – connect a 4.7 k pull-down resistor. |
| TDO | TBD | F5 | 110 | F5 | 110 | DO | Reserved – leave unconnected. |
| TDI | TBD | F4 | 82 | F4 | 82 | DI | Reserved – connect a 4.7 k pull-down resistor. |
| **General Purpose IOs** | | | | | | | |
| GPIO\_6 | TBD | E14 | 150 | E14 | 150 | DIO | General Purpose I/O |
| GPIO\_7 | TBD | D9 | 119 | D9 | 119 | DIO | General Purpose I/O |
| GPIO\_8 | TBD | C9 | 135 | C9 | 135 | DIO | General Purpose I/O |
| GPIO\_9 | TBD | E13 | 151 | E13 | 151 | DIO | General Purpose I/O |
| GPIO\_10 | TBD | E12 | 142 | E12 | 142 | DIO | General Purpose I/O |
| GPIO\_11 | TBD | A14 | 149 | A14 | 149 | DIO | General Purpose I/O |
| GPIO\_12 | TBD | E11 | 143 | E11 | 143 | DIO | General Purpose I/O |
| GPIO\_13 | TBD | E7 | 118 | E7 | 118 | DIO | General Purpose I/O |
| GPIO\_14 | TBD | G6 | 32 | G6 | 32 | DIO | General Purpose I/O |
| GPIO\_15 | TBD | A12 | 61 | A12 | 61 | DIO | General Purpose I/O |
| GPIO\_16 | TBD | A13 | 148 | A13 | 148 | DIO | General Purpose I/O |
| GPIO\_31 | TBD | G4 | 29 | G4 | 29 | DIO | General Purpose I/O |
| GPIO\_32 | TBD | G5 | 111 | G5 | 111 | DIO | General Purpose I/O |
| GPIO\_33 | TBD | F4 | 82 | F4 | 82 | DIO | General Purpose I/O |
| GPIO\_34 | TBD | F5 | 110 | F5 | 110 | DIO | General Purpose I/O |
| GPIO\_46 | TBD | D14 | 59 | D14 | 59 | DIO | General Purpose I/O |
| GPIO\_47 | TBD | C13 | 4 | C13 | 4 | DIO | General Purpose I/O |
| GPIO\_48 | TBD | D12 | 60 | D12 | 60 | DIO | General Purpose I/O |
| GPIO\_49 | TBD | D13 | 3 | D13 | 3 | DIO | General Purpose I/O |
| GPIO\_50 | TBD | B14 | 58 | B14 | 58 | DIO | General Purpose I/O |
| GPIO\_51 | TBD | C14 | 2 | C14 | 2 | DIO | General Purpose I/O |
| GPIO\_52 | TBD | C11 | 141 | C11 | 141 | DIO | General Purpose I/O |
| GPIO\_53 | TBD | D11 | 134 | D11 | 134 | DIO | General Purpose I/O |
| GPIO\_54 | TBD | B12 | 140 | B12 | 140 | DIO | General Purpose I/O |
| GPIO\_55 | TBD | C12 | 133 | C12 | 133 | DIO | General Purpose I/O |
| GPIO\_56 | TBD | B11 | 132 | B11 | 132 | DIO | General Purpose I/O |
| GPIO\_57 | TBD | C10 | 124 | C10 | 124 | DIO | General Purpose I/O |

Table 3: Module Pin Descriptions

## Chip Packages

| **Pin Name** | **Pin # in QMS** | **Pin # in WMS** | **Pin # in BTS** | **Type** | **Description** |
| --- | --- | --- | --- | --- | --- |
| **RF and Control** |  |  |  |  |  |
| RESET\_N\_PAD | A31 | M3 | TBD | AI | Active-low asynchronous reset signal. |
| RF\_BTTX | A11 |  | TBD | RO | BT 10dBm RF output |
| RF\_RX | A10 | R10 | TBD | RI | 2.4GHz RF Input |
| RF\_TX | A9 | N8 | TBD | RO | 2.4GHz RF Output |
| RF\_VBATT | A12 | R8 | TBD | P | VBAT Power Supply to RF and AFE |
| TRST | A15 | U4 | TBD | DIO | TRST |
| WURX | B27 | E2 | TBD | RI | 2.4GHz Wakeup receiver RF input |
| XTAL\_32KHZ\_N | B26 | L2 | TBD | OSC | XTAL 32KHz N |
| XTAL\_32KHZ\_P | A29 | K3 | TBD | OSC | XTAL 32KHz P |
| XTAL\_IN | B12 | U8 | TBD | OSC | XTAL P |
| XTAL\_OUT | A13 | U6 | TBD | OSC | XTAL N |
| FLY\_N1 | A32 | J2 | TBD | DIO | Flyback Capacitor for Switched cap DCDC |
| FLY\_P1 | B28 | F3 | TBD | DIO | Flyback Capacitor for Switched cap DCDC |
| RF\_AGND |  | M9,U10 | TBD | GND | RF Ground |
| **Power and Ground** |  |  | TBD |  |  |
| RF\_AVDD\_1 | A8 | NA | TBD | PI | RF and AFE Analog Power Supply |
| RF\_AVDD\_2 | B11 | NA | TBD | PI | RF and AFE Analog Power Supply |
| RF\_AVDD\_3 | A14 | NA | TBD | PI | RF and AFE Analog Power Supply |
| POC\_IN | A27 | NA | TBD | PI | Power On Control Input |
| POC\_OUT | B25 | NA | TBD | PO | Power On Control Output |
| AUX\_AVDD | B34 | E4 | TBD | PO | Analog Peripherals LDO Output |
| C\_VDD | A18 | E8 | TBD | PI | 1.1V Power to Digital Core |
| C\_VDD | B2 | H5 | TBD | PI | 1.1V Power to Digital Core |
| C\_VDD | B38 | U2 | TBD | PI | 1.1V Power to Digital Core |
| IO\_VDD\_1 | A3 | G6 | TBD | PI | IO GPIO Power Supply |
| IO\_VDD\_2 | B14 | NA | TBD | PI | IO GPIO Power Supply |
| PA\_AVDD | B8 | N10 | TBD | PI | PA Power Supply |
| QSPI\_IO\_VDD | A2 | NA | TBD | PI | QSPI GPIO Power Supply |
| SDIO\_IO\_VDD | B1 | A10 | TBD | PI | SDIO GPIO Power Supply |
| ULP\_IO\_VDD | B33 | A6 | TBD | PI | ULP GPIO Power Supply |
| USB\_AVDD\_1P1 | B35 | NA | TBD | PI | 1.1V USB Core Power Supply |
| USB\_AVDD\_3P3 | A39 | NA | TBD | PI | 3.3V USB Analog Power Supply |
| USB\_VBUS | A38 | NA | TBD | PI | 5V USB Bus Supply |
| UULP\_VBATT\_AVDD\_2 | A30 | NA | TBD | PI | UULP VBAT IO GPIO Power Supply |
| UULP\_VBATT | A26 | K1 | TBD | PI | UULP VBAT IO GPIO Power Supply |
| UULP\_VOUTSCDC | B23 | F1 | TBD | PO | 1V UULP Switched Cap DC-DC Output |
| UULP\_VOUTSCDC\_RETN | A28 | M1 | TBD | PO | UULP Retention Supply Output |
| VINBCKDC | A33 | B1 | TBD | PI | Buck Power Supply |
| VINLDORF | B31 | NA | TBD | PI | RF LDO Power Supply |
| VINLDOSOC | B30 | D3 | TBD | PI | SoC LDO Power Supply |
| VOUTBCKDC | B29 | C2 | TBD | PO | Buck Power Supply Output |
| VOUTLDOAFE | B13 | R6 | TBD | PO | AFE LDO Power Supply Output |
| VOUTLDORF | B32 | B3 | TBD | PO | RF LDO Power Supply Output |
| VOUTLDOSOC | A34 | A2 | TBD | PO | SoC LDO Power Supply Output |
| DGND |  | P3,F9,K5 | TBD | GD | Digital Ground |
| AGND |  | H1,G2 | TBD | GND | Analog Ground |
| **Host Interfaces and GPIOs** |  |  | TBD |  |  |
| USB\_DM | A40 | NA | TBD | DIO | USB D- Signal |
| USB\_DP | B36 | NA | TBD | DIO | USB D+ Signal |
| USB\_ID | A37 | NA | TBD | DI | USB Mini- Receptacle Identifier |
| USB\_TXRTUNE | B37 | NA | TBD | DO | USB Transmitter Resistance Tune |
| GPIO\_10 | B3 | G8 | TBD | DIO | General Purpose Input/Output |
| GPIO\_11 | B4 | J10 | TBD | DIO | General Purpose Input/Output |
| GPIO\_12 | A4 | H7 | TBD | DIO | General Purpose Input/Output |
| GPIO\_15 | A41 | B7 | TBD | DIO | General Purpose Input/Output |
| GPIO\_25 | B40 | B9 | TBD | DIO | General Purpose Input/Output |
| GPIO\_26 | A1 | E10 | TBD | DIO | General Purpose Input/Output |
| GPIO\_27 | B39 | D9 | TBD | DIO | General Purpose Input/Output |
| GPIO\_28 | A44 | C8 | TBD | IO | General Purpose Input/Output |
| GPIO\_29 | A43 | D7 | TBD | DIO | General Purpose Input/Output |
| GPIO\_30 | A42 | A8 | TBD | DIO | General Purpose Input/Output |
| GPIO\_31 | A17 | T3 | TBD | DIO | General Purpose Input/Output |
| GPIO\_32 | B16 | R4 | TBD | DIO | General Purpose Input/Output |
| GPIO\_33 | A16 | P5 | TBD | DIO | General Purpose Input/Output |
| GPIO\_34 | B15 | T5 | TBD | DIO | General Purpose Input/Output |
| GPIO\_46 | A5 | J6 | TBD | DIO | General Purpose Input/Output |
| GPIO\_47 | A7 | M5 | TBD | DIO | General Purpose Input/Output |
| GPIO\_48 | B7 | L6 | TBD | DIO | General Purpose Input/Output |
| GPIO\_49 | B6 | K7 | TBD | DIO | General Purpose Input/Output |
| GPIO\_50 | A6 | N4 | TBD | DIO | General Purpose Input/Output |
| GPIO\_51 | B5 | J8 | TBD | DIO | General Purpose Input/Output |
| GPIO\_6 | B20 | G10 | TBD | DIO | General Purpose Input/Output |
| GPIO\_7 | B19 | E6 | TBD | DIO | General Purpose Input/Output |
| GPIO\_8 | A20 | F7 | TBD | DIO | General Purpose Input/Output |
| GPIO\_9 | A21 | H9 | TBD | DIO | General Purpose Input/Output |
| ULP\_GPIO\_0 | A35 | NA | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_1 | B22 | NA | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_10 | A23 | L4 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_11 | B17 | A4 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_4 | B21 | D5 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_5 | A19 | F5 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_6 | A22 | B5 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_7 | B18 | C6 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_8 | A36 | G4 | TBD | DIO | Ultra Low Power GPIO |
| ULP\_GPIO\_9 | A24 | J4 | TBD | DIO | Ultra Low Power GPIO |
| UULP\_VBAT\_GPIO\_0 | B10 | N2 | TBD | DIO | Ultra Low Power GPIO |
| UULP\_VBAT\_GPIO\_2 | B24 | R2 | TBD | DIO | Ultra Low Power GPIO |
| UULP\_VBAT\_GPIO\_3 | A25 | P1 | TBD | DIO | Ultra Low Power GPIO |

Table 4: Chip Pin Descriptions

### GPIO

#### GPIO Pin Multiplexing

The SoC GPIOs below (GPIO\_6 to GPIO\_57) are available in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by a 4-bit GPIO Mode register.

| **GPIO** | **GPIO Mode**  **= 0** | **GPIO Mode**  **= 1** | **GPIO Mode**  **=2** | **GPIO Mode**  **= 3** | **GPIO Mode**  **= 4** | **GPIO Mode**  **= 5** | **GPIO Mode**  **= 6** | **GPIO Mode**  **= 7** | **GPIO Mode**  **= 8** | **GPIO**  **Mode**  **= 9** | **GPIO Mode**  **= 10** | **GPIO**  **Mode**  **= 14** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| GPIO\_6 | GPIO\_6 | SIO\_0 | UART2\_TX | SSI\_MST\_DATA0 | I2C1\_SDA | I2S\_2CH\_DOUT\_0 | SCT\_OUT\_0 | QEI\_IDX | M4SS\_SMIH\_CD\_N | CCI\_DATA\_4 | M4SS\_QSPI\_CLK | RMII\_TXD1 |
| GPIO\_7 | GPIO\_7 | SIO\_1 | UART2\_RX | SSI\_MST\_DATA1 | I2C1\_SCL | I2S\_2CH\_CLK | SCT\_OUT\_1 | QEI\_PHB | M4SS\_SMIH\_WP | CCI\_DATA\_5 | M4SS\_QSPI\_CSN0 | RMII\_TXD0 |
| GPIO\_8 | GPIO\_8 | SIO\_2 | USART1\_RX | SSI\_MST\_CLK | PLL\_TESTMODE\_SIG | PMU\_TEST\_1 | SCT\_OUT\_2 | QEI\_PHA | PWM\_1L | CCI\_DATA\_6 | M4SS\_QSPI\_D0 | RMII\_REF\_CLK |
| GPIO\_9 | GPIO\_9 | SIO\_3 | USART1\_TX | SSI\_MST\_CS0 | PMU\_TEST\_2 | SDMEM\_PRESENT | SCT\_OUT\_3 | QEI\_DIR | PWM\_1H | CCI\_DATA\_7 | M4SS\_QSPI\_D1 | RMII\_TXEN |
| GPIO\_10 | GPIO\_10 | USART1\_IR\_TX | USART1\_CLK | SSI\_MST\_CS1 | I2C2\_SCL | I2S\_2CH\_DIN\_0 | SCT\_OUT\_4 | RMII\_RXD1 | PWM\_2H | CCI\_CLK | M4SS\_QSPI\_D2 | SSI\_SLV\_CS |
| GPIO\_11 | GPIO\_11 | SIO\_5 | USB\_DRVVBUS | SSI\_MST\_CLK | I2C2\_SDA | I2S\_2CH\_WS | SCT\_OUT\_5 | RMII\_MDC | PWM\_2L | CCI\_CS[0] | M4SS\_QSPI\_D3 | SSI\_SLV\_CLK |
| GPIO\_12 | GPIO\_12 | USART1\_IR\_RX | UART2\_TX | SSI\_MST\_DATA0 | I2C1\_SCL | USART1\_RTS | SCT\_OUT\_6 | RMII\_MDO | SCT\_IN\_0 | CCI\_DATA\_0 | MCU\_CLK\_OUT | SSI\_SLV\_MISO |
| GPIO\_13 | GPIO\_13 | SIO\_7 | USART1\_TX | GSPI\_MST1\_MOSI | USB\_XTAL\_ON | SCT\_IN\_1 | XTAL\_ON\_IN | RMII\_REF\_CLK | PWM\_3L | CCI\_DATA\_4 | CCI\_DATA\_1 |  |
| GPIO\_14 | GPIO\_14 | ULP\_GPIO\_7 | USART1\_RX | GSPI\_MST1\_MISO | SCT\_IN\_2 | USB\_DRVVBUS | SCT\_OUT\_0 | RMII\_CRS\_DV | PWM\_3H | CCI\_DATA\_5 | CCI\_DATA\_2 |  |
| GPIO\_15 | GPIO\_15 | MCU\_CLK\_OUT | UART2\_RX | SSI\_MST\_DATA1 | I2C1\_SDA | USART1\_CTS | SCT\_OUT\_7 | RMII\_RXD0 | GSPI\_MST1\_CLK | CCI\_DATA\_6 | CCI\_DATA\_3 | SSI\_SLV\_MOSI |
| GPIO\_16 | GPIO\_16 | SIO\_4 | USB\_DRVVBUS | SSI\_MST\_CS0 | CAN1\_RXD | GSPI\_MST1\_CS0 | I2S\_2CH\_WS | XTAL\_ON\_IN | SSI\_SLV\_CS | CCI\_DATA\_0 | ULP\_GPIO\_1 | RMII\_CRS\_DV |
| GPIO\_17 | GPIO\_17 | SIO\_5 | USB\_XTAL\_ON | SSI\_MST\_CS1 | CAN1\_TXD | GSPI\_MST1\_CLK | I2S\_2CH\_CLK | SCT\_IN\_0 | SSI\_SLV\_CLK | CCI\_INTR[0] |  |  |
| GPIO\_18 | GPIO\_18 | SIO\_6 | USART1\_RTS | SSI\_MST\_DATA2 | I2C2\_SDA | GSPI\_MST1\_MOSI | I2S\_2CH\_DOUT\_1 | SSI\_SLV\_MOSI | USART1\_TX | PWM\_1H |  |  |
| GPIO\_19 | GPIO\_19 | SIO\_7 | USART1\_CTS | SSI\_MST\_DATA3 |  | GSPI\_MST1\_MISO | I2S\_2CH\_DIN\_1 | SSI\_SLV\_MISO | USART1\_RX | PWM\_1L | SCT\_OUT\_0 |  |
| GPIO\_20 | GPIO\_20 |  | USB\_CDC | SSI\_MST\_CS2 | I2C2\_SCL | GSPI\_MST1\_CLK |  | XTAL\_ON\_IN | USART1\_CLK | PWM\_2L | SCT\_OUT\_0 |  |
| GPIO\_21 | GPIO\_21 |  | USART1\_RTS | GSPI\_MST1\_CS0 | SCT\_IN\_0 | USB\_XTAL\_ON | ULP\_GPIO\_8 | PWM\_SLP\_EVENT\_TRIG | M4SS\_SMIH\_D4 | CCI\_CLK |  |  |
| GPIO\_22 | GPIO\_22 |  | USART1\_CTS | SOC\_PLL\_CLOCK | SCT\_IN\_1 | USB\_DRVVBUS | ULP\_GPIO\_9 | PWM\_FAULTA | M4SS\_SMIH\_D5 | CCI\_CS[0] |  |  |
| GPIO\_23 | GPIO\_23 | SIO\_2 |  | SSI\_MST\_CS3 | SCT\_IN\_2 | I2S\_2CH\_DIN\_1 | ULP\_GPIO\_10 | PWM\_FAULTB | M4SS\_SMIH\_D6 | CCI\_RDY[0] |  | Analog Function |
| GPIO\_24 | GPIO\_24 |  |  |  | SCT\_IN\_3 | I2S\_2CH\_DOUT\_1 | ULP\_GPIO\_11 |  | M4SS\_SMIH\_D7 | CCI\_DATA\_VALID |  | Analog Function |
| GPIO\_25 | GPIO\_25 | SIO\_4 | USART1\_CLK | SSI\_MST\_CLK | I2C1\_SCL | RMII\_TXD1 | SCT\_IN\_2 | SCT\_OUT\_0 | M4SS\_SMIH\_CLK | UART2\_TX | PMU\_TEST\_1 | Analog Function |
| GPIO\_26 | GPIO\_26 | SIO\_5 | USART1\_TX | SSI\_MST\_DATA0 | I2C1\_SDA | RMII\_TXD0 | SCT\_IN\_3 | SCT\_OUT\_1 | M4SS\_SMIH\_CMD | UART2\_RX | PMU\_TEST\_2 | Analog Function |
| GPIO\_27 | GPIO\_27 | SIO\_6 | USART1\_RX | SSI\_MST\_DATA1 | GSPI\_MST1\_CS0 | I2S\_2CH\_WS | SCT\_IN\_4 | USART1\_RTS | M4SS\_SMIH\_D0 | SSI\_SLV\_CS | QEI\_IDX | Analog Function |
| GPIO\_28 | GPIO\_28 | SIO\_7 | USART1\_CLK | SSI\_MST\_CS0 | GSPI\_MST1\_CLK | I2S\_2CH\_CLK | I2C2\_SCL | USART1\_CTS | M4SS\_SMIH\_D1 | SSI\_SLV\_CLK | QEI\_PHB | Analog Function |
| GPIO\_29 | GPIO\_29 | CAN1\_RXD | USART1\_RX | SSI\_MST\_CS1 | GSPI\_MST1\_MISO | I2S\_2CH\_DIN\_0 | I2C2\_SDA | SCT\_OUT\_2 | M4SS\_SMIH\_D2 | SSI\_SLV\_MOSI | QEI\_PHA | Analog Function |
| GPIO\_30 | GPIO\_30 | CAN1\_TXD | USART1\_TX | SSI\_MST\_CS2 | GSPI\_MST1\_MOSI | I2S\_2CH\_DOUT\_0 | RMII\_TXEN | SCT\_OUT\_4 | M4SS\_SMIH\_D3 | SSI\_SLV\_MISO | QEI\_DIR | Analog Function |
| GPIO\_31 | GPIO\_31 |  |  |  |  |  | SCT\_OUT\_4 | QEI\_PHA | PWM\_4L |  |  |  |
| GPIO\_32 | GPIO\_32 |  |  |  |  |  | SCT\_OUT\_5 | QEI\_PHB | PWM\_4H |  |  |  |
| GPIO\_33 | GPIO\_33 |  |  |  |  |  |  |  |  |  |  |  |
| GPIO\_34 | GPIO\_34 |  |  |  |  |  |  |  |  |  |  |  |
| GPIO\_35 | GPIO\_35 | SIO\_0 | REF\_CLK\_OUT | SSI\_MST\_CLK | SSI\_MST\_CS2 | I2C2\_SCL | SCT\_IN\_3 | RMII\_TXD1 | PWM\_4L | CCI\_RDY[0] | QEI\_PHA |  |
| GPIO\_36 | GPIO\_36 | SIO\_1 | UART2\_TX | SSI\_MST\_DATA0 | M4SS\_SMIH\_WP | I2C2\_SDA | SCT\_OUT\_5 | RMII\_TXD0 | PWM\_4H | CCI\_DATA\_VALID | QEI\_PHB |  |
| GPIO\_37 | GPIO\_37 | XTAL\_ON\_IN | UART2\_RX | SSI\_MST\_DATA1 | CCI\_INTR[0] | M4SS\_SMIH\_CD\_N | SCT\_OUT\_5 | RMII\_TXEN | PWM\_3L | CCI\_DATA\_0 | QEI\_IDX |  |
| GPIO\_38 | GPIO\_38 | RF\_REF\_CLK\_OUT | UART2\_CTS | SDMEM\_PRESENT | MEMS\_REF\_CLOCK |  | ULP\_GPIO\_12 |  | PWM\_3L | CCI\_DATA\_7 | PWM\_TMR\_EXT\_TRIG\_1 |  |
| GPIO\_39 | GPIO\_39 | XTAL\_ON\_IN | UART2\_RTS |  | USB\_PLL\_CLOCK |  | ULP\_GPIO\_13 | PWM\_TMR\_EXT\_TRIG\_2 | PWM\_3H | CCI\_DATA\_1 |  |  |
| GPIO\_40 | GPIO\_40 |  |  |  | I2S\_PLL\_CLOCK | I2C2\_SCL | ULP\_GPIO\_14 | PWM\_TMR\_EXT\_TRIG\_3 | PWM\_4L | CCI\_DATA\_2 |  |  |
| GPIO\_41 | GPIO\_41 |  |  |  | INTERFACE\_PLL\_CLOCK | I2C2\_SDA | ULP\_GPIO\_15 | PWM\_TMR\_EXT\_TRIG\_4 | PWM\_4H | CCI\_DATA\_3 |  |  |
| GPIO\_42 | GPIO\_42 |  | CCI\_DATA\_4 |  | I2S\_2CH\_CLK | SSI\_MST\_CS0 | SCT\_IN\_4 | GSPI\_MST1\_CS0 | PWM\_1L |  |  |  |
| GPIO\_43 | GPIO\_43 |  | CCI\_DATA\_5 | UART2\_RS485\_EN | I2S\_2CH\_WS | SSI\_MST\_CS1 | SCT\_IN\_5 | GSPI\_MST1\_CS1 | PWM\_1H | USB\_XTAL\_ON |  |  |
| GPIO\_44 | GPIO\_44 |  | CCI\_DATA\_6 | UART2\_RS485\_RE | I2S\_2CH\_DIN\_0 | SSI\_MST\_CS2 | SCT\_IN\_6 | GSPI\_MST1\_CS2 | PWM\_2L | USB\_DRVVBUS |  |  |
| GPIO\_45 | GPIO\_45 |  | CCI\_DATA\_0 | UART2\_RS485\_DE | I2S\_2CH\_DOUT\_0 | SSI\_MST\_CS3 | SCT\_IN\_7 | GSPI\_MST1\_CS3 | PWM\_2H |  |  |  |
| GPIO\_46 | GPIO\_46 | CAN1\_RXD | UART2\_RX | ULP\_GPIO\_12 | GSPI\_MST1\_CS3 | USART1\_DSR | SCT\_OUT\_2 | I2S\_2CH\_DIN\_1 | M4SS\_SMIH\_CLK | CCI\_INTR[1] | M4SS\_QSPI\_CLK |  |
| GPIO\_47 | GPIO\_47 | CAN1\_TXD | UART2\_TX | SSI\_MST\_CS3 | GSPI\_MST1\_CS2 | USART1\_DCD | SCT\_OUT\_3 | I2S\_2CH\_DOUT\_1 | M4SS\_SMIH\_CMD | CCI\_RDY[0] | M4SS\_QSPI\_D0 |  |
| GPIO\_48 | GPIO\_48 | SIO\_0 | ULP\_GPIO\_0 | SSI\_MST\_CS2 | UART2\_RS485\_EN | USART1\_DTR | SCT\_OUT\_4 | I2S\_2CH\_WS | M4SS\_SMIH\_D0 | CCI\_DATA\_VALID | M4SS\_QSPI\_D1 |  |
| GPIO\_49 | GPIO\_49 | SIO\_1 | ULP\_GPIO\_1 | UART2\_RTS | GSPI\_MST1\_CS1 | I2S\_2CH\_CLK | SCT\_OUT\_5 | RMII\_TXD1 | M4SS\_SMIH\_D1 | CCI\_CS[1] | M4SS\_QSPI\_CSN0 |  |
| GPIO\_50 | GPIO\_50 | SIO\_2 | ULP\_GPIO\_2 | UART2\_CTS | UART2\_RS485\_RE | I2C1\_SCL | SCT\_OUT\_0 | RMII\_TXD0 | M4SS\_SMIH\_D2 | CCI\_RDY[1] | M4SS\_QSPI\_D2 |  |
| GPIO\_51 | GPIO\_51 | SIO\_3 | ULP\_GPIO\_3 | USB\_XTAL\_ON | UART2\_RS485\_DE | I2C1\_SDA | SCT\_OUT\_1 | RMII\_TXEN | M4SS\_SMIH\_D3 | CCI\_INTR[0] | M4SS\_QSPI\_D3 |  |
| GPIO\_52 | GPIO\_52 | SIO\_4 | M4SS\_QSPI\_CLK | M4SS\_TRACE\_CLKIN | ULP\_GPIO\_13 | USART1\_RI | SCT\_OUT\_7 | RMII\_RXD1 | M4SS\_SMIH\_WP | CCI\_CLK | M4SS\_QSPI\_DQS |  |
| GPIO\_53 | GPIO\_53 | SIO\_5 | M4SS\_QSPI\_CSN0 | M4SS\_TRACE\_CLK | PMU\_TEST\_2 | USART1\_IR\_RX | SCT\_IN\_3 | RMII\_MDC | M4SS\_SMIH\_CD\_N | CCI\_CS[0] | M4SS\_QSPI\_CSN1 |  |
| GPIO\_54 | GPIO\_54 | SIO\_6 | M4SS\_QSPI\_D0 | M4SS\_TRACE\_D0 | CCI\_DATA\_0 | USART1\_IR\_TX | ULP\_GPIO\_4 | RMII\_MDO | M4SS\_SMIH\_D4 | CCI\_DATA\_4 | M4SS\_QSPI\_D4 |  |
| GPIO\_55 | GPIO\_55 | SIO\_7 | M4SS\_QSPI\_D1 | M4SS\_TRACE\_D1 | CCI\_DATA\_1 | USART1\_RS485\_EN | ULP\_GPIO\_5 | RMII\_REF\_CLK | M4SS\_SMIH\_D5 | CCI\_DATA\_5 | M4SS\_QSPI\_D5 |  |
| GPIO\_56 | GPIO\_56 |  | M4SS\_QSPI\_D2 | M4SS\_TRACE\_D2 | CCI\_DATA\_2 | USART1\_RS485\_RE | ULP\_GPIO\_6 | RMII\_CRS\_DV | M4SS\_SMIH\_D6 | CCI\_DATA\_6 | M4SS\_QSPI\_D6 |  |
| GPIO\_57 | GPIO\_57 |  | M4SS\_QSPI\_D3 | M4SS\_TRACE\_D3 | CCI\_DATA\_3 | USART1\_RS485\_DE | ULP\_GPIO\_7 | RMII\_RXD0 | M4SS\_SMIH\_D7 | CCI\_DATA\_7 | M4SS\_QSPI\_D7 |  |

Table 5: GPIO Pin Multiplexing

Note that GPIO's 23 to 30 can be used for Analog functions when GPIO Mode = 14. The analog function available on these GPIOs is further determined by GPIO Analog Mode (2-bit programmable value) for each of these GPIOs.

|  |  |  |  |
| --- | --- | --- | --- |
| **GPIO** | **GPIO Analog Mode = 0** | **GPIO Analog Mode = 1** | **GPIO Analog Mode = 4** |
| GPIO\_23 | ADCP9 |  |  |
| GPIO\_24 | ADCP19 / ADCN9 |  |  |
| GPIO\_25 | ADCP6 |  |  |
| GPIO\_26 | ADCP16 / ADCN6 |  |  |
| GPIO\_27 | ADCP7 | TOUCH\_VREF\_EXT | OPAMP3OUT0 |
| GPIO\_28 | ADCP17 / ADCN7 |  |  |
| GPIO\_29 | ADCP8 |  |  |
| GPIO\_30 | ADCP18 / ADCN8 |  |  |

#### ULP GPIO Pin Multiplexing

The ULP GPIOs listed in the table below (ULP\_GPIO\_0 to ULP\_GPIO\_15) are available in the normal mode of operation (Power-states 4 and 3) and also in Ultra-low power mode of operation of the Microcontroller (Power-states 2 and 1). For a description of power-states, refer to the Hardware Reference Manual. Each of these ULP GPIO's Pin function is controlled by a 3-bit ULP GPIO Mode register.

| **ULP\_GPIO** | **ULP GPIO Mode = 0** | **ULP GPIO Mode = 1** | **ULP GPIO Mode = 2** | **ULP GPIO Mode = 3** | **ULP GPIO Mode = 4** | **ULP GPIO Mode = 5** | **ULP GPIO Mode = 6** | **ULP GPIO Mode = 7** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ULP\_GPIO\_0 | ULP\_EGPIO[0] | ULP\_SPI\_CLK | ULP\_I2S\_DIN | ULP\_UART\_RTS | ULP\_I2C\_SDA | NPSS\_GPIO\_1 | SOC\_GPIO\_0 | Analog Function |
| ULP\_GPIO\_1 | ULP\_EGPIO[1] | ULP\_SPI\_DOUT | ULP\_I2S\_DOUT | ULP\_UART\_CTS | ULP\_I2C\_SCL | Timer0 | SOC\_GPIO\_1 | Analog Function |
| ULP\_GPIO\_2 | ULP\_EGPIO[2] | ULP\_SPI\_DIN | ULP\_I2S\_WS | ULP\_UART\_RX | ULP\_SPI\_CS1 | COMP1\_OUT | SOC\_GPIO\_2 | Analog Function |
| ULP\_GPIO\_3 | ULP\_EGPIO[3] | ULP\_SPI\_CS0 | ULP\_I2S\_CLK | ULP\_UART\_TX | ULP\_SPI\_DIN | AUX\_ULP\_TRIG\_0 | SOC\_GPIO\_3 | Analog Function |
| ULP\_GPIO\_4 | ULP\_EGPIO[4] | ULP\_SPI\_CS1 | ULP\_I2S\_WS | ULP\_UART\_RTS | ULP\_I2C\_SDA | AUX\_ULP\_TRIG\_1 | SOC\_GPIO\_4 | Analog Function |
| ULP\_GPIO\_5 | ULP\_EGPIO[5] | IR\_OUTPUT | ULP\_I2S\_DOUT | ULP\_UART\_CTS | ULP\_I2C\_SCL | AUX\_ULP\_TRIG\_0 | SOC\_GPIO\_5 | Analog Function |
| ULP\_GPIO\_6 | ULP\_EGPIO[6] | ULP\_SPI\_CS2 | ULP\_I2S\_DIN | ULP\_UART\_RX | ULP\_I2C\_SDA | NPSS\_GPIO\_1 | SOC\_GPIO\_6 | Analog Function |
| ULP\_GPIO\_7 | ULP\_EGPIO[7] | IR\_INPUT | ULP\_I2S\_CLK | ULP\_UART\_TX | ULP\_I2C\_SCL | Timer1 | SOC\_GPIO\_7 | Analog Function |
| ULP\_GPIO\_8 | ULP\_EGPIO[8] | ULP\_SPI\_CLK | ULP\_I2S\_CLK | ULP\_UART\_CTS | ULP\_I2C\_SCL | Timer0 | SOC\_GPIO\_8 | Analog Function |
| ULP\_GPIO\_9 | ULP\_EGPIO[9] | ULP\_SPI\_DIN | ULP\_I2S\_DIN | ULP\_UART\_RX | ULP\_I2C\_SDA | COMP1\_OUT | SOC\_GPIO\_9 | Analog Function |
| ULP\_GPIO\_10 | ULP\_EGPIO[10] | ULP\_SPI\_CS0 | ULP\_I2S\_WS | ULP\_UART\_RTS | IR\_INPUT | NPSS\_GPIO\_4 | SOC\_GPIO\_10 | Analog Function |
| ULP\_GPIO\_11 | ULP\_EGPIO[11] | ULP\_SPI\_DOUT | ULP\_I2S\_DOUT | ULP\_UART\_TX | ULP\_I2C\_SDA | AUX\_ULP\_TRIG\_0 | SOC\_GPIO\_11 | Analog Function |
| ULP\_GPIO\_12 | ULP\_EGPIO[12] | ULP\_SPI\_CS1 | ULP\_I2S\_CLK | NPSS\_TEST\_MODE\_0 | ULP\_I2C\_SDA | NPSS\_GPIO\_1 | SOC\_GPIO\_12 | Analog Function |
| ULP\_GPIO\_13 | ULP\_EGPIO[13] | ULP\_SPI\_CS2 | ULP\_I2S\_DIN | COMP2\_OUT | ULP\_I2C\_SCL | Timer1 | SOC\_GPIO\_13 | Analog Function |
| ULP\_GPIO\_14 | ULP\_EGPIO[14] | NPSS\_GPIO\_4 | ULP\_I2S\_WS | Timer0 | IR\_OUTPUT | COMP1\_OUT | SOC\_GPIO\_14 | Analog Function |
| ULP\_GPIO\_15 | ULP\_EGPIO[15] | Timer2 | ULP\_I2S\_DOUT | NPSS\_GPIO\_4 | IR\_INPUT | AUX\_ULP\_TRIG\_0 | SOC\_GPIO\_15 | Analog Function |

Note that each of the ULP\_GPIO's 0 to 15 can be used for Analog functions when ULP GPIO Mode = 7. The analog function available on these ULP\_GPIOs is further determined by ULP GPIO Analog Mode (3-bit programmable value) for each of these ULP\_GPIOs.

| **ULP\_GPIO** | **ULP GPIO Analog Mode = 0** | **ULP GPIO Analog Mode = 1** | **ULP GPIO Analog Mode = 2** | **ULP GPIO Analog Mode = 3** | **ULP GPIO Analog Mode = 4** | **ULP GPIO Analog Mode = 5** | **ULP GPIO Analog Mode = 6** | **ULP GPIO Analog Mode = 7** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ULP\_GPIO\_0 | ADCP0 | TOUCH6 |  | COMPA\_P0 | OPAMP1P2 |  |  |  |
| ULP\_GPIO\_1 | ADCP10 / ADCN0 |  |  | COMPA\_N0 |  | REF0 |  |  |
| ULP\_GPIO\_2 | ADCP1 |  |  | COMPB\_P0 | OPAMP1P3 |  |  |  |
| ULP\_GPIO\_3 | ADCP11 / ADCN1 | TOUCH5 |  | COMPB\_N0 |  | REF1 |  |  |
| ULP\_GPIO\_4 | ADCP2 | C\_int\_res\_in | DAC0 | COMPA\_N1 | OPAMP1OUT0 | REF2 |  |  |
| ULP\_GPIO\_5 | ADCP12 / ADCN2 | res\_out |  | COMPA\_P1 | OPAMP2P1 |  |  |  |
| ULP\_GPIO\_6 | ADCP3 | TOUCH4 |  |  | OPAMP1P4 |  |  |  |
| ULP\_GPIO\_7 | ADCP15 / ADCN5 | TOUCH3 |  |  | OPAMP1P1 / OPAMP1N1 |  |  |  |
| ULP\_GPIO\_8 | ADCP4 | TOUCH0 / C\_int\_res\_in |  |  | OPAMP1P5 |  |  | TESTOUT0 |
| ULP\_GPIO\_9 | ADCP14 / ADCN4 | TOUCH1 |  |  | OPAMP2OUT0 |  |  | TESTOUT1 |
| ULP\_GPIO\_10 | ADCP5 | TOUCH2 / res\_out |  |  | OPAMP3P0 / OPAMP3N0 |  | MEMSOUT0 |  |
| ULP\_GPIO\_11 | ADCP13 / ADCN3 | TOUCH7 |  |  | OPAMP2P0 / OPAMP2N0 |  |  |  |
| ULP\_GPIO\_12 |  |  |  | COMPB\_P1 | OPAMP1P0 / OPAMP1N0 |  |  |  |
| ULP\_GPIO\_13 |  |  |  | COMPB\_N1 |  |  |  |  |
| ULP\_GPIO\_14 |  |  |  |  | OPAMP3P1 |  |  |  |
| ULP\_GPIO\_15 |  |  | DAC1 |  | OPAMP1OUT1 | REF3 |  |  |

Table 6: ULP GPIO Pin Multiplexing

#### UULP VBAT GPIO Pin Multiplexing

The UULP VBAT GPIOs listed in the table below (UULP\_VBAT\_GPIO\_0 to UULP\_VBAT\_GPIO\_4) are available in the normal mode of operation (Power-states 4 and 3), in Ultra-low power mode of operation (Power-states 2 and 1) and also in the retention and deep sleep mode of operation (Retention and Power-state 0). For a description of power-states, refer to the Hardware Reference Manual. Each of this UULP VBAT GPIO's Pin function is controlled by a 3-bit UULP VBAT GPIO Mode register.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **UULP VBAT GPIO** | **UULP VBAT GPIO Mode = 0** | **UULP VBAT GPIO Mode = 1** | **UULP VBAT GPIO Mode = 2** | **UULP VBAT GPIO Mode = 4** | **UULP VBAT GPIO Mode = 5** | **UULP VBAT GPIO Mode = 6** | **Default** |
| UULP\_VBAT\_GPIO\_0 | UULP\_VBAT\_GPIO[0] | BUCK\_BOOST\_EN | MCU\_GPIO0\_WAKEUP |  |  |  | BUCK\_BOOST\_EN |
| UULP\_VBAT\_GPIO\_1 | UULP\_VBAT\_GPIO[1] | XTAL\_EN | MCU\_GPIO1\_WAKEUP |  |  |  | XTAL\_EN |
| UULP\_VBAT\_GPIO\_2 | UULP\_VBAT\_GPIO[2] |  | MCU\_GPIO2\_WAKEUP | 32KHZ\_XTAL\_CLK |  |  |  |
| UULP\_VBAT\_GPIO\_3 | UULP\_VBAT\_GPIO[3] |  | MCU\_GPIO3\_WAKEUP |  | 32KHZ\_XTAL\_CLK |  | NPSS\_GPIO[3] |
| UULP\_VBAT\_GPIO\_4 | UULP\_VBAT\_GPIO[4] |  | MCU\_GPIO4\_WAKEUP |  |  | 32KHZ\_XTAL\_CLK | NPSS\_GPIO[4] |

Table 7: UULP GPIO Pin Multiplexing

#### Description of Digital Pins Multiplexed on GPIOs

| **Pin Name** | **Direction** | **Description** |
| --- | --- | --- |
| **CAN (Controller Area Network) Interface** | | |
| CAN1\_RXD | Input | CAN Receive Data |
| CAN1\_TXD | Output | CAN Transmit Data |
| **CCI (Companion Chip Interface)** | | |
| CCI\_CLK | Output/ Input | Output Clock from the CCI Controller when CCI is in Arbiter-Master-Slave(AMS) Mode  Input Clock from the CCI Controller when CCI is in Master-Slave(MS) Mode |
| CCI\_CS[1: 0] | Output/ Input | Active Low Chip Select. Output in AMS Mode and input in MS Mode.  All the 3 bits are valid and CCI Controller can select three external slaves in AMS Mode.  Only bit [0] is only valid in MS Mode. |
| CCI\_DATA\_0 to CCI\_DATA\_7 | Input | Bidirectional Data. All the bits are under the control of AMS or one of the three MS |
| CCI\_DATA\_VALID | Output | Active high Indicates that the data on CCI\_DATA\_0 to CCI\_DATA\_7 is valid |
| CCI\_INTR[1:0] | Input/  Output | Active high interrupt. Input in AMS Mode and Output in MS Mode  All the 3 bits are valid and CCI Controller can get interrupt from any of the three external slaved in AMS Mode.  Only bit [0] is only valid in MS Mode. |
| CCI\_RDY[1:0] | Input/  Output | Active Low Ready. Input in AMS Mode and Output in MS Mode. MS accepts data from AMS only when corresponding CCI\_RDY is zero.  All the 3 bits are valid and CCI Controller can get ready from any of the three external slaved in AMS Mode.  Only bit [0] is only valid in MS Mode. |
| **GSPI (General SPI) Interface** | | |
| GSPI\_MST1\_CLK | Output | Output Clock from the GSPI master to external slave |
| GSPI\_MST1\_CS0 to GSPI\_MST1\_CS3 | Output | Active Low CSN. GSPI Master can select a maximum of 4 slaves. |
| GSPI\_MST1\_MISO | Input | Input data to master from external slave |
| GSPI\_MST1\_MOSI | Output | Output data from master to external slave |
| **I2C (Inter-integrated Circuit) Interface** | | |
| I2Cx\_SCL,  ULP\_I2C\_SCL | Inout | I2C Serial Clock  x= 1, 2 |
| I2Cx\_SDA,  ULP\_I2C\_SDA | Inout | I2C Serial Data  x= 1, 2 |
| **2 Channel I2S (Inter-IC Sound) Interface** | | |
| I2S\_2CH\_CLK | Output/  Input | I2S Clock  Output in Master Mode and Input in Slave Mode |
| I2S\_2CH\_WS | Output/  Input | Active high I2S Word Select  Output in Master Mode and Input in Slave Mode |
| I2S\_2CH\_DIN\_0 to I2S\_2CH\_DIN\_1 | Input | I2S Input Data |
| I2S\_2CH\_DOUT\_0 to I2S\_2CH\_DOUT\_1 | Output | I2S Output Data |
| **QSPI (Quad SPI) Interface** | | |
| M4SS\_QSPI\_CLK | Output | Output clock to the external SPI slave. |
| M4SS\_QSPI\_CSN0 to M4SS\_QSPI\_CSN1 | Output | Active Low Chip Select to select a maximum of two slaves. |
| M4SS\_QSPI\_D0 to M4SS\_QSPI\_D7 | Inout | QSPI Data. Supports both QUAD and OCTA Data. In Quad Mode, only Bits M4SS\_QSPI\_D0 to M4SS\_QSPI\_D3 are valid. In Octa Mode, all the bits are valid |
| M4SS\_QSPI\_DQS | Input | Data Strobe signal |
| **SMIH (SD/SDIO/MMC Host Controller) Interface** | | |
| M4SS\_SMIH\_CLK | Output | Output Clock from the SMIH Controller |
| M4SS\_SMIH\_CMD | Output | Output Command from the SMIH Controller |
| M4SS\_SMIH\_D0 to M4SS\_SMIH\_D7 | Inout | Bidirectional 8-bit Data |
| M4SS\_SMIH\_CD\_N | Input | Active Low Card Detect |
| M4SS\_SMIH\_WP | Input | Active Low Write Protect |
| **M4 Trace Interface** | | |
| M4SS\_TRACE\_CLK | Output | Trace Clock from Cortex M4 |
| M4SS\_TRACE\_CLKIN | Input | Trace Port Clock to Cortex M4 |
| M4SS\_TRACE\_D0 to M4SS\_TRACE\_D3 | Output | Trace Port Data bus from Cortex M4 |
| **PWM (Pulse Width Modulation) Interface** | | |
| PWM\_xH | Output | PWM output signals. The output pins are grouped in pairs, to facilitate driving the low side and high side of a power half-bridge.  x = 1,2,3,4 |
| PWM\_xL | Output |
| PWM\_FAULTA | Input | External fault signal A |
| PWM\_FAULTB | Input | External fault signal B |
| PWM\_SLP\_EVENT\_TRIG | Output | Special event trigger for synchronizing analog to digital conversions. |
| PWM\_TMR\_EXT\_TRIG\_1 to PWM\_TMR\_EXT\_TRIG\_4 | Input | External trigger for base timers to increment. Each Channel has separate trigger input. |
| **QEI (Quadrature Encode Interface)** | | |
| QEI\_DIR | Output | Position counter direction. ‘1’ means counter direction is positive. ‘0’ means counter direction is negative. |
| QEI\_IDX | Input | QE Index. Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position. |
| QEI\_PHA | Input | QE Phase A input |
| QEI\_PHB | Input | QE Phase B input |
| **RMII (Reduced media-independent interface)** | | |
| RMII\_CRS\_DV | Input | PHY Receive Data Valid |
| RMII\_MDC | Output | Management Data Clock |
| RMII\_MDO | Inout | Management Data |
| RMII\_REF\_CLK | Output/  Input | Output Clock when clock is provided from Internal PLL  The Clock is taken from external interface when internal PLL is not used. |
| RMII\_RXD0 to RMII\_RXD1 | Input | Receive Data |
| RMII\_TXD0 to RMII\_TXD1 | Output | Transmit Data |
| RMII\_TXEN | Output | Active High Transmit Data Enable. When asserted indicates that Transmit Data is valid. |
| **SCT (State Configurable Timer) Interface** | | |
| SCT\_IN\_0 to SCT\_IN\_7 | Input | Timer input event |
| SCT\_OUT\_0 to SCT\_OUT\_7 | Output | Timer output event |
| **SIO (Serial Input Output) Interface** | | |
| SIO\_0 to SIO\_7 | Inout | Serial Input-Output Data |
| **SSI (Synchronous Serial Interface) Master** | | |
| SSI\_MST\_CLK | Output | Output clock from SSI Master |
| SSI\_MST\_CS0 to SSI\_MST\_CS3 | Output | Active Low Chip select |
| SSI\_MST\_DATA0 to SSI\_MST\_DATA3 | Inout | Bidirectional Data |
| **SSI (Synchronous Serial Interface) Slave** | | |
| SSI\_SLV\_CLK | Input | Input clock to SSI Slave |
| SSI\_SLV\_CS | Input | Active Low Chip select |
| SSI\_SLV\_MISO | Output | Slave Output Data |
| SSI\_SLV\_MOSI | Input | Slave Input Data |
| **UART Interface** | | |
| UART2\_CTS,  ULP\_UART\_CTS | Input | Clear to Send |
| UART2\_RTS,  ULP\_UART\_RTS | Output | Request to Send |
| UART2\_RS485\_DE | Output | Driver Enable |
| UART2\_RS485\_EN | Output | Active high RS485 Enable |
| UART2\_RS485\_RE | Output | Receiver Enable |
| UART2\_RX,  ULP\_UART\_RX | Input | Serial Input |
| UART2\_TX,  ULP\_UART\_TX | Output | Serial Output |
| **USART Interface** | | |
| USART1\_CLK |  |  |
| USART1\_CTS | Input | Clear to Send |
| USART1\_RTS | Output | Request to Send |
| USART1\_DCD | Input | Data Carrier Detect |
| USART1\_DSR | Input | Data Set Ready |
| USART1\_DTR | Output | Data Terminal Ready |
| USART1\_IR\_RX | Input | IrDA SIR Input |
| USART1\_IR\_TX | Output | IrDA SIR Output |
| USART1\_RI | Input | Ring Indicator |
| USART1\_RS485\_DE | Output | Driver Enable |
| USART1\_RS485\_EN | Output | Active high RS485 Enable |
| USART1\_RS485\_RE | Output | Receiver Enable |
| USART1\_RX | Input | Serial Input |
| USART1\_TX | Output | Serial Output |
| **Miscellaneous Interface** | | |
| INTERFACE\_PLL\_CLOCK | Output | Clock from Interface PLL |
| I2S\_PLL\_CLOCK | Output | Clock from I2S PLL |
| USB\_PLL\_CLOCK | Output | USB Clock from Modem PLL |
| SOC\_PLL\_CLOCK | Output | Clock from SoC PLL |
| MEMS\_REF\_CLOCK | Output | Mems Ref Clock from Modem PLL |
| REF\_CLK\_OUT | Output | Reference Clock used by M4 SoC |
| RF\_REF\_CLK\_OUT | Output | Clock from Internal RF |
| MCU\_CLK\_OUT | Output | All the Clocks that are used by M4 SoC are multiplexed and connected on this pin |
| PLL\_TESTMODE\_SIG | Output | Test Mode Signal from SoC PLL for Debug |
| PMU\_TEST\_1 to PMU\_TEST\_2 | Inout | Test Pins from IPMU for Debug |
| SDMEM\_PRESENT |  |  |
| USB\_CDC |  |  |
| USB\_DRVVBUS | Output | Signal from USB Controller to be connected to off-chip charge pump circuit. |
| USB\_XTAL\_ON | Output | If the reference clock to the USB PLL is fed through GPIO\_25, this signal is used to control the Crystal Oscillator which generates the reference clock |
| XTAL\_ON\_IN | Input | Crystal oscillator enable input when crystal is shared by another chip |
| **UULP VBAT Pin Interface** | | |
| BUCK\_BOOST\_EN | Output | Enable to an external Buck boost regulator or Power gate that controls the supply to all supply pins of the chip except the UULP VBAT GPIO supply |
| XTAL\_EN | Output | External crystal oscillator enable |
| 32KHZ\_XTAL\_CLK | Input | Low Frequency clock input from an External 32KHz Crystal oscillator |
| MCU\_GPIO0/1/2/3/4\_WAKEUP | Input | GPIOs that can be used as Wakeup interrupt to MCU while in Retention or Deep sleep mode |
| NWP\_GPIO0/2/3\_WAKEUP | Input | GPIOs that can be used as Wakeup interrupt to Wireless Network processor (NWP) while in retention or deep sleep mode. |

Table 8: of Digital Pins Multiplexed on GPIOs

#### Description of Analog Pins Multiplexed on GPIOs

| **Pin Name** | **Direction** | **Description** |
| --- | --- | --- |
| **ADC Interface** |  |  |
| ADCP0 - ADCP19 | Input | The 20 single ended input channels that are multiplexed onto the ADC  P0 - P9 can be coupled with N0 - N9 for differential mode of operation of the ADC |
| ADCN0 - ADCN9 | Input | The N pins of the 10 possible differential channels multiplexed onto the ADC |
| **DAC Interface** |  |  |
| DAC0, DAC1 | Output | Possible output pins from the internal DAC |
| **OpAmp Interface** |  |  |
| OPAMP"*xyz*" | Input | Multiplexed inputs of the three OpAmps. *xyz* denote the OpAmp number, the terminal and the multiplexing on that pin of the OpAmp  x = OpAmp number (1, 2 or 3)  y = P or N terminal of OpAmp  z = 0, 1, 2, 3, 4, 5 (Multiplexing at OpAmp input pin). Note that OPAMP1P is available at 6 locations, OPAMP2P, 3P and 1N are available at 2 locations each and OPAMP2N and 3N pins are available at only one location |
| OPAMP1OUT0/1,  OPAMP2/3OUT0 | Output | Outputs of the three OpAmps. Note that OPAMP1 output is available at two possible pin locations whereas OPAMP2 and 3 outputs are available at a fixed pin |
| **Comparator Interface** |  |  |
| CMP"*xyz*" |  | Multiplexed inputs of the two Comparators. *xyz* denote the Comparator number, the terminal and the multiplexing on that pin of the Comparator  x = Comparator number (A or B)  y = P or N terminal of OpAmp  z = 0, 1 (Multiplexing at Comparator Input pin). Note that each input pin of both comparators is available on two possible GPIO pins. |
| **Touch Interface** |  |  |
| TOUCH0/1/2/3/4/5/6/7 | Input | Capacitive Touch inputs |

**Table 9: Analog Pins Multiplexed on GPIOs**

# RS14100 Regulatory Approvals

This section will outline the regulatory information for the RS14100 modules for the countries listed below. This information will be updated when available.

1. United States
2. Canada
3. Europe
4. Japan
5. Other Regulatory Jurisdictions

# RS14100 Electrical Specifications

1. [RS14100 Connectivity Absolute Maximum Ratings](#scroll-bookmark-26)
2. [RS14100 Connectivity Recommended Operating Conditions](#scroll-bookmark-27)
3. [RS14100 Connectivity Current Consumption](#scroll-bookmark-28)
4. [RS14100 Connectivity Wakeup and Transition Times](#scroll-bookmark-29)
5. [RS14100 Connectivity DC Characteristics](#scroll-bookmark-30)
6. [RS14100 Connectivity AC Characteristics](#_RS14100_Connectivity_AC)
7. [RS14100 Connectivity RF Characteristics](#scroll-bookmark-32)
8. [RS14100 Connectivity Reliability Parameters](#scroll-bookmark-33)
9. [RS14100 Connectivity Wakeup Receiver](#scroll-bookmark-34)

## Absolute Maximum Ratings

Functional operation above maximum ratings is not guaranteed and may damage the device.

| **Symbol** | **Parameter** | **Min** | **Max** | **Units** |
| --- | --- | --- | --- | --- |
| C\_VDD\_\* | All Core Supplies | -0.5 | 1.26 | V |
| IO\_VDD\_\* | All IO Supplies | -0.5 | 3.63 | V |
| GPIO\_x | All Digital Pads | -0.5 | IO\_VDD\_x + 0.5 | V |
| USB\_VBUS | USB VBUS voltage | -0.5 | 5 | V |
| USB\_VDDA | Input analog voltage for USB | -0.5 | 3.6 | V |
| USB\_VDDS | Input digital voltage for USB | -0.5 | 3.6 | V |
| Tstore | Storage temperature | -40 | +125 | oC |
| Tj(max) | Maximum junction temperature | - | +125 | oC |
| ESDHBM | Electrostatic discharge tolerance (HBM) - non RF IO  Electrostatic discharge tolerance (HBM) - RF IO  Compliant with JEDEC specification JS-001-2012 (April 2012) | - | 2000  1000 | V  V |
| ESDMM | Electrostatic discharge tolerance (MM)  Compliant with JEDEC specification JESD22-A115C (November 2010) | - | 200 | V |
| ESDCDM | Electrostatic discharge tolerance (CDM)  Compliant with JESD22-C101E (December 2009) | - | 500 | V |
| LU | Latchup Immunity I-Test criteria at max ambient temp of 125C  Compliant with JESD78D (November 2011) | -100 | 100 | mA |
| Imax | Maximum Current consumption in TX mode |  | 400 | mA |

| **Symbol** | **Parameter** | **Min** | **Max** | **Units** |
| --- | --- | --- | --- | --- |
| RF\_TX, RF\_RX, RF\_BT\_TX | RF Input Level | - | 10 | dBm |

Table 10: Absolute Maximum Ratings

## Recommended Operating Conditions

| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| fclk | Clock frequency | - | - | 180 | MHz |
| VBATT | Input supply voltage (Battery and IOs) - Direct Battery Mode | 2.1 | 3.3 | 3.6 | V |
| USB\_VDDS | Input digital supply voltage for USB interface | 3.0 | 3.3 | 3.6 | V |
| USB\_VDDA | Input analog supply voltage for USB analog portions | 3.0 | 3.3 | 3.6 | V |
| Tambient | Ambient temperature | -40 | 25 | 85/100 [[2]](#footnote-2) | oC |

Table 11: Recommended Operating Conditions

## Current Consumption

### POC

This block generates a POC (Power On Control) signal that is distributed to all I/O cells to prevent the I/O cells from powering up in undesired configuration and is also used inside the IC to safe state the IC till a valid supply is available for proper operation of the IC. This power management is functional in both power up and power down sequences.

During power up, until the core supply (VDD) reaches 0.7V and till the IO supply (DVDD) reaches 1.8V, the POC signal stays high. Once the core supply exceeds 0.7V and IO supply exceeds 1.8V POC becomes low and normal operation of the IC starts.

Once the POC becomes low, it stays low. However, if DVDD becomes lower than Blackout threshold voltage, POC becomes high.

VDD/VSS – core supply/ground

DVDD/DVSS – I/O supply/ground

The POC signal is in DVDD domain

| **ID** | **Description** | **Parameter Description** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| POC1 | POC threshold | VDD at which POC becomes low | 675 | 728 | 776 | mV |
| POC2 | BOD threshold | DVDD at which BOD occurs | 0.8 | 1.22 | 1.55 | V |
| POC1 | Quiescent current | Steady state current consumption from DVDD | 1.61 | 3.05 | 7.3 | nA |
| POC1 | Leakage current on VDD | Steady state current consumption from VDD |  | 0.12 | 4.18 | nA |
| POC3 | Minimum DVDD ramp down time | minimum ramp down time required for POC to act |  | 2 | 4 | ms |

Table 12: Power on Control

## DC Characteristics

### Reset Pin

| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| VIH | High level input voltage | 0.8 VDD | - | 3.6 | V |
| VIL | Low-level input voltage | -0.5 | - | 0.3 VDD | V |
| Vhys | Hysteresis voltage | 0.05 VDD | - | - | V |

Table 13: Reset Pin

### Digital Input Output Signals

| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| VIH | High level input voltage | 2.0 | - | 3.6 | V |
| VIL | Low level input voltage | -0.3 | - | 0.8 | V |
| Vhys | Hysteresis voltage | 0.1 VDD | - | - | V |
| VOL | Low level output voltage | - | - | 0.4 | V |
| VOH | High level output voltage | VDD-0.4 | - | - | V |
| IOL | Low level output current | 4.0 |  |  | mA |
| IOH | High level output current | 4.0 |  |  | mA |

Table 14: Digital I/O Signals

### USB

| **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| Vcm DC (DC level measured at receiver connector) | HS Mode  LS/FS Mode | -0.05  0.8 | -  - | 0.5  2.5 | V |
| Crossover Voltages | LS Mode  FS Mode | 1.3  1.3 | -  - | 2  2 | V |
| Power supply ripple noise (Analog 3.3V) | < 160 MHz | -50 | - | 50 | mV |

Table 15: USB

### Pin Capacitance

| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| Cio | Input/output capacitance, digital pins only | - | - | 2.0 | pF |

Table 16: Pin Capacitances

### Open-drain I2C pins

| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| VIH | High level input voltage | 0.7 VDD | - | - | V |
| VIL | Low level input voltage | 0 | - | 0.3 VDD | V |
| Vhys | Hysteresis voltage | 0.1 x VDD | - | - | V |
| IOL | VOL = 0.4, Low-level output current; pin configured as standard mode or fast mode | 4.0 | - | - | mA |
| IOL | VOL = 0.4 Low-level output current; pin configured as standard mode or fast mode | VDD-0.4 | - | - | V |

Table 17: Open-drain I2C pins

### Clocks

Following ULP clocks needed for sleep timers, calibration and other low power functional modes are available

* 7nA@0.6V 32KHz Low speed Ring oscillator
* 130nA@VBATT 32KHz RC oscillator
* 500nA@0.6V 32KHz Crystal Oscillator
* 60uA@0.9V 32MHz RC Oscillator
* 10uA@0.9V, 32MHz High Frequency Ring oscillator
* 20uA@0.9V ,32MHz Frequency Doubler

The ULP clocks module has an SPI control interface. Each of the clocks in this module has provision for calibration on power up and periodic calibration during run time.

#### 32KHz Low Speed Ring Oscillator

The 32KHz nW ring oscillator can be used for the following applications

* Bandgap reference sampling mode
* SC-DCDC module clock,
* RTC with internal clock
* <5nA typical power consumption from 0.6V supply
* Frequency trimming handles for continuous calibration during runtime and manufacturing test.
* No runt pulses in output and stable clock available from first cycle

| **ID** | **Symbol** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| RO32K1a | Iq |  | 221p | 229p | 9.74n | A/KHz |
| RO32K1aa | Itot |  | 3.81n | 7.88n | 111.3n | A |
| RO32K1b | Foscmin |  | 4.571 | 18.89 | 95.63\* | KHz |
| RO32K1c | Foscmid |  | 22.65 | 67.19 | 398.2 | KHz |
| RO32K1d | Foscmax |  | 48.04 | 121.9 | 735.8 | KHz |
| RO32K1e | Fstep |  | 1.39 | 3.81 | 23.76 | KHz/LSB |
| RO32K1f | Tstart | trim = 00100 trim = 10000 trim = 11111 | 7.59 | 10.52 | 11.25 | Cycles Cycles Cycles |
| RO32K1g | ΔFtemp |  | 12.21 | 20.01 | 22.61 | % |
| RO32K1h | ΔFV | frequency variation with VDD\_ULP frequency variation with VBATT | 22.23 | 32.94 | 35.83 | % % |
| RO32K1i | D |  | -23 | – | 473] | % |
| RO32K2 | Ileak |  | 3.33 | - | 28.95 | A |
| RO32K3a | JCrms,k=1e6 |  | 3.33 | - | 28.95 | s |
| RO32K3b | JCrms,k=4 |  | 43.25 | – | 55.02 | s |
| RO32K3c | JErms |  | – | 540p | – | s |

Table 18: 32KHz Low Speed Ring Oscillator

#### 32 KHz RC Oscillator

* Applications
* Bandgap reference sampling mode
* SC-DCDC module clock
* Accurate RTC with internal clock
* There will be a programmable output divider on this clock for generating different ULP-FSM clock frequencies as needed.
* <100nA typical power consumption for VBATT supply
* Frequency trimming handles for continuous calibration during runtime and manufacturing test.
* Low noise performance. Need to achieve less than 4ppm allan deviation after 2s for long term stability
* No runt pulses in output and stable clock available from first cycle

| **ID** | **Description** | **Parameter Description** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| RC32K1 | Nominal Frequency | Freq. across corners for coarse: 10 fine: 1000000  coarse: 10 fine :0000000  coarse: 10 fine :1111111  coarse: 01 fine :1111111 (ffp,-40oC,125oC)  coarse: 11 fine :0000000 (ssp,-40oC,125oC) | 21.42  13.36  40.08  56.91  26.12 | 29.54  -  -  57.61  26.43 | 55.58  -  -  -  - | KHz |
| RC32K2 | Minimum Frequency | Freq. across corners for coarse: 00 fine: 1000000 | 11.26 | 15.53 | 65.91 | KHz |
| RC32K3 | Maximum Frequency | Freq. across corners for coarse: 11 fine: 1000000 | 39.35 | 54.29 | 77.63 | KHz |
| RC32K5 | Temp Accuracy | Freq Variation with Temp | – | 1.92 | 194.06 | % |
| RC32K6 | Voltage Accuracy | Freq Variation with Voltage | – | 0.24 | 66.19 | % |
| RC32K4 | Quiescent Current | ON Current From VBATT | 127.3 | 148.4 | 363.6 | nA |
|  |  | ON Current From VDD\_ULP | 3.42 | 7.69 | 143.8 | nA |
| RC32K12 | Shut Down Current | OFF Current From VBATT | 175p | 1.14n | 492.1n | A |
| OFF Current From VDD\_ULP | 64p | 175p | 4.58n | A |
| RC32K8 | Output Duty Cycle | Average Duty cycle across corners | 50.57 | 54.04 | 61.34 | % |
| RC32K9 | Output Slew rate | Average slew rate across corners | 103.9M | 366.7M | 694.9M | V/sec |
| RC32K10 | Frequency Resolution | Change in frequency with fine step at typical corner with coarse = 10 | 86.09 | 305.71 | 912.96 | Hz |
| RC32K7 | Startup Time | Time after enable to get runt free clock | 115.8u | 212.6u | 334.6u | sec |
| RC32K13a | Noise | Allan deviation at 2sec from phase noise | - |  |  | ppm |
| RC32K13b | Jitter | rms value of Edge jitter (TIE) | – | 90.67n | – | sec |
| RC32K13c | Peak Period Jitter | Peak value of Cycle Jitter with 6σ variation | – | 789n | – | sec |
| RC32K15 | Voltage Reference current | Reference current from Bandgap | 13.57 | 20.67 | 33 | nA |

Table 19: 32KHz RC Oscillator

#### 32KHz Crystal Oscillator

* Applications
* Accurate RTC with Xtal clock
* There will be a programmable output divider on this clock for generating different ULP-FSM clock frequencies as needed.
* Calibration of inaccurate clocks such as 32KHz ring and RC oscillators
* <100nA typical power consumption from core supply with least current trim setting.

| **ID** | **Description** | **Parameter Description** | **[ Min Typ Max ]** | **[ Min Typ Max ]** | **Unit** |
| --- | --- | --- | --- | --- | --- |
|  |  |  | XTAL 1 (4pF load, trim=0000) | XTAL 2 (12pF load, trim=0111) |  |
| XO32K1 | Nominal Frequency | Freq. across corners | [32.7683 32.7684 32.7686] | [32.7681 32.7683 32.7684] | KHz |
| XO32K2 | Quiescent Current | ON Current From VBATT | [17 26.17 58.69 ] | [17 26.17 58.69 ] | nA |
|  |  | ON Current From AVDD\_ULP | [46.51 69.35 873.2 ] | [ 275.8 475 1066 ] | nA |
|  |  | ON Current From VDD\_ULP | [1.74 2.97 279 ] | [ 1.43 2.432 1029 ] | nA |
| XO32K3 | Temperature accuracy | Freq Variation with Temp | [ -3.47 – 2.83] | [ -6.43 – 2.83 ] | ppm |
| XO32K4 | Voltage accuracy | Freq Variation with Voltage | [ – – 1 ] | [ – – 2.31 ] | ppm |
| XO32K5 | Startup time | Time after enable to get runt free clock | 2.1 | - | s |
| XO32K6 | Output Duty Cycle | Average Duty cycle across corners | [ 31.81 42.42 45.78 ] | [ 46.8 51.07 53.16 ] | % |
| XO32K7 | Output Slew rate | Average slew rate across corners | [0.068 0.195 1.296] | [ 0.074 0.25 1.41 ] | GV/s |
| XO32K9 | Shut Down Current | OFF Current From VBATT | [ 21p 306p 14.4n] | [ 21p 306p 14.4n] | A |
|  |  | OFF Current From AVDD\_ULP | [ 0.83n 1.5n 51.1n ] | [ 0.83n 1.5n 51.1n ] | A |
|  |  | OFF Current From VDD\_ULP | [ 0.41n 0.731n 65.47n ] | [ 0.41n 0.731n 65.47n ] | A |
| XO32K10 | Rising jitter | cycle to cycle jitter(peak to peak) | [189.5 268.2 566.7] | [ 74.59 88.41 147.4] | ns |
| XO32K10 | Falling jitter | cycle to cycle jitter(peak to peak) | [113.6 185.2 448] | [ 64.81 76.02 130.0 ] | ns |
| XO32K11 | Drive level | Power dissipated across crystal | [1.16 1.78 11.58] | [ 10.52 14.42 18.55 ] | nW |
| XO32K11 | Loop Gain | Loop Gain of amplifier | [ 1.96 2.60 3.17 ] | [ 1.79 3.226 3.88 ] | - |
| XO32K12 | Startup Current | Current From VBATT | 26.14 | 26.2n | A |
|  |  | Current From AVDD\_ULP | 514n | 2.46u | A |
|  |  | Current From VDD\_ULP | 3.8n | 3.64n | A |

Table 20: 32KHz Crystal Oscillator

#### 32MHz RC Oscillator

* Applications
* Used for ULP-TA-Subsystem modules
* SOC in start-up state. This clock must be used by the SOC in start-up state while the 40MHz xtal is starting up. It might be possible to use this clock as reference for the SOC-PLL for initial start-up
* <70uA typical power consumption from core supply
* No runt pulses in output and stable clock available from first cycle

| **ID** | **Description** | **Parameter Description** | **[ Min Typ Max ]** | **Unit** |
| --- | --- | --- | --- | --- |
| RC32M0 | Startup Frequency | Freq. across Process, Voltage and Temperature corners for trim word: 90 | [24 33 47] | MHz |
| RC32M1 | Nominal Frequency | Freq. across Voltage and Temperature corners for  Trim bit: 90,Process corner: Typical  Trim bit: 102,Process corner: Slow  Trim bit: 66,Process corner: Fast | [32.16 33.65 34.1]  [31.08 33.13 33.71]  [32.1 33.15 33.5] | MHz  MHz  MHz |
| RC32M2 | Quiescent Current | ON Current From VDD\_ULP | [42u 68u 112u] | A |
|  |  | ON Current From VBATT | [0.5n 170n 500n] | A |
| RC32M3 | Temp Accuracy | Freq Variation with Temp | [-- – 3] | % |
| RC32M4 | Voltage Accuracy | Freq Variation with Voltage | [-- – 1] | % |
| RC32M5 | Startup Time | Time taken for output clock valid to be high after pu\_core/~POC is set high | [0.9 1.1 1.7] | us |
| RC32M6 | Output Duty Cycle | Average Duty cycle across corners | [47 49.2 49.55] | % |
| RC32M7 | Output Slew rate | Average slew rate across corners@load cap=100f | [1G 1.7G 2.7G] | V/sec |
| RC32M8 | Frequency Resolution | Average change in frequency with trim step at typical corner | [] | KHz |
| RC32M9 | Shut Down Current | OFF Current From VDD\_ULP | [2.5n 4.5n 0.15u] | A |
|  |  | OFF Current From VBATT | [150p 400p 24n] | A |
| RC32M10 | Noise analysis\* | Period jitter peak, BER 1e-3 | [ 270p 410p 560p] | s |
|  |  | Period jitter rms. Integrated from 1K-15MHz | [ 45p 67p 91p] | s |
|  |  | Rms Phase Jitter (sec) ,Integrated pn from 10Hz-15MHz | [ 3.1n ] | s |
| RC32M11 | Transient current | Transient current from VDD\_ULP | [9u 23u 51u ] | A |
|  |  | Transient current from VBATT | [100n 350n 700n] | A |
| RC32M13 | Frequency range | Freq. across Voltage and Temperature corners for  Trim bit=0 and 127,Process corner: Typical  Trim bit=0 and 127,Process corner: Slow  Trim bit=0 and 127,Process corner: Fast | [13M,85M]  [9.5M,70M]  [18.5M,103M] | Hz |
| RC32M14 | Integrator PM | Measure Phase Margin around the integrator loop after startup | [67 70 75 ] | deg C |

Table 21: 32MHz RC Oscillator

#### 32MHz Frequency Doubler

The frequency doubler is used to generate an output clock which is twice the frequency of the input clocks. Below is the summary of features of this block.

* 32 MHz input frequency
* 0.9V +/- 10% Voltage supply
* Input duty cycle range of 40 - 60%.
* Output duty cycle range of 48-52%
* Maximum instantaneous output frequency of 70MHz
* Minimum instantaneous output frequency 60MHz

| **ID** | **Description** | **Parameter Description** | **[ Min Typ Max ]** | **Unit** |
| --- | --- | --- | --- | --- |
| DBLR32M\_1a | Average Output Frequency |  | [ 64.03 64.19 64.21 ] | MHz |
| DBLR32M\_1b | Instantaneous Output frequency Variation |  | [ 2.32 7.06 7.33 ] | MHz |
| DBLR32M\_1c | Output Duty Cycle |  | [ 28.33 – 72.96 ] | % |
| DBLR32M\_5 | Average Current |  | [ 55.00 82.01 121.2 ] | uA |
| DBLR32M\_2 | Shut down current |  | [ 1.45 4.81 55.69 ] | nA |
| DBLR32M\_4a | Delay 000000 | Delay by the delay chain for delay\_2x = 000000 | [ 1.34 3.11 5.16 ] | ns |
| DBLR32M\_4b | Delay 100000 | Delay by the delay chain for delay\_2x = 100000 | [ 7.22 11.57 27.32 ] | ns |
| DBLR32M\_4c | Delay 111111 | Delay by the delay chain for delay\_2x = 111111 | [ 12.23 19.91 54.15 ] | ns |
| DBLR32M\_4d | Delay Resolution magnitude | Delay Resolution magnitude | [ 161.67 266.68 838.25 ] | ps |
| DBLR32M\_4e | Delay Resolution % | Delay Resolution as percentage of input time period (32MHz input) | [ 0.51 0.85 2.68 ] | % |
| DBLR32M\_3a | Peak Period Jitter (rise) | Peak to peak value of cycle to cycle jitter measured for rise edge | [ – 118.5 – ] | ps |
| DBLR32M\_3b | Peak Period Jitter (fall) | Peak to peak value of cycle to cycle jitter measured for fall edge | [ – 43.65 – ] | ps |
| DBLR32M\_3c | Edge Jitter (rise) rms |  | [ – ] | ps |
| DBLR32M\_3d | Edge Jitter (fall) rms |  | [ – ] | ps |

Table 22: 32MHz Frequency Doubler

#### High Frequency Ring Oscillator

* Programmable frequency from 1-50 MHz. Operation is divided in high and low frequency modes.
* Applications
* ULP-Subsystem modules and the SOC in start-up state. Most likely will be used for ULP-TA-Subsystem while working independently.
* Calibration of low frequency clocks
* Typical Power consumption
* 34uA @ 75 Mhz (Maximum trim) from core supply
* 6uA @ 12MHz from core supply
* 475nA @ 500KHz from core supply
* Fast start up
* 2us in High frequency mode
* 10us in lowest frequency mode
* No runt pulses in output and stable clock available from first cycle

##### Low frequency, Low trim

| **Low Freq RO** **Low Trim(0):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | MHz | 233.8k | 456.8k | 1.183M |
| Startup | Sec | 5.435n | 10.52u | 11.57u |
| Duty Cycle | % | 49.41 | 49.61 | 51.56 |
| On Current | A | 206n | 474n | 3.583u |
| Off Current | A |  | 300n |  |
| Freq. Pushing | Khz/V | 116 | 200 | 286.5 |
| Jitter(jcc)(pp)\* | sec |  | 83.81n |  |
| Freq Resolution (avg) | Hz | 200K | 415K | 685K |

| **Low Freq RO** **Low Trim(0)(new):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | MHz | 157.2k | 323.3k | 815.8k |
| Startup | Sec | 9.49u | 23.8u | 45.06u |
| Duty Cycle | % | 49.95 | 50.53 | 51.57 |
| On Current(I\_VDD) | A | 24n | 67.18n | 599.3n |
| On Current(I\_AVDD) | A | 23.26n | 66.39n | 599.1n |
| Off Current | A |  |  |  |
| Freq. Pushing | Khz/V | 116 | 200 | 286.5 |
| Jitter(jcc)(pp)\* | sec |  | 83.81n |  |
| Freq Resolution (avg) | Hz | 200K | 415K | 685K |

##### Low frequency, High trim

| **Low Freq RO** **High Trim(127):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | Hz | 21.89M | 34M | 50.46M |
| Startup | Sec | 0.544u | 0.6u | 0.689u |
| Duty Cycle | % | 49.54 | 50.47 | 51.31 |
| On Current | A | 15.49u | 20u | 29.35u |
| Off Current | A |  | 300n |  |
| Freq. Pushing | Mhz/V | 7.95 | 10 | 16 |
| Jitter(jcc)(pp)\* | sec |  | 635.9p |  |
| Freq. Resolution | Hz | 180K | 200K | 460K |

| **Low Freq RO** **High Trim(127)(new):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | Hz | 11.56M | 20.3M | 38.34M |
| Startup | Sec | 4.238u | 6.053u | 6.776u |
| Duty Cycle | % | 45.76 | 51.04 | 51.55 |
| On Current(I\_VDD) | A | 1.812u | 4.281u | 8.874u |
| On Current(I\_AVDD) | A | 1.87u | 4.422u | 9.162u |
| Off Current | A |  |  |  |
| Freq. Pushing | Mhz/V | 7.95 | 10 | 16 |
| Jitter(jcc)(pp)\* | sec |  | 635.9p |  |
| Freq. Resolution | Hz | 180K | 200K | 460K |

##### High frequency, Low trim

| **High Freq RO** **Low Trim(0):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | MHz | 7.785 | 12.54 | 21.63 |
| Startup | Sec | 6.3n | 3.245u | 3.421u |
| Duty Cycle | % | 47.71 | 48.39 | 51.03 |
| On Current | A | 3.43u | 6.006u | 14.34u |
| Off Current | A |  | 300n |  |
| Freq. Pushing | Mhz/V | 3.9 | 5 | 8.5 |
| Jitter(jcc)(pp)\* | sec |  | 2.3n |  |
| Freq Resolution (avg) | Hz | 362K | 620K | 960K |

| **High Freq RO** **Low Trim(0)(new):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | MHz | 3.954M | 7.932M | 15.51M |
| Startup | Sec | 10.83u | 17.1u | 20.26u |
| Duty Cycle | % | 49.38 | 51.59 | 52.5 |
| On Current(I\_VDD) | A | 339.8n | 944.5n | 3.213u |
| On Current(I\_AVDD) | A | 347.1n | 971.6n | 3.307u |
| Off Current | A |  |  |  |
| Freq. Pushing | Mhz/V | 3.9 | 5 | 8.5 |
| Jitter(jcc)(pp)\* | sec |  | 2.3n |  |
| Freq Resolution (avg) | Hz | 362K | 620K | 960K |

Table 7.3 - 8: High frequency, Low trim

##### High frequency, High trim

| **High Freq RO** **High Trim(127):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | MHz | 47.53 | 78.71 | 122.1M |
| Startup | Sec | 0.42u | 2u | 2.23u |
| Duty Cycle | % | 47 | 50.17 | 52.13 |
| On Current | A | 22.56u | 34.8u | 63u |
| Off Current | A |  | 300n |  |
| Freq. Pushing | Mhz/V | 24.55 | 25 | 52.6 |
| Jitter(jcc)(pp)\* | sec |  | 341p |  |
| Freq Resolution (avg) | Hz | 280K | 460K | 700K |

| **High Freq RO** **High Trim(127)(new):** | **Units** | **Min** | **Typ** | **Max** |
| --- | --- | --- | --- | --- |
| Frequency | MHz | 28.82M | 53.04M | 92.94M |
| Startup | Sec | 11.59u | 17.87u | 21.02u |
| Duty Cycle | % | 37.93 | 52.83 | 52.83 |
| On Current(I\_VDD) | A | 2.73u | 6.354u | 17.31u |
| On Current(I\_AVDD) | A | 2.813u | 6.568u | 17.88u |
| Off Current | A |  |  |  |
| Freq. Pushing | Mhz/V | 24.55 | 25 | 52.6 |
| Jitter(jcc)(pp)\* | sec |  | 341p |  |
| Freq Resolution (avg) | Hz | 280K | 460K | 700K |

Table 23: Ring Oscillator

### Analog Comparators

Analog comparators is a peripheral circuit that compares two analog voltage inputs and gives a logical output based on comparison.

There are 9 different inputs for each pin of comparator, and 2 of the 9 are external pin inputs.  
The following cases of comparison are possible

* Compare external pin inputs
* Compare external pin input to internal voltages.
* Compare internal voltages.

The comparator compares inputs p and n to produce an output, cmp\_out.  
p > n, cmp\_out = 1  
p < n, cmp\_out = 0

It consists of 2 comparators whose inputs can be programmed independently. The reference buffer and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

| **ID** | **Description** | **Parameter Description** | **[ Min Typ Max ]** | **Unit** |
| --- | --- | --- | --- | --- |
| CMP1 | Delay | Delay of the comparator | 45.6 68.52 116.4 | ns |
| CMP2 | Leakage current, VBATT | Current consumption when en\_cmp=0 | 1.52 3.31 20.48 | nA |
|  | Leakage current, vdd |  | 0.16 0.33 32.22 | nA |
|  | Leakage current, VDD\_ULP |  | 0.1 0.4 24.03 | nA |
| CMP3 | Quiescent current | Current consumption with all blocks enabled | 118.2 215.5 415.2 | uA |
| CMP4 | Average current at 32KHz | Current consumption with all blocks enabled, but enable toggles at 32KHz | 50.9 115.1 213.1 | uA |
| CMP5 | Input offset voltage | The minimum voltage difference required between inputs to make output high | -3.4 σ =1.25 3.1 | mV |
| CMP6 | Response time | The time delay from enable to output of comparator | 0.12 0.3 2.01 | us |
| CMP7 | hysteresis | hysteresis = 2'd1 | 46.15 56.88 71.33 | mV |
|  | hysteresis | hysteresis = 2'd3 | 74.41 91.91 115.8 | mV |
| CMP8 | Phase margin of ref buffer | CL=100fF | 55.53 63 70 | deg C |
| CMP9 | Settling time of ref buffer | CL=100fF | 0.32 0.67 1.39 | us |

Table 24: Analog Comparators

### Analog to Digital Convertor

* 12 bit precision ADC
* 68 dB SNR across all corners
* at 78.125kHz with 5MSPS @1.8V to 3.3 V.
* at 156.25kHz with 10MSPS @ 3.3V.
* Single ended mode/differential mode configuration
* Typical current consumption at 10MS/s is 2.5mA.
* Digital output has a latency of 2 clock cycles (1 clock cycle for noise averaging).

| **ID** | **Description** | **Parameter Description** | **Min** | **Typ.** | **Max** | **Units** |
| --- | --- | --- | --- | --- | --- | --- |
| 6 | Powerup\_3p3\_avdd  Powerup\_3p3\_dvdd  Powerup\_1p8\_avdd  Powerup\_1p8\_dvdd | input frequncy 100kHz at 5Msps and measure the average current across avdd and dvdd | 1.423m  51.42u  697u  50.14u | 1.457m  53.03u  731.8u  52.05u | 1.527m  113.3u  781.3u  110.6u | A |
| 7 | DNL |  |  | 1 |  | LSB |
| 8 | INL |  |  | 1.34 |  | LSB |
| 9 | ENOB\_single\_3p3  ENOB\_diff\_3p3  ENOB\_single\_1p8  ENOB\_diff\_1p8 |  | 10.25  9.621  11.13  11.10 | 11.12  11.04  11.47  11.27 | 11.47  11.25  11.52  11.49 | bits |
| 10 | SNDR\_single\_3p3  SNDR\_diff\_3p3  SNDR\_single\_1p8  SNDR\_diff\_1p8 |  | 63.44  59.68  68.79  68.59 | 68.69  68.22  69.73  69.6 | 70.81  69.52  71.13  70.93 | dB |
| 11 | SFDR\_single\_3p3  SFDR\_diff\_3p3  SFDR\_single\_1p8  SFDR\_diff\_1p8 |  | 70.31  69.77  75.07  72.16 | 73.75  74.41  79.99  76.94 | 79.53  78.55  80.54  79.27 | dB |
| 12 | Powdown\_3p3\_avdd  Powdown\_3p3\_dvdd  Powdown\_1p8\_avdd  Powdown\_1p8\_dvdd | input frequency 100kHz at 5Msps and measure the average current across avdd and dvdd | 34.29n  25.99p  7.583n  23.31p | 50.13n  128p  10.44n  127.8p | 2.337u  8.57n  713.1n  8.569n | A |
| 13 | Pulse mode i\_avdd  Pulse mode i\_dvdd | Enable power gate for 2 posedge of clock cycles and found the time taken in those three clock cycles along with current taken to enable and disable powergate at avdd and dvdd.(with pg\_en\_b on time as 1us with period of 100us) |  | 4.391u  188.9n |  | A |
| 14 | leakage current at dvdd in digital top | auxadc\_pg\_enb as 0 and measured the current at dvdd in auxadc\_dig\_top |  | 36.88n |  | A |
| 15 | Iavg\_dvdd\_pu | freq 5MHz and enable as 1 |  | 63.37u |  | A |
| 16 | Iavg\_avdd\_pu | freq 5MHz and enable as 1 |  | 1.672m |  | A |
| 17 | Iavg\_dvdd\_pd | freq 5MHz and enable as 0 |  | 8.44u |  | A |
| 18 | Iavg\_avdd\_pd | freq 5MHz and enable as 0 |  | 85.27n |  | A |

Table 25: Analog to Digital Convertor

### Digital to Analog Convertor

1. 10 bit precision DAC
2. 57 dB SNR across all corners at 100 kHz with 5MS/s.
3. Single ended voltage outputs
4. 1.8 to 3.6 volt supply operation.
5. Typical current consumption at 5MS/s is 1mA.

| **Testcase ID** | **Description** | **Parameter Description** | **[min typ max]** | **Units** |
| --- | --- | --- | --- | --- |
| 4 | Low voltage\_1p8  Low voltage\_2p5  Low voltage\_3p6 | Lowest output voltage vs Vbat | [243.6m 249.1m 257.2m] [338.8m 346.2m 356.9m] [487.9m 498.5m 513.4m] | V |
| 5 | Higher voltage\_1p8 Higher voltage\_2p5 Higher voltage\_3p6 | Highest output voltage vs Vbat | [1.538 1.547 1.554] [2.138 2.151 2.16] [3.08 3.098 3.111] | V |
| 6 | PowerupCurrent\_1p8  PowerupCurrent\_2p5  PowerupCurrent\_3p6 | average current consumption with load(50pF,5KOhm) vs Vbat | [673.6u 901.9u 1.275m] [765.3u 1.02m 1.449m] [905.4u 1.201m 1.715m] | A |
| 7 | STATIC DNL\_1p8  STATIC DNL\_2p5  STATIC DNL\_3p6 |  | [58.24m 88.35m 199.9m] [42.91m 71.45m 212.3m] [38.32m 73.89m 229.5m] | LSB |
| 8 | STATIC INL\_1p8  STATIC INL\_2p5  STATIC INL\_3p6 |  | [80.64m 126.9m 233.5m] [58.13m 94.29m 178.6m] [46.94m 76.11m 143m] | LSB |
| 9 | Voutpp\_1p8  Voutpp\_2p5  Voutpp\_3p6 | Output peak to peak vs Vbat | [1.28 1.298 1.31] [1.781 1.805 1.821] [2.57 2.6 2.623] | V |
| 10 | PSRR\_1p8  PSRR\_2p5  PSRR\_3p6 | PSRR at 100kHz vs Vbat | [-16.74 -16.62 -16.18] [-16.75 -16.66 -16.31] [-16.74 -16.65 -16.3] | dB |
| 11 | PowdownI\_1p8  PowdownI\_2p5  PowdownI\_3p6 | current when DAC is completely turned off vs Vbat | [1.459n 1.777n 372.4n] [2.274n 2.866n 442.7n] [58.37n 70.61n 736n] | A |
| 12 | SFDR\_1p8  SFDR\_2p5  SFDR\_3p6 | At an input frequency of 100kHz and sampling frequency of 5MHz , | [61.07 66.36 70.65] [67.95 70.29 71.35] [63.4 70.45 71.63] | dB |
| 13 | SNDR\_1p8  SNDR\_2p5  SNDR\_3p6 | At an input frequency of 100kHz and sampling frequency of 5MHz , | [53.49 57.19 60.18] [57.69 60.19 62.22] [56.8 60.29 62.75] | dB |
| 14 | ENOB\_1p8  ENOB\_2p5  ENOB\_3p6 | At an input frequency of 100kHz and sampling frequency of 5MHz , | [8.592 9.207 9.704] [9.291 9.705 10.04] [9.142 9.722 10.13] | bits |
| 15 | THD\_1p8 THD\_2p5 THD\_3p6 | At an input frequency of 100kHz and sampling frequency of 5MHz , | [-70.65 -66.36 -61.07] [-71.35 -70.29 -67.95] [-71.63 -70.45 -63.4] | dB |
| 16 | FSCurrent\_1p8  FSCurrent\_2p5  FSCurrent\_3p6 |  | [801.1u 1.086m 1.563m] [935.9u 1.263m 1.833m] [1.082m 1.544m 2.264m] | A |
| 17 | Settling Time\_1p8  Settling Time\_2p5  Settling Time\_3p6 |  | [73.5n 93.41n 115.9n] [76.11n 97.95n 119.4n] [78.38n 101.7n 120.2n] | s |
| 18 | Startup Time\_1p8  Startup Time\_2p5  Startup Time\_3p6 | endac\_in from 0 to 1 | [2.4u 2.612u 2.918u] [2.4u 2.607u 2.862u] [2.4u 2.61u 8.152u]] | s |
| 19 | leakage current at dvdd in digital top | auxdac\_pg\_enb as 0 | 72.26n | A |
| 20 | Iavg\_dvdd\_pu |  | 6.435u | A |
| 21 | Iavg\_avdd\_pu |  | 1.223m | A |
| 22 | Iavg\_dvdd\_pd |  | 5.046u | A |
| 23 | Iavg\_avdd\_pd |  | 76.25n | A |
| 24 | Iavg\_dvdd\_pd |  | 328.3n | A |
| 25 | Iavg\_avdd\_pd |  | 13.37n | A |

Table 26: Digital to Analog Convertor

### AUX LDO

This LDO gives **1.6V to 2.8V** Output voltage with a maximum load current of **25mA** with a dropout voltage of **300mV**. It is external compensated LDO which is stable for load current ranging from 0 to 25mA, with the load cap 1uF.

The LDO reference voltage is 1.2V.

#### 1.6V O/P, 25mA load current (VDD 2.1,3.6) ESR(100m, 500m)

| ID | Parameter | Min | Typ | Max | Unit |
| --- | --- | --- | --- | --- | --- |
| DC gain | DC Gain | 41 | 55 | 61 | dB |
| PM | Phase margin | 43 | 60 | 121 | deg C |
| GM | Gain Margin | 43 | 47 | 56 | dB |
| UGF | Unity Gain frequency or Phase margin frequency | 2.32 | 13 | 20.1 | MHz |
| GMF | Gain Margin Frequency | 0.8 | 1.13 | 1.39 | GHz |
| GMF/UGF | Ratio of GMF to UGF | 67 | 87 | 432 | - |
| VOUT | Output voltage | 1.60 | 1.61 | 1.61 | V |
| IQ | quiescent current | 55 | 77 | 100 | µA |
| I\_LEAK | The leakage current in the LDO when disabled | 0.9 | 4.77 | 127 | nA |
| I\_BYPASS | LDO current in Bypass mode | 1 | 5.5 | 160 | nA |
| T\_STARTUP | Time taken for vout to reach 95% of its stable value when a step enable is given to ldo | 13 | 15 | 15.8 | us |

Table 27: 6V O/P, 25mA load current (VDD 2.1,3.6) ESR(100m, 500m)

#### 1.6V O/P, 1nA load current (VDD 2.1,3.6)

| ID | Parameter | Min | Typ | Max | Unit |
| --- | --- | --- | --- | --- | --- |
| PM | Phase margin | 64 | 77 | 89 | deg C |
| VOUT | Output voltage | 1.61 | 1.62 | 1.64 | V |
| IQ | quiescent current | 31 | 53 | 73 | µA |

Table 28: 1.6V O/P, 1nA load current (VDD 2.1,3.6)

#### 2.8V O/P, 25mA load current (VDD 3.1,3.6)

| ID | Parameter | Min | Typ | Max | Unit |
| --- | --- | --- | --- | --- | --- |
| DC Gain | DC gain | 39 | 46 | 59 | dB |
| PM | Phase margin | 54 | 67 | 145 | deg C |
| GM | Gain Margin | 43 | 48 | 54 | dB |
| UGF | Unity Gain frequency or Phase margin frequency | 0.75 | 12.7 | 19.7 | MHz |
| GMF | Gain Margin Frequency | 1 | 1.14 | 1.42 | GHz |
| GMF/UGF | Ratio of GMF to UGF | 66 | 89 | 1.43k | - |
| VOUT | Output voltage | 2.784 | - | 2.795 | V |
| IQ | quiescent current | 65 | - | 103 | µA |
| I\_LEAK | The leakage current in the LDO when disabled | 0.9 | - | 127 | nA |
| I\_BYPASS | LDO current in Bypass mode | 1 | 5.5 | 160 | nA |
| T\_STARTUP | Time taken for vout to reach 95% of its stable value when a step enable is given to ldo | 23 | 27 | 31 | us |

Table 29: 2.8V O/P, 25mA load current (VDD 3.1,3.6)

### Opamp

The opamps top consists of 3 general purpose Operational Amplifiers (OPAMP) offering rail-to-rail inputs and outputs.  
The opamps can be configured as:

1. Unity gain amplifier
2. Trans-Impedance Amplifier (TIA)
3. Non-inverting Programmable Gain Amplifier (PGA)
4. Inverting Programmable Gain Amplifier (PGA)
5. Non-inverting Programmable hysteresis comparator
6. Inverting Programmable hysteresis comparator
7. Cascaded Non-Inverting PGA
8. Cascaded Inverting PGA
9. Two opamps Differential Amplifier
10. Instrumentation Amplifier

* 7, 8, 9 are configured by cascading 2 opamps.
* 10 is configured by cascading 3 op-amps.

| Parameter | Symbol | Test Conditions | min | typical | max | units |
| --- | --- | --- | --- | --- | --- | --- |
| Input Voltage range | Vin |  | gnd |  | vdd |  |
| output voltage range | Vo | 1mA, source or sink | 0.1 |  | vdd-0.1 | V |
| output current capability, source or sink | Iout | 0.5<Vout<vdd-0.5 | 4 |  |  | mA |
| Input offset voltage | Vos | power mode = high | -284 | -126 | 32 | uV |
|  |  | power mode = low | -106 | -25 | 26 | uV |
| Input offset voltage drift with temperature | TCVos | power mode = high | 0.18 | 0.49 | 1.87 | uV/C |
|  |  | power mode = low | 0.04 | 0.08 | 0.48 | uV/C |
| Gain error, unity gain buffer mode, RL=1Kohm | Ge1 | power mode = high | -0.33 | -5m | 0.01 | % |
|  |  | power mode = low | -0.24 | -6.8m | 0.04 | % |
| Phase margin, in UGB mode | PM | power mode = high | 49.91 | 58.87 | 82.1 | deg C |
|  |  | power mode = low | 43.78 | 63.08 | 85.74 | deg C |
| Gain-bandwidth product | GBW | power mode = high | 8.05 | 16.97 | 24.06 | MHz |
|  |  | power mode = low | 4.16 | 7.64 | 13.07 | MHz |
| Startup time |  | power mode = high | 0.29 | 0.5 | 1.47 | us |
|  |  | power mode = low | 0.45 | 0.96 | 2.18 | us |
| Settling time |  | power mode = high | 47 | 91 | 182 | ns |
|  |  | power mode = low | 116 | 256 | 570 | ns |
| Total Harmonic Distortion, at 100KHz (UGB mode) | THD | power mode = high | -99 | -86.6 | -65.26 | dB |
|  |  | power mode = low | -92.5 | -85.4 | -54 | dB |
| Total Harmonic Distortion, at 100KHz (Non inv amp mode, gain = 13.5) | THD | power mode = high | -82.57 | -80.65 | -65.78 | dB |
|  |  | power mode = low | -78.64 | -76.47 | -62.49 | dB |
| Power supply rejection ratio | PSRR | power mode = high | 85.85 | 148 | 179 | dB |
|  |  | power mode = low | 85.93 | 148 | 179.1 | dB |
| Common mode rejection ratio | CMRR | power mode = high | 52.7 | 131.9 | 131.9 | dB |
|  |  | power mode = low | 38.89 | 130 | 170 | dB |
| Quiescent current | Idd | power mode = high | 446u | 946u | 1.58m | A |
|  |  | power mode = low | 157u | 327u | 614u | A |
| Leakage current (opamps\_top) | Ileak |  | 14 | 25 | 378 | nA |
| Output integrated noise | en | power mode = high | 28.61 | 33.03 | 53.96 | uV |
|  |  | power mode = low | 29.7 | 39.18 | 55.98 | uV |
| Input offset voltage (monte carlo) | Vos | power mode = high | -6.13 | 2.13(std) | 4.7 | mV |
|  |  | power mode = low | -4.96 | 1.78(std) | 3.97 | mV |
| Settling time with gain change (inv amp mode from min to max gain) |  | power mode = high | 2.145u | 3.241u | 5.702u | s |
|  |  | power mode = low | 2.874u | 4.461u | 7.811u | s |

Table 30: Opamp

### Cap Sensor

The capacitance sensor can detect changes in the input capacitance and represent it in the form of changes in raw counts. The increase in input capacitance is an indication of the presence of a human body near the touch panel connected to the PCB. The increased capacitance should be detected as an increase in the raw counts.

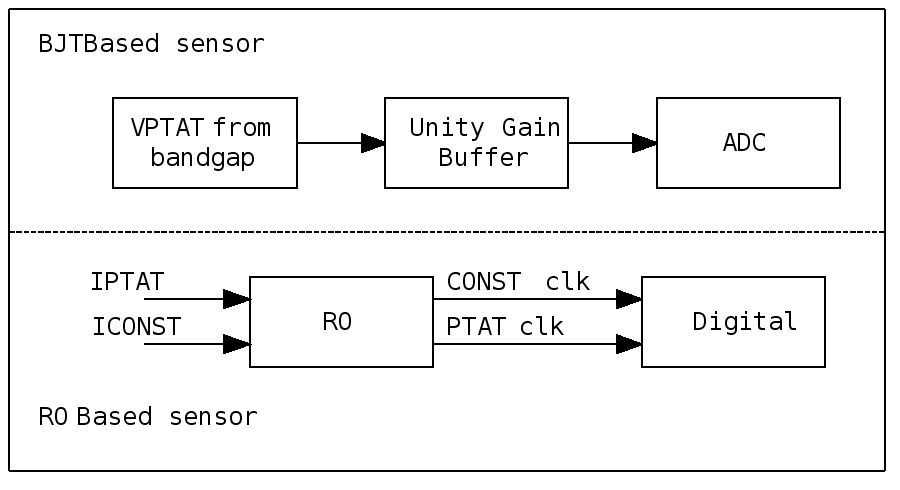
This consists of 8 input channels.

| **Description** | **Parameter Description** | **/[ min typ max]** | **Units** |
| --- | --- | --- | --- |
| Leakage current | Current consumption when disabled. capsens\_comp\_en =0 | 2.5 4.9 120 | nA |

Table 31: Cap Sensor

### Temperature Sensor

* Consist of RO based and bjt based temp sens.
* Generate PTAT Voltage from BJT based band gap.
* Buffered PTAT voltage is given at ADC Input.
* Output of the ADC is linear function of temperature.
* Generate Temperature dependent and independent clock.
* Digital logic to convert the output clock to temperature



BJT based sensor works for temperature range from -40º C to 125º C and voltage variation from 1.8V to 3.3V. It outputs the digital word having resolution of nearly 1º C. The conversion time is 2clock cycle of ADC after turning ON the temperature sensor. Typically, the block consumes 110uA of current and leakage current is 800pA.  
The RO based sensor will output 2 clocks i.e. one varies linearly with temperature and other is independent of temperature. We are counting the PTAT clock cycle in the fixed duration set by the other constant clock and this count value is proportional to temperature. Current consumption of RO based sensor is 5uA and leakage of nearly 1.15nA.

#### RO based Temp sensor Specs

| ID | Parameter | [ Min Typ Max ] | Unit |
| --- | --- | --- | --- |
| f1 | Frequency of constant clock(PVT) | [82.06k 101.1k 137.1k] | Hz |
| f2 | Frequency of PTAT clock(PVT) | [81.3k 105.9k 141k] | Hz |
| f2/f1 | Ratio of count | [882.154m 1.048 1.257] |  |
| Iq | quiescent current | [ 3.8u 4.95u 7.3u ] | A |
| I\_leak | The leakage current in the Tempsens when disabled | 1.15n | A |
| Settling Time f1 | Settling time for constant clock | [4.96u 12u 28.65u] | Sec |
| Settling Time f2 | settling time for PTAT clock | [4.79u 18.98u 40u] | Sec |
| Sensor Gain | Gain is the average slope of F2/F1 | [2.01 2.274 2.488] | m/deg C |
| Accuracy | maximum variation in F2/F1 across corners. Report at T=-40º, 25º, 120º | [5.5 0 8]\* | deg C |
| Non Linearity | Measured deviation from straight line fit. | 3 | deg C |
| Line Regulation(vddulp) | Swept supply voltage and measured variation in F1/F2 Reported at T=25º C | [0.092m(-40) 0.028m 0.162m] |  |
| Line Regulation(vbatt) | Swept supply voltage and measured variation in F1/F2 Reported at T=25º C | [2.08m 1.583m 7.138m] |  |

Table 32: RO based Temp sensor Specs

**Note:** All Results are at 3.3V (VBATT) and 1.1V (ULP). Supply effect is considered separately in line Regulation that too is reported for typical case.  
\*Accuracy is calculated by merging the slow, fast and typical curve at 25º C and checked the error at -40º C and 125º C. This step is part of calibration.

#### Simulation results for BJT based Temperature sensor

| **ID** | **Parameter** | **[ Min Typ Max ]** | **Unit** |
| --- | --- | --- | --- |
| PM buffer | Phase margin | [ 66 72 78 ] | deg C |
| Vout | Output voltage | [ 0.761 0.977 1.293 ] | V |
| Iq | quiescent current | [ 61u 106u 180u ] | A |
| I\_leak | The leakage current in the Tempsens when disabled | 800p | A |
| PM Error amp | Phase margin | [ 81 82 85 ] | deg C |
| Settling Time | Settling time of buffer | [-- 80n 100n] | Sec |
| Startup Time | Startup time of tempsens when step enable is given. | [-- 1u 5u] | Sec |
| Sensor Gain | Run swept DC operating across temperature. Measure average slope in mV/degC | [3.189 3.233 3.342] | mV/deg C |
| Accuracy | Run DC operating point across corners. Note maximum variation across corners. Report at T=-40,25,120 | [1.7(-40) 0 3(125)]\* | deg C |
| Non Linearity | Run swept DC and measure deviation from best fit straight line. | <1(linear) | deg C |
| Line Regulation | Sweep supply voltage and measure variation in output voltage. | [-0.4 0.6 8.497] | mV |
| Noise | Run noise analysis and report noise PSD. Report integrated noise. | [1.073m 1.477m 1.925m] | V |

Table 33: Simulation results for BJT based Temperature sensor

## AC Characteristics

### SDIO 2.0 Slave

#### Full Speed Mode

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| SDIO\_CLK | Tsdio | - | - | 25 | MHz |
| SDIO\_DATA, input setup time | Ts | 4 | - | - | ns |
| SDIO\_DATA, input hold time | Th | 1 | - | - | ns |
| SDIO\_DATA, clock to output delay | Tod | - | - | 13 | ns |
| Output Load |  | 5 |  | 10 (40 TBD) | pF |

Table 34: AC Characteristics SDIO 2.0 Full Speed Mode

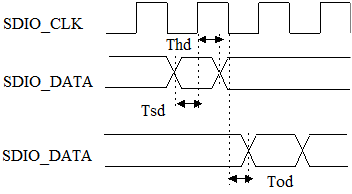


Figure 2: Interface Timing Diagram for SDIO Full Speed Mode

#### High speed mode

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| SDIO\_CLK | Tsdio | 25 | - | 50 | MHz |
| SDIO\_DATA, input setup time | Ts | 4 | - | - | ns |
| SDIO\_DATA, input hold time | Th | 1 | - | - | ns |
| SDIO\_DATA, clock to output delay | Tod | 2.5 | - | 13 | ns |
| Output Load |  | 5 |  | 10 (40 TBD) | pF |

Table 35: AC Characteristics SDIO 2.0 High Speed Mode

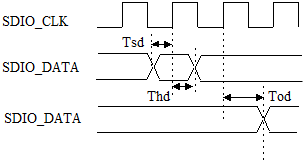


Figure 3: Interface Timing Diagram for SDIO High Speed Mode

### SPI

#### Low Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| SPI\_CLK | Tspi | 0 |  | 25 | MHz |
| SPI\_CS to output delay | Tcs | - | - | 7.5 | ns |
| SPI CS to input setup time | Tcst | 5 | - | - |  |
| SPI\_MOSI, input setup time | Ts | 1.33 | - | - | ns |
| SPI\_MOSI, input hold time | Th | 1 | - |  | ns |
| SPI\_MISO, clock to output delay | Tod | 2.5 | - | 8.7 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 36: AC Characteristics SPI Low Speed Mode

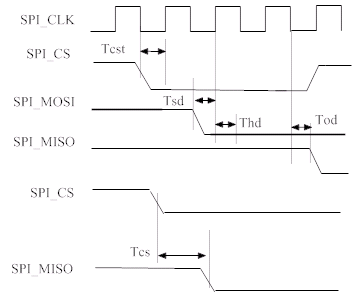


Figure 4: Interface Timings for SPI low-speed mode

#### High Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| SPI\_CLK | Tspi | 25 | - | 80 | MHz |
| SPI\_CS to output delay | Tcs | - | - | 7.5 | ns |
| SPI CS to input setup time | Tcst | 5 | - | - |  |
| SPI\_MOSI, input setup time | Ts | 1.3 | - |  | ns |
| SPI\_MOSI, input hold time | Th | 1.2 | - |  | ns |
| SPI\_MISO, clock to output delay | Tod | 2.5 | - | 8.7 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 37: AC Characteristics SPI high-speed mode

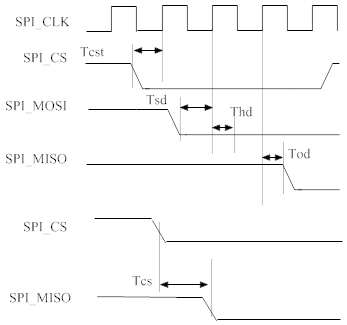


Figure 5: Interface Timings for SPI high-speed mode

#### Ultra High Speed Mode

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SPI\_CLK | Tspi |  | - | 120 | MHz |
| SPI\_CS to output delay | Tcs | - | - | 7.5 | ns |
| SPI CS to input setup time | Tcst | 1.3 | - | - |  |
| SPI\_MOSI, input setup time | Ts | 1.3 | - |  | ns |
| SPI\_MOSI, input hold time | Th | 1.2 | - |  | ns |
| SPI\_MISO, clock to output delay | Tod | 1.5 | - | 8.7 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 38: AC Characteristics SPI ultra high-speed mode

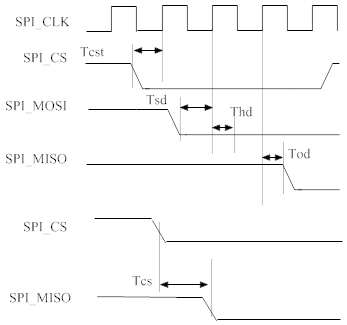


Figure 6: Interface timings for SPI ultra high-speed mode

### USB

#### Low Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| Rise Time | Trise | 75 |  | 300 | ns |
| Fall Time | Tfall | 75 | - | 300 | ns |
| Jitter | Jitter | - | - | 10 | ns |

Table 39: AC Characteristics USB Low speed mode

#### Full Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| Rise Time | Trise | 4 |  | 20 | ns |
| Fall Time | Tfall | 4 | - | 20 | ns |
| Jitter | Jitter | - | - | 1 | ns |

Table 40: AC Characteristics USB Full speed mode

#### High Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| Rise Time | Trise | 0.5 |  | - | ns |
| Fall Time | Tfall | 0.5 | - | - | ns |
| Jitter | Jitter | - | - | 0.1 | ns |

Table 41: AC Characteristics USB High speed mode

### UART

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| CLK |  | 0 |  | 20 | MHz |
| Output delay | Tod | 0 |  | 10 | ns |
| Input setup time | Ts | 0 |  | 5 | ns |
| Output load |  | 5 |  | 25 | pF |

Table 42: AC Characteristics UART

### GPIO pins

| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| tr | Rise time | Pin configured as output; SLEW = 1(fast mode) | 1.0 | - | 2.5 | ns |
| tf | Fall time | Pin configured as output; SLEW = 1(fast mode) | 0.9 | - | 2.5 | ns |
| tr | Rise time | Pin configured as output; SLEW = 0(standard mode) | 1.9 | - | 4.3 | ns |
| tf | Fall time | Pin configured as output; SLEW = 0(standard mode) | 1.9 | - | 4.0 | ns |
| tr | Rise time | Pin configured as input | 0.3 | - | 1.3 | ns |
| tf | Fall time | Pin configured as input | 0.2 | - | 1.2 | ns |

Table 7.5 - 1: GPIO pins

### Flash Memory

| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| Nendu | Endurance | Sector erase/program | 10000 | - | - | cycles |
| Page erase/program, page in large sector | 10000 | - | - | cycles |
| Page erase/program, page in small sector | 10000 | - | - | cycles |
| tret | Retention time | Powered | 10 | - | - | years |
| Unpowered | 10 | - | - | years |
| ter | Erase time | Page, sector or multiple consecutive sectors | - | 100 | - | ms |
| tprog | Programming time |  | - | 1 | - | ms |

Table 7.5 - 2: Flash Memory

### Ethernet

#### RMII Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| ETH\_RMII\_CLK |  | 0 |  | 50 | MHz |
| PPM |  | -50 |  | +50 |  |
| setup time  (ETH\_PHY\_TXD\_O[3:0], ETH\_PHY\_TXEN\_O, ETH\_PHY\_RXD\_I[3:0], ETH\_PHY\_RXER\_I, ETH\_PHY\_RXDV\_I) | Tsu | 4.05 | - | - | ns |
| hold time  (ETH\_PHY\_TXD\_O[3:0], ETH\_PHY\_TXEN\_O, ETH\_PHY\_RXD\_I[3:0], ETH\_PHY\_RXER\_I, ETH\_PHY\_RXDV\_I) | Th | 2 | - | - | ns |
| Output Load |  | 5 (25 TBD) |  | 10 | pF |
| Output Delay | Tod | 3 |  | 5.5 | ns |
| Output Rise Time(0.8V to 2V) |  | 1 |  | 5 | ns |
| Output Fall Time(2V to 0.8V) |  | 1 |  | 5 | ns |
| Duty Cycle |  | 35 |  | 65 | % |

Table 43: AC Characteristics Ethernet RMII mode

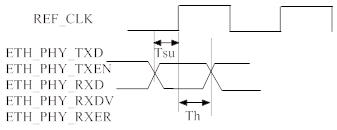


Figure 7: Interface Timings Ethernet RMII mode

### QSPI GPIO PADS

#### SDR mode - Full Speed Mode (posedge sampling) - M4

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| qspi\_clk | Tspi | 0 | - | 58 | MHz |
| qspi\_cs, to clock edge(this is achieved functionally) | Tcs | 8.6 | - |  | ns |
| qspi\_miso, setup time | Tsd | 1.53 | - | - | ns |
| qspi\_miso, hold time | Thd | 1.2 | - | - | ns |
| qspi\_mosi, clock to output valid | Tod | 0.5 | - | 2.4 | ns |
| Output Load |  | 5 |  | 10 (20 TBD) | pF |

Figure 8: AC Characteristics QSPI Peripheral Interface Full Speed Mode

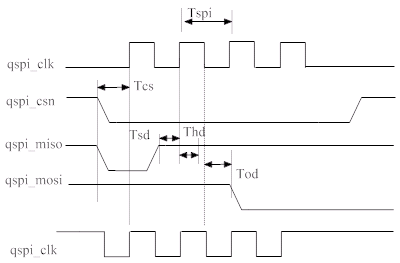


Figure 9: Interface Timings QSPI Peripheral Interface Full Speed Mode

#### SDR mode - High Speed Mode (negedge sampling) - M4

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| qspi\_clk | Tspi | 0 | - | 116 | MHz |
| qspi\_cs, to clock edge(this is achieved functionally) | Tcs | 4.3 | - |  | ns |
| qspi\_miso, setup time | Tsd | 1.53 | - | - | ns |
| qspi\_miso, hold time | Thd | 1.2 | - | - | ns |
| qspi\_mosi, clock to output valid | Tod | 0.5 | - | 2.4 | ns |
| Output Load |  | 5 |  | 10 (20 TBD) | pF |

Table 44: AC Characteristics – QSPI Peripheral Interface High Speed Mode

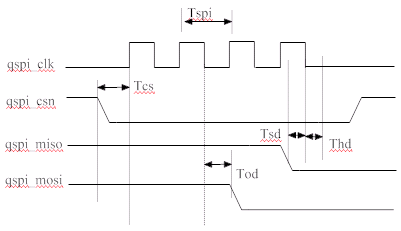


Figure 10:Interface Timings QSPI Peripheral Interface High Speed Mode

#### DDR Mode - M4

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| qspi\_clk | Tspi | 0 | - | 80 | MHz |
| qspi\_cs, to clock edge(this is achieved functionally) | Tcs | 6.2 | - |  | ns |
| qspi\_miso, setup time | Tsd | 1.4 | - | - | ns |
| qspi\_miso, hold time | Thd | 1 | - | - | ns |
| qspi\_mosi, clock to output valid | Tod | -0.9 | - | 4.9 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 45: AC Characteristics QSPI DDR Peripheral Interface

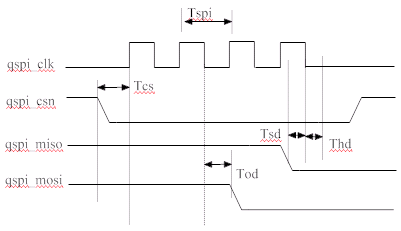


Figure 11: Interface Timings – QSPI DDR Peripheral Interface

### QSPI DDR Pads

#### SDR Mode - Full speed mode (posedge sampling) - M4

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| qspi\_clk | Tspi | 0 | - | 66 | MHz |
| qspi\_cs, to clock edge(this is achieved functionally) | Tcs | 7.5 | - |  | ns |
| qspi\_miso, setup time | Tsd | 5.5 | - | - | ns |
| qspi\_miso, hold time | Thd | 0 | - | - | ns |
| qspi\_cs, clock to cs output delay | Tcsod | 0 | - | 7 | ns |
| qspi\_mosi, clock to output valid | Tod | 0.5 | - | 7 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 46: AC Characteristics – QSPI Peripheral Interface DDR Pads Full Speed Mode

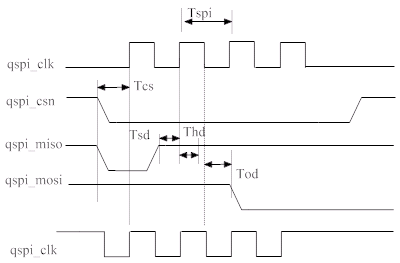


Figure 12: Interface Timings QSPI Peripheral Interface DDR Pads Full Speed Mode

#### SDR mode - High Speed Mode (negedge sampling)

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| qspi\_clk | Tspi | 0 | - | 133 | MHz |
| qspi\_cs, to clock edge(this is achieved functionally) | Tcs | 3.7 | - |  | ns |
| qspi\_miso, setup time | Tsd | 5.5 | - | - | ns |
| qspi\_miso, hold time | Thd | 0 | - | - | ns |
| qspi\_cs, clock to cs output delay | Tcsod | 0 | - | 7 | ns |
| qspi\_mosi, clock to output valid | Tod | 0.5 | - | 7 | ns |
| Output Load |  | 5 |  | 10 (20 TBD) | pF |

Figure 13:AC Characteristics QSPI Peripheral Interface DDR Pads High Speed Mode

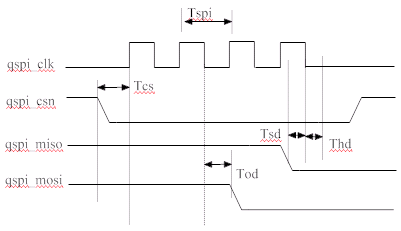


Figure 14: Interface Timings QSPI Peripheral Interface DDR Pads High Speed Mode

#### DDR Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| qspi\_clk | Tspi | 0 | - | 166 | MHz |
| qspi\_cs, to clock edge(this is achieved functionally) | Tcs | 3 | - |  | ns |
| qspi\_dqs to input data delay | Tsd | -0.1 | - | 0.7 | ns |
| qspi\_miso, hold time | Thd | 0 | - | - | ns |
| qspi\_cs, clock to cs output delay | Tcsod | 0.5 | - | 2.2 | ns |
| qspi\_mosi, clock to output valid | Tod | 0.5 | - | 2.2 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 47: AC Characteristics QSPI DDR Peripheral Interface for DDR pads

**Note:**

The above timing are w.r.t both edges.

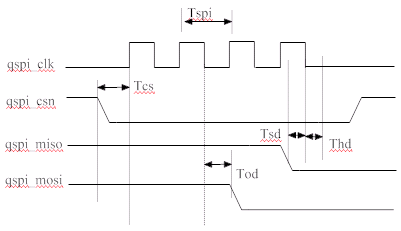


Figure 48: Interface Timings QSPI DDR Peripheral Interface for DDR pads

### I2C master and slave

#### Fast Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| scl | Ti2c | 100 | - | 400 | KHz |
| clock low period | Tlow | 1.3 | - | - | us |
| clock high period | Thigh | 0.6 | - | - | us |
| start condition, setup time | Tsstart | 0.6 | - | - | us |
| start condition, hold time | Thstart | 0.6 | - | - | us |
| data, setup time | Tsd | 100 | - | - | ns |
| stop condition, setup time | Tsstop | 0.6 | - | - | us |
| Output Load |  | 5 |  | 10 (40 TBD) | pF |

Table 49: AC Characteristics I2C Interface Fast-Speed Mode

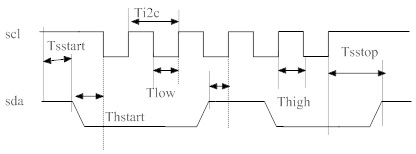


Figure 15Interface Timings I2C Interface Fast-Speed Mode

#### High Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| Scl | Ti2c | 0.4 | - | 3.4 | MHz |
| clock low period | Tlow | 160 | - | - | ns |
| clock high period | Thigh | 60 | - | - | ns |
| start condition, setup time | Tsstart | 160 | - | - | ns |
| start condition, hold time | Thstart | 160 | - | - | ns |
| data, setup time | Tsd | 10 | - | - | ns |
| data, hold time | Thd | 0 | - | 70 | ns |
| stop condition, setup time | Tsstop | 160 | - | - | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 50: AC Characteristics I2C Interface High-Speed Mode

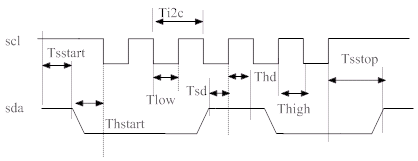


Figure 16:Interface Timings – I2C Interface High-Speed Mode

### M4 I2S/PCM master and slave

#### I2S/PCM Master mode

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| i2s\_clk | Tclk | 0 | - | 25 | MHz |
| i2s\_din,i2s\_ws setup time | Tsetup | 9 | - |  | ns |
| i2s\_din,i2s\_ws hold time | Thold | 0 | - | - | ns |
| i2s\_dout output delay | Tdout | 0 | - | 5 | ns |
| i2s\_dout output load | Tod | 5 |  | 10 | pF |

Table 51: AC Characteristics – I2S/PCM Peripheral Interface master mode

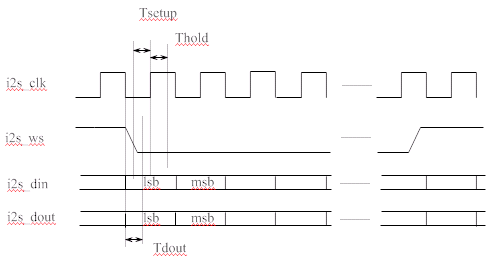


Figure 17: Interface Timings I2S Peripheral Interface master mode

#### I2S/PCM Slave mode

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| i2s\_clk | Tclk | 0 | - | 25 | MHz |
| i2s\_din,i2s\_ws setup time | Tsetup | 5 | - |  | ns |
| i2s\_din,i2s\_ws hold time | Thold | 0 | - | - | ns |
| i2s\_dout output delay | Tdout | 0 | - | 14 | ns |
| i2s\_dout output load | Tod | 5 |  | 10 | pF |

Table 52: AC Characteristic I2S/PCM Peripheral Interface slave mode

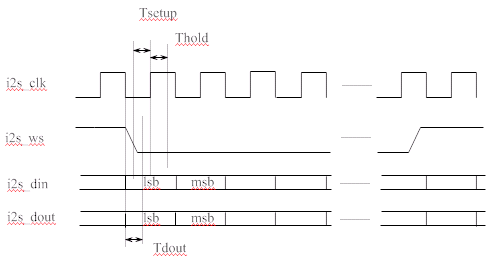


Figure 18: Interface Timings I2S Peripheral Interface slave mode

### ULP I2S/PCM master and slave

**I2S/PCM master**

Negedge driving and posedge sampling for I2S

posedge driving and negedge sampling for PCM

| Paramter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| i2s\_clk | Tclk | 0 | - | 20 | MHz |
| i2s\_din,i2s\_ws setup time w.r.t negedge | Tsetup | 15 | - |  | ns |
| i2s\_din,i2s\_ws hold time w.r.t negedge | Thold | 0 | - | - | ns |
| i2s\_dout output delay | Tdout | 0 | - | 16.7 | ns |
| i2s\_dout output load | Tod | 5 |  | 10 | pF |

Table 53: AC Characteristics – I2S/PCM Peripheral Interface Master Mode

### I2S/PCM Slave

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

| Paramter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| i2s\_clk | Tclk | 0 | - | 20 | MHz |
| i2s\_din,i2s\_ws setup time w.r.t negedge | Tsetup | 5 | - |  | ns |
| i2s\_din,i2s\_ws hold time w.r.t negedge | Thold | 0 | - | - | ns |
| i2s\_dout output delay | Tdout | 0 | - | 19 | ns |
| i2s\_dout output load | Tod | 5 |  | 10 | pF |

Table 54: AC Characteristics I2S/PCM Peripheral Interface Slave Mode

### M4 SSI Master/Slave

#### SSI Master Full Speed Mode

Negedge driving and posedge sampling

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SSI\_CLK | Tssi | 0 |  | 20 | MHz |
| SSI\_MISO, input setup time | Ts | 17 | - | - | ns |
| SSI\_MISO, input hold time | Th | 0 | - |  | ns |
| SSI\_CS, SSI\_MOSI, clock to output valid | Tod | 0 | - | 15 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 55: AC Characteristics SSI Master Peripheral Interface in Full Speed Mode

#### SSI Master High Speed Mode

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SSI\_CLK | Tssi | 0 |  | 40 | MHz |
| SSI\_MISO, input setup time | Ts | 17 | - | - | ns |
| SSI\_MISO, input hold time | Th | 2 | - |  | ns |
| SSI\_CS,SSI\_MOSI, clock to output valid | Tod | 1 | - | 15 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 56: AC Characteristics SSI Master Peripheral Interface in High Speed Mode

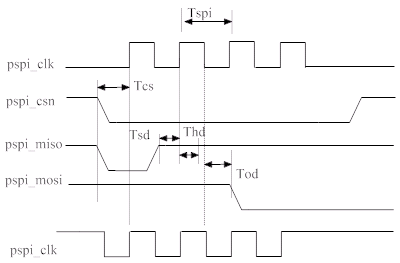


Figure 19: Interface Timings – SSI Master Peripheral Interface

#### SSI Slave Full Speed Mode

Negedge driving and posedge sampling

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| SSI\_CLK | Tssi | 0 |  | 20 | MHz |
| SSI\_MOSI,CS, input setup time | Ts | 20 | - | - | ns |
| SSI\_MOSI, input hold time | Th | 0 | - |  | ns |
| SSI\_MISO, clock to output delay | Tod | - | - | 24 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 57:AC Characteristics – SSI Slave Interface in Full Speed Mode

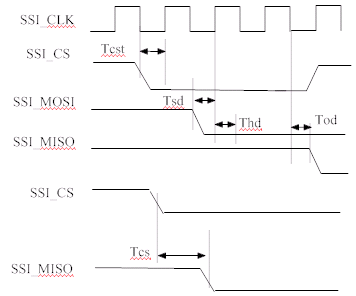


Figure 20: Interface Timings SSI Slave Interface

### ULP SSI Master

#### SSI Master Full Speed Mode

Negedge driving and posedge sampling

| Paramter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SSI\_CLK | Tssi | 0 |  | 10 | MHz |
| SSI\_MISO, input setup time | Ts | 20 | - | - | ns |
| SSI\_MISO, input hold time | Th | 0 | - |  | ns |
| SSI\_CS, SSI\_MOSI, clock to output valid | Tod | 0 | - | 15 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 58:AC Characteristics SSI Master Peripheral Interface in Full Speed Mode

#### SGPIO/MC-PWM/QEI/SCT Timer/SIO Interfaces

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| CLK |  | 0 |  | 20 | MHz |
| Output delay | Tod | 0 |  | 10 | ns |
| Input setup time | Ts | 0 |  | 5 | ns |
| Output load |  | 5 |  | 25 | pF |

Table 59: AC Characteristics – SGPIO/PWM/QEI Interface

Max/Min input delay (pad to flop) - 5ns/0ns  
Max/Min output delay (flop to pad) - 10ns/0ns  
Max Load - 25pF (for 12 inches of PCB)  
  
(Info - Max 20MHz signal frequency is assumed. 50ns period. Max frequency of QE inputs - 10KHz)

### USART

Maximum USART clock is 20MHz.

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| Interface CLK |  | 0 |  | 20 | MHz |
| Clock to Output delay | Tod | 0 |  | 10 | ns |
| Input setup time | Ts | 0 |  | 5 | ns |
| Output load |  | 5 |  | 25 | pF |

Table 60: Characteristics USART Interface

### GSPI master

#### Full Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| gspi\_clk | Tspi | 0 | - | 58 | MHz |
| gspi\_cs, to clock edge(this is achieved functionally) | Tcs | 4.16 | - |  | ns |
| gspi\_miso, setup time | Tsd | 1.66 | - | - | ns |
| gspi\_miso, hold time | Thd | 1.2 | - | - | ns |
| gspi\_cs, clock to cs output delay | Tcsod | 1 | - | 7.33 | ns |
| gspi\_mosi, clock to output valid | Tod | 1 | - | 7.33 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 61: AC Characteristics GSPI Peripheral Interface Full Speed Mode

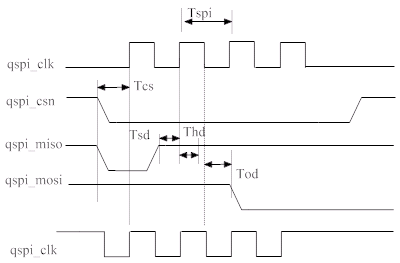


Figure 21: Interface Timings PSPI Peripheral Interface Full Speed Mode

#### High Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| gspi\_clk | Tspi | 0 | - | 116 | MHz |
| gspi\_cs, to clock edge(this is achieved functionally) | Tcs | 4.16 | - |  | ns |
| gspi\_miso, setup time | Tsd | 1.66 | - | - | ns |
| gspi\_miso, hold time | Thd | 1.2 | - | - | ns |
| gspi\_cs, clock to cs output delay | Tcsod | 1 | - | 7.33 | ns |
| gspi\_mosi, clock to output valid | Tod | 1 | - | 7.33 | ns |
| Output Load |  | 5 |  | 10 | pF |

Table 62: AC Characteristics GSPI Peripheral Interface High Speed Mode

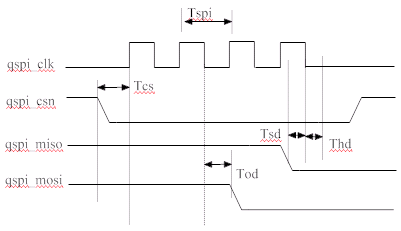


Table 63: Interface Timings GSPI Peripheral Interface High Speed Mode

### CAN interface

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| Interface CLK |  | 0 |  | 20 | MHz |
| Clock to Output delay | Tod | 0 |  | 10 | ns |
| Input setup time | Ts | 0 |  | 5 | ns |
| Output load |  | 5 |  | 25 | pF |

### SD memory host controller

#### Full Speed Mode

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| SMIH\_CLK | Tsdio | - | - | 26 | MHz |
| SMIH\_DATA, input to setup time | Ts | 6 | - | - | ns |
| SMIH\_DATA , input to hold time | Th | 2 | - | - | ns |
| SMIH\_DATA , clock to output delay | Tod | 0 | - | 14 | ns |
| Output Load |  | 5 |  | 10 (40 TBD) | pF |
| Voltage |  |  | 1.8/3.3 |  | V |

Table 64: AC Characteristics SMIH Interface full- speed mode

#### High Speed Mode

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SMIH\_CLK | Tsdio | 26 | - | 52 | MHz |
| SMIH\_DATA, input to setup time | Ts | 6 | - | - | ns |
| SMIH\_DATA , input to hold time | Th | 2 | - | - | ns |
| SMIH\_DATA , clock to output delay | Tod | 2.45 | - | 14 | ns |
| Output Load |  | 5 |  | 10(40 TBD) | pF |
| Voltage |  |  | 1.8/3.3 |  | V |

Table 65: AC Characteristics SMIH Interface high-speed mode

#### Ultra High Speed Mode

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SMIH\_CLK | Tsdio | 52 | - | 80 | MHz |
| SMIH\_DATA, input setup time (w.r.t input clock) | Ts | 3 | - | - | ns |
| SMIH\_DATA, input hold time | Th | 0.8 | - | - | ns |
| SMIH\_DATA, clock to output delay | Tod | 1.25 | - | 7.5 | ns |
| Output Load |  | 5 |  | 10 (20 TBD) | pF |
| Voltage |  |  | 1.8 |  | V |

Table 66: AC Characteristics SMIH Interface Ultra high-speed mode

### SMIH/MMC DDR Mode

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| SMIH\_CLK | Tsdio | 0 | - | 40 | MHz |
| SMIH\_DATA, input setup time (w.r.t input clock) | Ts | 3 | - | - | ns |
| SMIH\_DATA, input hold time | Th | 0.8 | - | - | ns |
| SMIH\_DATA, clock to output delay | Tod | 1.25 | - | 8 | ns |
| Output Load |  | 5 |  | 10 (20 TBD) | pF |
| Voltage |  |  | 1.8 |  | V |

Table 67: AC Characteristics SMIH DDR Interface

### CCI

#### SDR mode on GPIO pads -Master

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| CCI\_CLK | Tsdio | 0 | - | 85 | MHz |
| CCI\_DATA, input setup time (w.r.t input clock) | Ts | 1 | - | - | ns |
| CCI\_DATA, input hold time | Th | 1 | - | - | ns |
| CCI\_DATA, clock to output delay | Tod | 0 | - | 8 | ns |
| Output Load |  | 5 |  | 10 | pF |
| Voltage |  |  | 3.3/1.8 |  | V |

Table 68: AC Characteristics CCI Interface SDR mode for master

#### SDR mode on GPIO pads -Slave

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| CCI\_CLK | Tsdio | 0 | - | 85 | MHz |
| CCI\_DATA, input setup time (w.r.t input clock) | Ts | 2 | - | - | ns |
| CCI\_DATA, input hold time | Th | 0 | - | - | ns |
| CCI\_DATA, clock to output delay | Tod | 2 | - | 9 | ns |
| Output Load |  | 5 |  | 10 | pF |
| Voltage |  |  | 3.3/1.8 |  | V |

Table 69: AC Characteristics CCI Interface SDR mode for slave

#### DDR mode on GPIO pads -Master

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| CCI\_CLK | Tsdio | 0 | - | 55 | MHz |
| CCi\_DATA, input setup time (w.r.t input clock) | Ts | 2 | - | - | ns |
| CCI\_DATA, input hold time | Th | 1 | - | - | ns |
| CCI\_DATA, clock to output delay | Tod | 1.5 | - | 5 | ns |
| Output Load |  | 5 |  | 10 | pF |
| Voltage |  |  | 3.3/1.8 |  | V |

Table 70: AC Characteristics CCI Interface DDR mode for master

#### DDR mode on GPIO pads -Slave

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| CCI\_CLK | Tsdio | 0 | - | 55 | MHz |
| CCi\_DATA, input setup time (w.r.t input clock) | Ts | 2 | - | - | ns |
| CCI\_DATA, input hold time | Th | 1 | - | - | ns |
| CCI\_DATA, clock to output delay | Tod | 1.5 | - | 5 | ns |
| Output Load |  | 5 |  | 10 | pF |
| Voltage |  |  | 3.3/1.8 |  | V |

Table 71: SDR mode on DDR pads -Master

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| CCI\_CLK | Tsdio | 0 | - | 100 | MHz |
| CCI\_DATA, input setup time (w.r.t input clock) | Ts | 1.55 | - | - | ns |
| CCI\_DATA, input hold time | Th | 0.5 | - | - | ns |
| CCI\_DATA, clock to output delay | Tod | 0.5 | - | 4.85 | ns |
| Output Load |  | 5 |  | 10 | pF |
| Voltage |  |  | 3.3/1.8 |  | V |

Table 72: AC Characteristics CCI Interface DDR mode for master

#### SDR mode on DDR pads -Slave

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| --- | --- | --- | --- | --- | --- |
| CCI\_CLK | Tsdio | 0 | - | 100 | MHz |
| CCI\_DATA, input setup time (w.r.t input clock) | Ts | 1.55 | - | - | ns |
| CCI\_DATA, input hold time | Th | 0.5 | - | - | ns |
| CCI\_DATA, clock to output delay | Tod | 2 | - | 4.55 | ns |
| Output Load |  | 5 |  | 10 | pF |
| Voltage |  |  | 3.3/1.8 |  | V |

Table 73:AC Characteristics SDR mode for slave

### M4 JTAG

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| TCK period | Ttck |  |  | 20 | MHz |
| Setup | Tsetup | 5 | - | - | ns |
| Hold | Thold | 4 | - | - | ns |
| Output Delay | Tod | 0 |  | 38.5 | ns |
| Output Load |  | 5 |  | 10 (25 TBD) | pF |

Table 74: AC Characteristics JTAG Debug Interface

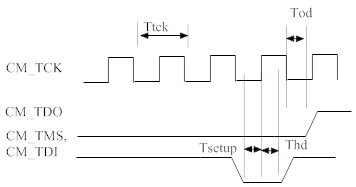


Figure 22: Interface Timings M4 JTAG Debugger

### M4 TRACE

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Unit** |
| TRACECLK Period | Tclk | 0 |  | 100 | MHz |
| Output Delay | Tod | 0.8 |  | 8 | ns |
| Output Load |  | 5 |  | 10 (25 TBD) | pF |

Table 75:AC Characteristics M4 TRACE PORT

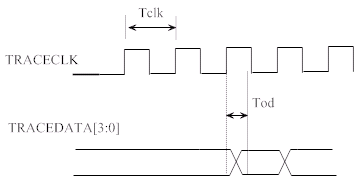


Figure 23: Interface Timings – M4 TRACE PORT

## RF Characteristics[[3]](#footnote-3)

### WLAN 2.4 GHz Transmitter Characteristics

| **Parameter** | **Condition** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM | 1 Mbps DSSS |  | 20 |  | dBm |
| 2 Mbps DSSS |  | 20 |  | dBm |
| 5.5 Mbps CCK |  | 20 |  | dBm |
| 11 Mbps CCK |  | 20 |  | dBm |
| 6 Mbps OFDM |  | 20 |  | dBm |
| 9 Mbps OFDM |  | 20 |  | dBm |
| 12 Mbps OFDM |  | 20 |  | dBm |
| 18 Mbps OFDM |  | 20 |  | dBm |
| 24 Mbps OFDM |  | 20 |  | dBm |
| 36 Mbps OFDM |  | 19 |  | dBm |
| 48 Mbps OFDM |  | 18 |  | dBm |
| 54 Mbps OFDM |  | 17 |  | dBm |
| MCS0 Mixed Mode |  | 20 |  | dBm |
| MCS1 Mixed Mode |  | 20 |  | dBm |
| MCS2 Mixed Mode |  | 20 |  | dBm |
| MCS3 Mixed Mode |  | 20 |  | dBm |
| MCS4 Mixed Mode |  | 19 |  | dBm |
| MCS5 Mixed Mode |  | 18 |  | dBm |
| MCS6 Mixed Mode |  | 17 |  | dBm |
| MCS7 Mixed Mode |  | 15 |  | dBm |
| Transmit Power for 40MHz Bandwidth, compliant with IEEE mask and EVM | MCS0 Mixed Mode |  | 18 |  | dBm |
| MCS7 Mixed Mode |  | 13 |  | dBm |

Table 76: WLAN 2.4 GHz Transmitter Characteristics

### WLAN 2.4 GHz Receiver Characteristics

| **Parameter** | **Condition** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| Sensitivity for 20MHz Bandwidth | 1 Mbps DSSS |  | -97.0 |  | dBm |
| 2 Mbps DSSS |  | -92.0 |  | dBm |
| 5.5 Mbps CCK |  | -89.5 |  | dBm |
| 11 Mbps CCK |  | -88.0 |  | dBm |
| 6 Mbps OFDM |  | -93.0 |  | dBm |
| 9 Mbps OFDM |  | -91.5 |  | dBm |
| 12 Mbps OFDM |  | -90.5 |  | dBm |
| 18 Mbps OFDM |  | -88.5 |  | dBm |
| 24 Mbps OFDM |  | -85.5 |  | dBm |
| 36 Mbps OFDM |  | -82.0 |  | dBm |
| 48 Mbps OFDM |  | -78.0 |  | dBm |
| 54 Mbps OFDM |  | -76.0 |  | dBm |
| MCS0 Mixed Mode |  | -91.5 |  | dBm |
| MCS1 Mixed Mode |  | -89.5 |  | dBm |
| MCS2 Mixed Mode |  | -87.0 |  | dBm |
| MCS3 Mixed Mode |  | -84.5 |  | dBm |
| MCS4 Mixed Mode |  | -81.0 |  | dBm |
| MCS5 Mixed Mode |  | -76.5 |  | dBm |
| MCS6 Mixed Mode |  | -74.5 |  | dBm |
| MCS7 Mixed Mode |  | -73.0 |  | dBm |
| Sensitivity for 40MHz Bandwidth | MCS0 Mixed Mode |  | -88.0 |  | dBm |
| MCS7 Mixed Mode |  | -69.5 |  | dBm |
| Maximum Input Level for PER below 10% | 1 Mbps DSSS |  | -4 |  | dBm |
| 11 Mbps CCK |  | -4 |  | dBm |
| 54 Mbps OFDM |  | -10 |  | dBm |
| MCS0 Mixed Mode |  | -10 |  | dBm |
| Adjacent Channel Rejection | 1 Mbps DSSS |  | 35 |  | dB |
| 11 Mbps CCK |  | 32 |  | dB |
| 6 Mbps OFDM | 32 |  |  | dB |
| 54 Mbps OFDM | 18 |  |  | dB |
| PER Floor |  |  |  | 0.1 | % |
| RSSI Accuracy |  |  | ±1 | ±3 | dB |

Table 77: WLAN 2.4 GHz Receiver Characteristics

### Bluetooth Receiver Characteristics

| **Parameter** | **Condition** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| Sensitivity | BR (1 Mbps), 339 bytes, DH5 Packet |  | -94.0 |  | dBm |
| EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet |  | -92.0 |  | dBm |
| EDR3 (3 Mbps), 1020 bytes, 3-DH5 Packet |  | -84.0 |  | dBm |
| LE (1 Mbps), 37 bytes, Advertising Channel |  | -96 |  | dBm |
| Maximum Input Level | BR, EDR2, EDR3 |  | -20 |  | dBm |
| LE |  | -8 |  | dBm |
| BER Floor |  |  |  | 1e-4 | % |
| C/I Performance | BR, co-channel |  | 5 |  | dB |
| BR, adjacent +1 MHz |  | -4 |  | dB |
| BR, adjacent -1 MHz |  | -7 |  | dB |
| BR, adjacent +2 MHz |  | -31 |  | dB |
| BR, adjacent -2 MHz (image) |  | -25 |  | dB |
| BR, adjacent >=|±3| MHz |  | -41 |  | dB |
| EDR2, co-channel |  | 10 |  | dB |
| EDR2, adjacent +1 MHz |  | -6 |  | dB |
| EDR2, adjacent -1 MHz |  | -4.5 |  | dB |
| EDR2, adjacent +2 MHz |  | -32 |  | dB |
| EDR2, adjacent -2 MHz (image) |  | -23 |  | dB |
| EDR2, adjacent >=|±3| MHz |  | -42 |  | dB |
| EDR3, co-channel |  | 19 |  | dB |
| EDR3, adjacent +1 MHz |  | 3 |  | dB |
| EDR3, adjacent -1 MHz |  | 4 |  | dB |
| EDR3, adjacent +2 MHz |  | -26 |  | dB |
| EDR3, adjacent -2 MHz (image) |  | -16 |  | dB |
| EDR3, adjacent >=|±3| MHz |  | -37 |  | dB |
| LE, co-channel |  | 21 |  | dB |
| LE, adjacent +1 MHz |  | 15 |  | dB |
| LE, adjacent -1 MHz |  | 15 |  | dB |
| LE, adjacent +2 MHz |  | -17 |  | dB |
| LE, adjacent -2 MHz |  | -17 |  | dB |
| LE, adjacent >=|±3| MHz |  | -27 |  | dB |

Table 78: Bluetooth Receiver Characteristics

### Bluetooth Transmitter Characteristics

| **Parameter** | **Condition** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| Transmit Power | BR, EDR |  | 20 |  | dBm |
| LE |  | 20 |  | dBm |
| Power Control Step | BR, EDR |  | 1 |  | dB |
| Adjacent Channel Power |M-N| = 1 | EDR |  | -30 |  | dB |
| Adjacent Channel Power |M-N| = 2 | BR |  | -24 |  | dB |
| EDR |  | -25 |  | dB |
| LE |  | -22 |  | dB |
| Adjacent Channel Power |M-N| > 2 | BR |  | -42 |  | dB |
| EDR |  | -45 |  | dB |
| LE |  | -40 |  | dB |

Table 79: Bluetooth Transmitter Characteristics

### ZigBee Performance

| **Parameter** | **Condition** | **Min.** | **Typ.** | **Max.** | **Units** |
| --- | --- | --- | --- | --- | --- |
| Receive Sensitivity with 1% PER limit | 250 kbps, 21 bytes packet size |  | -102 |  | dBm |
| Receiver Maximum Input Level | 250 kbps, 21 bytes packet size |  | -10 |  | dBm |
| C/I Performance  (250 kbps, 21 bytes packet size) | Adjacent Channel +5 MHz |  | 38 |  | dB |
| Adjacent Channel -5 MHz |  | 25 |  | dB |
| Alternate Channel +10 MHz |  | 45 |  | dB |
| Alternate Channel -10 MHz |  | 45 |  | dB |
| Frequency Error Tolerance |  |  | ±100 |  | ppm |
| Symbol Error Rate Tolerance |  |  | ±100 |  | ppm |
| Transmit Power |  |  | 20 |  | dBm |

Table 80:ZigBee Performance

## Wakeup Receiver

The wake-up receiver is an ultra low power OOK receiver designed to periodically sample the RF band and correlate for a wake-up pattern that would wake-up the main SoC upon detection.

* Operates in the 2.4 GHz frequency band.
* Works on 1.1 V +/-10% supply
* Gain and bandwidth are programmable.
* Down-converts RF to IF.
* The receiver uses uncertain IF with +/-1MHz post calibration variability over +/-10% supply and -40 to 125C temp variation
* Transmitter sends a narrowband signal or CW centered around 8MHz uncertain IF. i.e, fc\_tx = fc\_rx + 4MHz.
* LO generated using VCO
* Programmable Duty cycling of blocks and Programmable correlation length to achieve tradeoff between sensitivity, average power consumption and wakeup latency
* Correlation to ensure robust pattern detection and optimum low-bit rate message reception.

# RS14100 Ordering Information

## Module Marking Information

The figure below illustrates the marking on the modules.



Figure 24: Module Marking Information

The table below explains the marking on the modules.

| **Marking** | | **Description** |
| --- | --- | --- |
| Model | RS14100 SB  RS14100 DB | Model Numbers for Single-band and Dual-band modules |
| Firmware | RS14100W-SBT0-345S-BA1N | Software/Firmware supported – refer to the [Part Ordering](#_Part_Ordering_Options) Section for more details. |
| FCC | FCC ID TBD | FCC Grant IDs for Single-band and Dual-band modules. |
| IC | IC ID TBD | IC Grant IDs for Single-band and Dual-band modules. |
| Lot Code Information | ABC-WWYY | ABC – Internal usage  WW – Week of manufacture  YY – Year of manufacture |
| Compliance Marks |  | FCC Compliance Mark |
|  | CE Compliance Mark |

Table 81: Module Marking Information

## Package Options

### Module Packages

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Package Code** | **Package Type, Pins** | **Dimensions (mm)** | **Frequency Band** | **Integrated Antenna** |
| CA0 | LGA,173 | 9.1 x 9.8 x 1.2 | Single Band (2.4 GHz) | No |
| CC0 | LGA,173 | 9.1 x 9.8 x 1.2 | Dual Band (2.4 GHz/5 GHz) | No |
| CA1 | LGA,107 | 15 x 15.7 x 2.2 | Single Band (2.4 GHz) | Yes |
| CC1 | LGA,107 | 15 x 15.7 x 2.2 | Dual Band (2.4 GHz/5 GHz) | Yes |
| B00 | LGA,126 | 4.63 x 7.8 x 1.2 | Single Band (2.4 GHz) | No |

Table 82: Module Packages

### Chip Packages

|  |  |  |  |
| --- | --- | --- | --- |
| **Package Code** | **Package Type, Pins** | **Dimension, Pitch (mm)** | **Frequency Band** |
| WMS | WLCSP, 79 | 3.5 x 3.6 x 0.5, 0.4 | Single Band (2.4 GHz) |
| QMS | QFN, 84 | 7 x 7 x 0.85, 0.5 | Single Band (2.4 GHz) |
| BTS | BGA,196 | 6 x 6.3 x 0.9,0.5 | Single Band (2.4 GHz) |

Table 83: Chip Packages

## Part Ordering Options

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Part Number** | **Wireless** | **Other Wireless** | **CPU Freq** | **Flash+RAM** | **Chip Packages (ppg)** | **Module Packages (ppg)** |
| RS14100-0B00-140F-ppg | BT5 | - | 100 MHz | 4 MB+208 KB | QMS, WMS,BTS | B00 |
| RS14100-SB00-140F-ppg | SBW+BT5 | - | 100 MHz | 4 MB+208 KB | QMS, WMS,BTS | B00, CA0, CA1 |
| RS14100-SBT0-140F-ppg | SBW+BT5+ZB/THR | - | 100 MHz | 4 MB+208 KB | QMS, WMS,BTS | B00, CA0, CA1 |
| RS14100-SB00-240F-ppg | SBW+BT5 | - | 180 MHz | 4 MB+208 KB | QMS, WMS,BTS | B00, CA0, CA1 |
| RS14100-SBT0-24SF-ppg2 | SBW+BT5+ZB/THR | - | 180 MHz | 4 MB+208 KB | QMS, WMS,BTS | B00, CA0, CA1 |
| RS14100-SBT1-24SF-ppg2 | SBW+BT5+ZB/THR | Wake-Fi | 180 MHz | 4 MB+208 KB | QMS, WMS,BTS | B00, CA0, CA1 |
| RS14100-DB00-140F-ppg | DBW+BT5 | - | 100 MHz | 4 MB+208 KB | - | CC0, CC1 |
| RS14100-DBT0-140F-ppg | DBW+BT5 | - | 100 MHz | 4 MB+208 KB | - | CC0, CC1 |
| RS14100-DB00-240F-ppg2 | DBW+BT5 | - | 180 MHz | 4MB+208KB |  | CC0, CC1 |
| RS14100-DBT0-240F-ppg2 | DBW+BT5+ZB/THR | - | 180 MHz | 4MB+208KB |  | CC0, CC1 |
| RS14100-DBT1-240F-ppg2 | DBW+BT5+ZB/THR | Wake-Fi | 180 MHz | 4MB+208KB | - | CC0, CC1 |

**Note:**

Replace 'ppg' with desired SoC / Module Packages code;**SBW:** Single Band Wi-Fi (2.4 GHz)**; DBW:** Dual Band Wi-Fi (2.4/5 GHz)**; ZB:** ZigBee**; THR:** Thread

Table 84: Part-Ordering Options

**Notes**:

Subject to change. Contact Redpine Signals for final numbers. Contact Redpine for availability.

# RS14100 Package Descriptions

## Module Packages

### Modules with package Codes CC0/CA0

#### Mechanical Characteristics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (L X W X H)** | **Units** |
| Module Dimensions | 9.1 x 9.8 x 1.2 | mm |
| Tolerance | ±0.2 | mm |

Table 85: Mechanical Characteristics-CC0/CA0

#### Mechanical Drawing

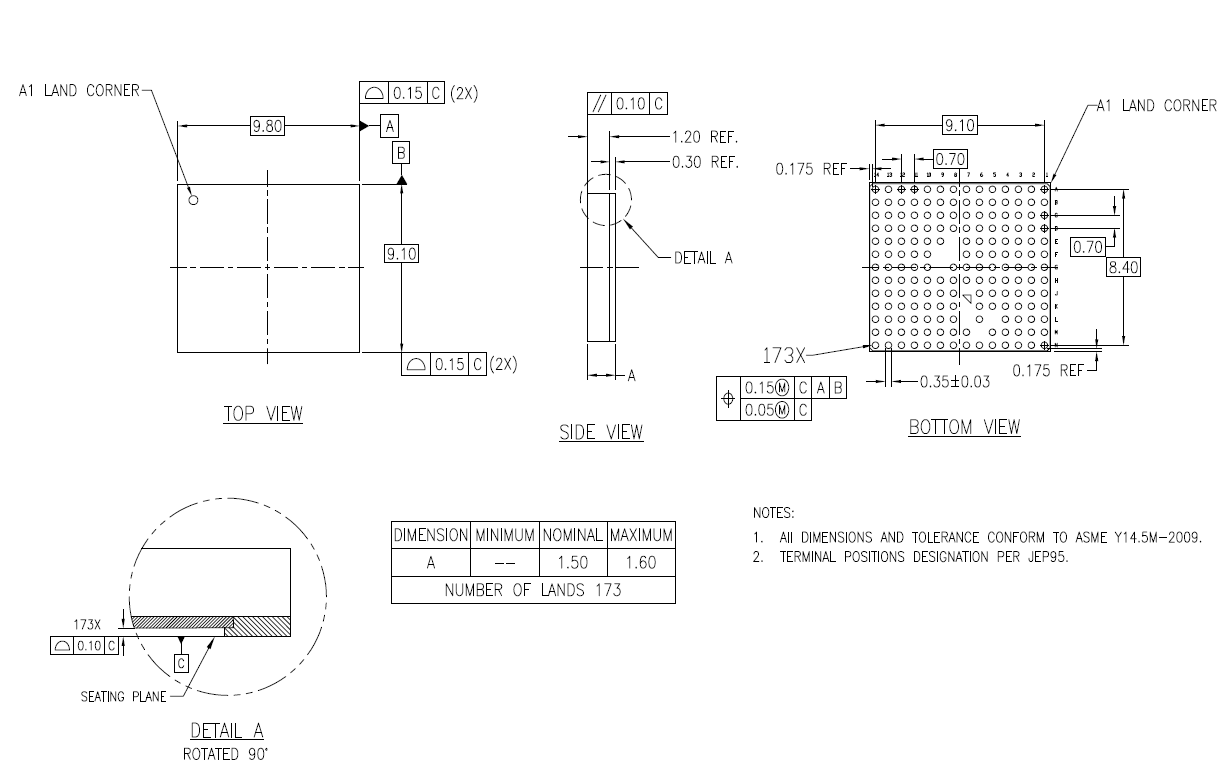


Figure 25: Mechanical Drawing-CC0/CA0

#### Pin Locations

|  |  |  |
| --- | --- | --- |
| **Pin Number** | **X-Coordinate** | **Y-Coordinate** |
| A1 | ‐4.55 | 4.2 |
| A2 | ‐3.85 | 4.2 |
| A3 | ‐3.15 | 4.2 |
| A4 | ‐2.45 | 4.2 |
| A5 | ‐1.75 | 4.2 |
| A6 | ‐1.05 | 4.2 |
| A7 | ‐0.35 | 4.2 |
| A8 | 0.35 | 4.2 |
| A9 | 1.05 | 4.2 |
| A10 | 1.75 | 4.2 |
| A11 | 2.45 | 4.2 |
| A12 | 3.15 | 4.2 |
| A13 | 3.85 | 4.2 |
| A14 | 4.55 | 4.2 |
| B1 | ‐4.55 | 3.5 |
| B2 | ‐3.85 | 3.5 |
| B3 | ‐3.15 | 3.5 |
| B4 | ‐2.45 | 3.5 |
| B5 | ‐1.75 | 3.5 |
| B6 | ‐1.05 | 3.5 |
| B7 | ‐0..35 | 3..5 |
| B8 | 0.35 | 3.5 |
| B9 | 1.05 | 3.5 |
| B10 | 1.75 | 3.5 |
| B11 | 2.45 | 3.5 |
| B12 | 3.15 | 3.5 |
| B13 | 3.85 | 3.5 |
| B14 | 4.55 | 3.5 |
| C1 | ‐4.55 | 2.8 |
| C2 | ‐3.85 | 2.8 |
| C3 | ‐3.15 | 2.8 |
| C4 | ‐2.45 | 2.8 |
| C5 | ‐1.75 | 2.8 |
| C6 | ‐1.05 | 2.8 |
| C7 | ‐0.35 | 2.8 |
| C8 | 0.35 | 2.8 |
| C9 | 1.05 | 2.8 |
| C10 | 1.75 | 2.8 |
| C11 | 2.45 | 2.8 |
| C12 | 3.15 | 2.8 |
| C13 | 3.85 | 2.8 |
| C14 | 4.55 | 2.8 |
| D1 | ‐4.55 | 2.1 |
| D2 | ‐3.85 | 2.1 |
| D3 | ‐3.15 | 2.1 |
| D4 | ‐2.45 | 2.1 |
| D5 | ‐1.75 | 2.1 |
| D6 | ‐1.05 | 2.1 |
| D7 | ‐0.35 | 2.1 |
| D8 | 0.35 | 2.1 |
| D9 | 1.05 | 2.1 |
| D10 | 1.75 | 2.1 |
| D11 | 2.45 | 2.1 |
| D12 | 3.15 | 2.1 |
| D13 | 3.85 | 2.1 |
| D14 | 4.55 | 2.1 |
| E1 | ‐4.55 | 1.4 |
| E2 | ‐3.85 | 1.4 |
| E3 | ‐3.15 | 1.4 |
| E4 | ‐2.45 | 1.4 |
| E5 | ‐1.75 | 1.4 |
| E6 | ‐1.05 | 1.4 |
| E7 | ‐0.35 | 1.4 |
| E9 | 1.05 | 1.4 |
| E10 | 1.75 | 1.4 |
| E11 | 2.45 | 1.4 |
| E12 | 3.15 | 1.4 |
| E13 | 3.85 | 1.4 |
| E14 | 4.55 | 1.4 |
| F1 | ‐4.55 | 0.7 |
| F2 | ‐3.85 | 0.7 |
| F3 | ‐3.15 | 0.7 |
| F4 | ‐2.45 | 0.7 |
| F5 | ‐1.75 | 0.7 |
| F6 | ‐1.05 | 0.7 |
| F7 | ‐0.35 | 0.7 |
| F10 | 1.75 | 0.7 |
| F11 | 2.45 | 0.7 |
| F12 | 3.15 | 0.7 |
| F13 | 3.85 | 0.7 |
| F14 | 4.55 | 0.7 |
| G1 | ‐4.55 | 0 |
| G2 | ‐3.85 | 0 |
| G3 | ‐3.15 | 0 |
| G4 | ‐2.45 | 0 |
| G5 | ‐1.75 | 0 |
| G6 | ‐1.05 | 0 |
| G7 | ‐0.35 | 0 |
| G8 | 0.35 | 0 |
| G10 | 1.75 | 0 |
| G11 | 2.45 | 0 |
| G12 | 3.15 | 0 |
| G13 | 3.85 | 0 |
| G14 | 4.55 | 0 |
| H1 | ‐4.55 | ‐0.7 |
| H2 | ‐3.85 | ‐0.7 |
| H3 | ‐3.15 | ‐0.7 |
| H4 | ‐2.45 | ‐0.7 |
| H5 | ‐1.75 | ‐0.7 |
| H6 | ‐1.05 | ‐0.7 |
| H7 | ‐0.35 | ‐0.7 |
| H8 | 0.35 | ‐0.7 |
| H9 | 1.05 | ‐0.7 |
| H10 | 1.75 | ‐0.7 |
| H11 | 2.45 | ‐0.7 |
| H12 | 3.15 | ‐0.7 |
| H13 | 3.85 | ‐0.7 |
| H14 | 4.55 | ‐0.7 |
| J1 | ‐4.55 | ‐1.4 |
| J2 | ‐3.85 | ‐1.4 |
| J3 | ‐3.15 | ‐1.4 |
| J4 | ‐2.45 | ‐1.4 |
| J5 | ‐1.75 | ‐1.4 |
| J6 | ‐1.05 | ‐1.4 |
| J8 | 0.35 | ‐1.4 |
| J9 | 1.05 | ‐1.4 |
| J10 | 1.75 | ‐1.4 |
| J11 | 2.45 | ‐1.4 |
| J12 | 3.15 | ‐1.4 |
| J13 | 3.85 | ‐1.4 |
| J14 | 4.55 | ‐1.4 |
| K1 | ‐4.55 | ‐2.1 |
| K2 | ‐3.85 | ‐2.1 |
| K3 | ‐3.15 | ‐2.1 |
| K4 | ‐2.45 | ‐2.1 |
| K5 | ‐1.75 | ‐2.1 |
| K6 | ‐1.05 | ‐2.1 |
| K8 | 0.35 | ‐2.1 |
| K9 | 1.05 | ‐2.1 |
| K10 | 1.75 | ‐2.1 |
| K11 | 2.45 | ‐2.1 |
| K12 | 3.15 | ‐2.1 |
| K13 | 3.85 | ‐2.1 |
| K14 | 4.55 | ‐2.1 |
| L1 | ‐4.55 | ‐2.8 |
| L2 | ‐3.85 | ‐2.8 |
| L3 | ‐3.15 | ‐2.8 |
| L4 | ‐2.45 | ‐2.8 |
| L6 | ‐1.05 | ‐2.8 |
| L8 | 0.35 | ‐2.8 |
| L9 | 1.05 | ‐2.8 |
| L10 | 1.75 | ‐2.8 |
| L11 | 2.45 | ‐2.8 |
| L12 | 3.15 | ‐2.8 |
| L13 | 3.85 | ‐2.8 |
| L14 | 4.55 | ‐2.8 |
| M1 | ‐4.55 | ‐3.5 |
| M2 | ‐3.85 | ‐3.5 |
| M3 | ‐3.15 | ‐3.5 |
| M4 | ‐2.45 | ‐3.5 |
| M5 | ‐1.75 | ‐3.5 |
| M7 | ‐0.35 | ‐3.5 |
| M8 | 0.35 | ‐3.5 |
| M9 | 1.05 | ‐3.5 |
| M10 | 1.75 | ‐3.5 |
| M11 | 2.45 | ‐3.5 |
| M12 | 3.15 | ‐3.5 |
| M13 | 3.85 | ‐3.5 |
| M14 | 4.55 | ‐3.5 |
| N1 | ‐4.55 | ‐4.2 |
| N2 | ‐3.85 | ‐4.2 |
| N3 | ‐3.15 | ‐4.2 |
| N4 | ‐2.45 | ‐4.2 |
| N5 | ‐1.75 | ‐4.2 |
| N6 | ‐1.05 | ‐4.2 |
| N7 | ‐0.35 | ‐4.2 |
| N8 | 0.35 | ‐4.2 |
| N9 | 1.05 | ‐4.2 |
| N10 | 1.75 | ‐4.2 |
| N11 | 2.45 | ‐4.2 |
| N12 | 3.15 | ‐4.2 |
| N13 | 3.85 | ‐4.2 |
| N14 | 4.55 | ‐4.2 |

Table 86: Pin Locations-CC0/CA0

### Modules with Package Code CA1, CC1

#### Mechanical Characteristics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (L X W X H)** | **Units** |
| Module Dimensions | 15 x 15.7 x 2.2 | mm |
| Tolerance | ±0.2 | mm |

Table 87: Mechanical Characteristics-CA1/CC1

#### PCB Landing Pattern

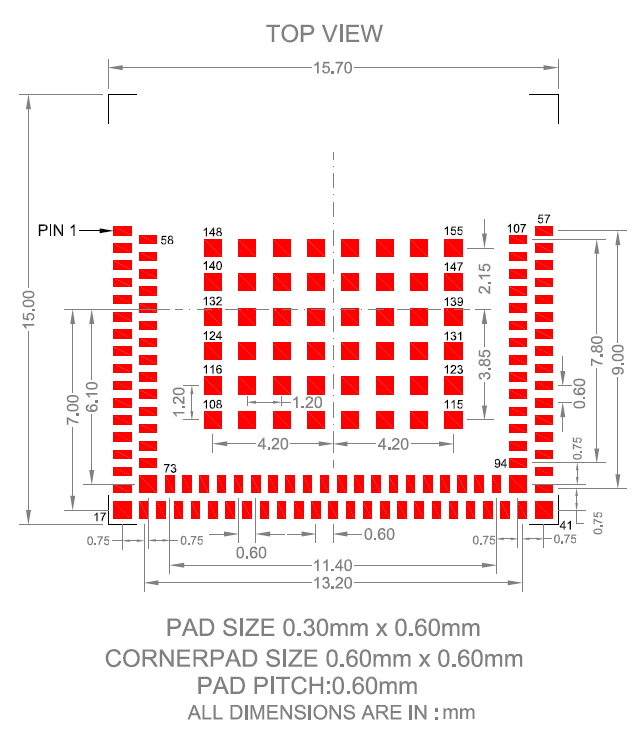


Figure 26: PCB Landing Pattern of Modules with package codes CA1, CC1

### Modules with Package Code B00

#### Mechanical Characteristics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (L X W X H)** | **Units** |
| Module Dimensions | 7.9 x 4.63 x 1.2 | mm |
| Tolerance | ±0.1 | mm |

Table 88: Mechanical Characteristics-B00

#### Mechanical Drawing

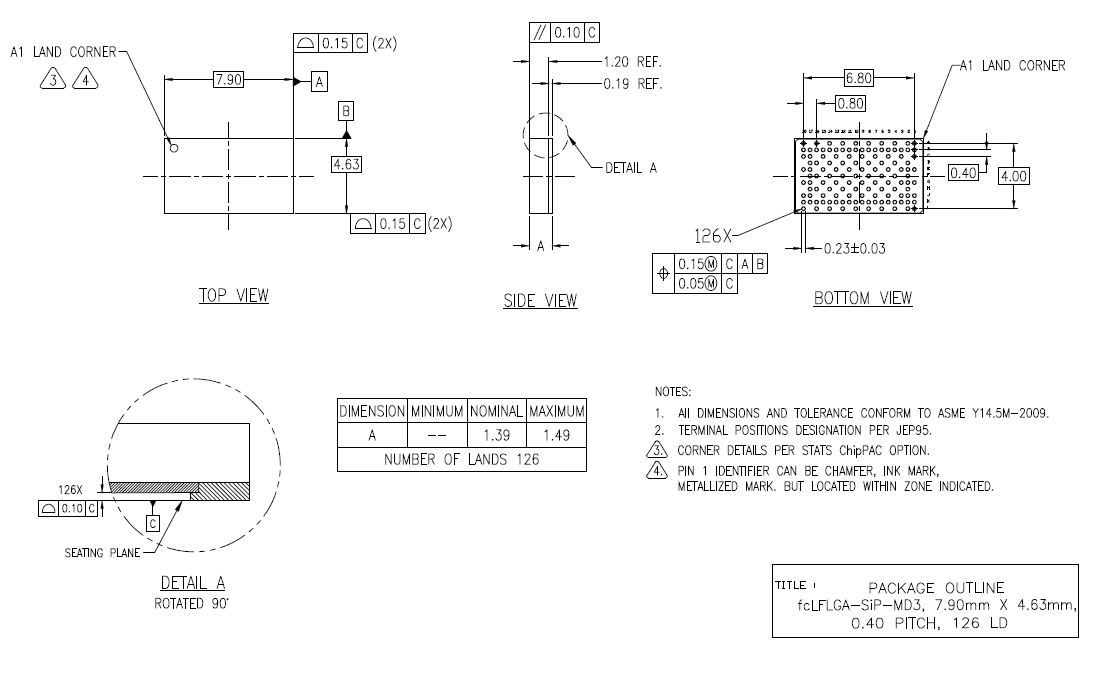


Figure 27: Mechanical Drawing-B00

## Chip Packages

### Chip with Package Code QMS

#### Mechanical Characteristics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (L X W X H)** | **Units** |
| Module Dimensions | 7 x 7 x 0.85, 0.5 | mm |
| Tolerance | ±0.1 | mm |

Table 89: Mechanical Characteristics-QMS

#### Package Dimensions

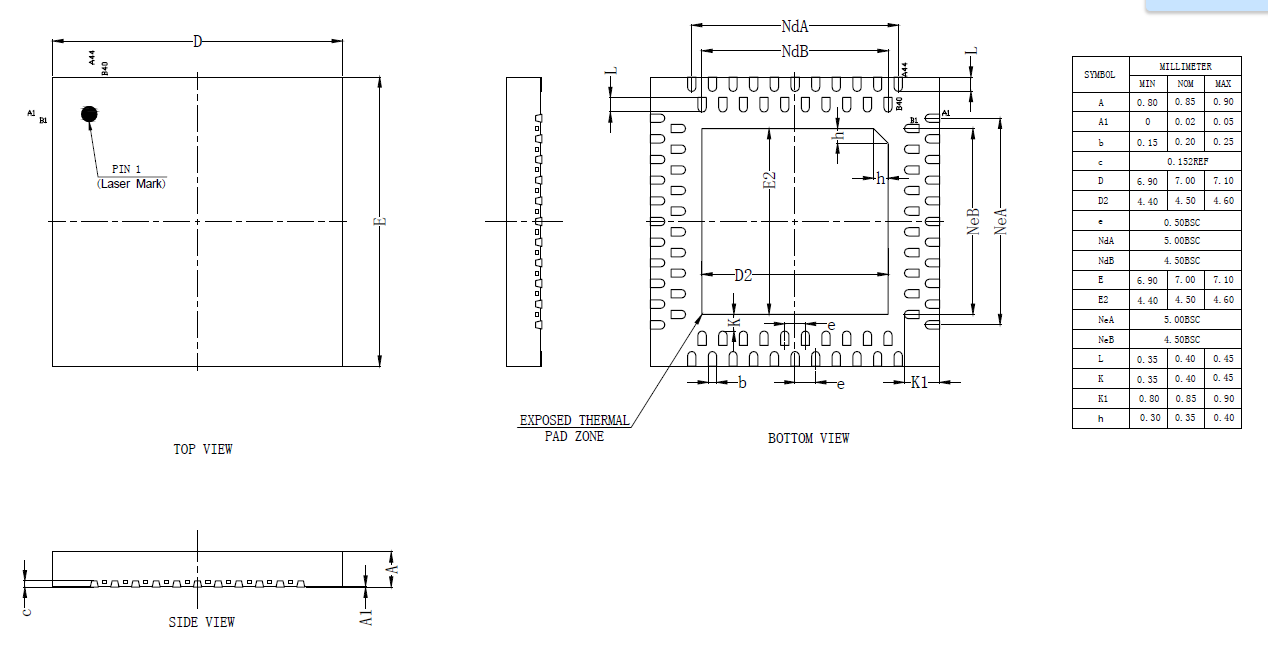


Figure 28: Package Dimensions of Chip with Package Code QMS

#### PCB Landing Patterns

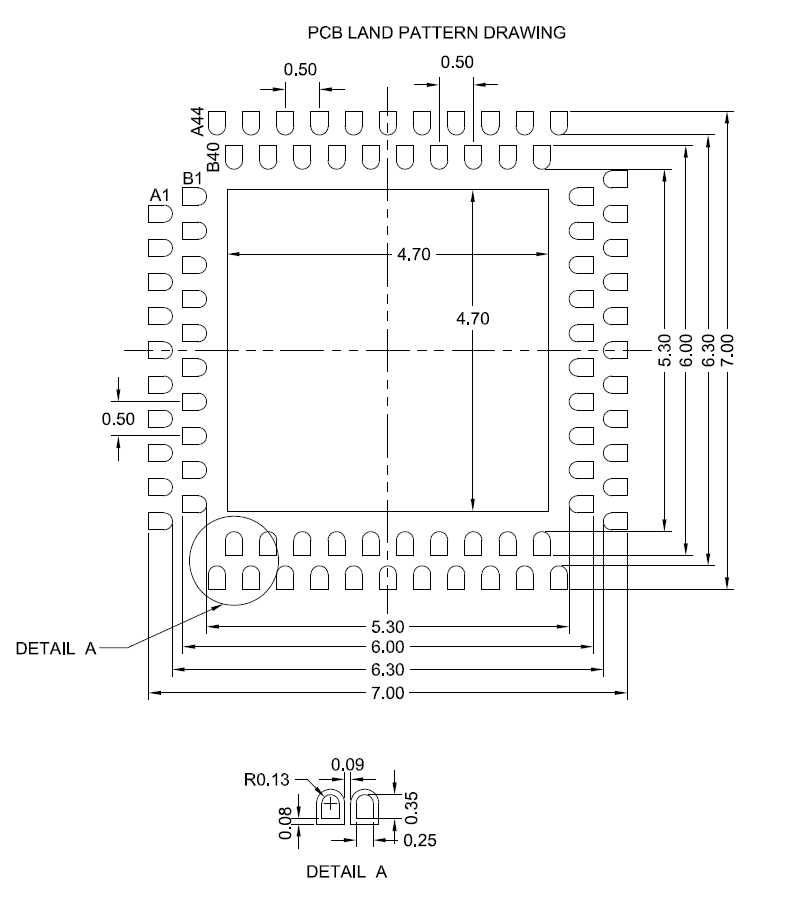


Figure 29: PCB Landing Pattern of Chip with Package Code QMS

## Chip with Package Code WMS

#### Mechanical Characteristics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (L X W X H)** | **Units** |
| Module Dimensions | 3.5 x 3.6 x 0.5, 0.4 | mm |
| Tolerance | ±0.1 | mm |

Table 90: Mechanical Characteristics-WMS

### Mechanical Drawing

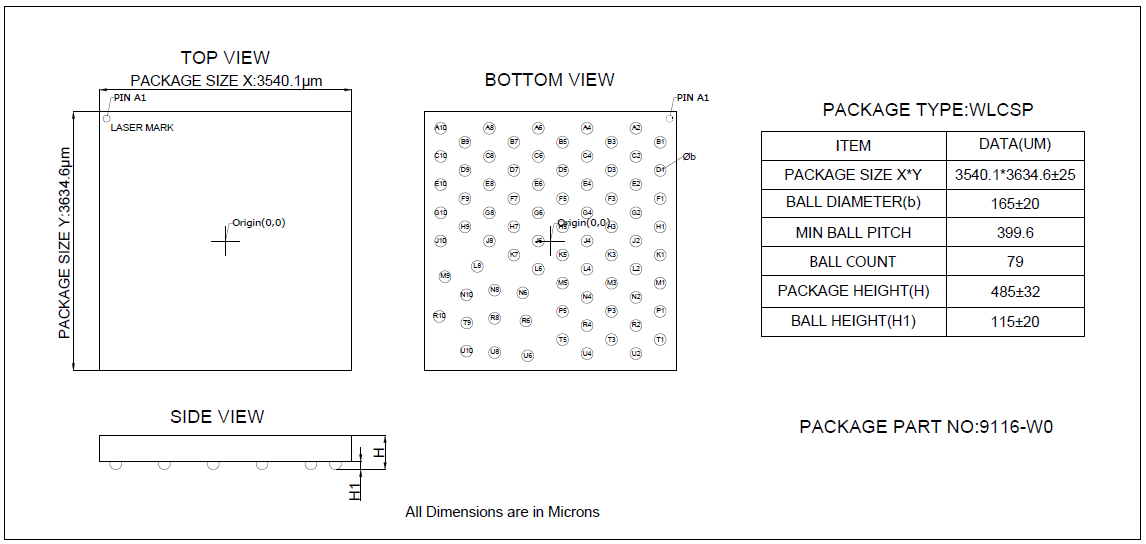


Figure 30: Mechanical Drawing-WMS

### Pin Locations

|  |  |  |
| --- | --- | --- |
| **Pin Number** | **X-Coordinates** | **Y-Coordinates** |
| A2 | -1211.490 | 1598.400 |
| A4 | -519.210 | 1598.400 |
| A6 | 173.070 | 1598.400 |
| A8 | 865.350 | 1598.400 |
| A10 | 1557.630 | 1598.400 |
| B1 | -1557.630 | 1398.600 |
| B3 | -865.350 | 1398.600 |
| B5 | -173.070 | 1398.600 |
| B7 | 519.210 | 1398.600 |
| B9 | 1211.490 | 1398.600 |
| C2 | -1211.490 | 1198.800 |
| C4 | -519.210 | 1198.800 |
| C6 | 173.070 | 1198.800 |
| C8 | 865.350 | 1198.800 |
| C10 | 1557.630 | 1198.800 |
| D1 | -1557.630 | 999.000 |
| D3 | -865.350 | 999.000 |
| D5 | -173.070 | 999.000 |
| D7 | 519.210 | 999.000 |
| D9 | 1211.490 | 999.000 |
| E2 | -1211.490 | 799.200 |
| E4 | -519.210 | 799.200 |
| E6 | 173.070 | 799.200 |
| E8 | 865.350 | 799.200 |
| E10 | 1557.630 | 799.200 |
| F1 | -1557.630 | 599.400 |
| F3 | -865.350 | 599.400 |
| F5 | -173.070 | 599.400 |
| F7 | 519.210 | 599.400 |
| F9 | 1211.490 | 599.400 |
| G2 | -1211.490 | 399.600 |
| G4 | -519.210 | 399.600 |
| G6 | 173.070 | 399.600 |
| G8 | 865.350 | 399.600 |
| G10 | 1557.630 | 399.600 |
| H1 | -1557.630 | 199.800 |
| H3 | -865.350 | 199.800 |
| H5 | -173.070 | 199.800 |
| H7 | 519.210 | 199.800 |
| H9 | 1211.490 | 199.800 |
| J2 | -1211.490 | 0.000 |
| J4 | -519.210 | 0.000 |
| J6 | 173.070 | 0.000 |
| J8 | 865.350 | 0.000 |
| J10 | 1557.630 | 0.000 |
| K1 | -1557.630 | -199.800 |
| K3 | -865.350 | -199.800 |
| K5 | -173.070 | -199.800 |
| K7 | 519.210 | -199.800 |
| L2 | -1211.490 | -399.600 |
| L4 | -519.210 | -399.600 |
| L6 | 173.070 | -399.600 |
| L8 | 1039.254 | -359.960 |
| M1 | -1557.630 | -599.400 |
| M3 | -865.350 | -599.400 |
| M5 | -173.070 | -599.400 |
| M9 | 1496.466 | -505.470 |
| N2 | -1211.490 | -799.200 |
| N4 | -519.210 | -799.200 |
| N6 | 391.298 | -736.066 |
| N8 | 790.970 | -696.395 |
| N10 | 1190.570 | -762.714 |
| P1 | -1557.630 | -999.000 |
| P3 | -865.350 | -999.000 |
| P5 | -173.070 | -999.000 |
| R2 | -1211.490 | -1198.800 |
| R4 | -519.210 | -1198.800 |
| R6 | 349.296 | -1134.739 |
| R8 | 790.970 | -1095.995 |
| R10 | 1576.245 | -1070.753 |
| T1 | -1557.630 | -1398.600 |
| T3 | -865.350 | -1398.600 |
| T5 | -173.070 | -1398.600 |
| T9 | 1185.114 | -1162.339 |
| U2 | -1211.490 | -1598.400 |
| U4 | -519.210 | -1598.400 |
| U6 | 323.185 | -1629.900 |
| U8 | 790.970 | -1583.564 |
| U10 | 1190.570 | -1561.914 |

Table 91: Pin Locations-WMS

## Chip with Package Code BTS

### Mechanical Characteristics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (L X W X H)** | **Units** |
| Module Dimensions | 6 x 6.3, 0.4 | mm |
| Tolerance | ±0.1 | mm |

Table 92: Mechanical Characteristics-BTS

### Mechanical Drawing

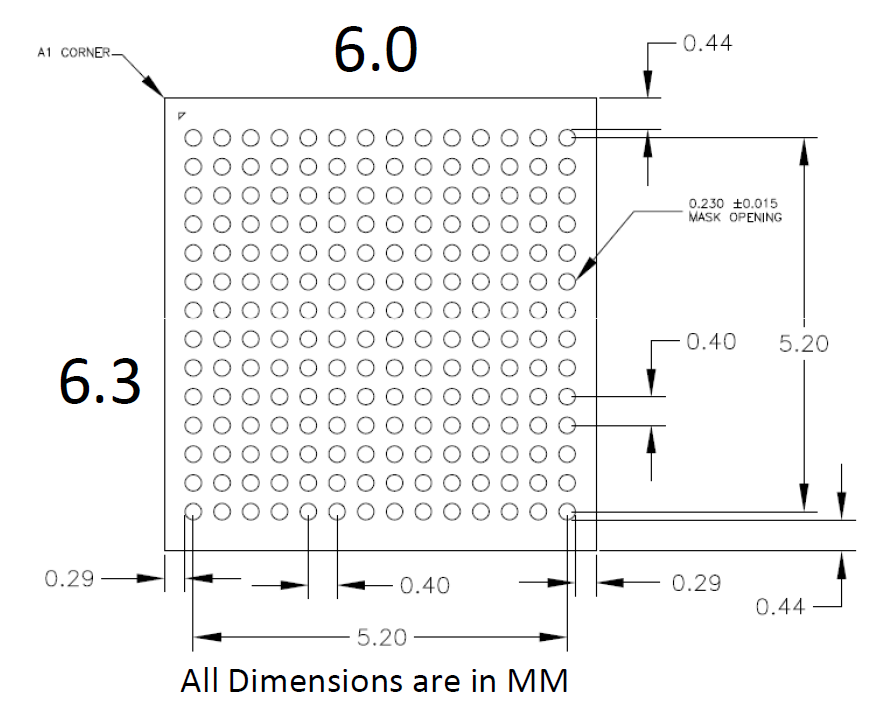


Figure 31: Mechanical Drawing-BMS

# Revision History

| **Revision No.** | **Version No.** | **Date** | **Changes** |
| --- | --- | --- | --- |
| 1 | v1.0 | August 2017 | Advance version |
| 2 | v1.1 | November 2017 | * + - 1. Added a section on Related Resources       2. Revised Pin Details       3. Revised System Block Diagram       4. Revised Package details |
| 3 | v1.2 | December 2017 | 1. Added details for QMS package |
| 4 | v1.3 | January 2018 | 1. Added details for CC1/CA1 packages |

1. Contact Redpine for availability and options. [↑](#footnote-ref-1)
2. Maximum ambient temperature varies with part number. Refer to Section on Ordering Information for more information [↑](#footnote-ref-2)
3. All specifications are subject to change. Contact Redpine signals for final numbers. [↑](#footnote-ref-3)