Digital Logic Design (EL-1005)

LABORATORY MANUAL

Spring-2024

LAB 06 - A
Simplification of Digital Circuits Using Karnaugh map

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STUDENT NAME ROLL NO SEC

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INSTRUCTOR SIGNATURE & DATE

MARKS AWARDED: /35

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NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI

Lab Session 06: Simplification of Digital Circuits Using Karnaugh Map

OBJECTIVES:

The objectives of this lab is:

- To learn K-map and its usage in order to obtain cost effective circuit for implementation
- Implementation of Digital Circuits on Logisim.

SOFTWARE:

- Logisim

Introduction:

De-Morgan 's laws provide mathematical verification of the equivalency of the NAND and negative-OR gates and the equivalency of the NOR and negative-AND gates. The complement of a product of variables is equal to the sum of the complements of the variables. The complement of two or more AND variables is equivalent to the OR of the complements of the individual variables. The De Morgan's statements are,

Statement 1:

"The negation of conjunction is the disjunction of the negations". Or we can define that as "The compliment of the product of 2 variables is equal to the sum of the compliments of individual variables".

$$(A.B)' = A' + B'$$

Statement 2:

"The negation of disjunction is the conjunction of the negations". Or we can define that as "The compliment of the sum of two variables is equal to the product of the compliment of each variable".

$$(A + B)' = A'. B'$$

Figures of the about two statement shown below:

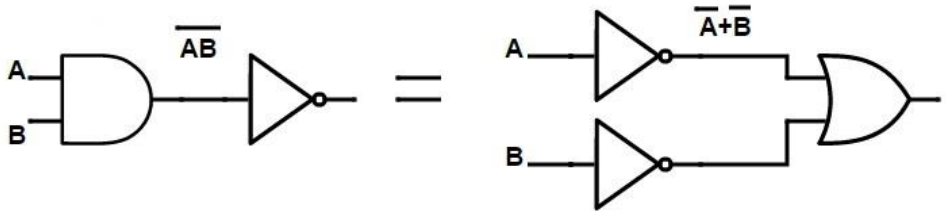


Figure 1 : NAND gate= Bubbled OR gate

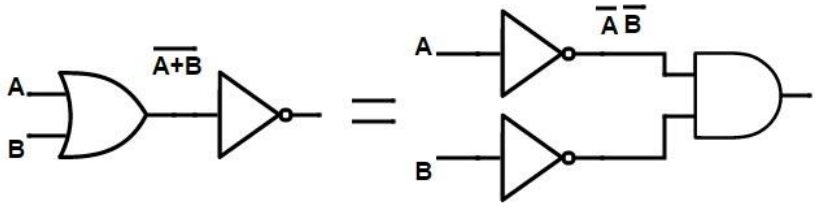
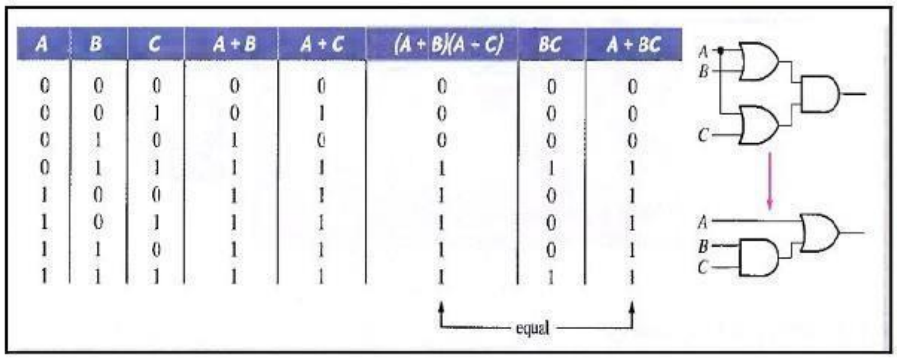


Figure 2 : NOR gate= Bubbled AND gate

Simpler expressions yield simpler hardware:

The proof is shown in table, which shows the truth table and the resulting logic circuit simplification.



A	B	C	A + B	A + C	(A + B)(A + C)	BC	A + BC
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

Figure 2 : Simplification of circuit

K-MAP:

The Karnaugh map (K-map) is a method used to simplify Boolean expressions. K-Map is a grid- like representation of a truth table that gives more insight. The required Boolean results are transferred from a truth table onto a two-dimensional grid where the cells are ordered in gray code and each cell position represents one combination of input conditions, while each cell value represents the corresponding output value. Optimal groups of 1s or 0s are identified, which represent the terms of a canonical form of the logic in the original truth table. These terms can be used to write a minimal Boolean expression representing the required logic.

Karnaugh map is used to obtain optimized logic representation so that it can be implemented using a minimum number of logic gates. The sum-of-product form can always be implemented using AND gates feeding into an OR gate, and a product-of-sum form leads to OR gates feeding an AND gate.

Universality of logic Gates:

1. **The NAND Gate as a Universal Logic Element**

Any logic expression can be implemented using only NAND gates or only NOR gates and no other type of gate. NAND gates alone in the proper combination, can be used to perform each of the basic Boolean operations OR, AND, and INVERT.

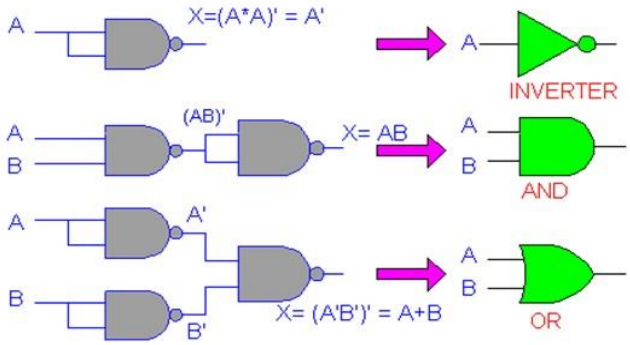


Figure 3 : NAND gate based Basic Gates

2. The NOR Gate as a Universal Logic Element

It can be shown that NOR gate can be arranged to implement any of the Boolean operations.

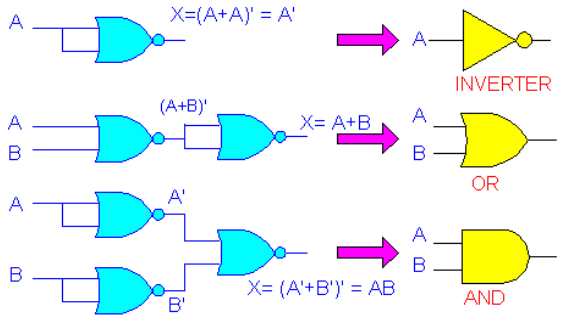


Figure 4 : NOR gate based Basic Gates

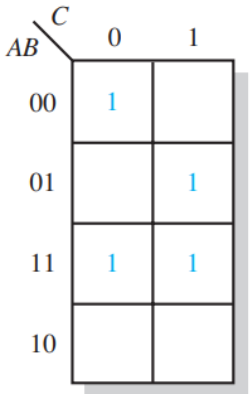
Lab Session 06-A Report Section BSE-2A

Student_ ID_____Date 26th Feb 2024

Question: 1

Using K-MAP, write down minimum SOP and actual expression for each case. Create Truth Table of Actual expression and implement Both actual and reduced expression on Logic Works.

1.



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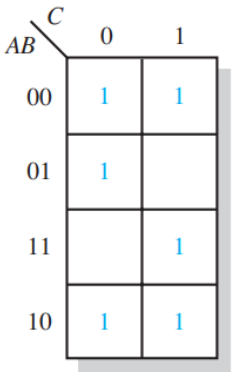

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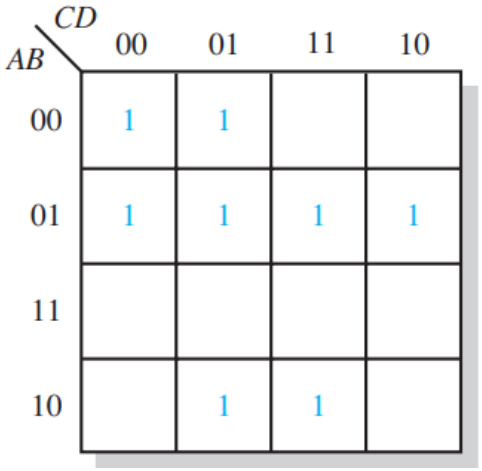
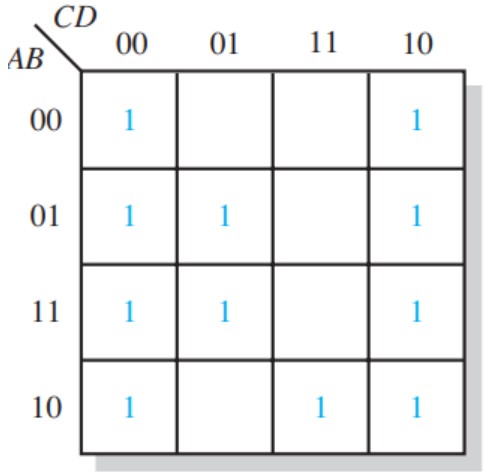


AB \ CD	00	01	11	10
00	1	1		
01	1	1	1	1
11				
10		1	1	

4.



AB \ CD	00	01	11	10
00	1			1
01	1	1		1
11	1	1		1
10	1		1	1

Question: 2 Use K-MAP to minimize the given SOP expression. Implement the minimized SOP on breadboard and draw Complete Truth Table.

$$A\overline{B}C + \overline{A}BC + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C}$$

Question: 3 Use K-MAP to minimize the given SOP expression. Implement the minimized SOP on Logic Works and Complete Truth Table.

$$\overline{B}\,\overline{C}\,\overline{D} + \overline{A}B\overline{C}\,\overline{D} + AB\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + A\overline{B}CD + \overline{A}\,\overline{B}C\overline{D} + \overline{A}BC\overline{D} + ABC\overline{D} + A\overline{B}C\overline{D}$$

Question: 4 Implement the following scenario on Logic Works

Two tanks store certain liquid chemicals that are required in a manufacturing process. Each tank has a sensor that detects when the chemical level drops to 25% of full. The sensors produce a HIGH level of 5 V when the tanks are more than one-quarter full. When the volume of chemical in a tank drops to one-quarter full, the sensor puts out a LOW level of 0 V.
It is required that a single red light-emitting diode (LED) on an indicator panel show when both tanks are more than one-quarter full. Show how a NAND gate can be used to implement this function.

Question: 5 Analysis and Design Logic Circuit on Logic Works.

For the process described in Exercise 01 it has been decided to have a red LED display come on when at least one of the tanks falls to the quarter-full level rather than have the green LED display indicate when both are above one quarter. Design circuit on logic works that shows how this requirement can be implemented.

Question: 6 Analysis and Design Logic Circuit on Logic Works for the following scenario.

As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. A green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing.
A red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement.

Question: 7 Design the circuit following scenario on Logic Works.

A certain system contains two identical circuits operating in parallel. As long as both are operating properly, the outputs of both circuits are always the same. If one of the circuits fails, the outputs will be at opposite levels at some time. Devise a way to monitor and detect that a failure has occurred in one of the circuits.

INSTRUCTIONS FOR SUBMISSION

1. **Create a Word file, having screenshots of circuits given as Lab task.**
2. **Upload World file and. CCT file of Logic Works on Google Classroom.**

INSTRUCTOR: Muhammad Nadeem Ghouri