National University of Computer and Emerging Sciences, Lahore Campus

Course:	DLD Lab	**Course Code:**	EL227	
Program:	BS (Computer Science)	**Semester:**	Spring 2017	
Duration:	50 minutes	**Total Marks:**	25	
Date	26-03-18	**Weight**	25%	
Section:	B2 (A)	**Pages:**	2	

Mid Term Exam

NAME: _____   **Roll #:_____**

READ THE INSTRUCTIONS CAREFULLY.

1. For your ease, Pin Configurations of all ICs is given in word file named **"ICs Info"** placed in folder at
sandata/xeon/Spring2018/AbdulKhaliq/DLDSectionB2.

2. You will be immediately **disqualified** from the exam if:

   i. You are seen talking, whispering, borrowing or looking at someone's Paper.

Problem Statement: Implement the following Boolean functions using 3x8 Decoder and external gates.

$$F1 = y'z + xz$$
$$F2 = xy'z' + x'y + x'y(z + z')$$

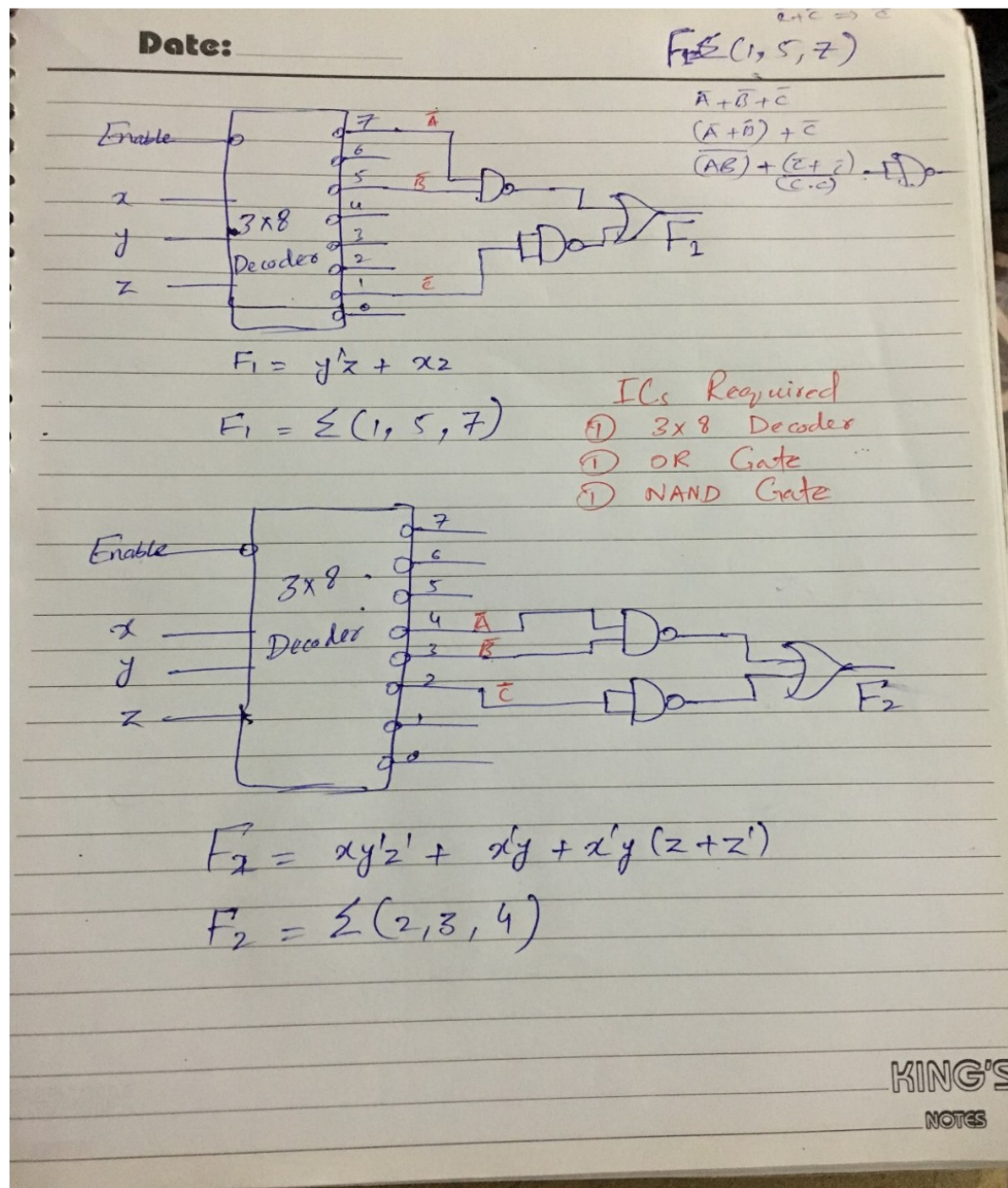   **a.** Draw the truth table for above problem statement.   **[3 Point]**

A	B	C	F1	F2
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	0

b. Draw the complete circuit using 3x8 Decoder and 2-input NAND gates.
[5 Points]
Note: Your circuit should be neat and clean.

Date:

$a + c \Rightarrow c$

$F_1 \Sigma (1, 5, 7)$

$\bar{A} + \bar{B} + \bar{C}$

$(\bar{A} + \bar{D}) + \bar{C}$

$(\overline{AB}) + \overline{(\bar{C} + \bar{c})} \cdot \overline{(C \cdot c)}$

Enable

3×8
Decoder

F_1

$F_1 = y'z + xz$

$F_1 = \Sigma (1, 5, 7)$

ICs Required
① 3×8 Decoder
① OR Gate
① NAND Gate

Enable

3×8
Decoder

F_2

$F_2 = xy'z' + x'y + x'y(z + z')$

$F_2 = \Sigma (2, 3, 4)$

KING'S
NOTES

c. Implement the circuit of part (b) on the trainer board and verify the results.
(Note: Use as minimum no. of logic gates as possible)
[15 Points]