Digital Logic Design
Assignment No. 03

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(BSE-2A)

I_1

For Active-LOW:-

S	R	Q
0	0	1
0	1	1
1	0	0
1	1	0

I_2

For Active-HIGH:-

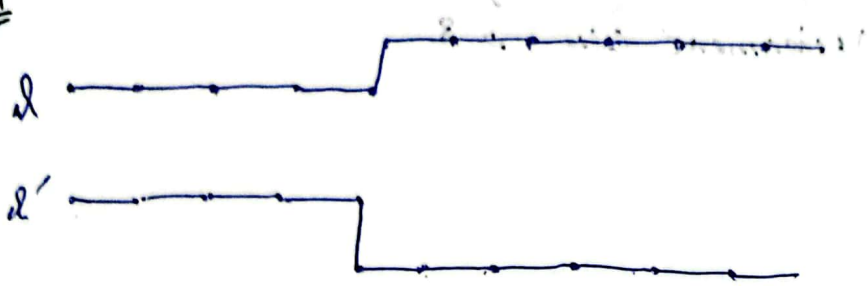
S	R	Q
0	0	1
0	1	0
1	0	1
1	1	0

I_3

(active-HIGH)

(active-LOW)

Q4



Q5 (for fig-5)

(for fig- 6)

D	En	Q
0	1	0
1	1	1
X	0	Q_0

Q6

Q7

Q8

(for figure-9)

Q

(for figure - 10)

Q9 ∵ Q initially LOW (given)

Q

$\bar{J}$	K	Clock	Q
0	0	↑	Q_0
0	1	↑	0
1	0	↑	1
1	1	↑	$\bar{Q}_0$

↓

Toggle

Q10 ∵ Negative Triggered J-K flipflop

∵ Q is initially LOW (given)

Q

Q11

Q

12

Since the input 'D' of D-flipflop also known as (data flip-flop) is connected to $\bar{Q}$ it gives toggling function

if we consider D is '1' initially then $\bar{Q}_0$ is '0' and Q_0 is '1' for next clock $\bar{Q}_0$ becomes D ~~and~~ so, Q is 0 ; which shows that the output toggles for every clock.

13 ∴ (considered Q_A to be initially zero)