Digital Logic Design (EL-1005)

LABORATORY MANUAL

Spring-2024

LAB 03-B
Universal Logic Gates

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STUDENT NAME ROLL NO SEC

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INSTRUCTOR SIGNATURE & DATE

MARKS AWARDED: /10

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI

Date: 9th Feb 2024

Lab Session 03-B: Universal Logic Gates

OBJECTIVES:

The objectives of this lab is:

- To study the realization of basic gates using universal gates (NAND gate & NOR gate)
- To learn technology mapping (NAND-NAND & NOR-NOR implementation) and its significance in order to obtain cost effective circuit for implementation

APPARATUS:

- Logic trainer
- Logic probe

COMPONENTS:

ICs 74LS02, 74LS00, Jumper Wire

Introduction:

The design of a combinational circuit starts from the specification of the problem and culminates in a logic diagram or net-list that describes a logic diagram. The procedure involves the specification, formulation, optimization, & technology mapping.

Technology mapping is actually transformation of logic diagram or net-list to a new diagram using the available implementation technology. Typically, NAND and NOR gates are more desirable to use in technology mapping due to the following reasons:

1. NAND and NOR gates are said to be universal gates where universal gate is a gate which can implement any Boolean function without needing any other type of gate.
2. Using universal gate in technology mapping may further reduce cost of optimized logic diagram.
3. Universal gates are easier to fabricate with electronic components.

A convenient way to implement a Boolean function with NAND gates only (NAND-NAND implementation) is to begin with the optimized logic diagram of the circuit consisting of AND, OR and NOT gates. The function is converted to pure NAND logic by replacing each gate in logic diagram with its representation using NAND gates only as shown in figure 5-1. After that, all inverter pairs are cancelled. The same conversion procedure is applied to implement a Boolean function with NOR gates only (NOR-NOR implementation).

Universal Logic Gates:

A. **NAND Gate:**

"It is a device whose output is 1 if at least one or all of the inputs are low (0)"

Symbol:

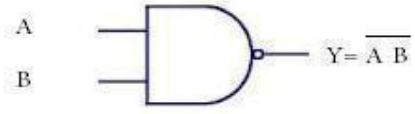


Figure 2 NAND Gate Symbol

Function Table:

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

Table: 1 NAND Gate Truth Table

H= Logic High, L= Logic Low

Connection Diagram:

74LS00 IC contains four 2-input NAND gates. The connection diagram for this IC are shown below:

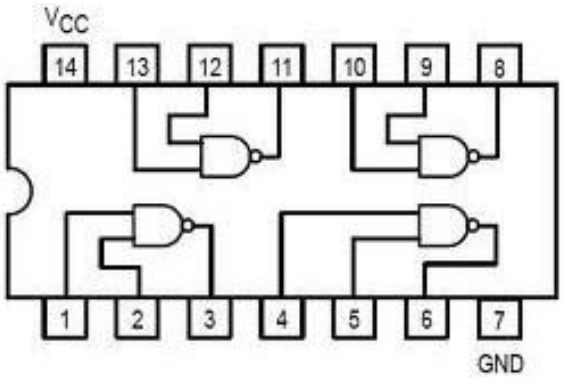


Figure 2 NAND Gate Connection diagram

B. **NOR Gate:**

"It is a device whose output is 1 if all the given inputs are low (0)".

Symbol:

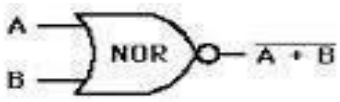


Figure 3 NOR Gate Symbol

Function Table:

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

Table: 2 NOR Gate Truth Table

H= Logic High, L= Logic Low

Connection Diagram:

74LS02 IC contains four 2-input NOR gates. The function table and connection diagram for this IC are shown below:

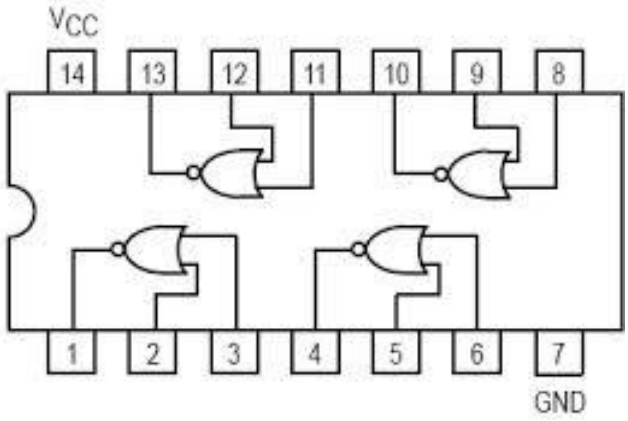


Figure 4 NOR Gate Connection diagram

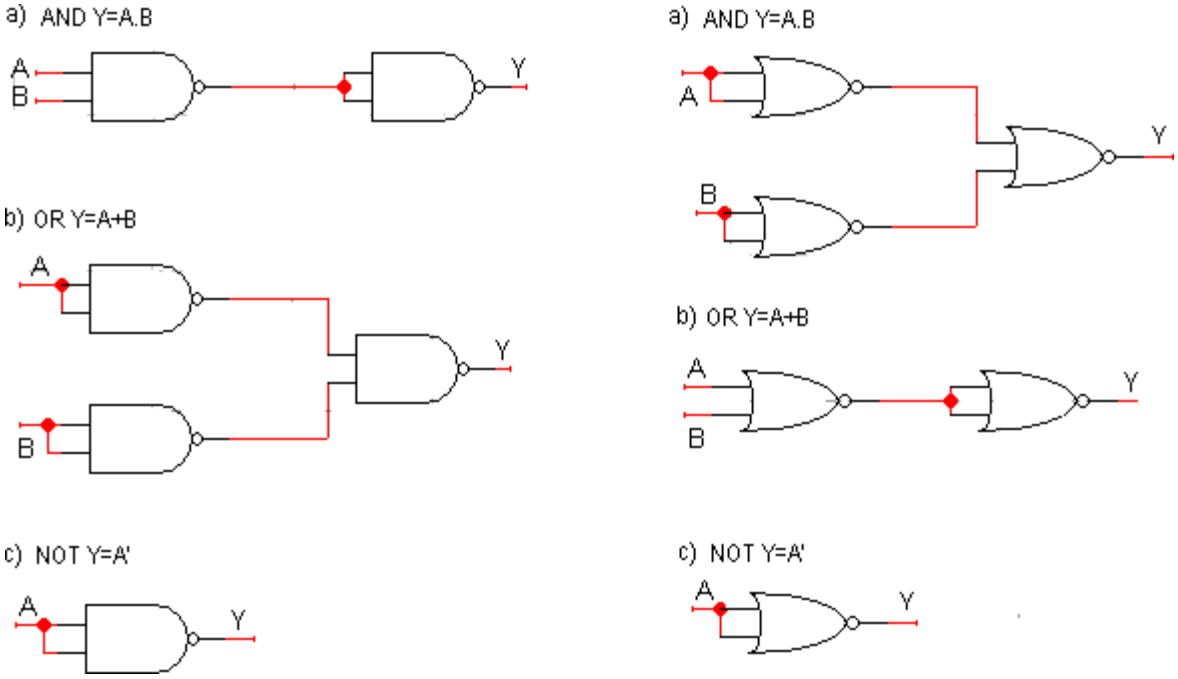


Figure 5 NAND-NAND and NOR-NOR representation of basic logic gates

Lab Session 03-B Report Section BSE-2A

Student_ ID Date 9th Feb 2024

Lab Task#1:

Implement the following logic circuit on logic trainer, and write Boolean Expression and draw Truth table.

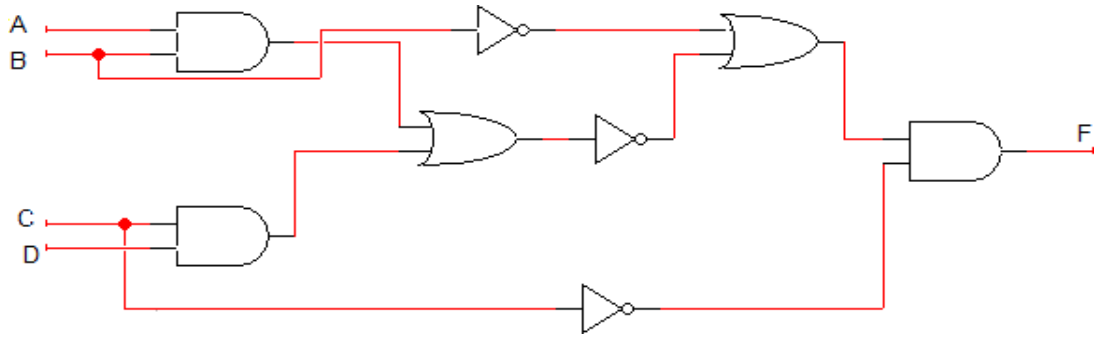


Figure 5: Combinational Circuit

Lab Task#2

Write the Boolean expression for the logic circuits in Figure 6. Also implement the given circuits on breadboard and draw Truth tables:

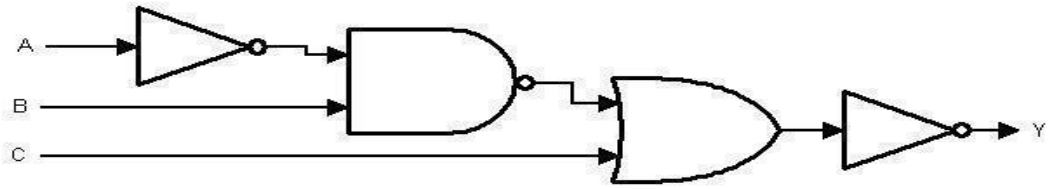


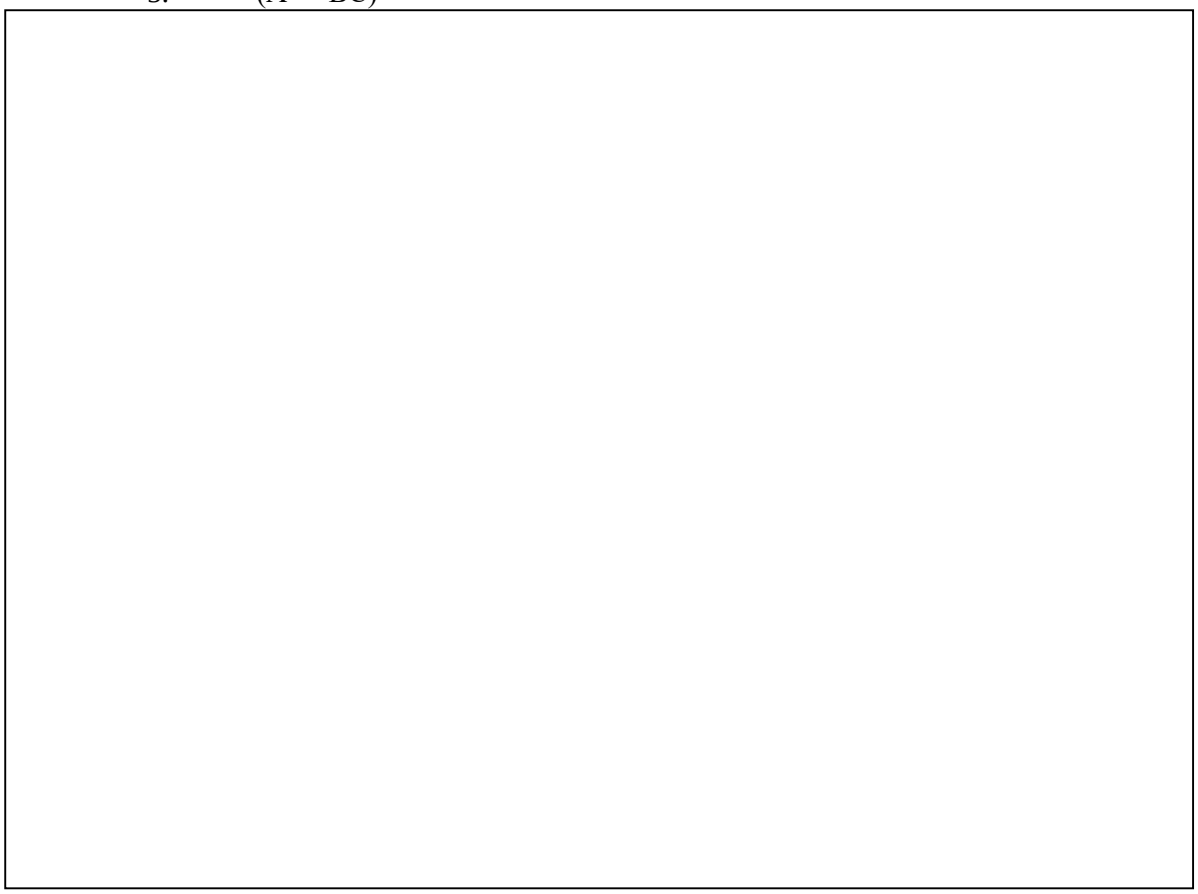
Figure 6: Combinational Circuit

POST LAB TASK

Lab Task#3

Draw a circuit diagram corresponding to the following Boolean expression.

1. (A + B) (B + C)
2. (AB + C) D
3. ((A + B'C) (A + BC))'
4. A'BC + AB'C + ABC' + (ABC)'
5. (A' + BC)'



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