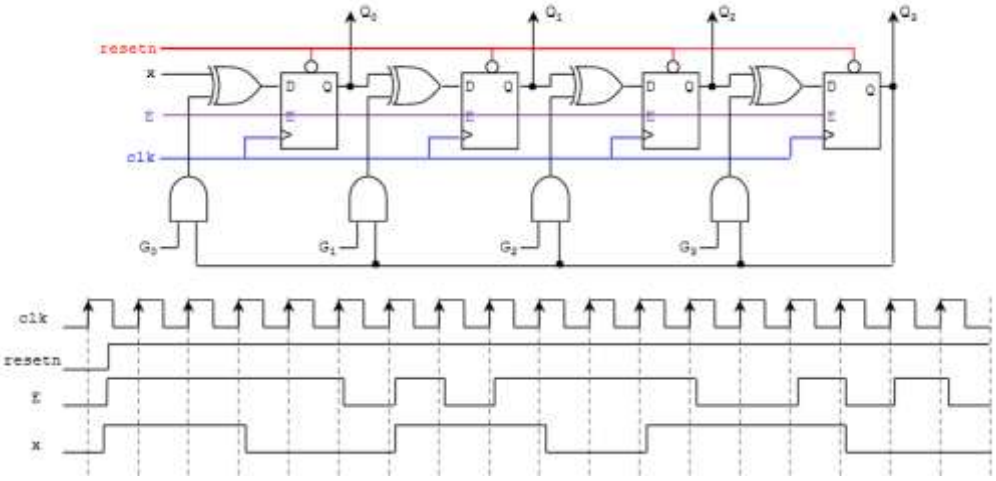
National University of Computer & Emerging Sciences, Karachi
Spring-2020 CS-Department
Final DLD Lab Exam
11th July 2020, 09:00 am – 12:00 pm

Course Code: EL-227	Course Name: Digital logic design
Instructor Name: Engr. Bilal Yousuf, Musawar Ali, Muhammad Nadeem, Hamza Ahmed, Mubashra Fayyaz, Faheem Ahmed siddiqui	
Student Roll No:	Section No:

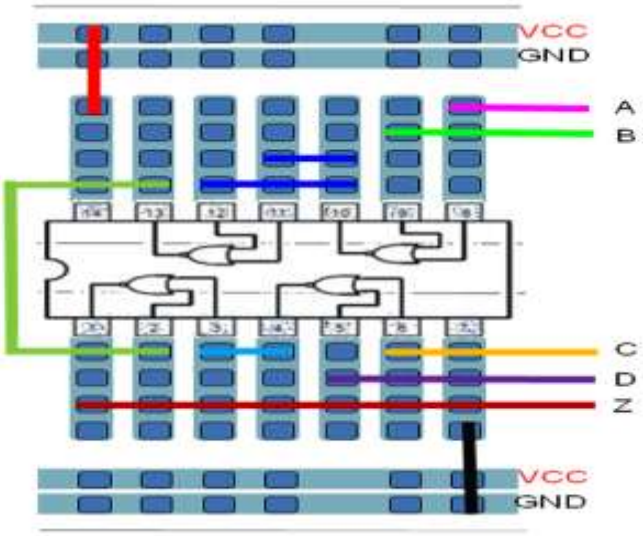
Time: 180 mint. **Max Marks:** 50 points

Question1 Use the Karnaugh map below to find a minimum sum-of-products expression for Σm (0,1,3,4,5,8,9,12,14). How many simple gates of each type are needed to implement this expression (without further simplification) implement it on logicism/ logics works. [6]

Question 2 Complete the timing diagram of the following circuit. G=$G3G1G2G0$=1001, Q=$Q3Q2Q1Q0$ by using logic works. Redesign this circuit and show me the output of all q in that. [5]



Question 3 Given the following breadboard wiring diagram, derive a SOP equation for the single output, Z, through the use of Boolean algebra. The package in the center is a set of 4 NOR gates. [2]



Question 4: Given the function Z = B'C + A'BD + AB', define it truth table and implement via multiplexer. Either 16:1 or 8:1. [6]

Question 5: Design a synchronous up down counter with the following binary sequence 1, 2, 4,5,7 using J-K Flip Flop and implement it on logic work/ logicism [12]

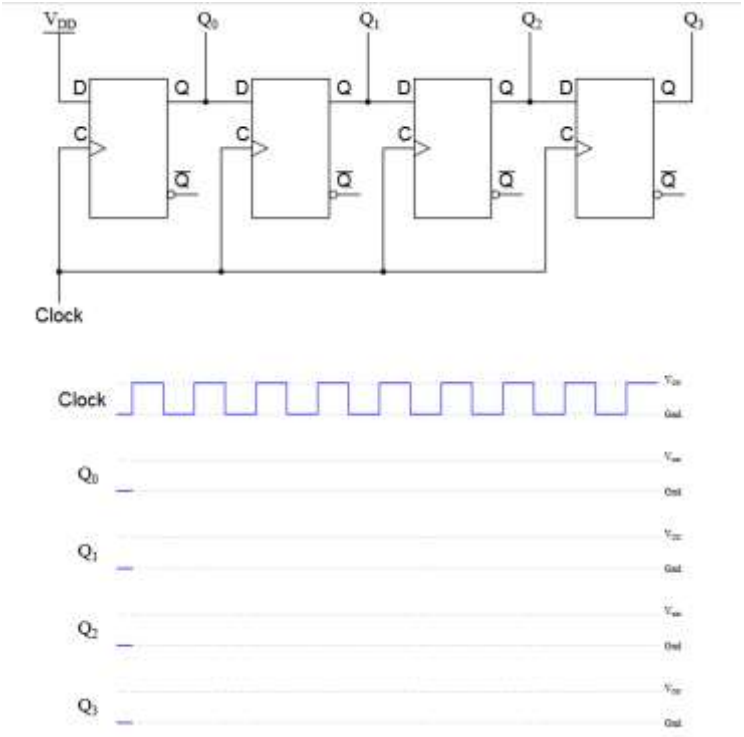
Question: 6 Design 4*4 Bit Binary Multiplier Circuit in Logic Works. [7]

Question: 7 The truth table shown here is for a 4-line to 16-line *binary decoder* circuit: [4]

D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

For each of the sixteen output lines, there is a Boolean SOP expression describing its function. Just for example, write the Boolean expressions for output lines 2,5,8,12, 11, and 14. And Implement the circuit using logic works

Question :8(a) Complete the timing diagram for this circuit, assuming all Q outputs begin in the low state [4]



Question :8(b): Draw the necessary connecting wires between flip-flops so that serial data is shifted from right to left instead of left to right as you may be accustomed to seeing in a shift register schematic: [4]