National University of Computer and Emerging Sciences, Lahore Campus

Course:	DLD Lab	Course Code:	EL227
Program:	BS (Computer Science)	Semester:	Spring 2018
Duration:	50 mints	Total Marks:	50
Date	26-03-18	Weight	25%
Section:	D2 (B)	Pages:	2

Mid Term Exam

NAME: _____ **Roll #:**_____

READ THE INSTRUCTIONS CAREFULLY.

1. Final Submissions should be done in your respective section folder on **sandata/xeon/Spring2018/AbdulKhaliq/DLDSectionD2/MidSubmission**.

2. LogicWorks File must be renamed after your roll number e.g., **"17L-4125".** Multiple submissions are not allowed (if done, only first one will be considered)**.**

3. For your ease, Pin Configurations of all ICs is given in word file named **"ICs Info"** in **folder sandata/xeon/Spring2018/AbdulKhaliq/DLDSectionD2.**

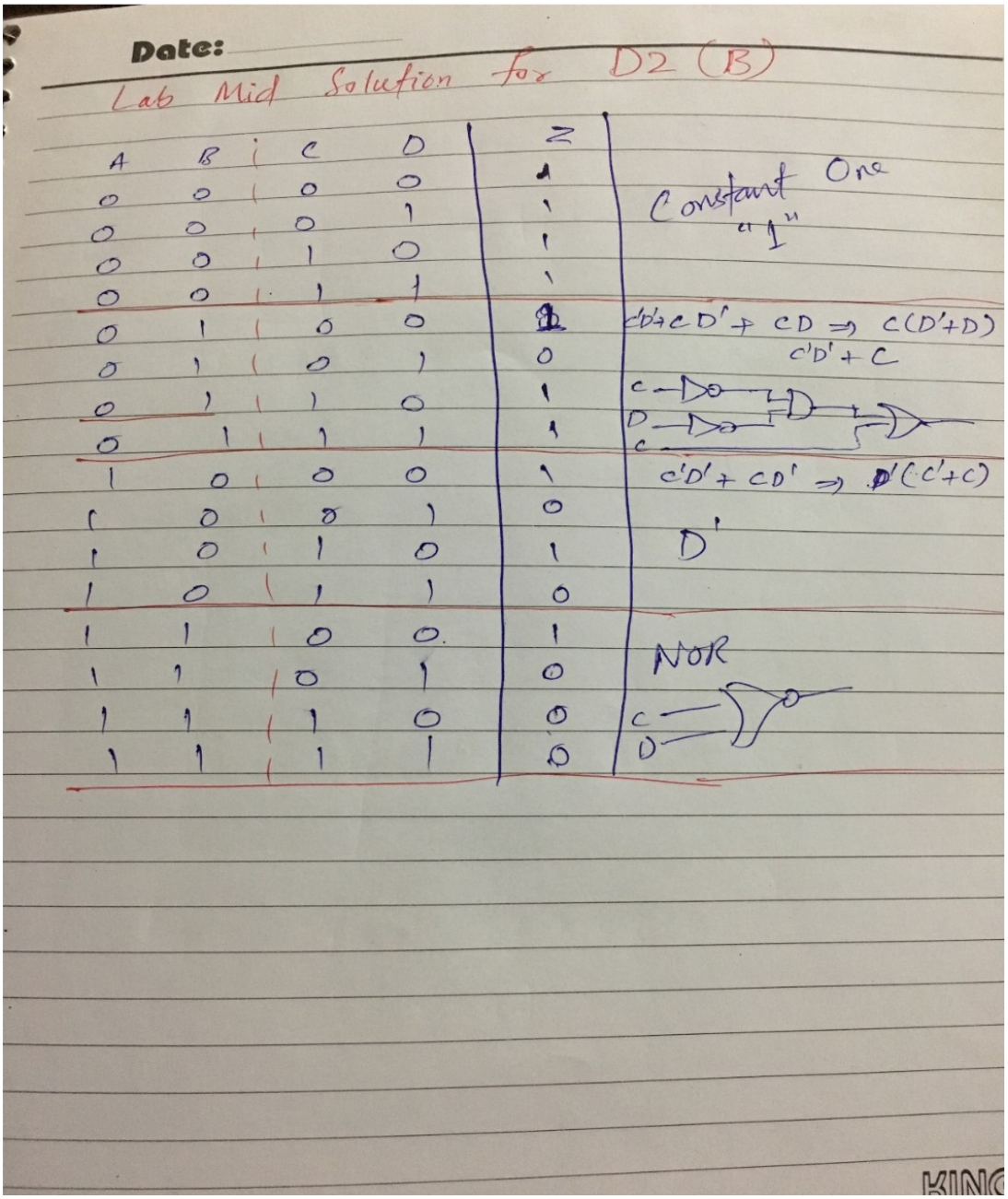
Problem Statement: Implement the following Boolean function using 4x1 multiplexer and external logic gates.

$$F(A,B,C,D) = \sum(0,1,2,3,4,6,7,8,10,12)$$

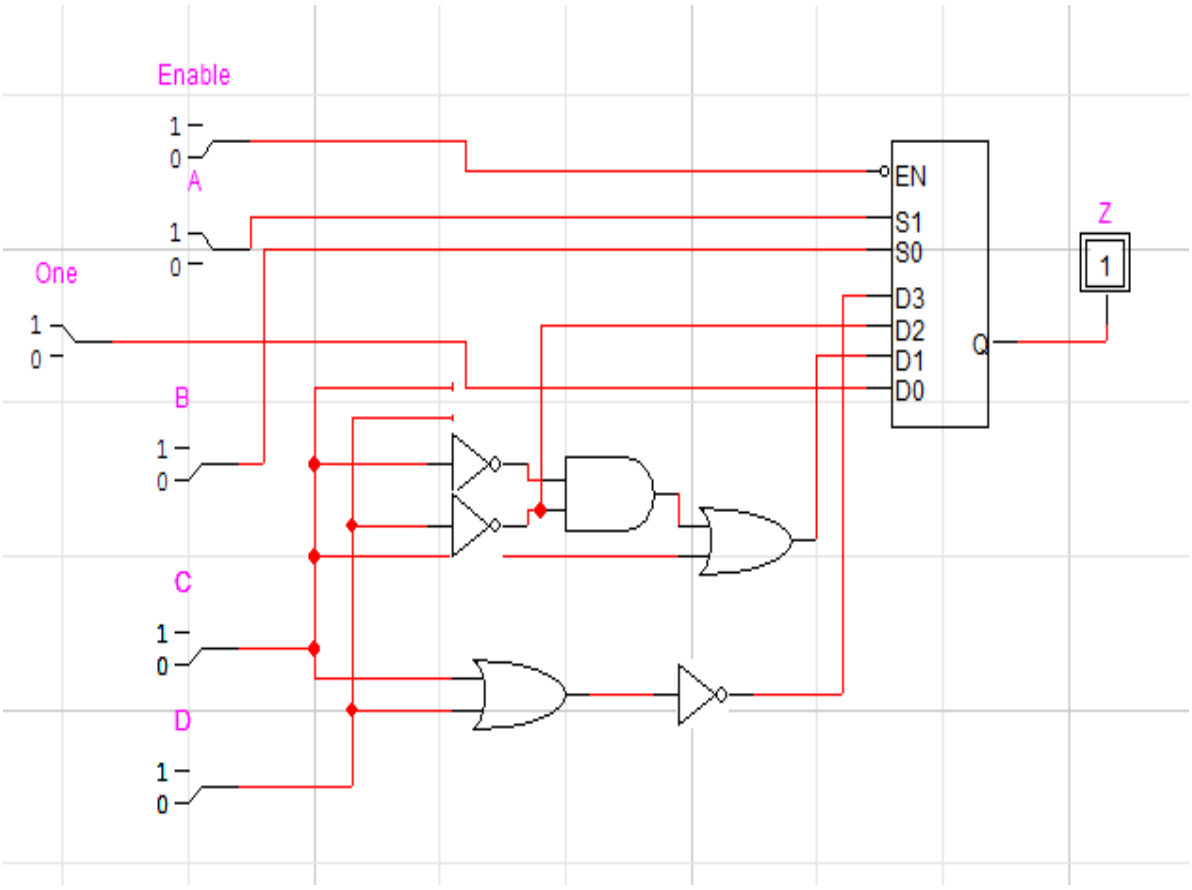
a. Draw the truth table for above problem statement. **[4 Point]**

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

b. Draw the complete circuit diagram using 2-input logic gates only.
[6 Points]



c. Implement the circuit of part (b) on LogicWorks Tool and verify the results using timing diagrams. **[15 Points]**



d. Implement the circuit of part (b) on the trainer board and verify the outputs. **(Note: Use as minimum no. of logic gates as possible)**
[25 Points]