DLD Quiz

Instructions:

i) Try to submit 5 minutes before to avoid any inconvenience. You won't be able to submit after the deadline, ultimately you will lose marks of the quiz
ii) Only hand written quiz will be accepted.
iii) In section B, write the complete answer along with the option (a/b/c/d)
iv) Name & IDs must be mentioned at the top of each page.
v) Try to provide Truth table or K-Map in section A for each question.
vi) Quiz is based on 2 sections (A & B)

Time allowed: 45 mins Marks: 90

Section A

Question 01:

The NAND and the negative-OR symbols represent equivalent operations, but they are functionally different. For the NOR symbol, look for at least one HIGH on the inputs to give a LOW on the output. For the negative-AND, look for two LOWs on the inputs to give a HIGH output. Using these two functional points of view, show that both gates in Figure 3–88 will produce the same output for the given inputs.

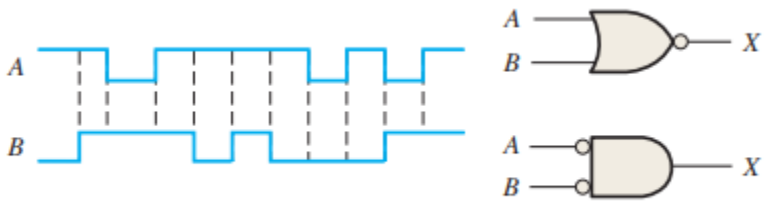

FIGURE 3–88

Question 02:

The notation A1 A0 represents a two-bit binary number that can have any value (00, 01, 10,11); for example, when A1= 1, A0 = 0, the binary number is 10, and so on. Similarly, B1, BO represent another two-bit binary number. Design a logic circuit, using A1, AO, B1, and BO inputs, whose output will be Low only when the two binary numbers A1 AO and B1 BO are invert.

Question 03:

Use a Karnaugh map to reduce the following expression to a minimum SOP form:

A'B' + AB' + C'D' + CD'

Question 04:

Design a 4 to 16 line decoder using 2 to 4 line decoders.

Question 05:

Draw parallel adder which can add (A=00111 and B=10101), determine complete sum by analysis of the logical operation of the circuit.

Question 06:

Show how the following expressions can be implemented as stated using only NOR gates:

X = AB[C((DE)' + (AB)') + (BCE)']

Question 07:

For a gated S-R latch, determine the Q and Q' outputs for the inputs in Figure 7–73. Show them in proper relation to the enable input. Assume that Q starts LOW.

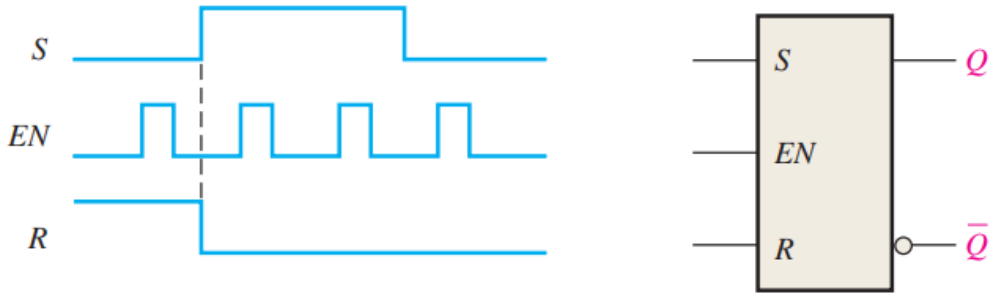

FIGURE 7–73

Question 08:

a) Determine the Q waveform relative to the clock if the signals shown in Figure 7–83 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

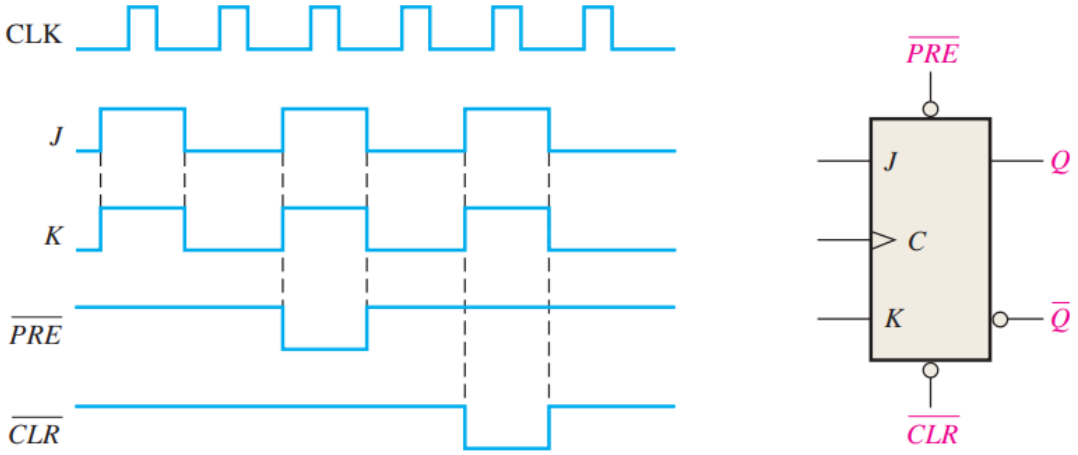

FIGURE 7–83

b) For a negative edge-triggered J-K flip-flop with the inputs in Figure 7–84, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.

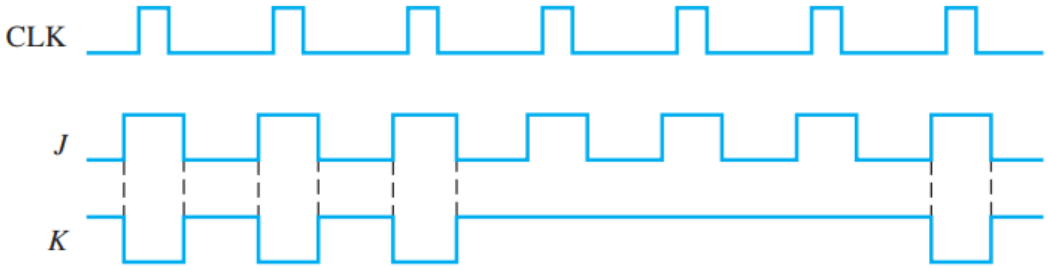

FIGURE 7–84

Section B (MCQs)

1) What must be used along with synchronous control inputs to trigger a change in the flip flop?
   a) 0
   b) 1
   c) Clock
   d) Previous output

2) What will be the output from a D flip-flop if D = 1 and the clock is low?
   a) No change
   b) Toggle between 0 and 1
   c) 0
   d) 1

3) Which of the following gives the correct number of multiplexers required to build a 32 x 1 multiplexer?
   a) Two 16 x 1 mux
   b) Three 8 x 1 mux
   c) Two 8 x 1 mux
   d) Three 16 x 1 mux

4) Which of the following options represent the correct reduction of XYZ + XYZ ?
   a) 0
   b) YZ
   c) X + X
   b) 2YZ

5) What frequency division of the pulsed clock signal can be obtained by connecting 4 flip – flops in cascade?
   a) 2
   b) 4
   c) 8
   d) 16

Good Luck ☺