Digital Logic Design (EL-1005)

LABORATORY MANUAL

Spring-2024

LAB 07-B
Binary Comparator

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STUDENT NAME ROLL NO SEC

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INSTRUCTOR SIGNATURE& DATE

MARKS AWARDED: /10

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI

Lab Session 07-B: Binary Comparator

OBJECTIVES:

- To learn and understand how to design a multiple output combinational circuit
- To learn and understand the working of 2-bit binary comparator
- To learn and understand the working and usage of Exclusive-OR and Exclusive-NOR gates

APPARATUS: Logic trainer, Logic probe

COMPONENTS: ICs 74LS08, 74LS32, 74LS04, 74LS86, 74LS02

THEORY:

Binary comparator is a combinational circuit that compares magnitude of two binary data signals A & B and generates the results of comparison in the form of three output signals A>B, A=B, A<B. Binary comparator is a multiple input and multiple output combinational circuit. When a combinational circuit has two or more than two outputs then each output is expressed separately as a function of all inputs. Separate K-map is made for each output.

One-bit comparator:

One-bit comparator compares magnitude of two numbers A and B, 1 bit each, and generates the comparison result. The result consists of three outputs let us say L, E, G, so that

$$L = 1 \; if \; A < B$$

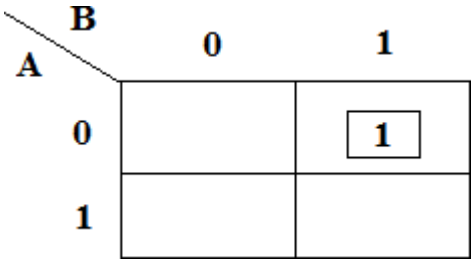
$$E = 1 \; if \; A = B$$

$$G = 1 \; if \; A > B$$

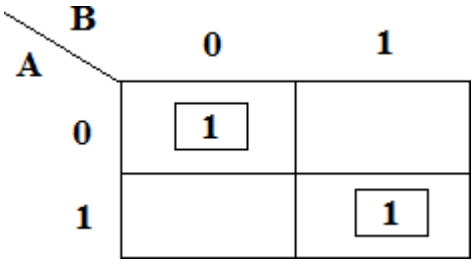
Truth Table:

Inputs		Outputs		
A	**B**	**L**	**E**	**G**
0	**0**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**
1	**1**	**0**	**1**	**0**

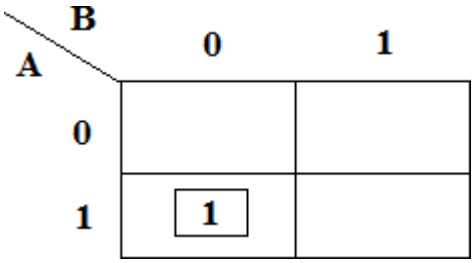
K-Maps for Outputs:



K-Map for Output **L**



K-Map for Output **E**



K-Map for Output **G**

Boolean Expressions of Outputs:

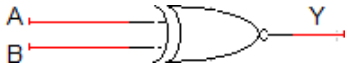
L: $\bar{A}B$

E: $AB + \bar{A}\bar{B}$_

G: $A\bar{B}$_

Exclusive-OR & Exclusive-NOR gates:

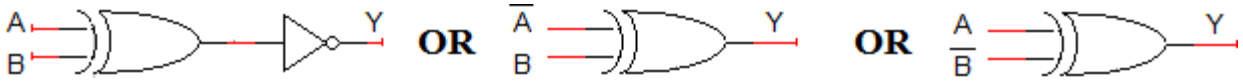
The figure given below shows the symbol of Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates.



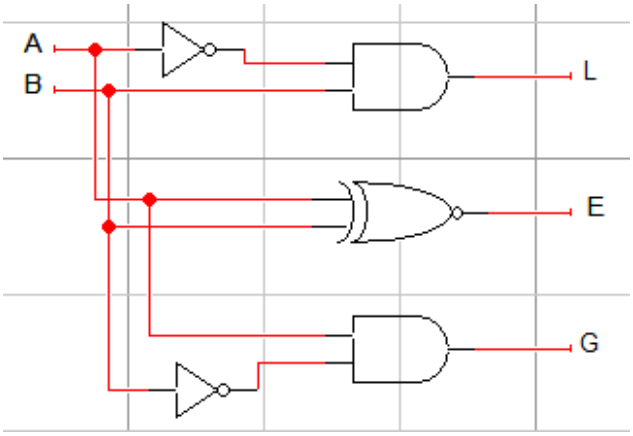
XNOR gate

XOR gate

Boolean expression of XNOR gate is $AB + \bar{A}\bar{B}$ and Boolean expression of XOR is $\bar{A}B + A\bar{B}$ .Boolean expression of XNOR gate can be implemented using XOR gate as shown in figure below:



Circuit Diagram for one-bit comparator:



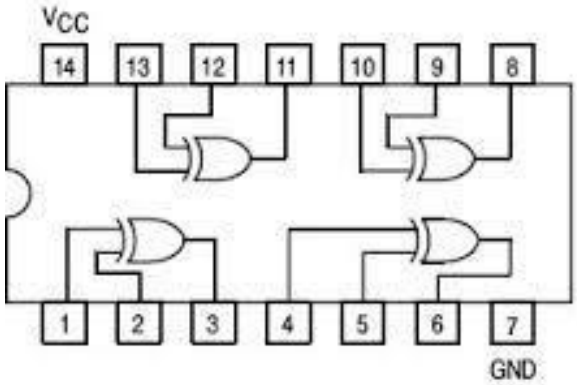
In this experiment 74LS86 IC will be used for implementation of XOR gate function. 74LS86 IC contains four 2-input XOR gates. The function table and connection diagram for this IC are shown below:

Function Table:

Inputs		Output
A	**B**	**Y**
L	**L**	**L**
L	**H**	**H**
H	**L**	**H**
H	**H**	**L**

H= Logic High, L= Logic Low

Connection Diagram:



Lab Session 07-B Report Section BSE-2A

Student_ ID_____Date 4th March 2024

Lab Task #1

Design a combinational circuit that compares two 2-bit numbers and generates the comparison result. The result consists of three outputs let us say L, E, G, so that

$$L = 1 \; if \; A < B$$

$$E = 1 \; if \; A = B$$

$$G = 1 \; if \; A > B$$

Lab Task #2

Design the combinational circuit of 2-Bit Binary comparator on Logic Works.

INSTRUCTION FOR SUBMISSION

Upload circuits of Task # 1 and Task # 2 on Google Classroom

National University of computer and emerging sciences

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