

School of Sciences and Engineering

CMOS Circuit SPICE Generator Project

By:

Abdallah Saba ID:900204018 Shahd Elmahallawy ID: 900194441 Muhammad El-Mahdi ID:900202967

CSCE 330301- Fundamental Microelectronics

Description:

A program that takes an input from the user as a boolean expression, and outputs the circuit corresponding to this expression. It checks the input and starts to call the main three functions we have, which are NOT, AND, and OR according to the precedence. Our Code output Y`, so we used the Not gate at the end to invert the output. After all, the output shows the connection between all MOSEFTS in detail.

Main Data Structures & Algorthims:

Data Structures:

Class MOSFET:

It has the attributes that we need to show in the output which is the name, drain, gate, body, source, and type. We pass an object of this class to each function we have.

Vectors:

Vector of CMOS.

Vector of strings.

We mainly depended on string manipulation in this project to adjust the input and validate it.

Algorithms:

We mainly used Brute Force Algorithm and applied it in the following functions:

1. Notgate Function:

We pass to it the input by reference and two boolean flags. "Flag" is used to handle the case of the buffer when we have two Not gate after each other. For example, if the input is $Y=a\sim$. The other flag is to check if the Not is last in the expression or not. If it is last it generates its output to Y otherwise it generates t a wire. Finally, we used it at the end to invert the output because our functions generate Y`, so we use it to get Y.

2. Andgate Function:

It takes the input by reference and the two boolean flags. One to check if it is the first. In that case, it generates 4 Mosfets: 2 PMOS, and 2 NMOS. Otherwise, it generates only 2

MOSFETS: 1 PMOS, and 1 NMOS. The other boolean is to check if the last operator in the expression maps the output to be Y.

It generates the Pull-up MOSFETS to be parallel and the Pull Down to be series.

3. Orgate Function:

The or gate takes the same inputs as the AND gate and the same booleans, but the only difference is that it generates the Pull-up Mosfets to be in series and the Pull Down to be parallel.

4. Adjust Function:

It takes the input vector of CMOS and the vector of string includes the variables. Then, it loops over the vector of CMOS to finalize the expression as it was used to correct any mistakes in the expression and to connect any redundant points to make them the same, it looped over every point of the MOSFET to make sure it's correct.

5. Get expression Function:

This function is used to get the boolean expression. Then, we save the indices of each operator we have in vector for each operator. For example, "notindices" save the indices of the operators. Then, we loop over each vector and after we call any gate function we replace what we finish by "@".

- 6. There were some more functions that we used inside these functions, like getting the missing characters and so on.
- 7. We used the function (indices of the operators) to where (&,| and ~) are found in our input

User Guide:

After running the code, the user will be asked to enter the Boolean expression. The user must enter the expression in the form of a letter = expression for example (y=a&b|c&d). The user Otherwise, the code will not run properly. An example of what the user should enter would be the following: After entering the expression, the output SPICE netlist will be displayed after pressing enter. The input can be (y=x (buffer), $Y=x\sim$ (inverter), or any other circuit)

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roelectronics project

Microsoft Visual Studio Debug Console

Enter the boolean expression

y=a|b&c|d

In this netlist, we have a VDD source of 5 volts and 0 is the GND

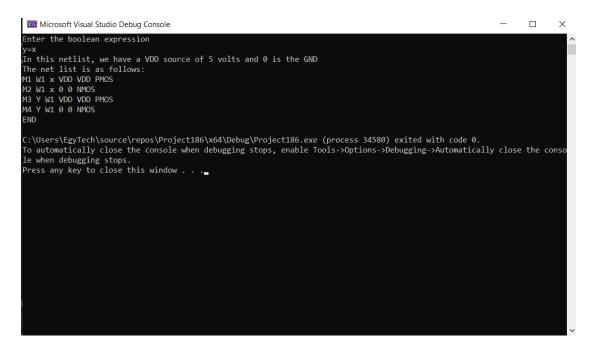
The net list is as follows:

M1 W1 b VDD VDD PMOS
```

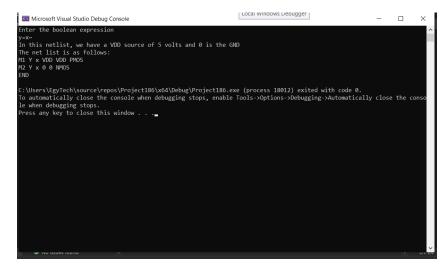
Test Cases:

1. The first test case is the buffer gate where the user enters y=x, in this case we put 2 not gates together

screenshot:-



2. The second test case was the simple not gate($y=x\sim$)



3. The third test case was (y=a&b&c&d&e&f&g&h)

```
Inter the boolean expression
y=abb&c&dee*Rig&h
In this netlist, we have a VDD source of 5 volts and 0 is the GND
The net list is as follows:

MI Y a VDD VDD PMOS
MI W2 a V DO VDD PMOS
MI W2 a V DO VDD PMOS
MI W2 a V DO VDD PMOS
MI W2 a W2 NWOS
MS W4 c W3 W3 NWOS
MS W4 c W3 W3 NWOS
MS W4 d w4 NWOS
MS W5 d W4 W4 NWOS
MS W5 d W4 W4 NWOS
MS W5 d W4 W4 NWOS
MS W5 d W6 W5 NMOS
MI1 Y f VDD VDD PMOS
MI2 W7 f W6 W6 NWOS
MI3 Y g VDD VDD PMOS
MI4 W8 g W7 W7 NWOS
MI5 Y h VDD VDD PMOS
MI5 Y h VDD VDD PMOS
MI6 Y h W8 W8 NWOS
MI7 out Y VDD VDD PMOS
MI8 out Y 0 0 NMOS
MI7 out Y VDD VDD PMOS
MI8 out Y 0 0 NMOS
C:\Users\EgyTech\source\repos\Project186\x64\Debug\Project186.exe (process 27524) exited with code 0.
To automatically close the console when debugging stops, enable Tools->Options->Debugging->Automatically close the console when debugging stops, press any key to close this window . . .
```

4. The fourth test case was (y=a|b|c|d|e|f|g|h)

Screenshot:-

```
Microsoft Visual Studio Debug Console
                                                                                                                                      /=a|b|c|d|e|f|g|h
In this netlist, we have a VDD source of 5 volts and 0 is the GND The net list is as follows:
M1 W1 a VDD VDD PMOS
M2 W2 b W1 W1 PMOS
M3 Y a 0 0 NMOS
M4 Y b 0 0 NMOS
M5 W4 c W2 W2 PMOS
M6 Y c 0 0 NMOS
M7 W5 d W4 W4 PMOS
M8 Y d 0 0 NMOS
M9 W6 e W5 W5 PMOS
M10 Y e 0 0 NMOS
M11 W7 f W6 W6 PMOS
M12 Y f 0 0 NMOS
M13 W8 g W7 W7 PMOS
M14 Y g 0 0 NMOS
M15 Y h W8 W8 PMOS
M16 Y h 0 0 NMOS
 117 out Y VDD VDD PMOS
M18 out Y 0 0 NMOS
C:\Users\EgyTech\source\repos\Project186\x64\Debug\Project186.exe (process 38524) exited with code 0.
To automatically close the console when debugging stops, enable Tools->Options->Debugging->Automatically close the conso
le when debugging stops.
Press any key to close this window . . .
```

5. y=a&b|c|d|e

screenshot:-

```
Microsoft Visual Studio Debug Console

Enter the boolean expression

"y-a&b[c]d[e
In this netlist, we have a VDD source of 5 volts and 0 is the GND

The net list is as follows:

MI W1 a VDD VDD PMOS

M2 W1 b VDD VDD PMOS

M3 W2 a 0 0 NMOS

M4 Y b W2 W2 NMOS

M5 W4 c W1 M1 PMOS

M6 Y c 0 0 NMOS

M7 W5 d W4 W4 PMOS

M8 Y d 0 0 NMOS

M9 Y e W5 W5 PMOS

M10 Y e 0 0 NMOS

M11 out Y VDD VDD PMOS

M12 out Y VDD VDD PMOS

M12 out Y VDD VDD PMOS

M12 out Y 0 0 NMOS

END

C:\Users\EgyTech\source\repos\Project186\x64\Debug\Project186.exe (process 36096) exited with code 0.
To automatically close the console when debugging stops, enable Tools->Options->Debugging->Automatically close the console when debugging stops, enable Tools->Options->Debugging->Automatically close the console when debugging stops, Press any key to close this window . . . __
```

6. y=a&b&c&d|e

screenshot:-

```
Microsoft Visual Studio Debug Console

Enter the boolean expression
y=a&b&c&d|e
In this netlist, we have a VDD source of 5 volts and 0 is the GND
The net list is as follows:
MI W1 a VDD VDD PMOS
M2 W1 b VDD VDD PMOS
M3 W2 a 0 0 NMOS
M4 W3 b W2 W2 NMOS
M5 W1 c VDD VDD PMOS
M6 W4 c W3 W3 NMOS
M7 W1 d VDD VDD PMOS
M8 Y d W4 W4 NMOS
M9 Y e W1 W1 PMOS
M10 Y e 0 0 NMOS
M11 out Y VDD VDD PMOS
M11 out Y VDD VDD PMOS
M12 out Y 0 0 NMOS
END
C:\Users\EgyTech\source\repos\Project186\x64\Debug\Project186.exe (process 34144) exited with code 0.
To automatically close the console when debugging stops, enable Tools->Options->Debugging->Automatically close the console when debugging stops, Press any key to close this window . . .
```

7. y=a|b&c&d&e

```
Enter the boolean expression
y=a|b&c&d&e
In this netlist, we have a VDD source of 5 volts and 0 is the GND
The net list is as follows:
MI WI b VDD VDD PMOS
M2 WI c VDD VDD PMOS
M3 W2 b 0 0 NMOS
M4 W3 c W2 W2 NMOS
M5 W1 d VDD VDD PMOS
M6 W4 d W3 W3 NMOS
M7 WI e VDD VDD PMOS
M8 Y e W4 W4 NMOS
M9 Y a W1 W1 PMOS
M10 Y a 0 0 NMOS
M10 Y Y 0 0 NMOS
M11 out Y VDD VDD PMOS
M12 out Y 0 0 NMOS
END
C:\Users\EgyTech\source\repos\Project186\x64\Debug\Project186.exe (process 13116) exited with code 0.
To automatically close the console when debugging stops, enable Tools->Debugging->Automatically close the console when debugging stops, Press any key to close this window . . .
```

8. y=a|b&c|d|e|f

```
### Microsoft Visual Studio Debug Console

Enter the boolean expression

y=a|b&c|d|e|f
In this netlist, we have a VDD source of 5 volts and 0 is the GND

The net list is as follows:

MI WI b VDD VDD PMOS

M3 W2 b 0 0 NMOS

M4 Y c W2 W2 NMOS

M5 W4 a W1 W1 PMOS

M6 Y a 0 0 NMOS

M7 W5 d W4 W4 PMOS

M8 Y d 0 0 NMOS

M9 W6 e W5 W5 PMOS

M10 Y e 0 0 NMOS

M11 Y f W6 W6 PMOS

M12 Y f 0 0 NMOS

M13 out Y vDD VDD PMOS

M14 out Y 0 0 NMOS

END

C:\Users\EgyTech\source\repos\Project186\x64\Debug\Project186.exe (process 29084) exited with code 0.

To automatically close the console when debugging stops, enable Tools->Options->Debugging->Automatically close the console when debugging stops, press any key to close this window . . .
```

9. y=a&b|c&d|e&f

Contributions:

In this project, we all worked together equally as it was done through on-campus meetings where we used to brainstorm together, write the codes together and solve the bugs that we used to see in the code. Since we are all dorm residents, we met in the library and worked together on the project from A to Z and no one worked on something alone as we liked to share ideas together as if someone worked on a part alone, it was a bit difficult to adjust his ideas to the rest of the code.

Presentation link:-

https://drive.google.com/file/d/1WrV3fAmrGaFUtIyp5uXfe69ahdqg 41hY/view?usp=sharing