**Full-Custom Design 8-bit**

**CAM using 9T SRAM for Digital Integrated Design**

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Abstract—This project's main goal is to create an 8-bit Content Addressable Memory (CAM) in the Electric Generic 22nm CMOS Library by utilizing a 9T SRAM architecture. In the context of the 22nm process technology, the design implementation is concentrated on decreasing the space needed for the CAM cell and maximizing power savings, particularly during the write operation. In order to maximize the CAM's performance, this design strategy seeks to achieve a balance between low power consumption and minimal

latency. The use of 9T SRAM, CAM cell design, low power concerns, XOR function, and effective read and write operations are among of the project's main features.

1. **INTRODUCTION**

RAM is a common computing acronym that stands for random-access memory. Sometimes it’s called PC memory or just memory. In essence, RAM is your computer or laptop’s short-term memory. It’s where the data is stored that your computer processor needs to run your applications and open your files.

Inside your computer, RAM typically comes in the form of a rectangular flat circuit board with memory chips attached, also referred to as a memory module. Computers typically come with at least two RAM modules with room to add more, if needed. These RAM modules are critical components that work hand in hand with your computer’s central processing unit (CPU) and must be working optimally for you to have a good experience.

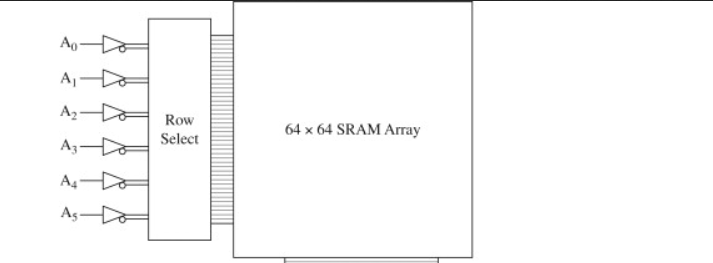


Figure 1-RAM

CAM is a special type of [computer memory](https://en.wikipedia.org/wiki/Computer_memory" \o "Computer memory) used in certain very-high-speed searching applications. It is also known as associative memory or associative storage and compares input search data against a table of stored data, and returns the address of matching data.

CAM is frequently used in [networking devices](https://en.wikipedia.org/wiki/Networking_device" \o "Networking device) where it speeds up [forwarding information base](https://en.wikipedia.org/wiki/Forwarding_information_base" \o "Forwarding information base) and [routing table](https://en.wikipedia.org/wiki/Routing_table" \o "Routing table) operations. This kind of associative memory is also used in cache memory. In associative cache memory, both address and content is stored side by side. When the address matches, the corresponding content is fetched from cache memory.

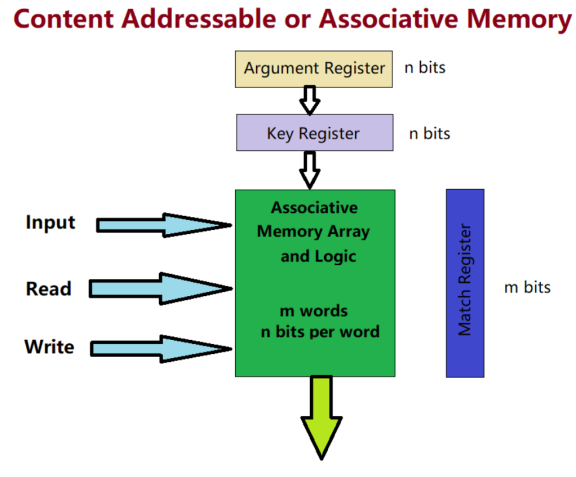


Figure 2-CAM

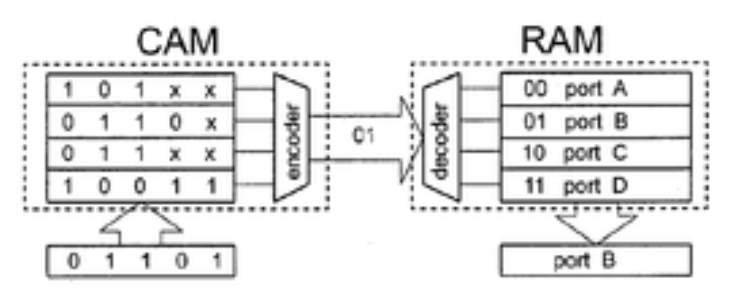


Figure 3-RAM Vs CAM

RAM and CAM are memory technologies, they have different access methods, search operations, speeds, applications, capacities, and costs. RAM is more widely used and has a higher capacity, while CAM is used in specialized applications where fast search operations are required.

1. **DESIGN AND IMPLEMENTATION**

A 22nm CMOS library was used in this project's implementation to guarantee precise timing and reduce signal skew. Achieving balanced rise and fall periods for both NMOS and PMOS devices was our main goal. This necessitated giving considerable thought to elements like each transistor's output resistance and inherent delay. We found that a roughly 2:1 ratio between PMOS and NMOS devices produced the best results in terms of obtaining equal rise and fall timings inside the 22nm process after thorough simulation and testing.

First, we added a 9T SRAM cell as part of the design process. Because of its well-known simplicity, dependability, and quick functioning, this kind of memory cell is frequently used in digital systems. The goal of adding the 9T SRAM cell was to improve the CAM design's overall read performance. A schematic depiction of the 9T SRAM's structural arrangement and connections .

By incorporating these design considerations and leveraging

the benefits of the 9T SRAM cell, our objective was to

optimize the performance and functionality of the CAM

design while adhering to the constraints imposed by the 22nm

CMOS process technology.

The components are as the following:

1. 9T SRAM

A 9T SRAM cell with low power and high speed that works in the ultra-low-power supply is presented. This SRAM is the modified structure of single ended 8T SRAM by connecting word line and one nMOS with high width in the bottom of the twisted connected inverter pair. This work illustrates a 9T SRAM cell that dissipates low power and has high speed during read time and write time. This SRAM cell is a little modification of the SE8T SRAM cell, in which one of the ends of the cell is used to write the information and the other is used to read the information written on the cell. In the same cell, one nMOS transistor has been added to provide better read access time. This stacking of the transistor provides the cell a better path to discharge the bit lines.

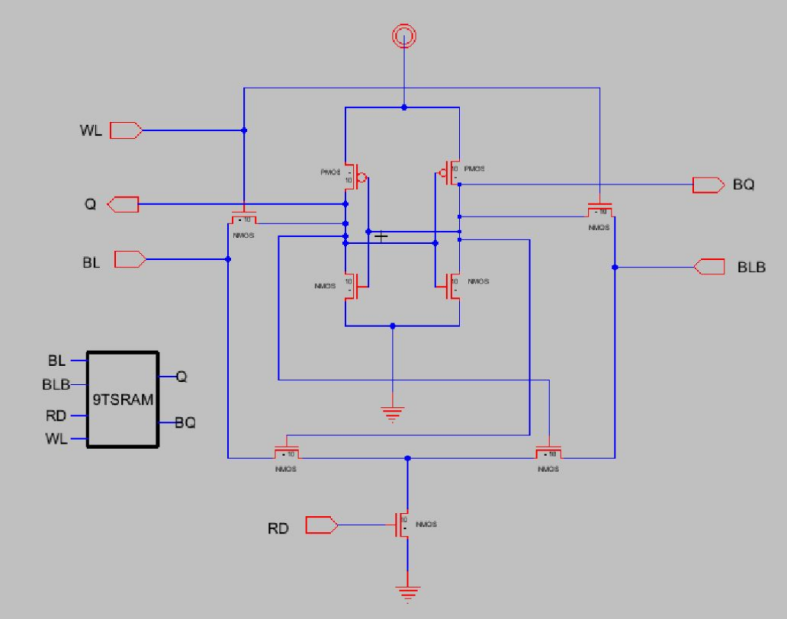


Figure 4- 9T SRAM Schematics

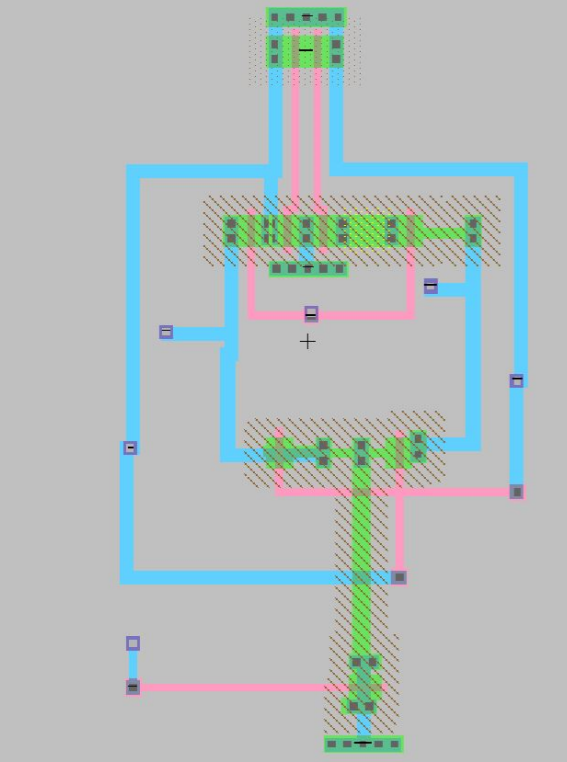


Figure 5-9RAM LayOut

1. INVERTOR

An inverter converts the DC voltage to an AC voltage. In most cases, the input DC voltage is usually lower while the output AC is equal to the grid supply voltage of either 120 volts, or 240 Volts depending on the country.

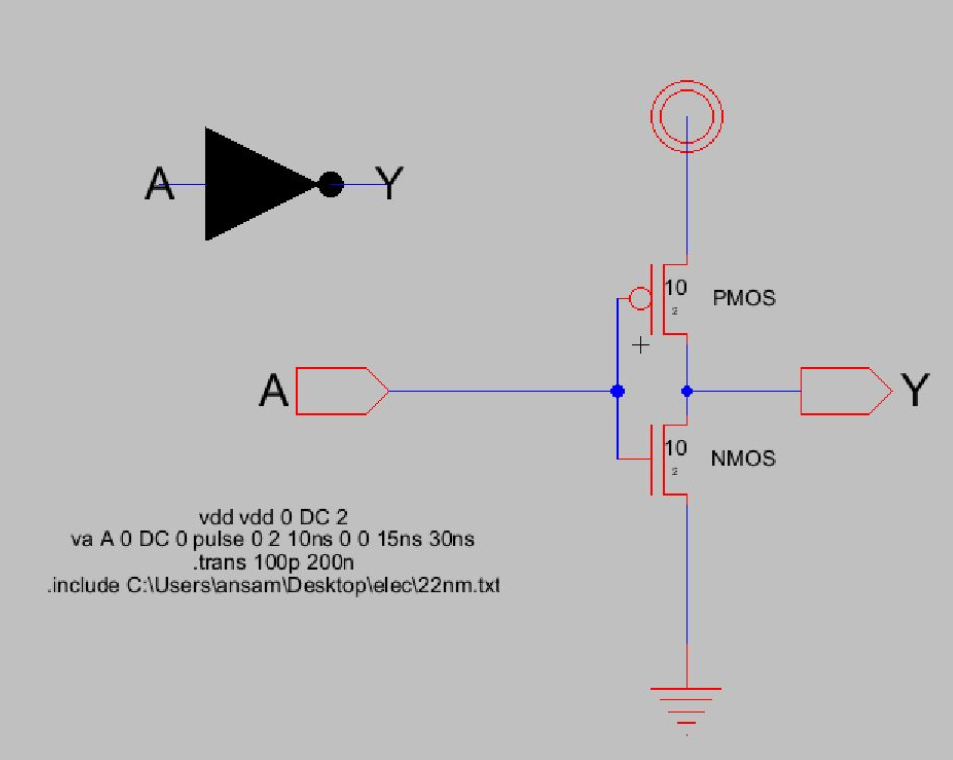


Figure 6- Invertor Schematics

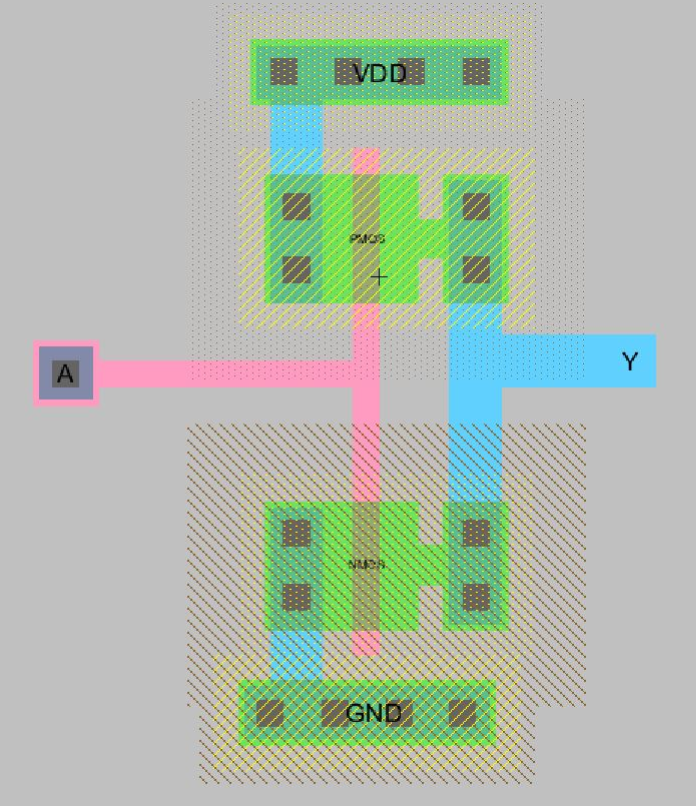


Figure 7-Invertor Layout

1. NOR

The NOR gate is a digital [logic gate](https://en.wikipedia.org/wiki/Logic_gate" \o "Logic gate) that implements [logical NOR](https://en.wikipedia.org/wiki/Logical_NOR" \o "Logical NOR) - it behaves according to the [truth table](https://en.wikipedia.org/wiki/Truth_table" \o "Truth table) to the right. A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the [negation](https://en.wikipedia.org/wiki/Negation" \o "Negation) of the [OR](https://en.wikipedia.org/wiki/OR_gate" \o "OR gate) operator. It can also in some senses be seen as the inverse of an [AND gate](https://en.wikipedia.org/wiki/AND_gate" \o "AND gate). NOR is a [functionally complete](https://en.wikipedia.org/wiki/Functionally_complete" \o "Functionally complete) operation—NOR gates can be combined to generate any other logical function. It shares this property with the [NAND gate](https://en.wikipedia.org/wiki/NAND_gate" \o "NAND gate). By contrast, the [OR](https://en.wikipedia.org/wiki/Logical_disjunction" \o "Logical disjunction) operator is *monotonic* as it can only change LOW to HIGH but not vice versa.

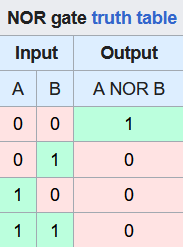


Figure 8- NOR Truth Table

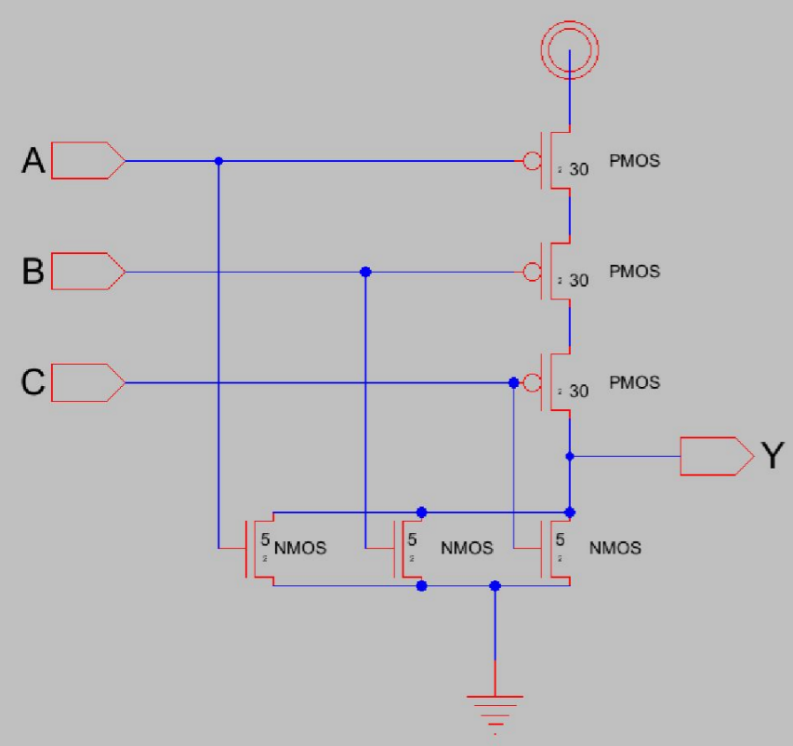


Figure 9-NOR Schematic

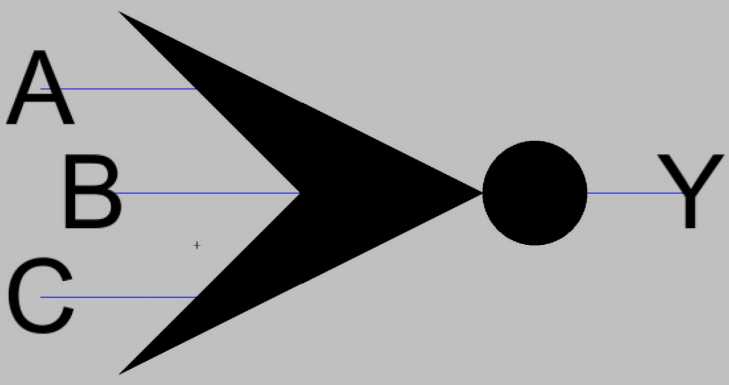


Figure 10-NOR Icon

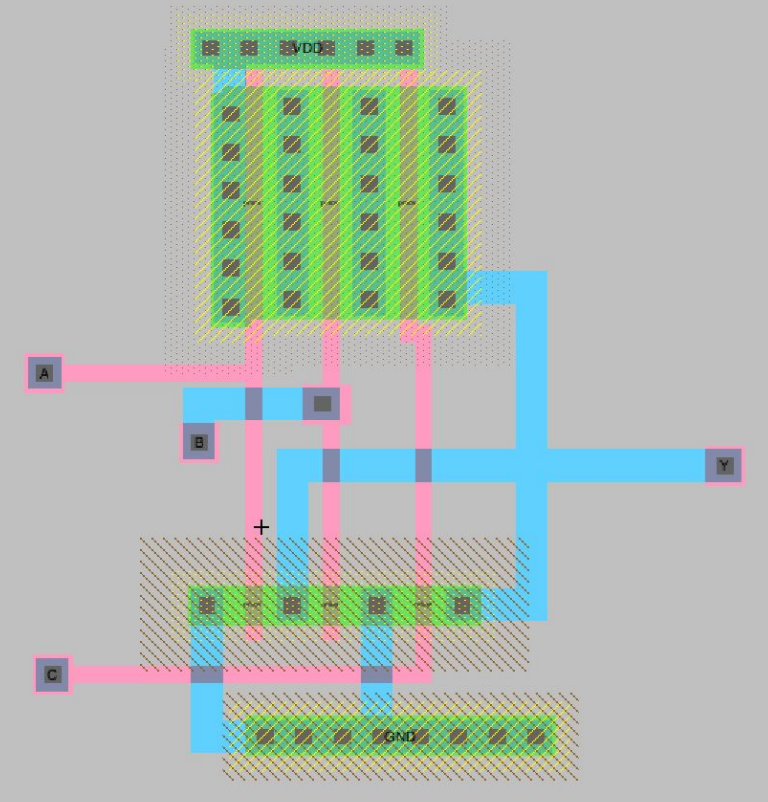


Figure 11-NOR LayOut

## DECODERS

A *decoder* is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is one-to-one mapping from input code words into output code words. The general structure of a decoder circuit is shown in [Figure 1](https://www.oreilly.com/library/view/introduction-to-digital/9780470900550/chap7-sec008.html" \l "fig7.16)2. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. The most commonly used input code is an *N*-bit binary code, where an *N*-bit word represents one of 2*N* different coded values. Normally, they range from 0 through 2*N* − 1. The input code lines select which output is active. The remaining output lines are disabled. Thus, the decoder is intended to provide a binary code to other circuits, such as a memory circuit. In this case, the decoder is referred to as an address decoder because it selects one address of a memory location. However, a decoder could also be used to channel a stream of data on a designated output line selected by the input code lines.

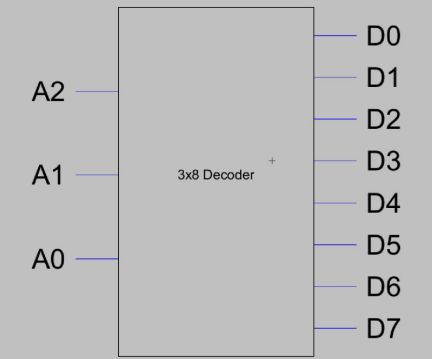


Figure 12-Decoder Icon

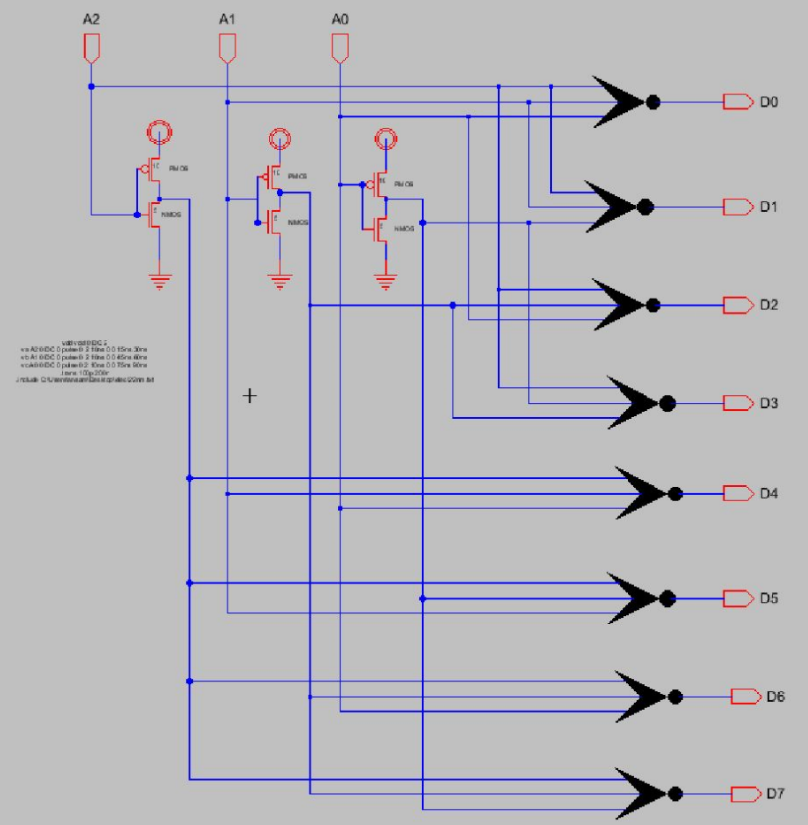


Figure 13-Decoder Schematic

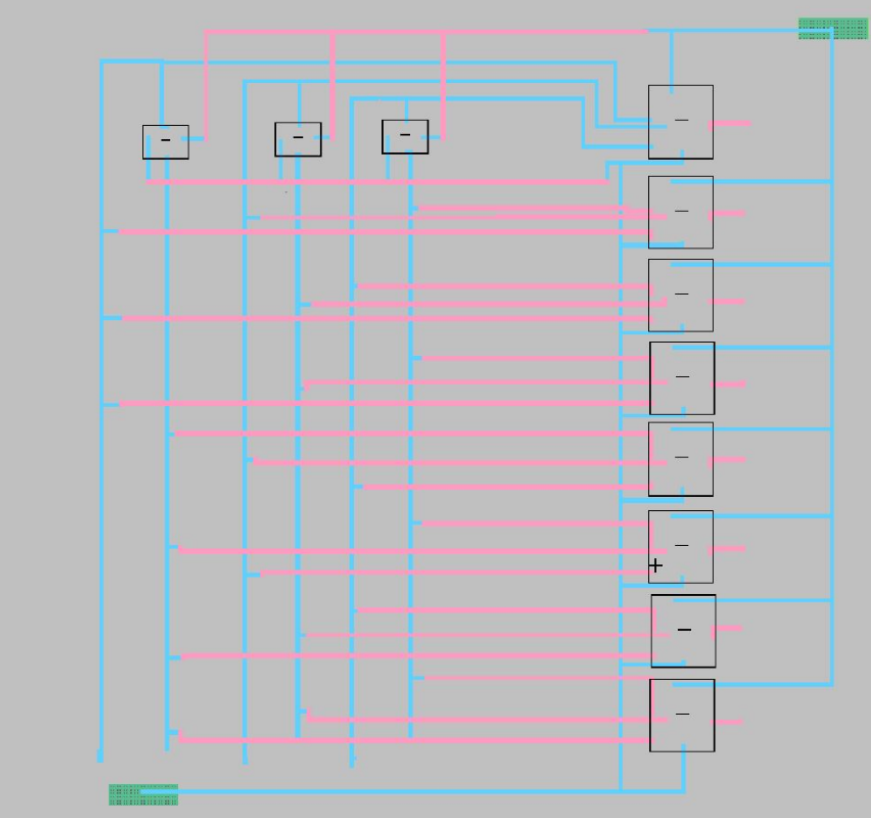


Figure 14-Decoder LayOut

1. NAND

NAND gate (NOT-AND) is a [logic gate](https://en.wikipedia.org/wiki/Logic_gate" \o "Logic gate) which produces an output which is false only if all its inputs are true; thus its output is [complement](https://en.wikipedia.org/wiki/Complement_(set_theory)" \o "Complement (set theory)) to that of an [AND gate](https://en.wikipedia.org/wiki/AND_gate" \o "AND gate). A LOW (0) output results only if all the inputs to the gate are HIGH (1); if any input is LOW (0), a HIGH (1) output results.

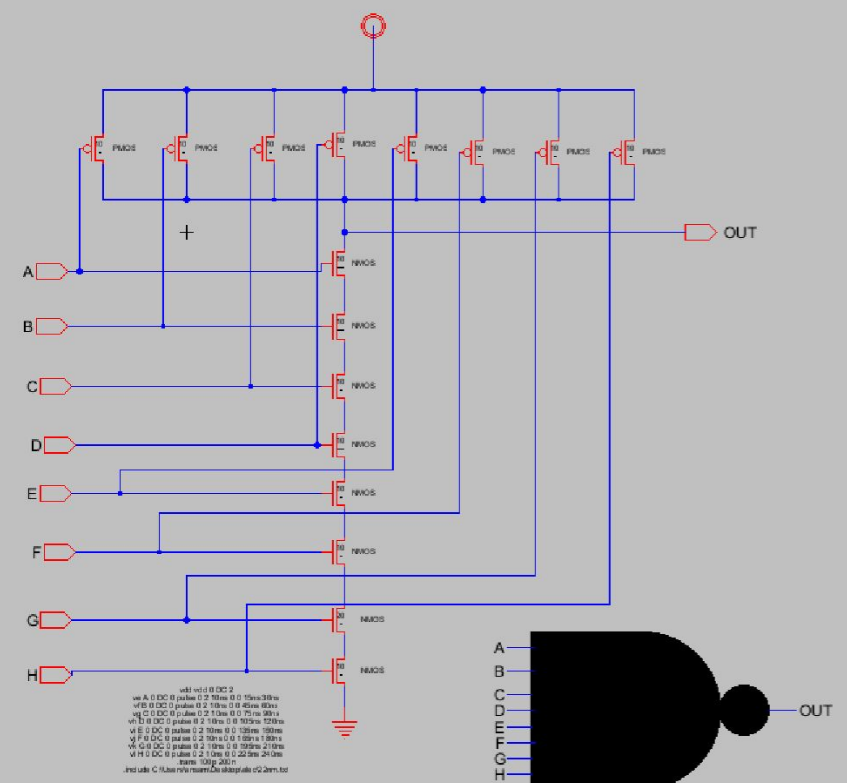


Figure 15-NAND Schematic

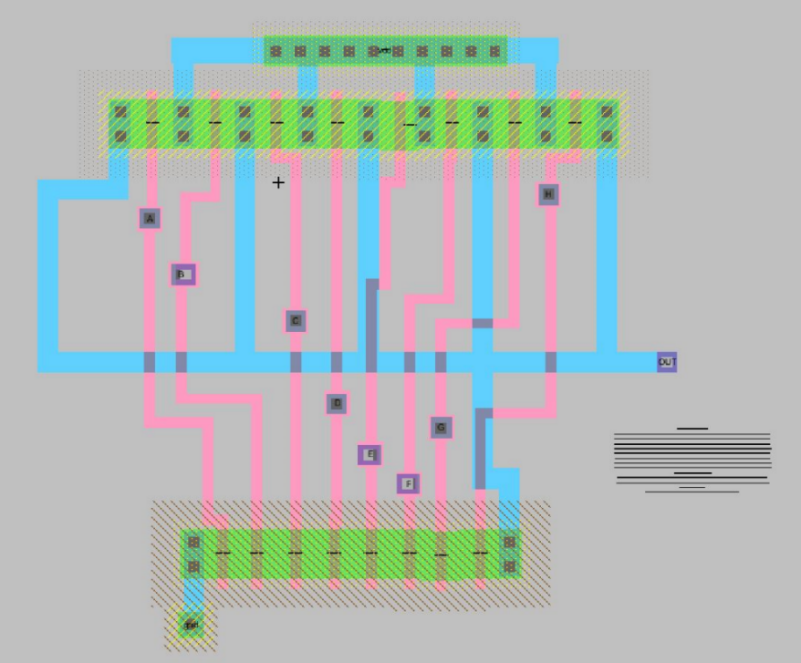


Figure 16-NAND LayOut

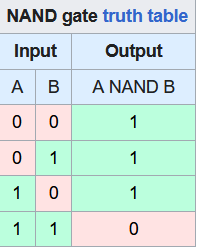


Figure 17-NAND truth table

1. 1-Bit CAM

The 1-bit Content-Addressable Memory (CAM) cir-cuit was implemented by incorporating additional inverters,

pass gates, and SRAM components for the purpose of com-

parison, which ultimately resulted in the generation of a match

signal [9]. Figure 4 depicts the schematic representation of the

1. bit CAM circuit.

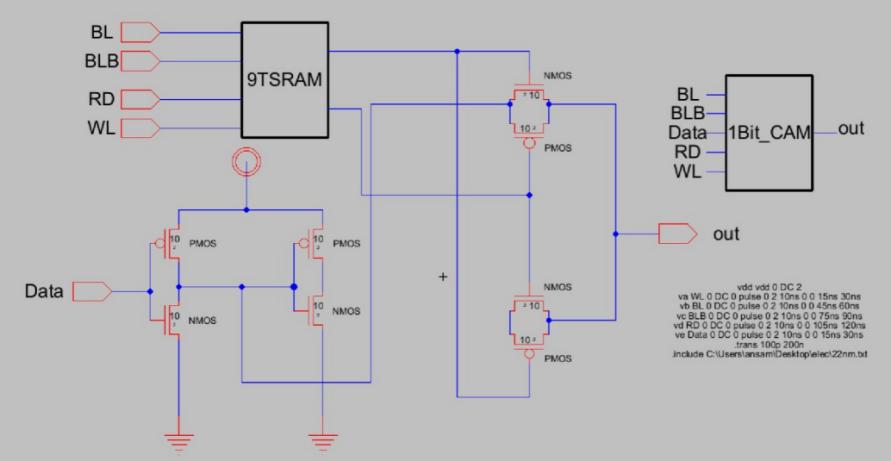
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Figure 18-1-bit CAM Schematic

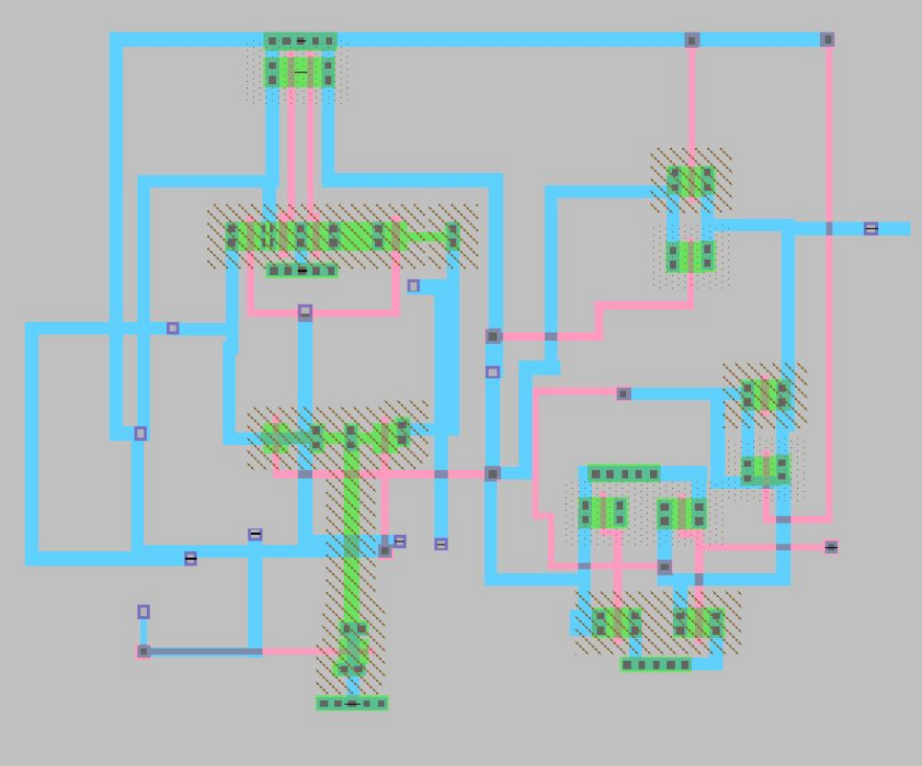


Figure 19-1-bit LayOut

g . 8-Bit CAM

The accompanying figure shows the completed circuit of the 8-Bit CAM with 9T SRAM. This was accomplished by using an inverter, NAND gates, a decoder, and a 1-bit CAM in the design and implementation to ascertain the 8-Bit CAM's output.

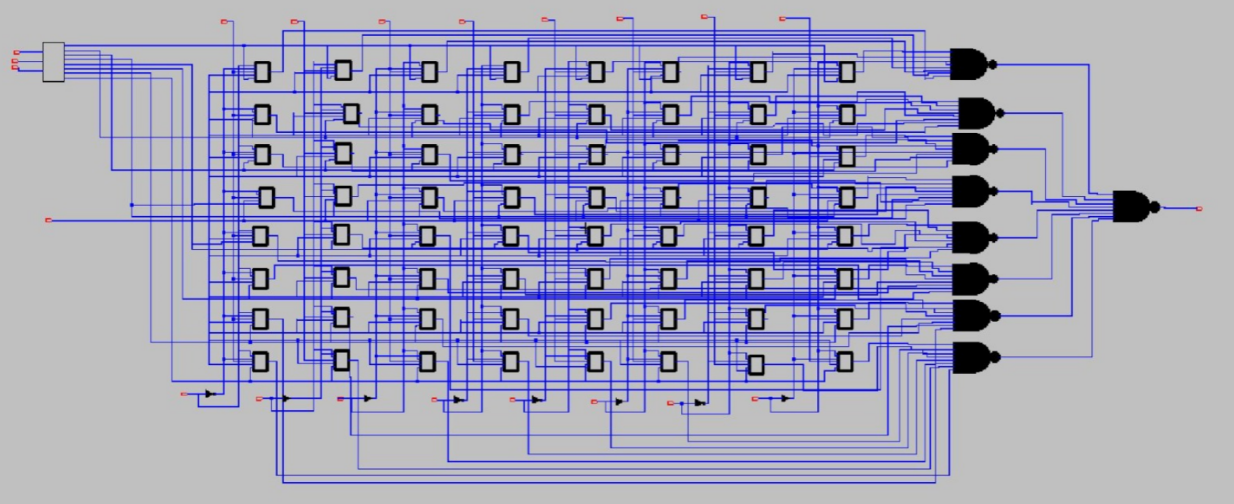


Figure 20-8bit schematic

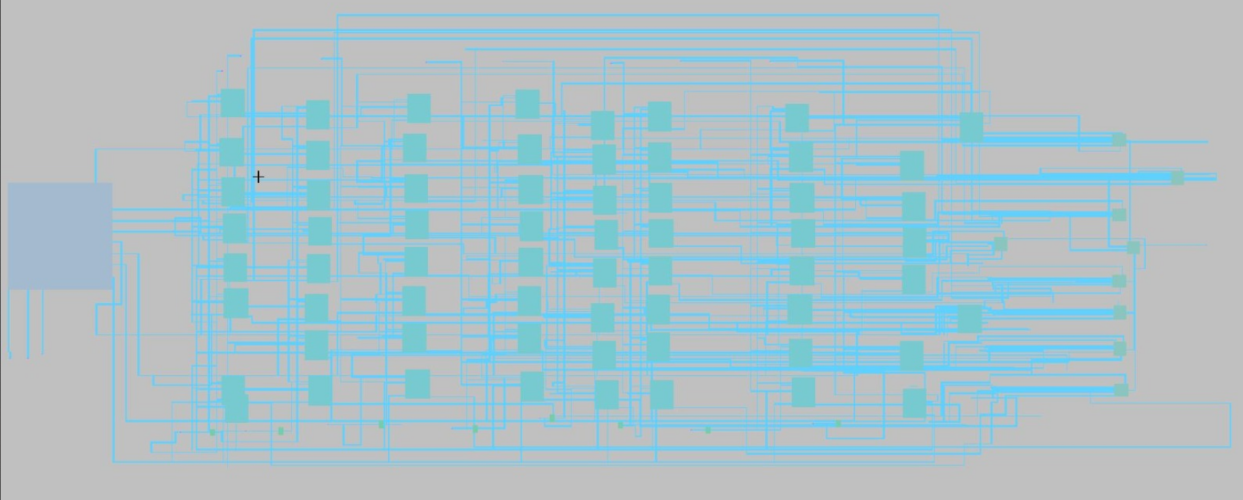


Figure 21-8bit LayOut

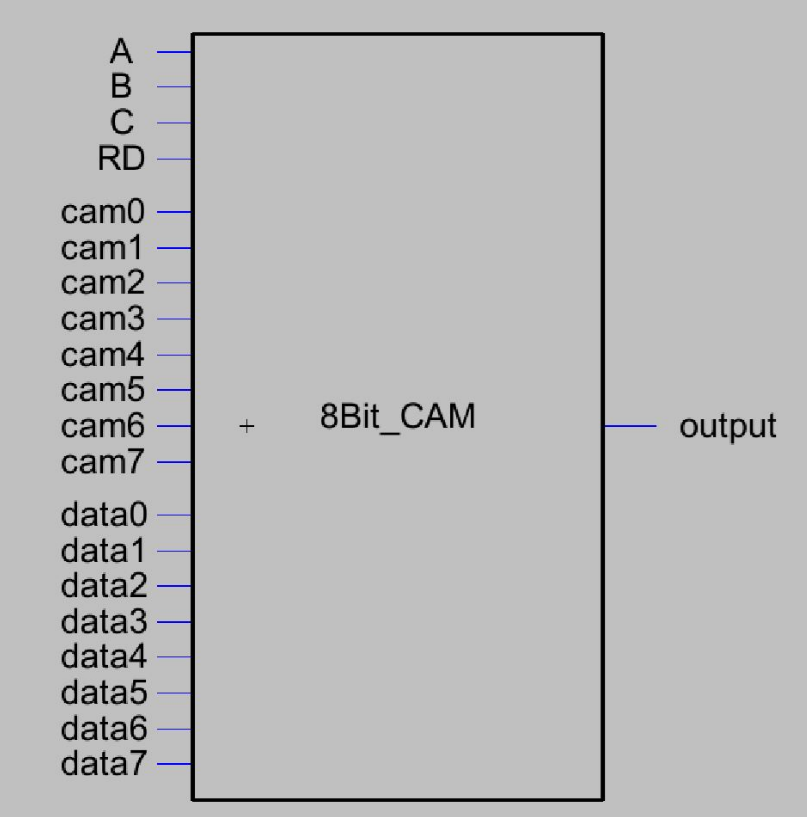


Figure 22-8-bit Icon

1. **RESULTS**

follows is the simulation for all the component built and

integrated in the 8 bit Cam along with the simulation and

testing for the 8 bit Cam.

1. 9STRAM

The write operation is controlled by the write line. When the write line is low, the memory cells are in a read-only mode.but When the write line is high, indicating a write.

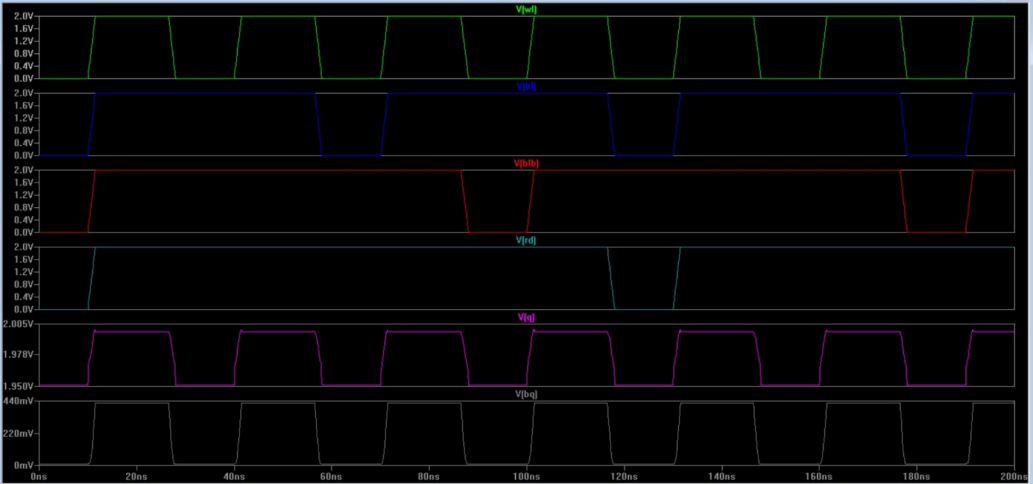


Figure 23-9STRAM result

1. INVERTOR

It was found that the inverter's output was the input signal's logical complement.

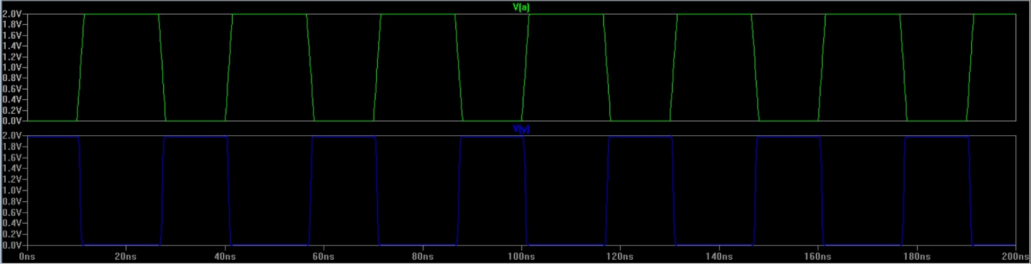


Figure 24-INVERTOT result

1. NOR GATE

When at least one of the three input signals was true, the gate's output was observed to be false; otherwise, it was observed to be true.



Figure 25-NOR result

1. DECODER

The figure shows that there is only one active in the output in every situation since the decoder's output can only have one active in it.

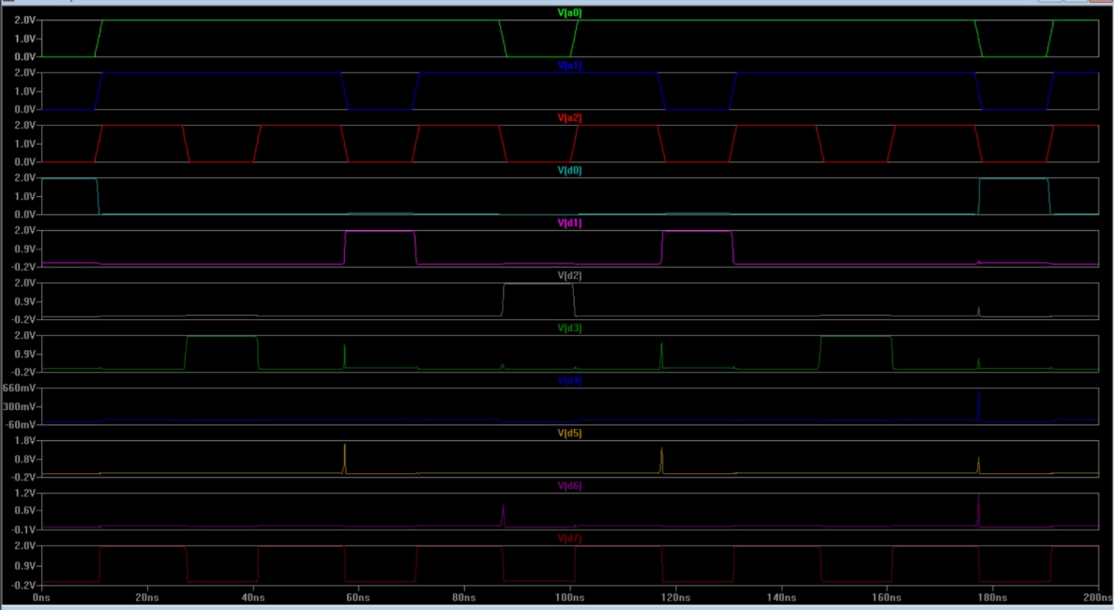


Figure 26-DECODER result

1. NAND GATE

The results here are as accurate as those in the truth table.

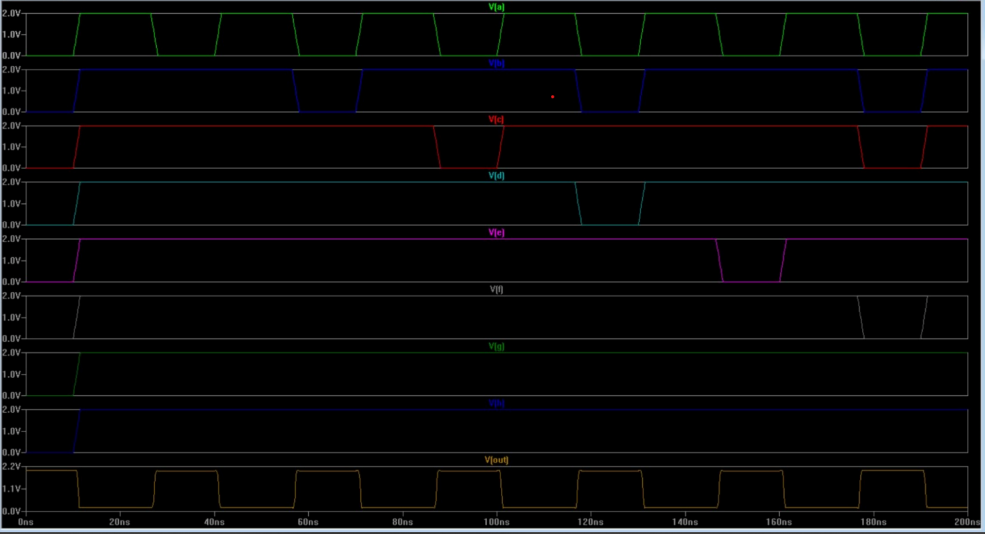


Figure 27-NAND result

1. 1-Bit CAM

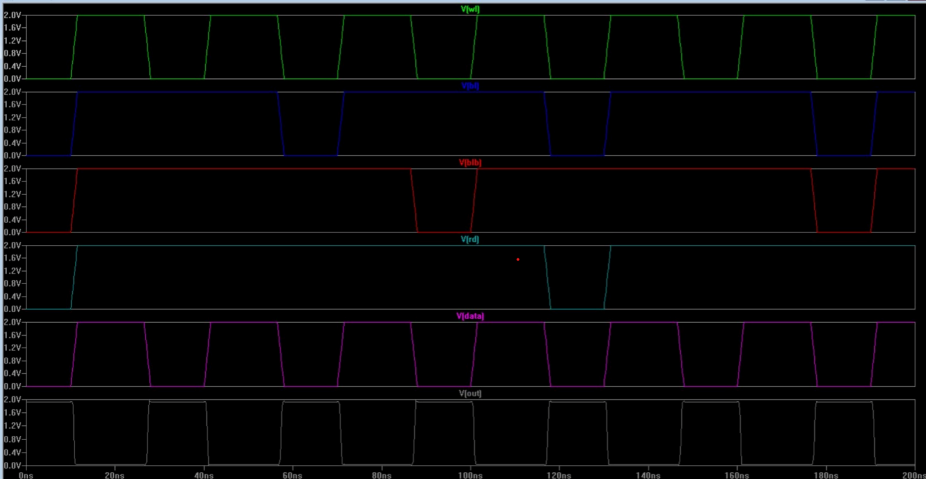


Figure 28-1BIT CAM result

1. 8 bit CAM

A complete computational analysis is used to predict the functionality and performance of the 8-Bit Content-Addressable Memory (CAM) circuit enhanced with a 9T static random-access memory (SRAM).

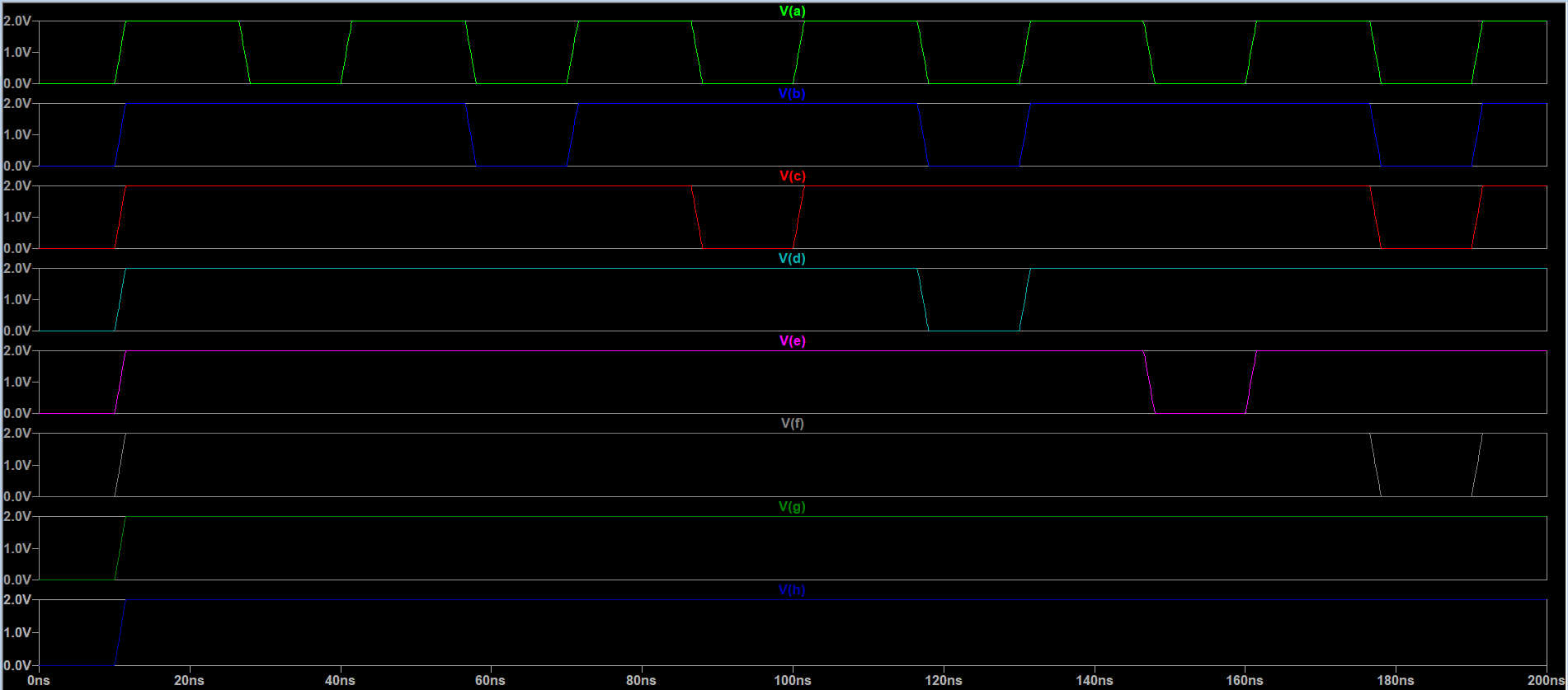


Figure 29-8 BIT CAM result

1. AREA, POWER, AND DELAY OPTIMIZATION

|  |  |  |
| --- | --- | --- |
| COMPONANT | DELAY | POWER |
| 9TSRAM | 25u | 5ps |
| 1 BIT CAM | 21 ps | 43.8 MW |
| 8 BIT CAM | 38 | 54.1 MW |
| TRANSISTOT width= 10 | 0.05ns | 1.2MW |

TABLE I: DEAY AND POWER

1. CONCLUSION

In conclusion, a complete analysis and comprehensive presentation of the design and implementation phases of the 8-Bit CAM circuit were made. Every component used in the final circuit has a precisely defined layout and schematic circuit. Furthermore, particular methods were used to optimize the 8-Bit CAM's power consumption, area utilization, and latency while making sure that these optimizations didn't impair the Content Address Memory's (CAM) performance or searching abilities. It is noteworthy that the simulation findings for different circuits were carefully gathered, painstakingly examined, and clearly conveyed.

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