

# Mohd Shahedur Rahman

Electrical & Electronics Engineer

☎ 017614678019

✉ shahedsajal03@gmail.com

🌐 <https://www.linkedin.com/in/mohd-shahedur-rahman-85ba35283>

🏠 Kasseler Straße 37, 28215, Bremen.

## Profile

M.Sc. in Control, Microsystems, and Microelectronics student at Universität Bremen with hands-on experience in ASIC design (RTL-to-GDSII) and industrial production engineering. Combines strong technical skills in Cadence Innovus/Genus, Verilog, and COMSOL with practical knowledge of manufacturing optimization (6S, Kaizen, ERP/MES systems). Proven ability to bridge theoretical concepts (e.g., PPA optimization in 40nm FinFET designs) with real-world applications (e.g., automated assembly line management).

## Skills

**Manufacturing & Equipment:** Machine setup/adjustment, production line monitoring, quality assurance, equipment maintenance.

**Software & Tools:** Cadence Innovus, Cadence Genus, Verilog, Synnopsys Design Vision, Verilator, COMSOL, MATLAB & Simulink, Microsoft Office, Linux, KiCad (PCB & schematic design), Altium (basic), Oracle ERP, MES (Manufacturing Execution System).

**Design:** CSS, HTML, Photoshop CS6.

**Programming:** Python (basic), C (basic).

**Languages:** English (B2), German (A2), Bangla (native), Hindi (advanced), Urdu (advanced).

**Certifications:** Introduction to SAP (2024), Arduino & Embedded Systems (IEEE), LaTeX Workshop.

## Academic Project

**ASIC Implementation of RISC-V & OpenPOWER Cores (RTL-to-GDSII) with hierarchical-Based Acceleration and Static time analysis. (G-1.3)**

*Universität Bremen*

**Tools:** Cadence Genus (Synthesis), Innovus (Physical Design), Chipyard, Verilog/SystemVerilog, TCL

Implemented end-to-end RTL-to-GDSII flow and gate level simulation for RISC-V (Ibex, BOOM) and OpenPOWER (A20) cores in 40/45nm FinFET, achieving 500 MHz timing closure with optimized PPA, DRC/LVS-clean GDSII, and automated the flow using TCL scripts for synthesis and P&R.

**Solar Cell Performance Optimization using Double Exponential Model**

*Bangladesh University of Business and Technology (BUBT)*

**Tools:** MATLAB, Simulink

Applied MATLAB modeling to evaluate Si, GaAs, and Ge solar cells, demonstrating GaAs as the most efficient material for high-performance photovoltaic applications.

## Experience

**VIVO Communication Technology Co. Ltd. (Best Tycoon)**

*Narayanganj, Bangladesh*

**Production Engineer & IN-CHARGE**

*20<sup>th</sup> November 2019 - 20<sup>th</sup> May 2021*

Optimized high-volume automated assembly lines by applying 6S/Kaizen/PDCA, managing material flow, quality control, fault analysis, and component procurement to improve efficiency and reduce defects.

**Solid State Ltd.**

*Dhaka, Bangladesh*

**Assistant Engineer**

*1<sup>st</sup> February 2018 - 31<sup>st</sup> January 2019*

Assisted in installation and commissioning of industrial electrical equipment. Conducted cost-benefit analysis for electrical machinery and supplies and Provided technical support during implementation and maintenance.

## Education

---

<b>M.Sc. in Control, Microsystems and Microelectronics(G-2.07 without Thesis)</b>	<i>Bremen, Germany</i>
UNIVERSITÄT BREMEN	
<b>B.Sc. in Electrical and Electronic Engineering (CGPA-3.80)</b>	<i>Dhaka, Bangladesh</i>
Bangladesh University of Business and Technology (BUBT) Major in Electronics	<i>Jan, 2018</i>

## Extra Curriculum

---

**Secretary at IEEE BUBT Student Branch.**

*Dhaka, Bangladesh*

Bangladesh University of Business and Technology (BUBT)

*2017 - 2018*

**CMM & CIT examination board Member**

*Bremen, Germany*

University of Bremen

*2024-continue*

## References

---

**Prof. Dr.-Ing. A. Garcia-Ortiz**

*Msc Supervisor*

Chair for Integrated Digital Systems, Universität Bremen

[agarcia@item.uni-bremen.de](mailto:agarcia@item.uni-bremen.de)

**Abdullah Bin Shams**

*Bsc Supervisor*

PhD student, University of Toronto, M.Sc., Karlsruhe School of Optics and Photonics, KIT

[abdullahbinshams@gmail.com](mailto:abdullahbinshams@gmail.com), [shams@bubt.edu.bd](mailto:shams@bubt.edu.bd)