SYNOPSYS®
Silicon to Software™

Embed-It! Integrator Quick Start Guide

DesignWare Foundation IP AE Team

March 2022

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Installation

Software and Licensing

- Integrator software
  - You need to install this software before you can use the memory compilers.
  - Installation instructions are available at the link below (SolvNetPlus account required):
    - Designware Embedded Memory IP installation and usage
  - Download location
    - https://solvnet.synopsys.com/DownloadCenter

- Install license file and set the path to the file:

```
setenv LM_LICENSE_FILE /<path>/<license_file>
```

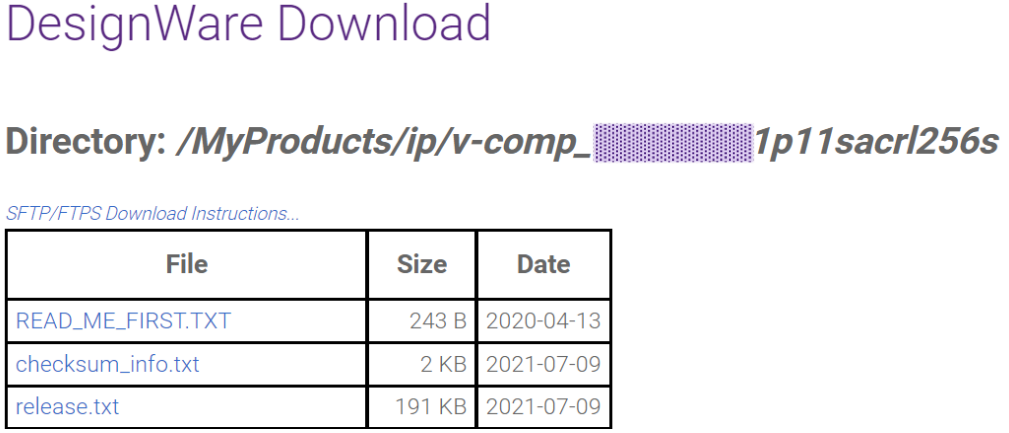
- Latest Installation Guides
  - https://www.synopsys.com/support/licensing-installation-computeplatforms/licensing.html

- CAUTION: if you install a new memory compiler, you may need to install the latest version of Integrator software. Check the release.txt in the memory compiler directory for the required Integrator (EMBEDIT) version:
  - `EMBEDIT_VERSION : R-2021.03-SP1+`
    - Requires version R-2021.03-SP1 or later

Installation

Memory compilers

- Download memory compilers
  - Download location: myDesignWare
  - Follow SFTP/FTPS Download Instructions


DesignWare Download

Directory: /MyProducts/ip/v-comp_[redacted]1p11sacrl256s

SFTP/FTPS Download Instructions...

File	Size	Date
READ_ME_FIRST.TXT	243 B	2020-04-13
checksum_info.txt	2 KB	2021-07-09
release.txt	191 KB	2021-07-09

- Define the memory compiler directory in your setup

```
setenv VL_COMPLIB_PATH /<path>/<memory_compiler_library_directory>
```

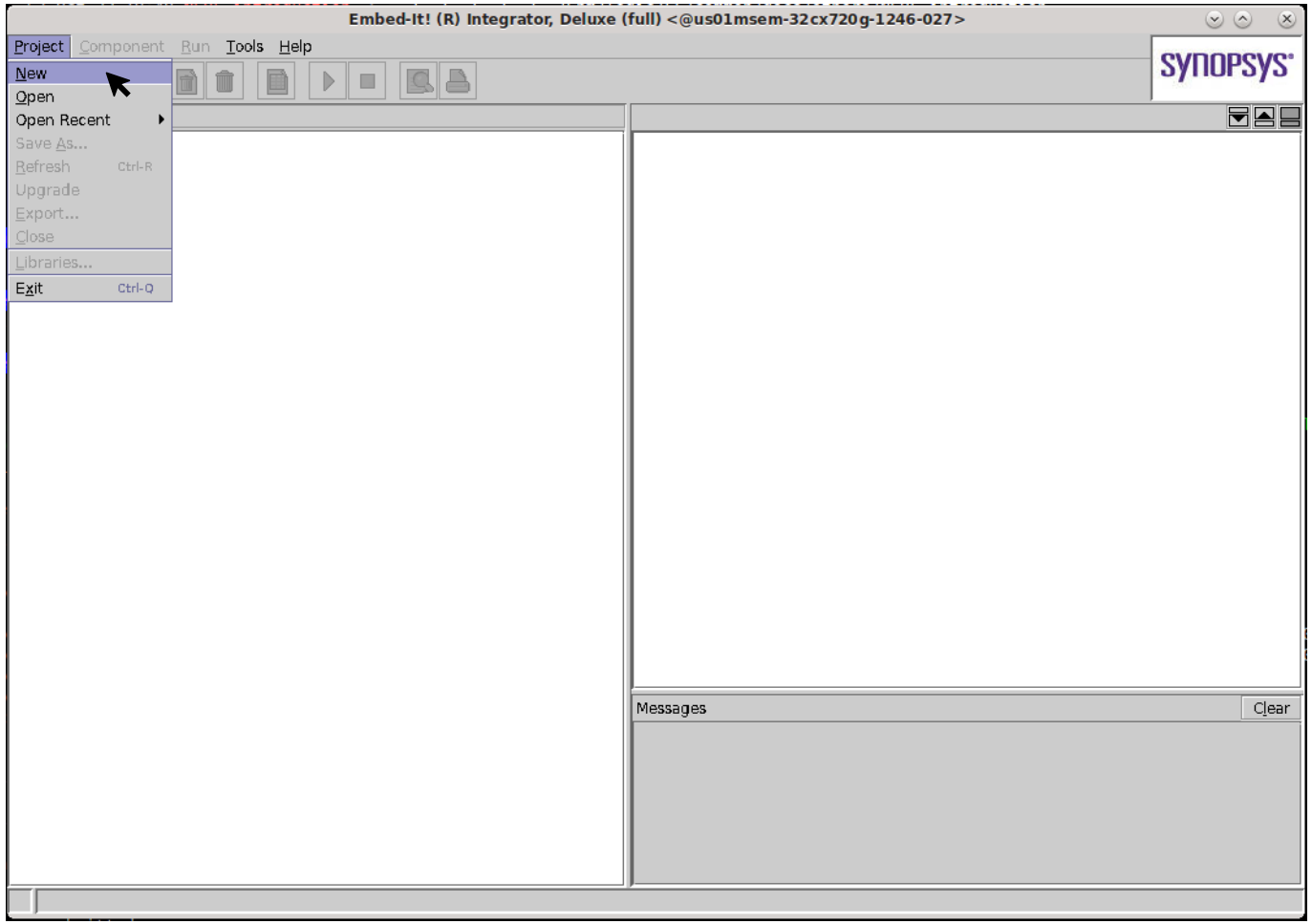
IMPORTANT! Do NOT point to the actual memory compiler directory, e.g., xx16n…

Point to one level above the actual memory compiler directory.

Documentation Resources

- Memory Compiler Release Notes
  - `release.txt` in the memory compiler folder
- Memory Compiler User Manual
  - `edoc*.pdf` in the memory compiler folder
- Embed-It! Integrator User Manual
  - `<integrator_install_path>/doc/integrator.pdf`
- Application Notes
  - Step 1: Login to myDesignWare with your SolvNetPlus credentials
  - Step 2: Search for IP…
  - Step 3: Check all the application notes under the "Documentation“ section
- SolvNet**Plus** Articles
  - Step 1: Login to SolvNet**Plus**
  - Step 2: Search for key words
- Memory Datasheet
  - `<instance_name>_allpvt.ds` in the instance generation output folder

Ready? Let’s start memory generation!

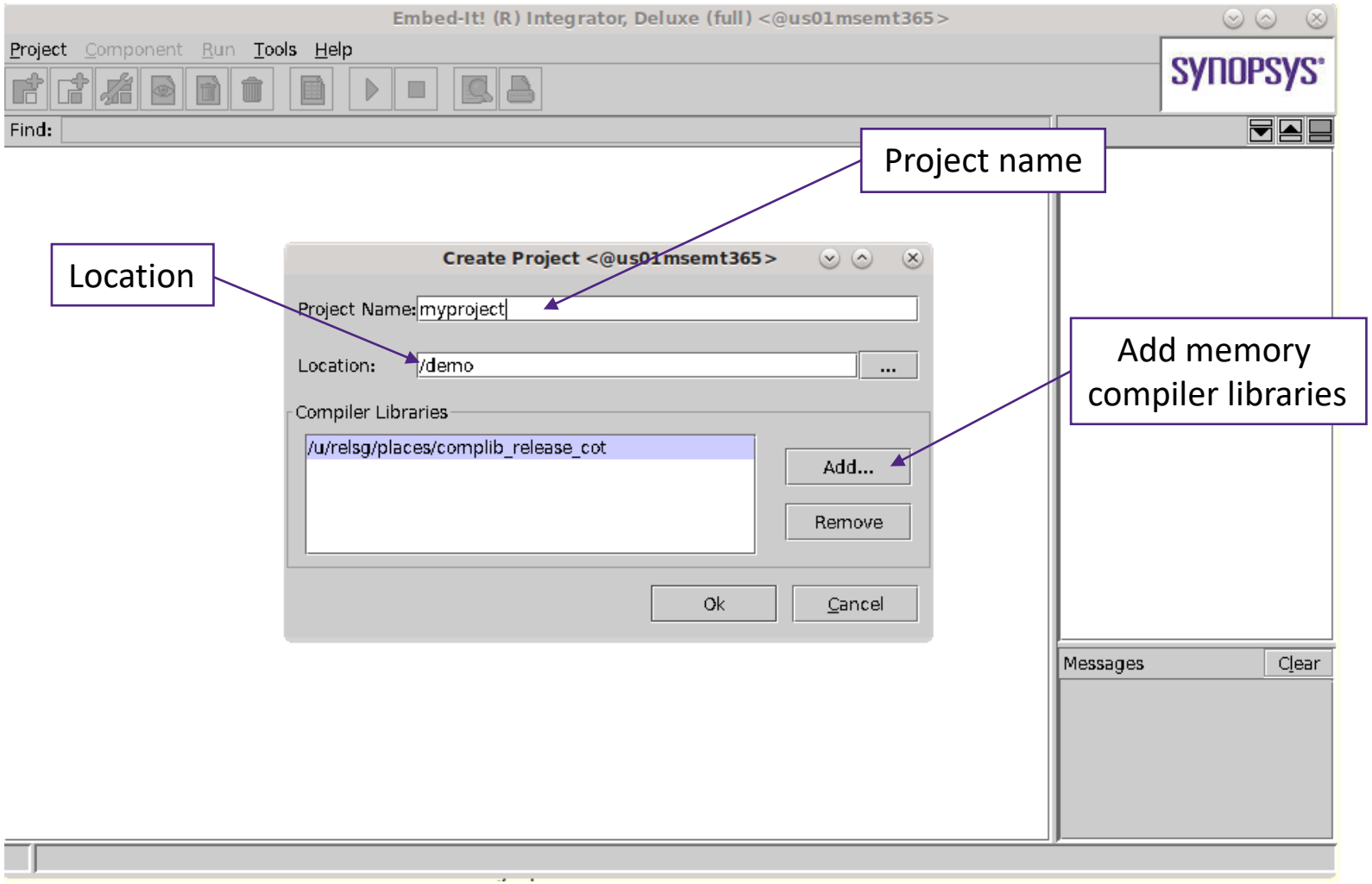


- Launch Embed-It! Integrator

```
unix%> integrator &
```

- Create “New” Project

Create Project

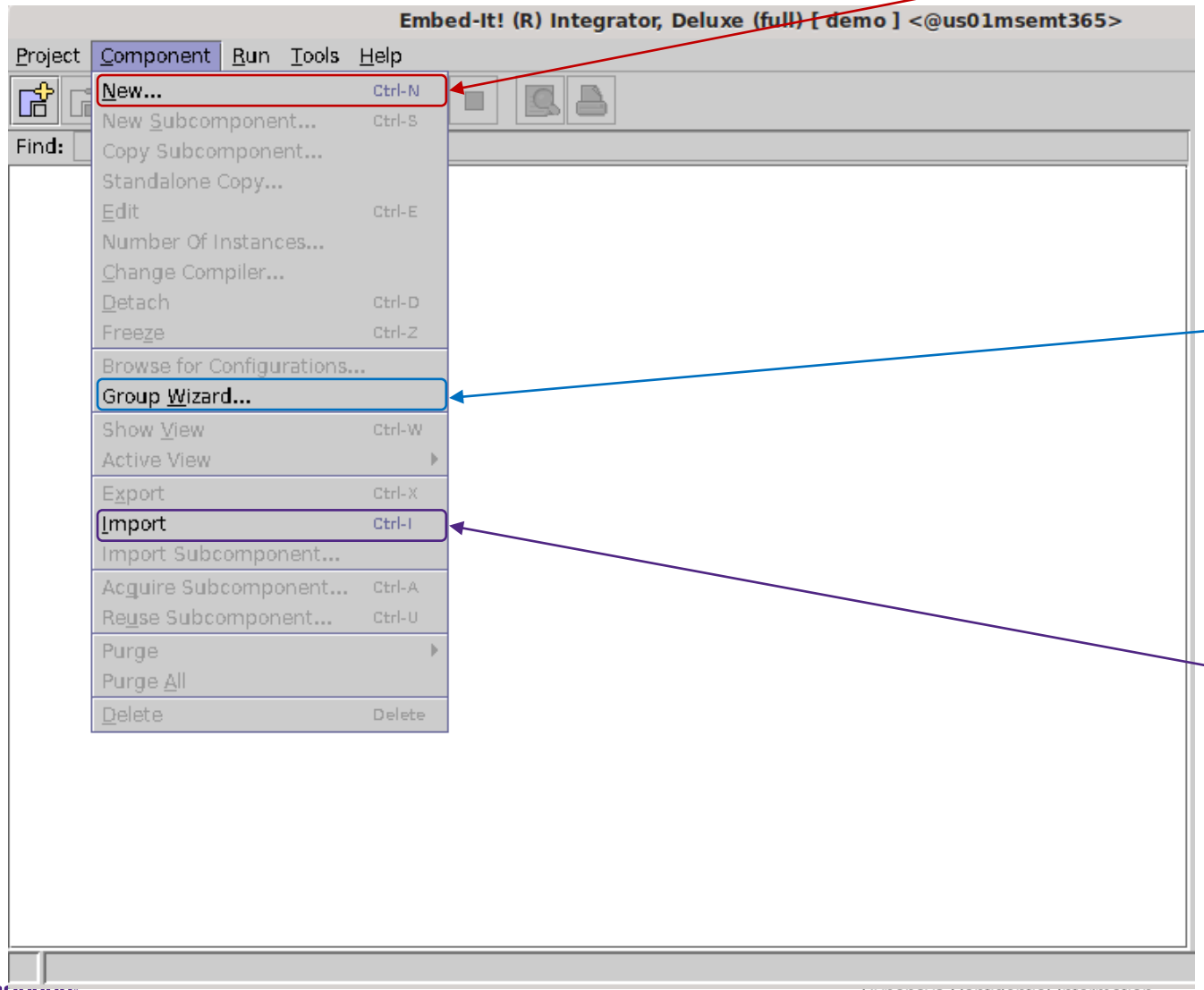


- Enter Project Name and Location
- Add compiler libraries

Please enter the folder where the memory compilers are located.

Do NOT enter the compiler folder itself here.

Configuring Memory Instances – 3 ways



❶

Select “Component” → “New…” to add individual instances

OR

❷

Select “Component” → “Group Wizard” to select optimum instances

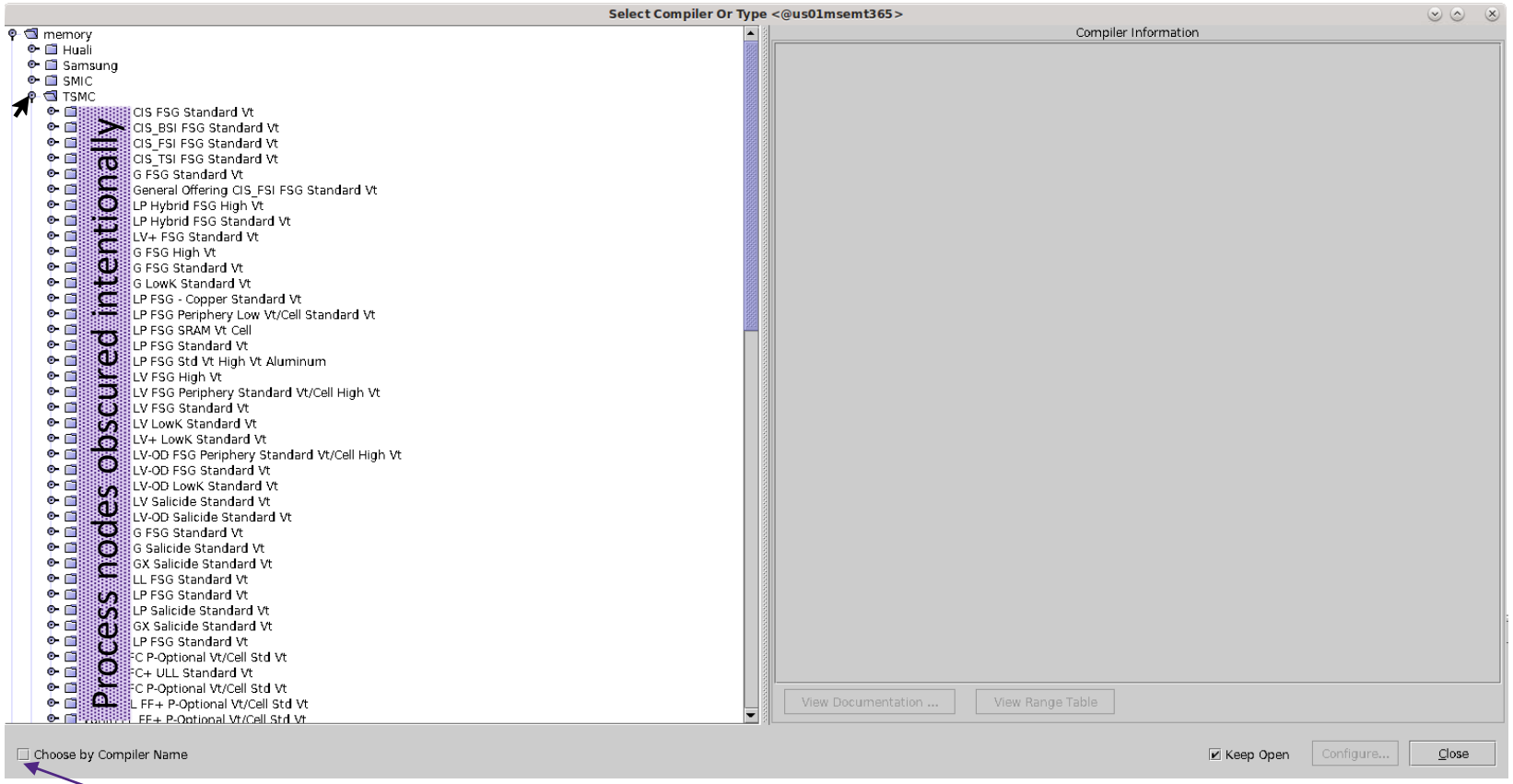
OR

❸

Import instance configuration (`.cfg`) files

Select Compiler Or Type

Project Window → “Component” → “New” → “Memory” (or “ROM”)



❶

Select Memory Type

➢ “Memory” = SRAM, Register File, TCAM

➢ “ROM”

❷

Select

“Foundry” → “Process Node”

Select Compiler Or Type

Project Window → Component → New → “Memory” (or “ROM”)

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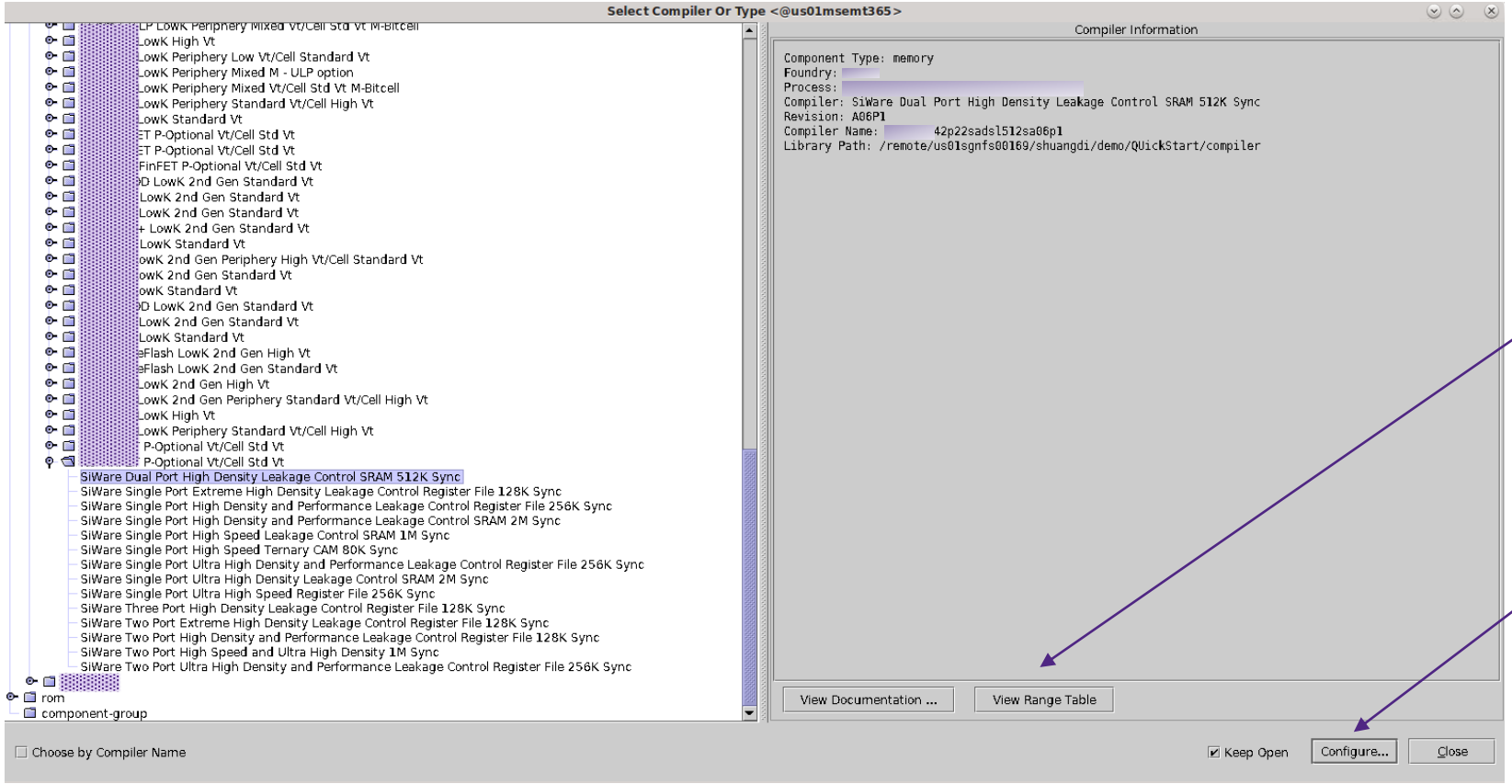
Subscribe to get automatic notifications of updates.

SolvNetPlus account required.

Must have active Maintenance to get updates.

Select Compiler Or Type

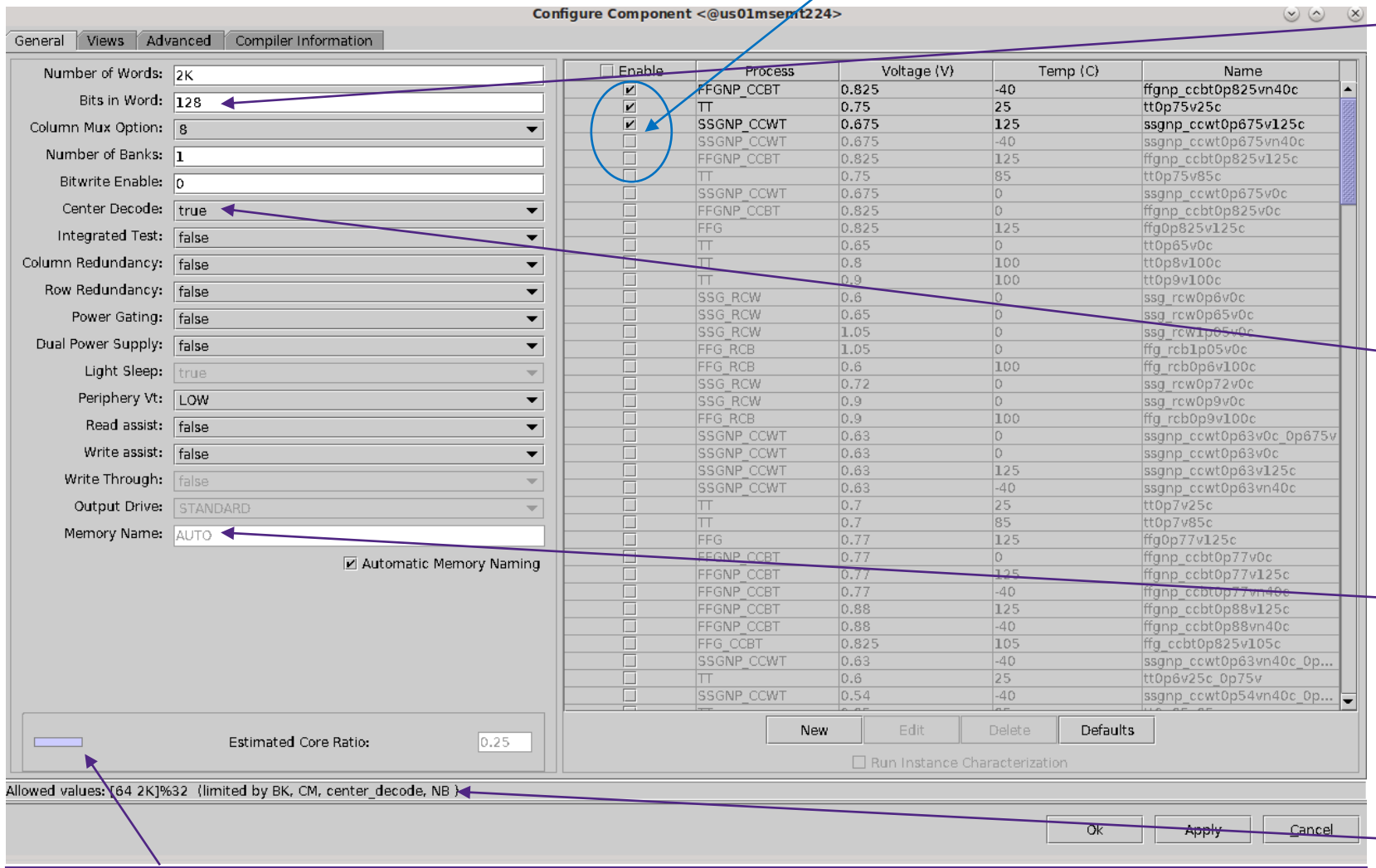
Project Window -> Component -> New -> “Memory” (or “ROM”)



- Click “View Range Table” to check the compiler support range
- Select “Configure…” to enter memory configuration data

The compiler name are hidden on purpose

Configure Component



- If required Bits in Word is greater than shown in Allowed values, adjust Center Decode, Number of Words or Banks accordingly
- Center Decode changed to true, then Allowed value for Bits in Word increase
- Refer to memory compiler User Manual for instance naming convention
- Valid data range shown

  % = allowed increment

Memory Configuration Basics

Feature*	Description/Notes
Number of Words (NW)	• Memory depth
Bits in Word (NB)	• Word width

Column Mux Option (CM)	• Changes aspect ratio with area trade-off
	  • NW / CM = # physical rows
	  • NB * CM = # physical columns

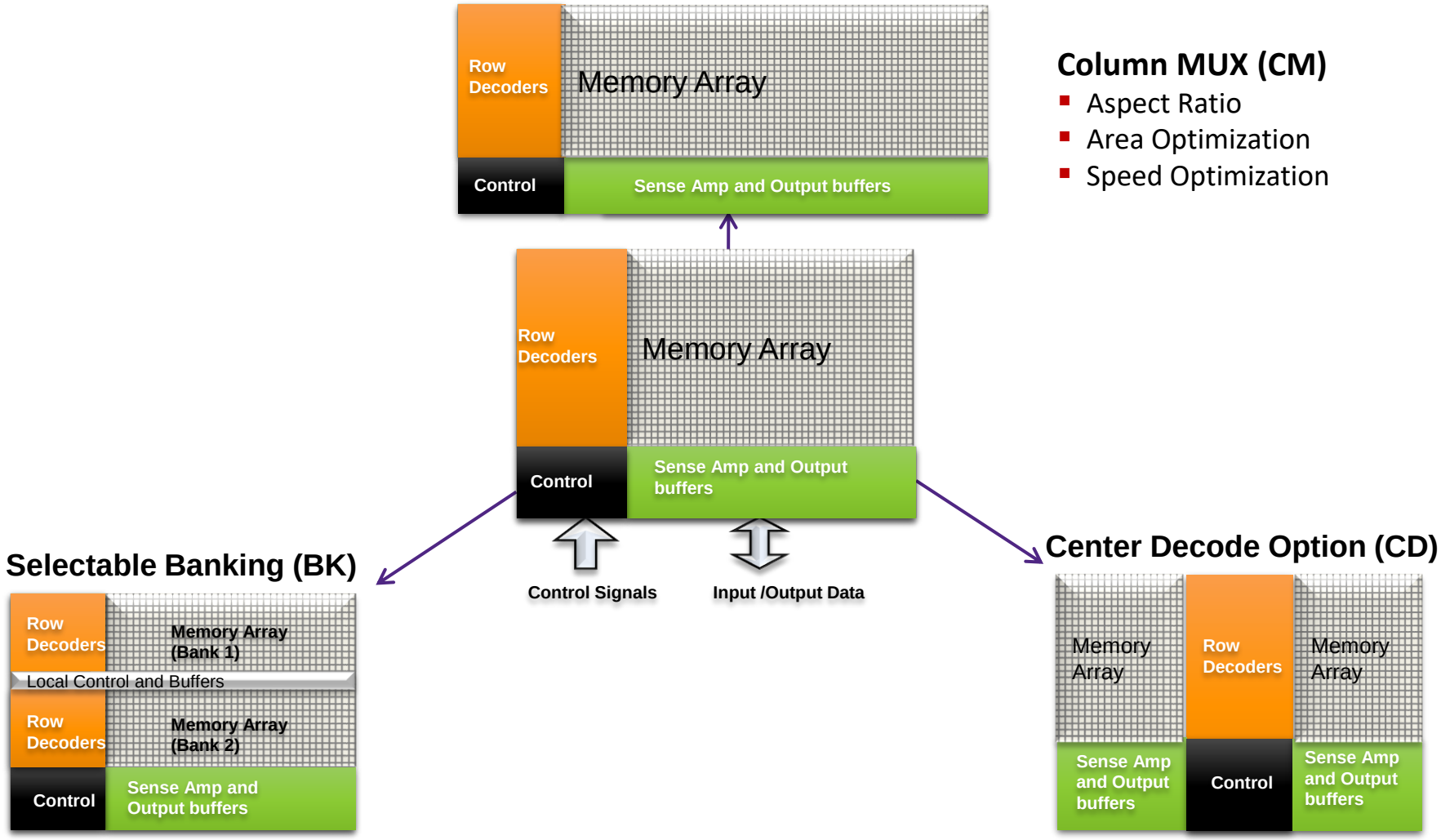
Center Decode	• Memory default has row decoder on left side, and a contiguous bit-cell array • Splits memory array into left and right halves, places row decoders in center of memory (left and right row decoders) • Extends word width • May improve performance, area trade-off for most of the compiler envelope
Number of Banks	• Splits the memory to create vertically stacked banks • Extends the range of number of words that can be used • May improve performance or dynamic power • Area trade-off
Bit Write Enable	• Enables Write Mask (per bit) • No area impact • Also called Sub-word (SW)
Periphery Vt (28nm and smaller geometries, some 40nm compilers)	• Allows selection of the Vt used in the periphery • Use to trade-off performance vs. leakage • No direct area impact (may allow use of smaller area instance to meet speed) • Note that the periphery Vt selected may not reflect the actual Vt mix used, although it will be the dominant Vt
Memory Name	• Allows customization of memory instance name. • Refer to memory compiler User Manual (edocxxx.pdf) for instance auto naming convention

Please note that listed features may not be available in all compilers

Please refer to the `<compiler_name>_custom.glb` file in the memory compiler directory for target memory compiler features.

Memory Configuration Basics cont'd

Column MUX, Banking, and Center Decode compile-time options



Memory Configuration Basics cont'd

Feature*	Description/Notes
Power Gating (40nm and smaller geometries)	• Adds internal power gating for power management modes • Enables Deep Sleep and Shut Down modes • Light Sleep mode is always available, regardless of Power Gating
Dual Rail (40nm and smaller geometries)	• Separates Array and Periphery power supplies • Adds level shifters between Array and Periphery • Allows Periphery to run at lower voltage than Array to reduce dynamic power and leakage
Leakage Control (65nm)	• Adds option to reduce leakage, controlled by Memory Enable pin (earlier version of Light Sleep mode)
Integrated Test	• Adds BIST MUXs • 40nm and smaller, also adds scan registers on memory input and output signals and compare/capture logic • Note that the BIST test data bus is 4 bits wide, designed to work with Synopsys memory BIST solution (STAR Memory System – SMS), can also be used with 3rd party BIST solutions
Scan Enable (12nm and smaller geometries)	• Adds scan chain and DFTMASK functionality • Can be found in the "Advanced" Tab → "Generic" Tree in the Configure Component dialog
Column Redundancy	• Adds redundant Column elements to the memory • Check with your foundry contact for redundancy guidance on your target node
Row Redundancy	• Adds redundant Row elements to the memory • Typically on single port memories, used when SoC has very high bit count • Check with your foundry contact for redundancy guidance on your target node

Please note that listed features may not be available in all compilers

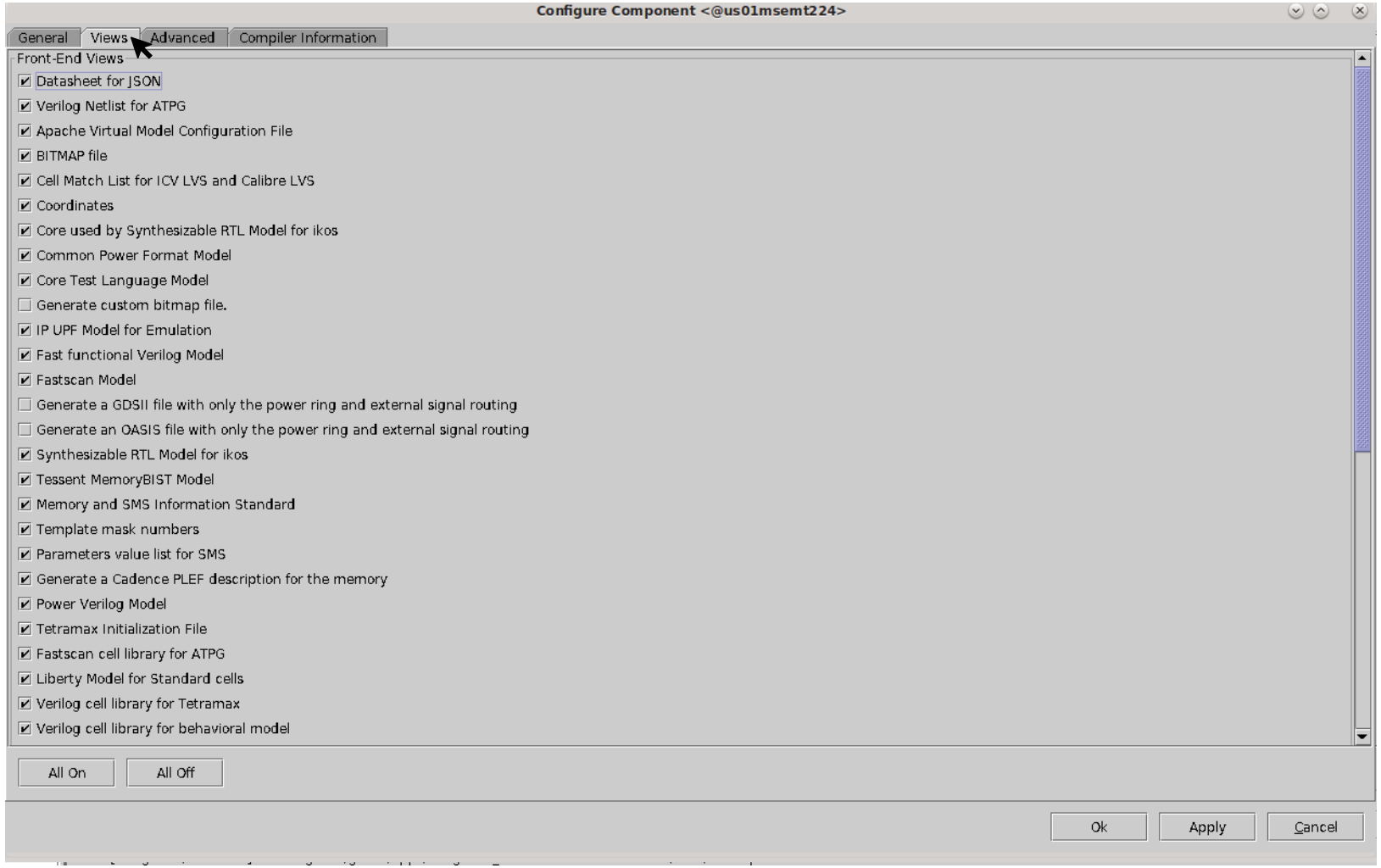
Please refer to the `<compiler_name>_custom.glb` file in the memory compiler directory for target memory compiler features.

About PVTs

- PVTs are available in two basic types: Single Rail and Dual Rail
  - PVT name includes extraction information
  - Single Rail example
    - tt0p75v25c, Typical extraction
  - Dual Rail example
    - tt0p65v85c_0p75v (separate periphery / array supplies, Typical extraction)
- Extraction
  - For information on RC extraction conditions for specific PVTs, please refer to the compiler User Manual.
- Supported PVTs
  - Refer to PVT_CORNER_SUPPORTED in the release.txt for specific memory compiler.
  - PVT definitions are also specified in the custom GLB file (<compiler>_custom.glb)
  - Some PVT clusters (e.g., Low Voltage, Overdrive) require an add-on license feature
    - This is listed in the custom GLB file
      - Please contact your Synopsys Account Team

View Selection

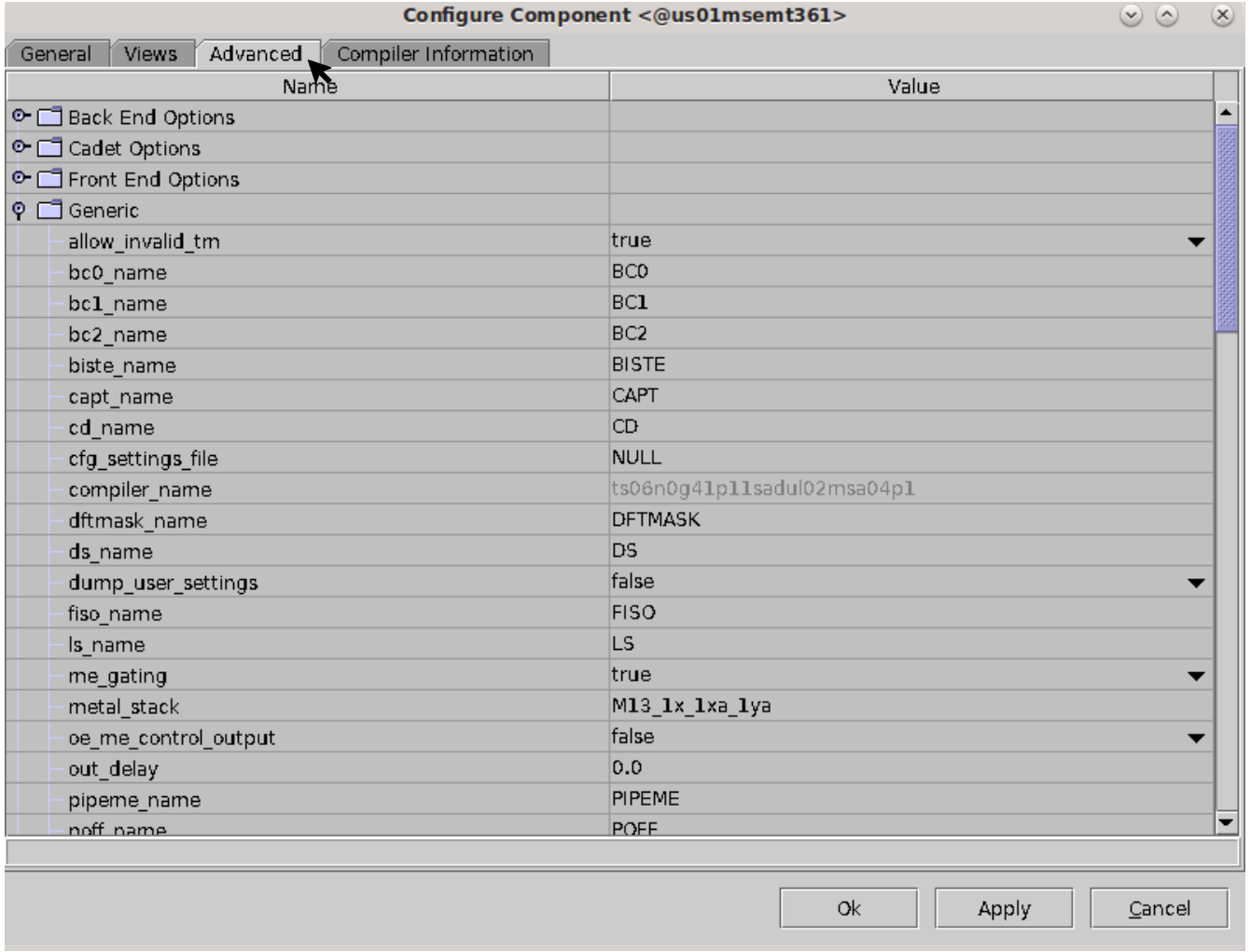
Select “Views” to define which EDA models are to be generated



If running with an evaluation license, only Front-End Views will be available (includes LEF)

Back-End Views will not be available (GDSII, Structural Spice netlist, Structural Verilog netlist and OASIS)

Advanced Settings

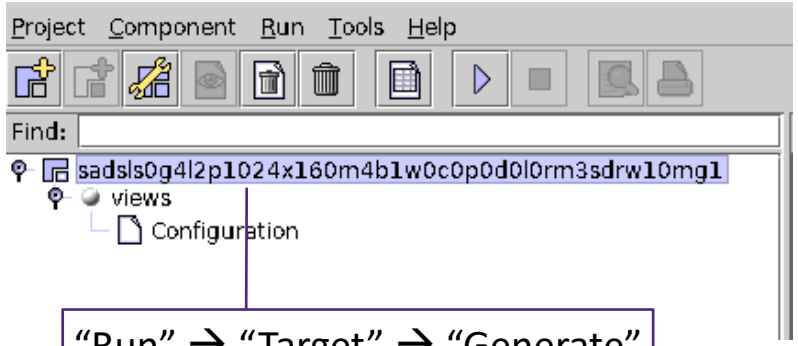


GUI Advanced Options

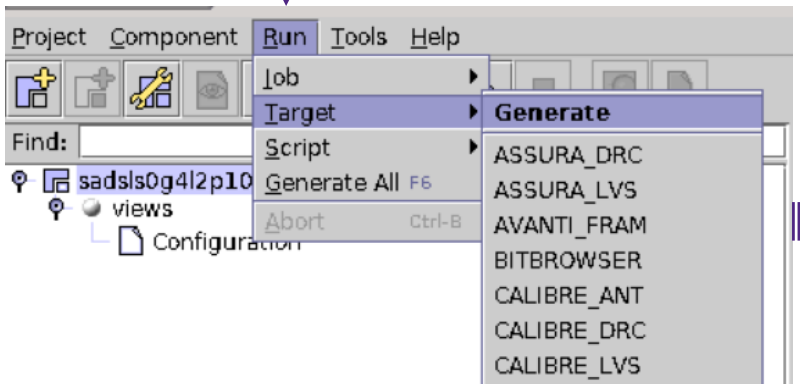
- Back End Options
- Cadet Options
- Front End Option
- Generic
- Parameter Options
- Pin Names

- Definitions for all the above settings are specified in the custom GLB file <compiler>_custom.glb.

Instance Generation



"Run" → "Target" → "Generate" to initiate generation

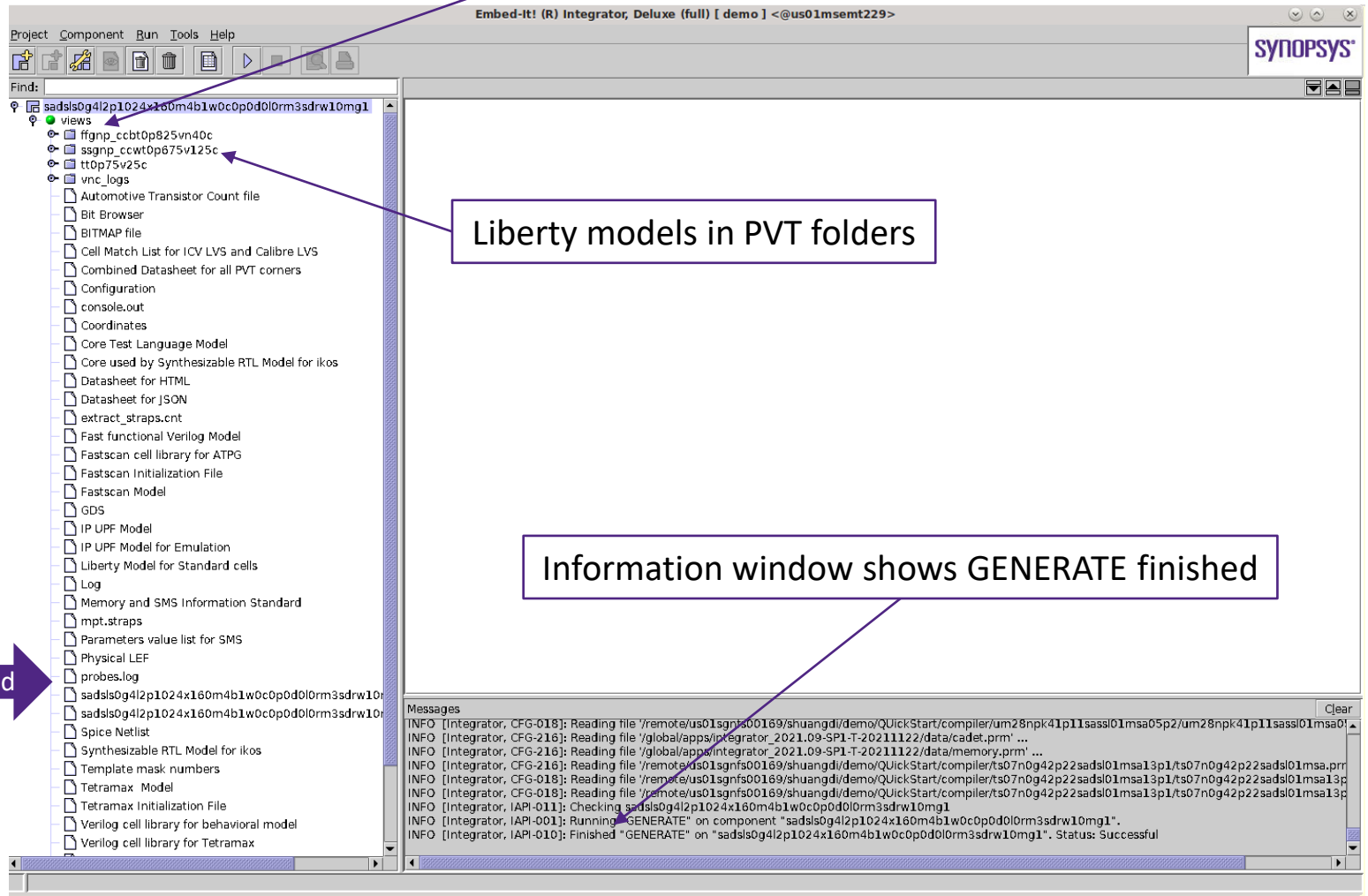


Finished

All selected views generated; instance completed

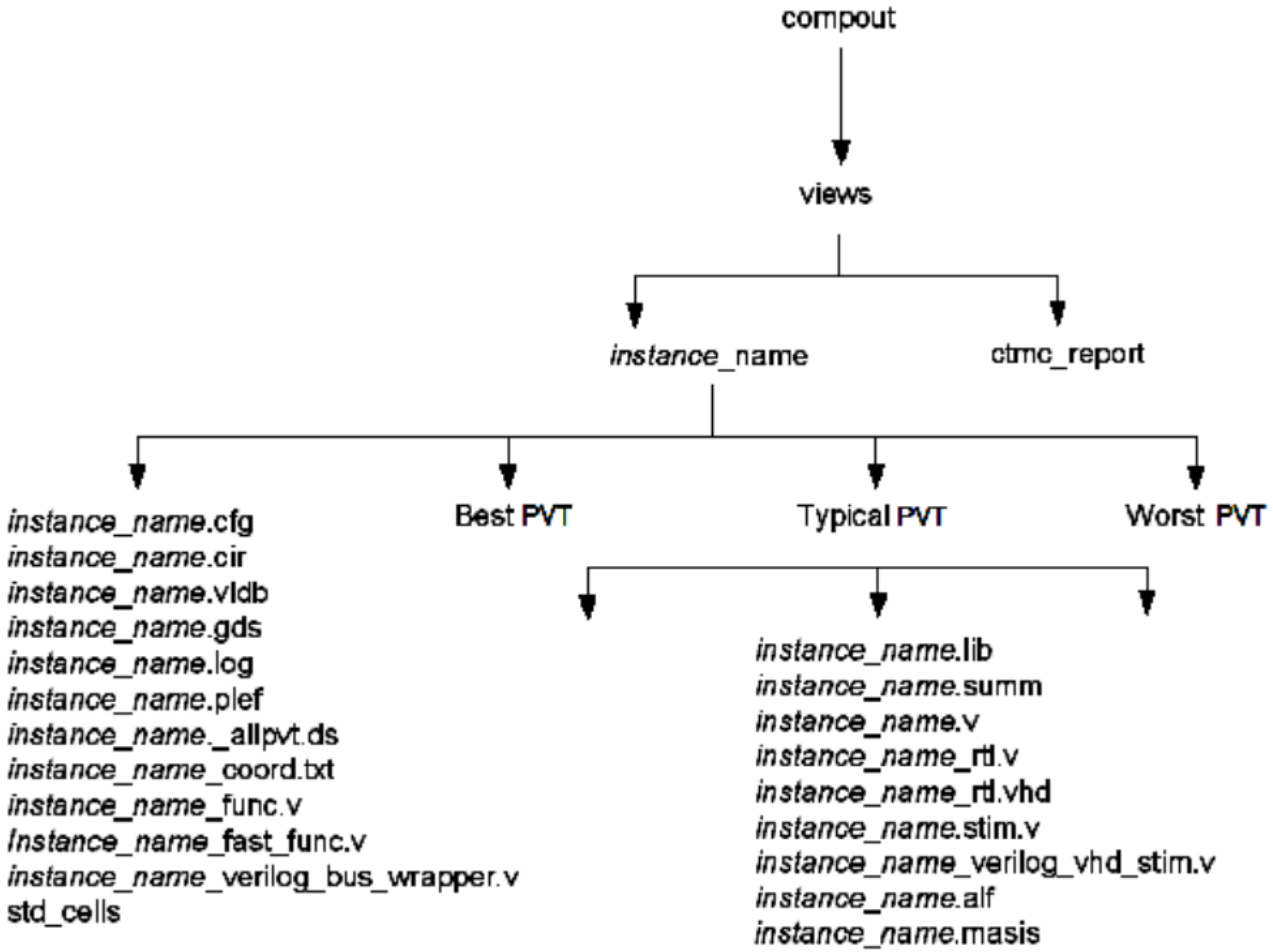
Liberty models in PVT folders

Information window shows GENERATE finished



Generated Instance Views

File Structure

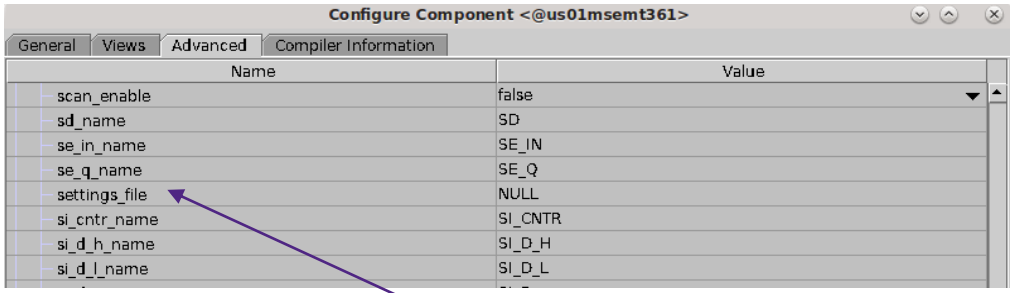


Refer to the respective memory compiler User Manual for additional details

Custom Settings File

- Can be used to define global settings for a project or block
  - e.g. PVTs, BIST, Power Gating, Dual Rail, custom pin names, periphery Vt, etc.
  - Simplifies changes
    - Only need to change data in the custom settings file, versus for each memory instance in the project
    - Can be used with scripts in batch mode
- Can have multiple custom settings files
  - Project level
  - Block level
  - Latest file overrides early settings
- Uses same syntax as `<memory_compiler_name>_custom.glb`
  - Located in in the compiler directory
  - Refer to additional details in Integrator.pdf manual

- Path to custom settings file is relative to memory compiler directory
  - Can specify absolute path
- The `.cfg` file will take priority over the custom settings file
- ***CAUTION!*** Memory Instance name is NOT updated to reflect changes made when a custom settings file is used



Scroll down to Settings File, enter path to custom settings file

Custom GLB File

`<compiler>_custom.glb` is located in the compiler directory

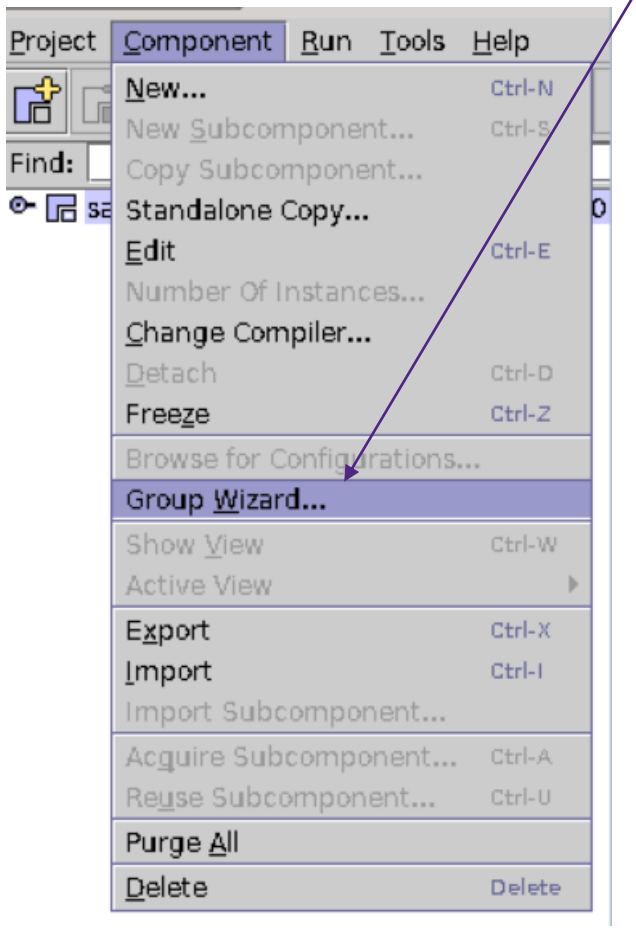
Parameter Group	Description
Feature Control	Parameters that influence the memory architecture
Timing Control	Timing mode selection
Views Generation	Parameters used to select which EDA views are generated
Verilog Options	Parameters defining syntax in the Verilog model
Naming Convention	Change the default signal pin naming
PVT Definitions	Selection of PVTs to be generated
Front End Options	Definitions of templates and associated parameters used for Front End EDA views

See `<compiler>_custom.glb` file for more parameters and refer to the Integrator User Manual for additional details.

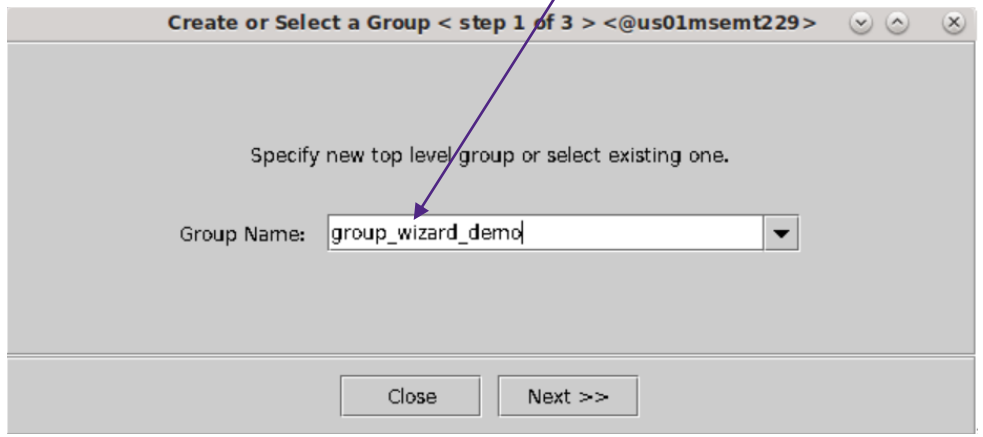
Group Wizard

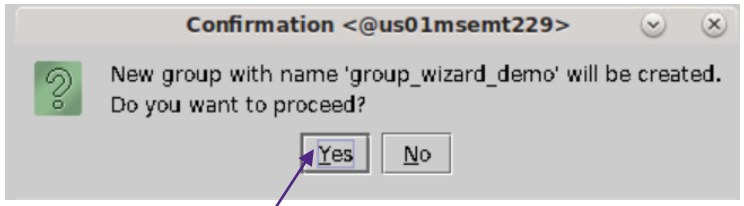
Group Wizard

Select “Group Wizard…” from Component menu



Enter Group name and select “Next…”

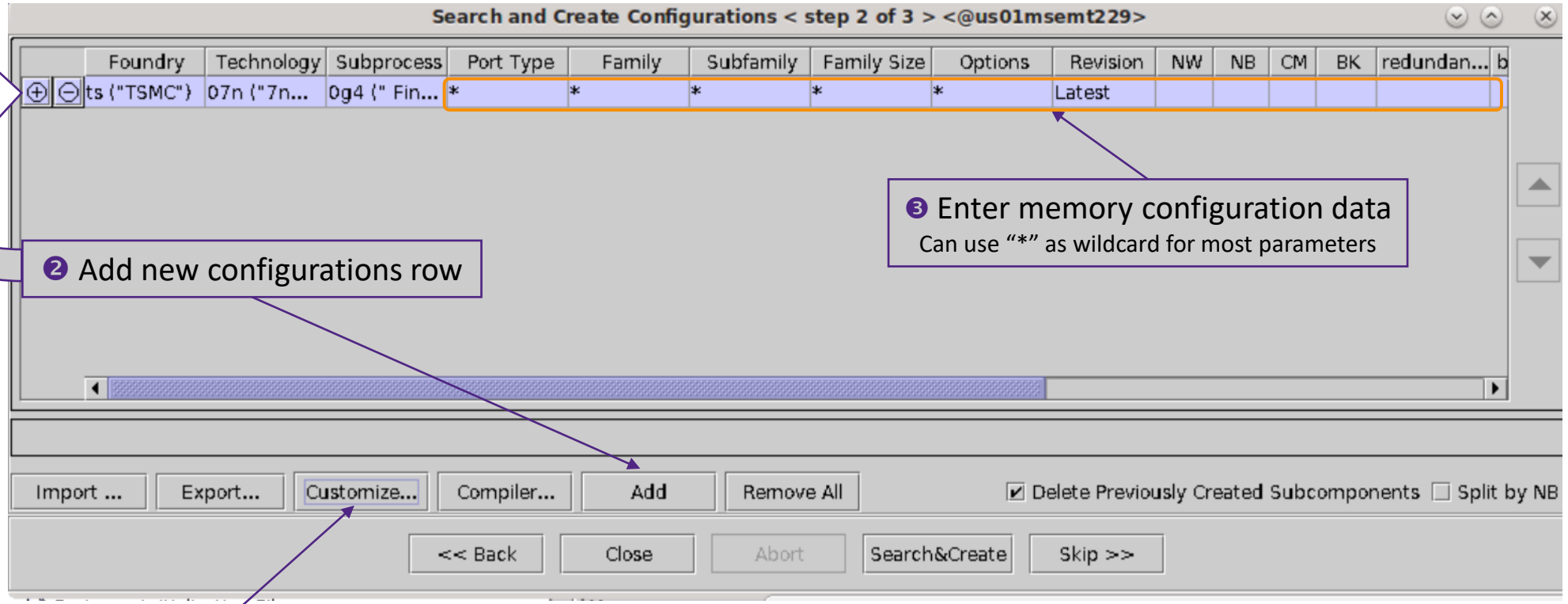


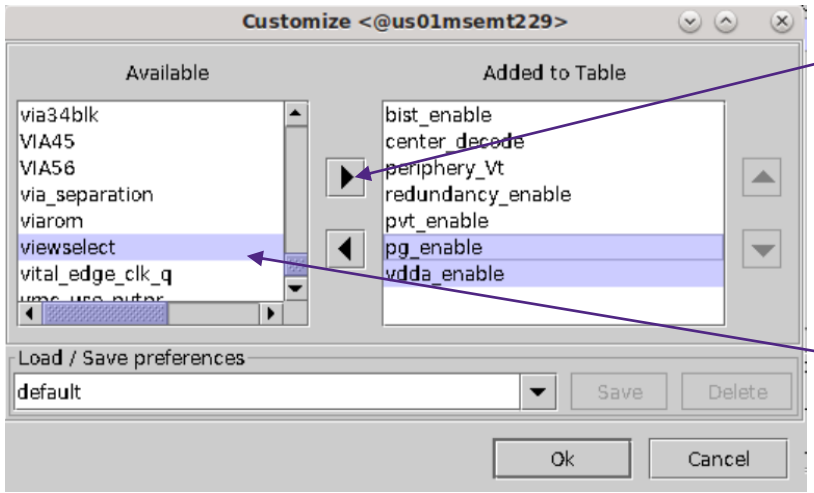


Select “Yes” on the popup window to setup the group

About Group Wizard

- Used for configuration browsing
- Generates PPA (Performance, Power and Area) reports in .csv format
- Intuitive GUI to create many instance configurations with ease
  - Use with caution though because the number of instances can grow quickly, and memory generation time will increase
- Multiple groups of instance in one project
  - All use the same report setup



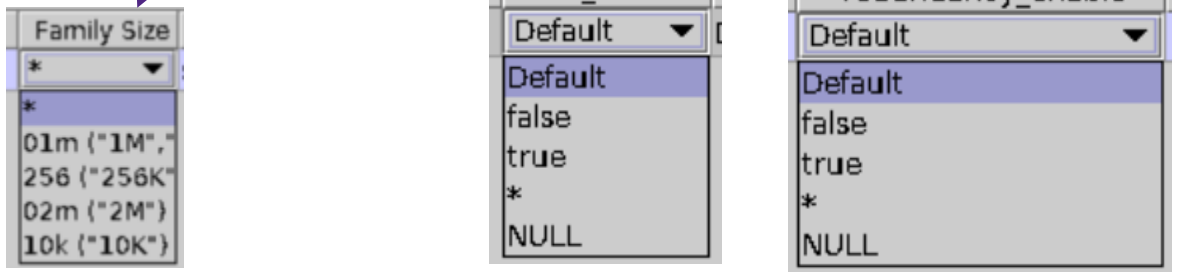


Select parameters on left to add, then click right arrow to add to table

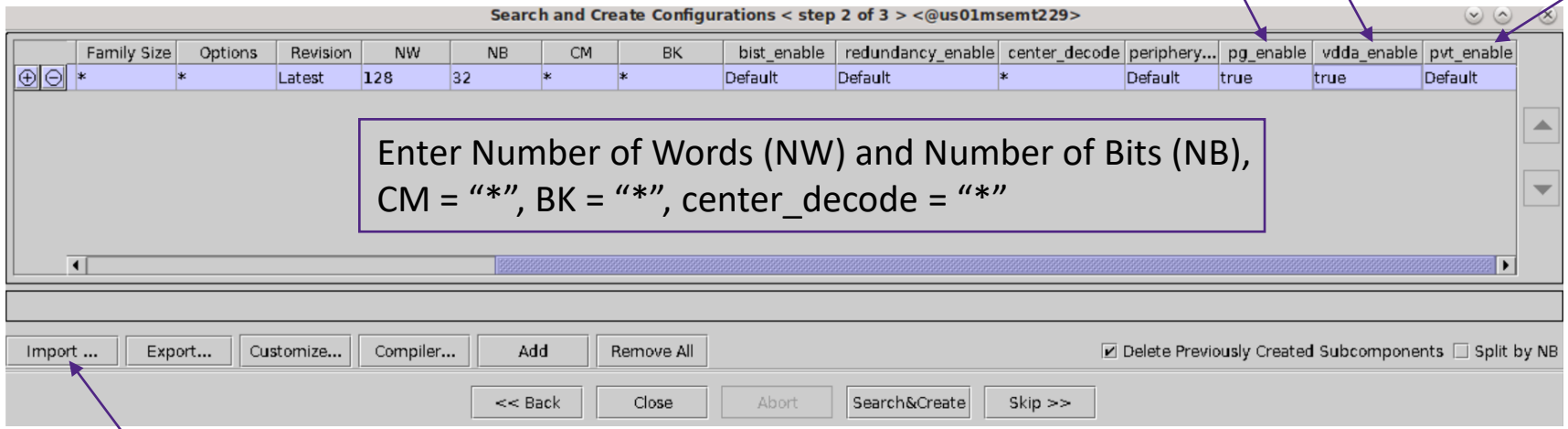
To add desired EDA views, choose "viewselect" and add to table, then enter the list of views in braces "{ }" (see Appendix A for sample list of EDA views)

If wildcard used for Subfamily, use wildcard for Family Size

Set redundancy and BIST as needed; can use wildcard to check area impact, however, instance count may quadruple



pg_enable = “true” for extra Power modes
vdda_enable = “true” for Dual Rail



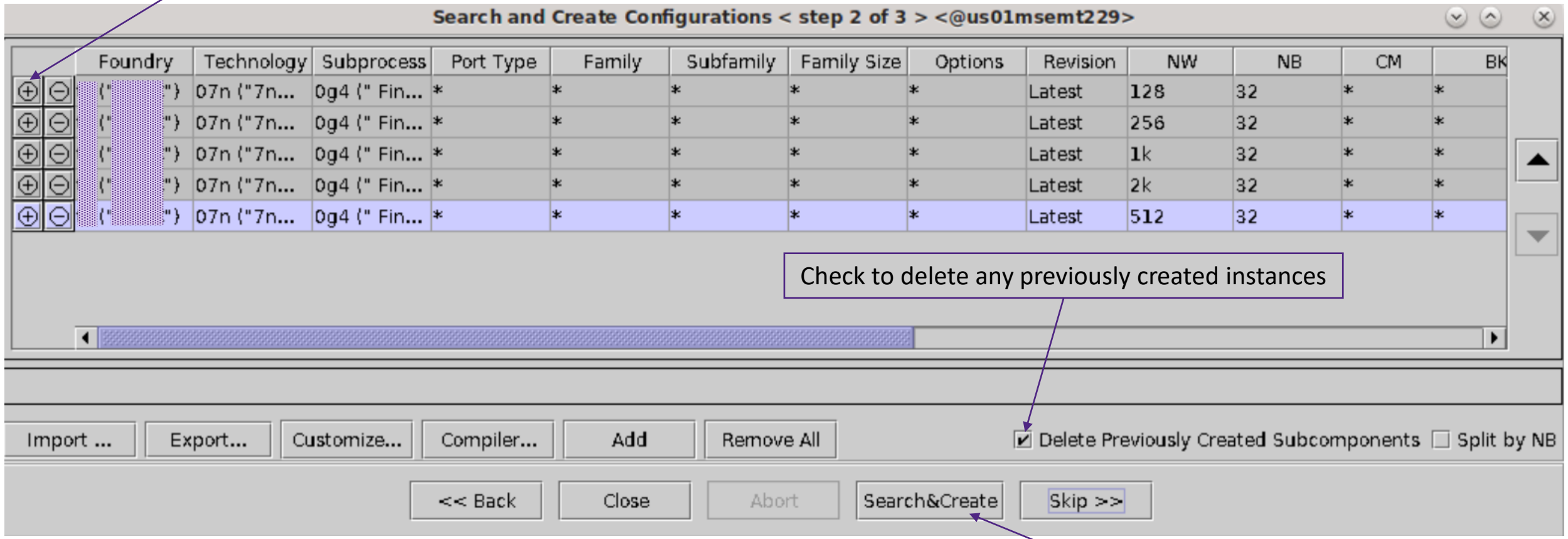
Enter Number of Words (NW) and Number of Bits (NB), CM = “*”, BK = “*”, center_decode = “*”

Can import spreadsheet; must be in .csv format

Configuration Settings

- If wild cards are used for any of Port Type, Family, Subfamily, Family Size, Options or Revision, then pvt_enable can only be “Default”
- To customize the PVT list, you must select **only one** memory compiler per row

Select “+” to duplicate and then edit to add more configurations, “-” to remove configurations

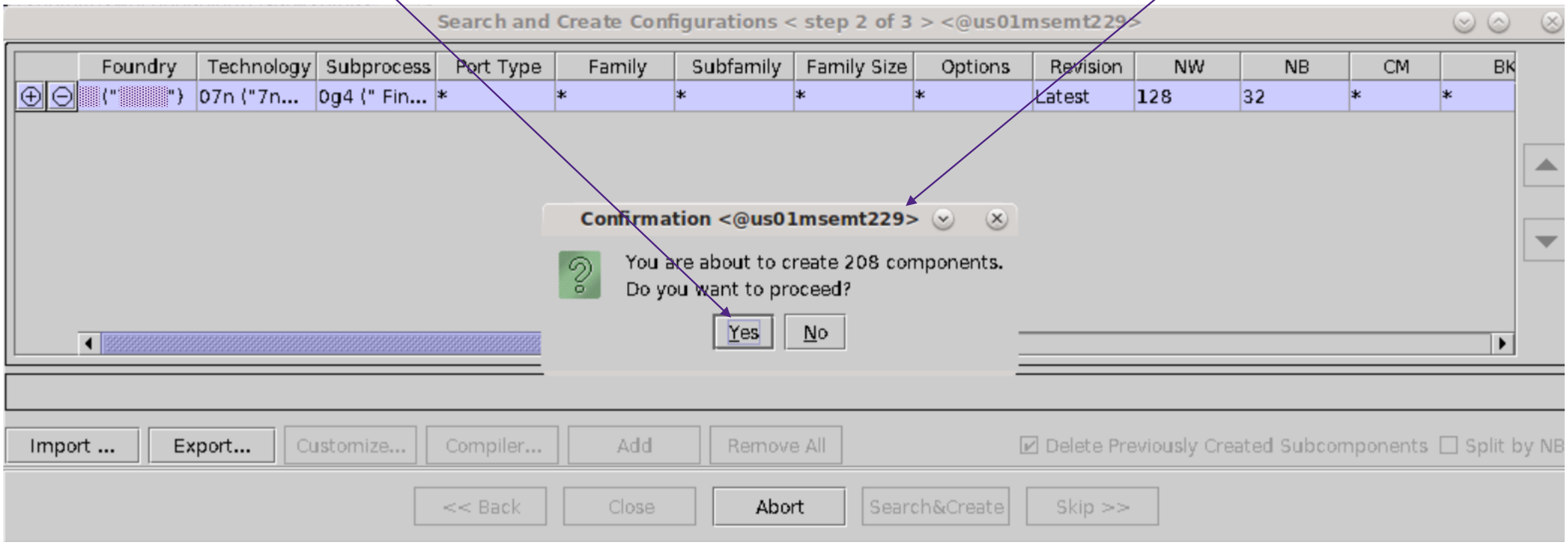


Check to delete any previously created instances

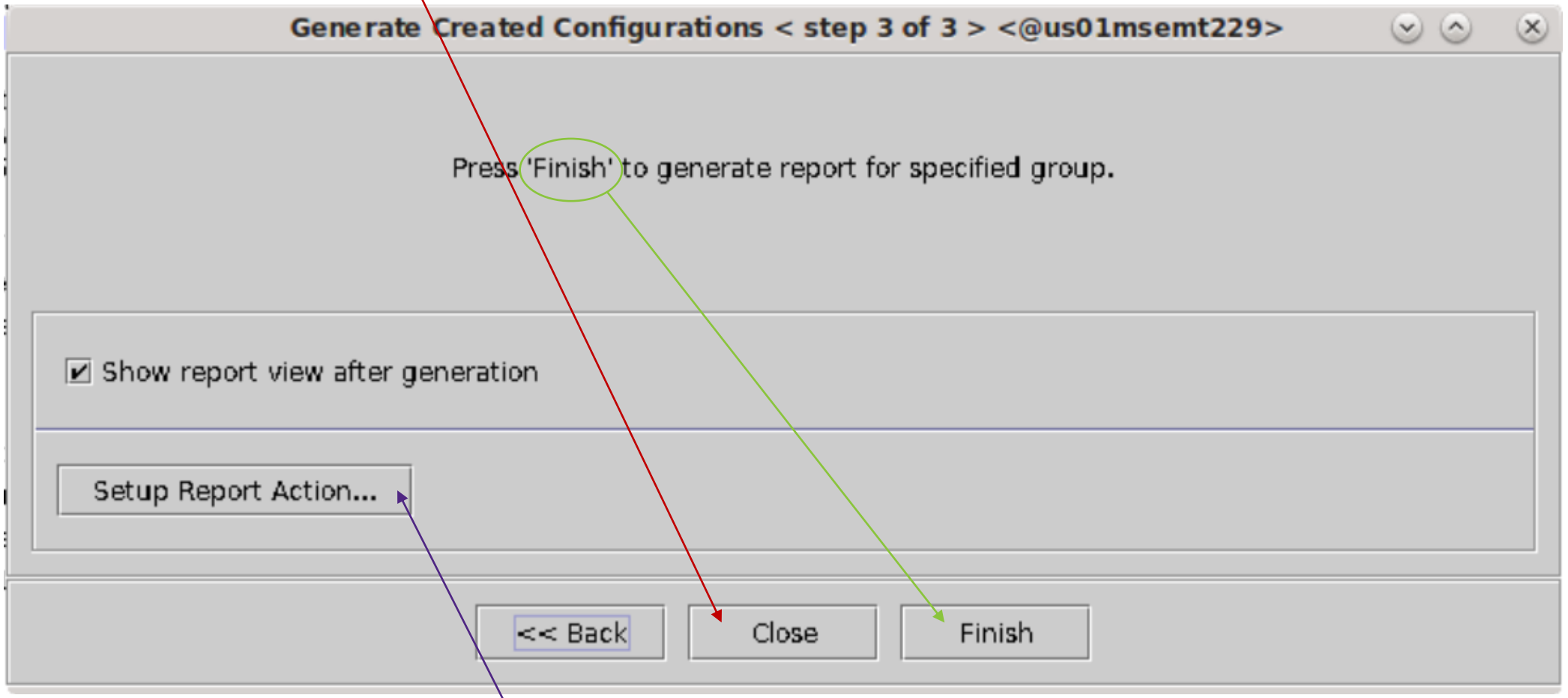
Select “Search&Create” to determine (approximately) how many instances will be created; does NOT start instance generation

Select “Yes” to create instances; does NOT generate data, just creates instance configurations

Instance count can grow quickly with wildcards. This popup will show if instance count estimate is > ~50



Press “Close” instead, if you’d like to adjust Report Settings and Job Control; instance generation can be launched later

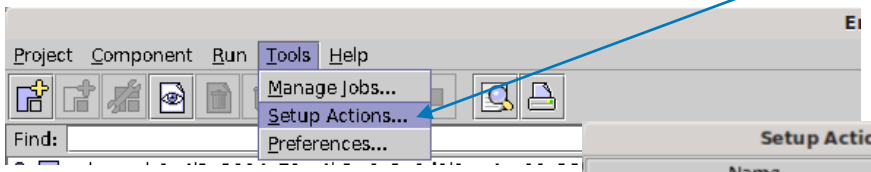


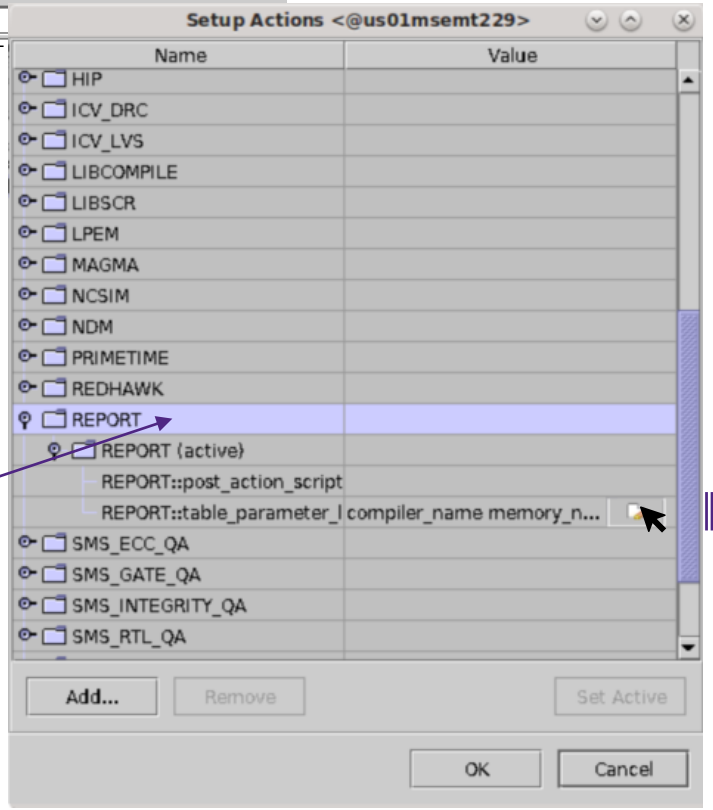
Select this to setup parameters for the Excel (. csv) report

Also available in the main Integrator window under “Tools” → “Setup Actions” → “REPORT”

Setup Report Actions…

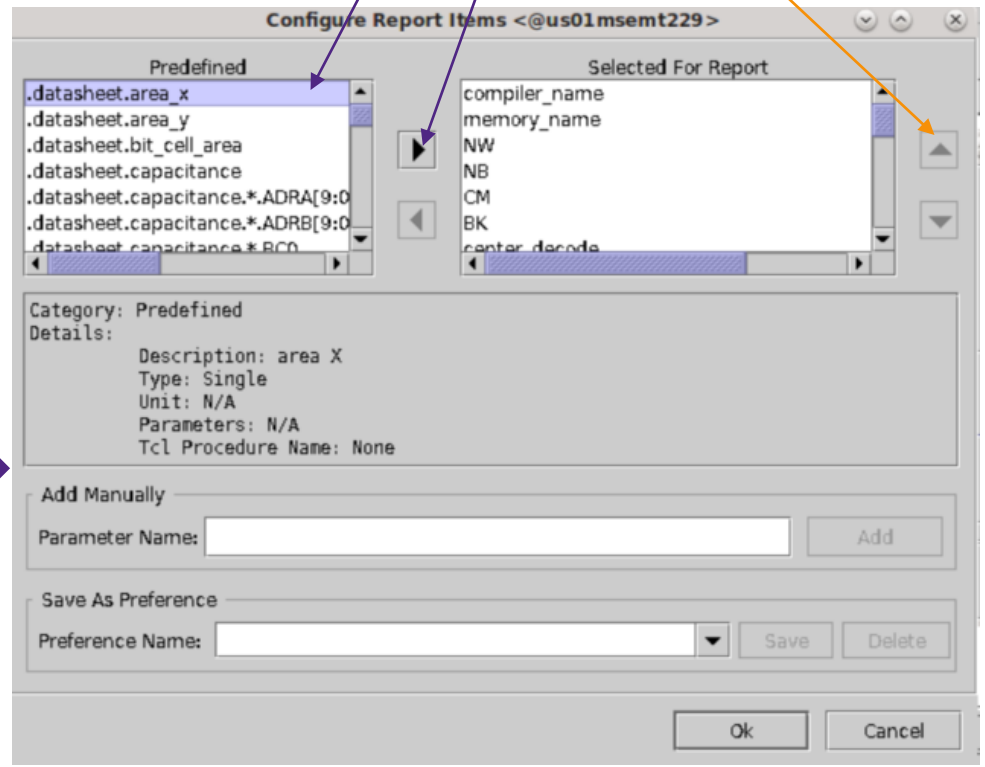
In the main Integrator window, select “Tools” → “Setup Actions” → “REPORT” to setup parameters for the Excel (`.csv`) report





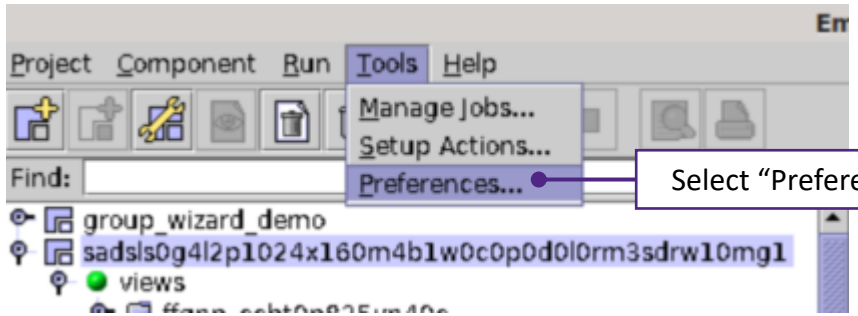
Expand to set up parameters for the Excel (`.csv`) report

Add or remove parameters for report, optionally change order that the parameters appear in the report, then select “Ok”

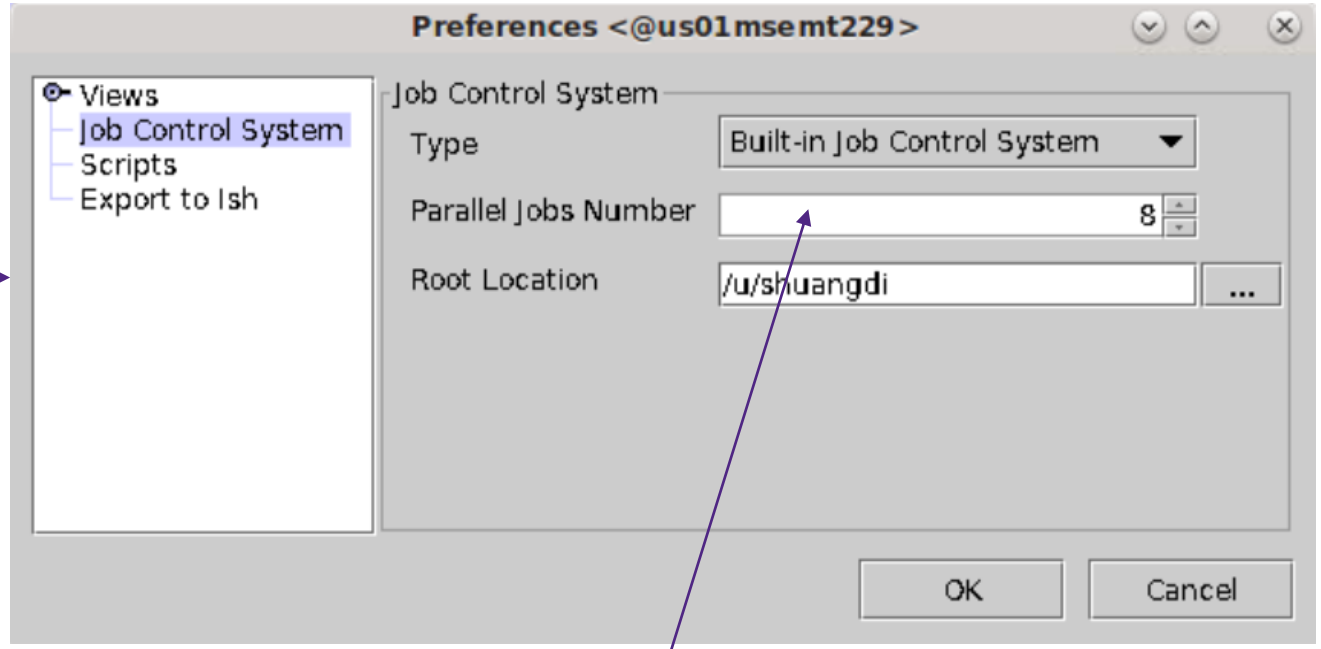


Job Control

Increasing the number of parallel jobs will generally decrease run time



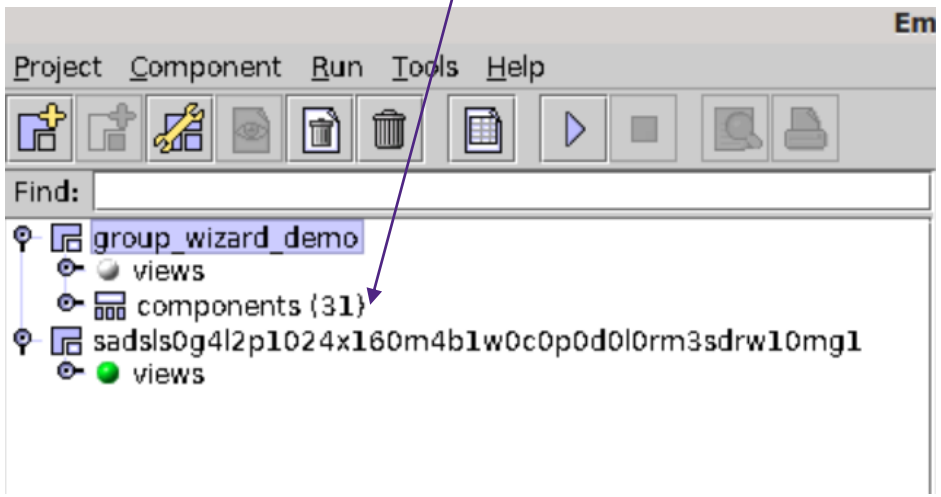
Select “Preferences…”



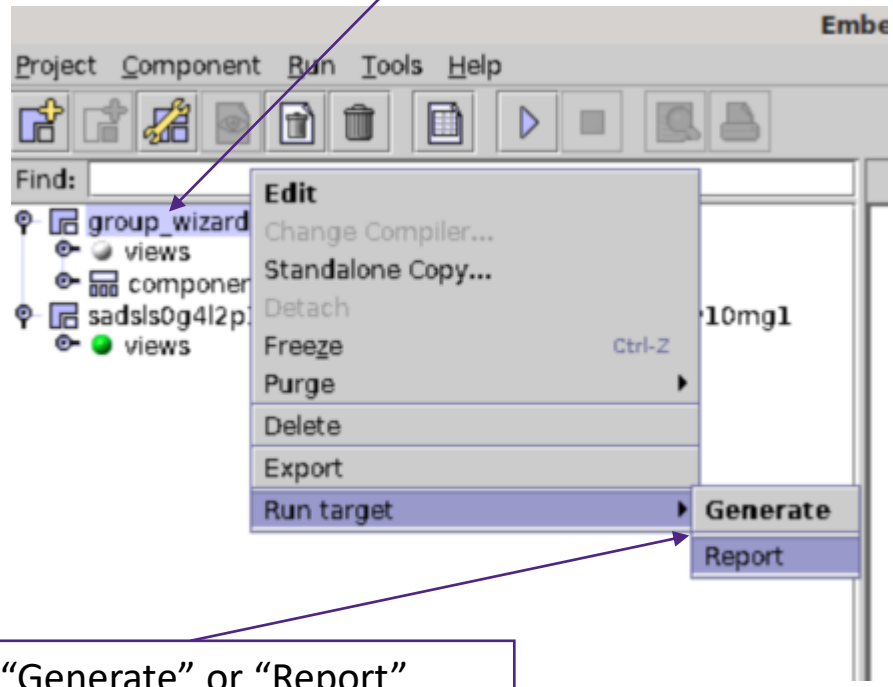
Select Job Control System and enter the number of Parallel Jobs (4 to 16 is usually a good number to start with; you can experiment to see what is optimum for your environment)
This setting will be remembered even if you close and reopen Integrator

…and finally… Generating the Report!

Component search result can be found here



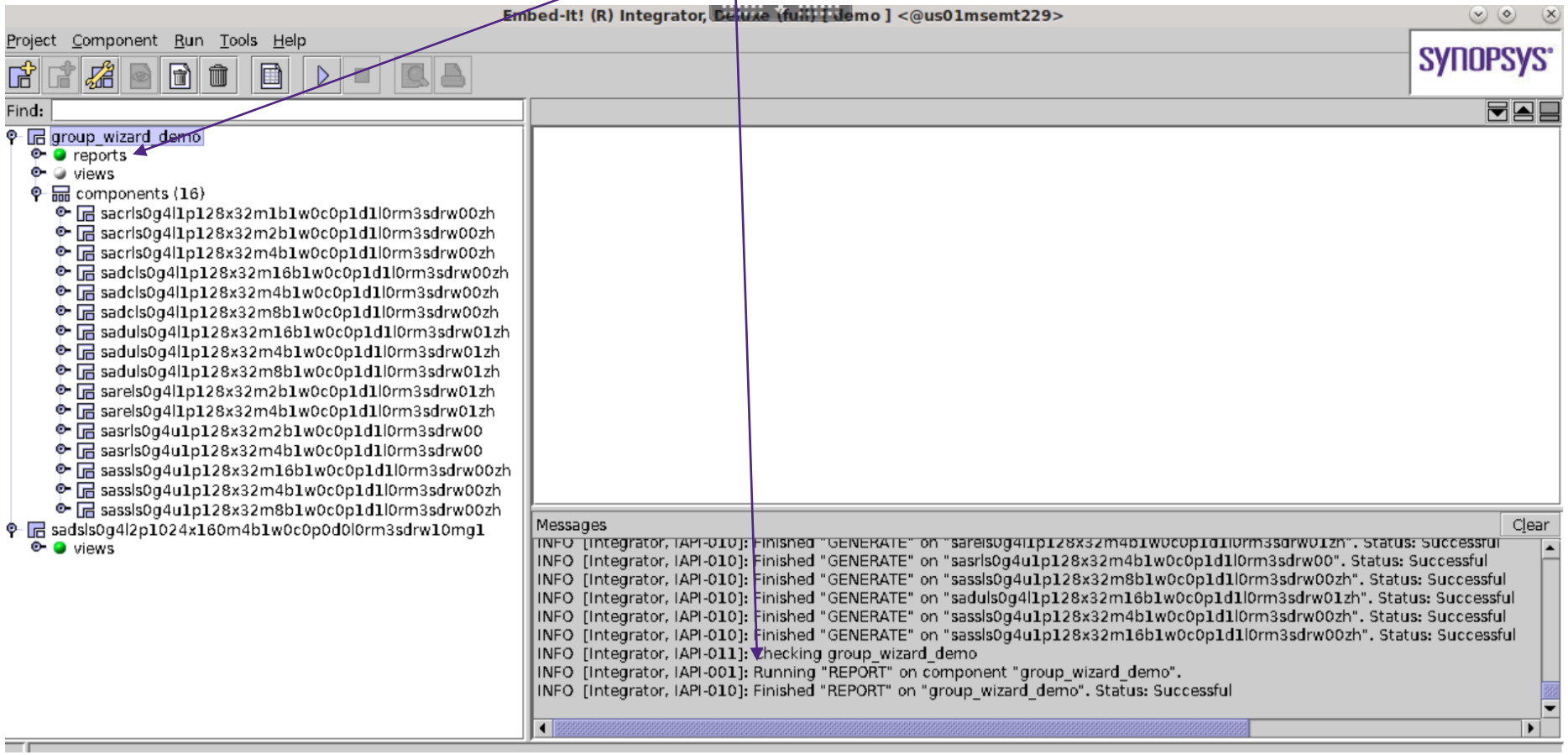
If the report has not been generated, right click on Group name



Select “Generate” or “Report”

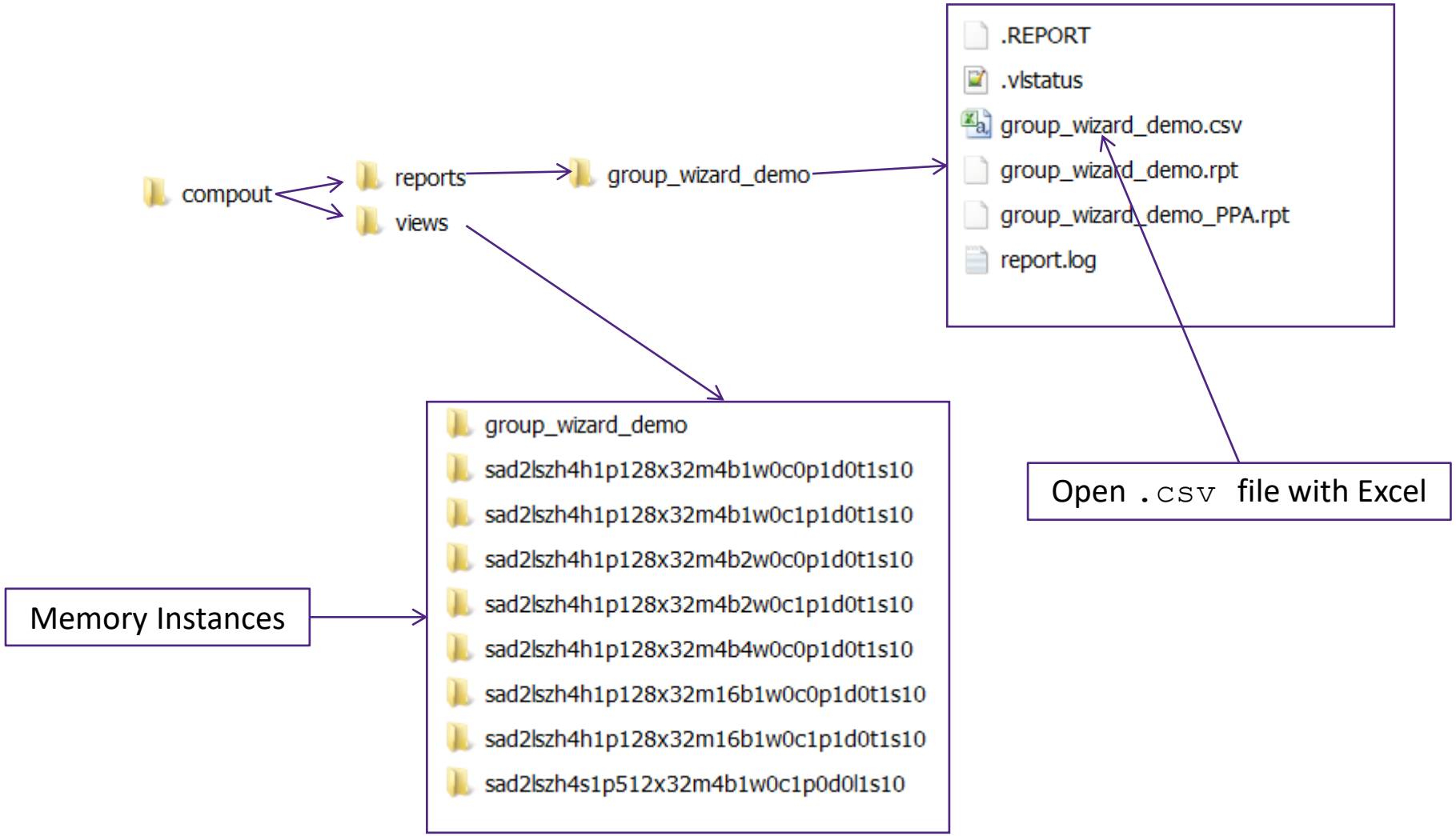
- **“Generate”** will generate/compile all un-generated instances
  Instances that are already generated will not be run again
- **“Report”** will run Generate and create the reports (`.csv` format)

Generation of group instances and report completed



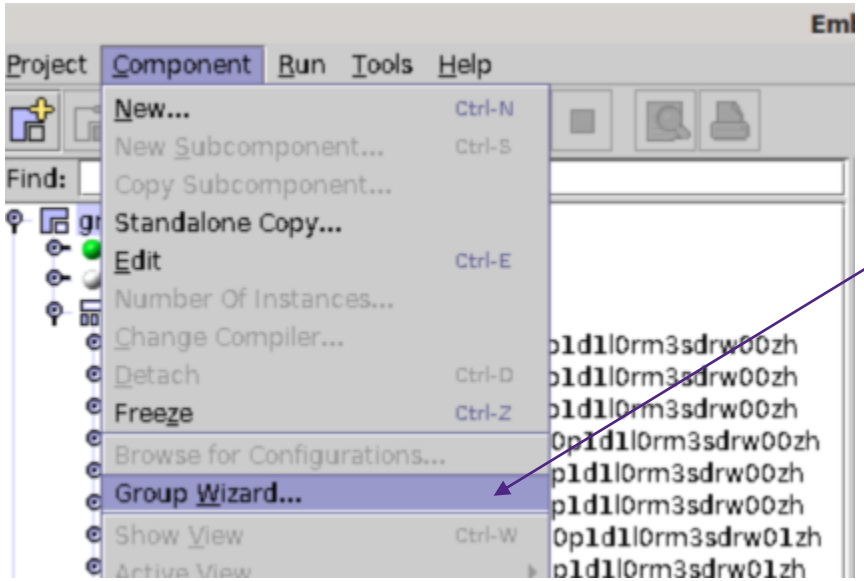
NOTE: Only 16 memory instances generated for this example

Output Directories and Files



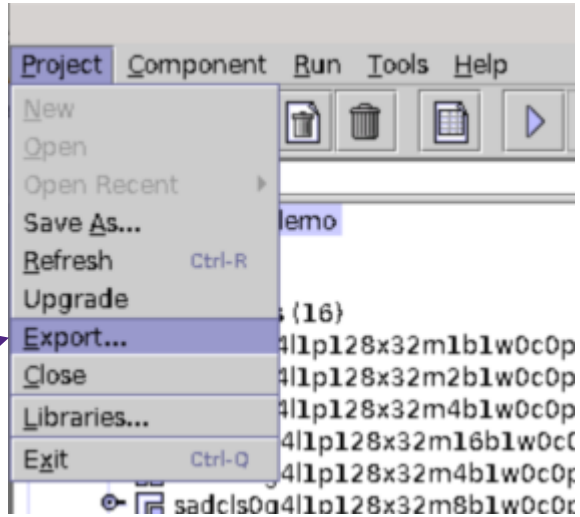
Other Features

Edit Group Wizard



To edit a group created with Group Wizard, select “Component” → “Group Wizard…”, and then select the group you want to edit

Export project



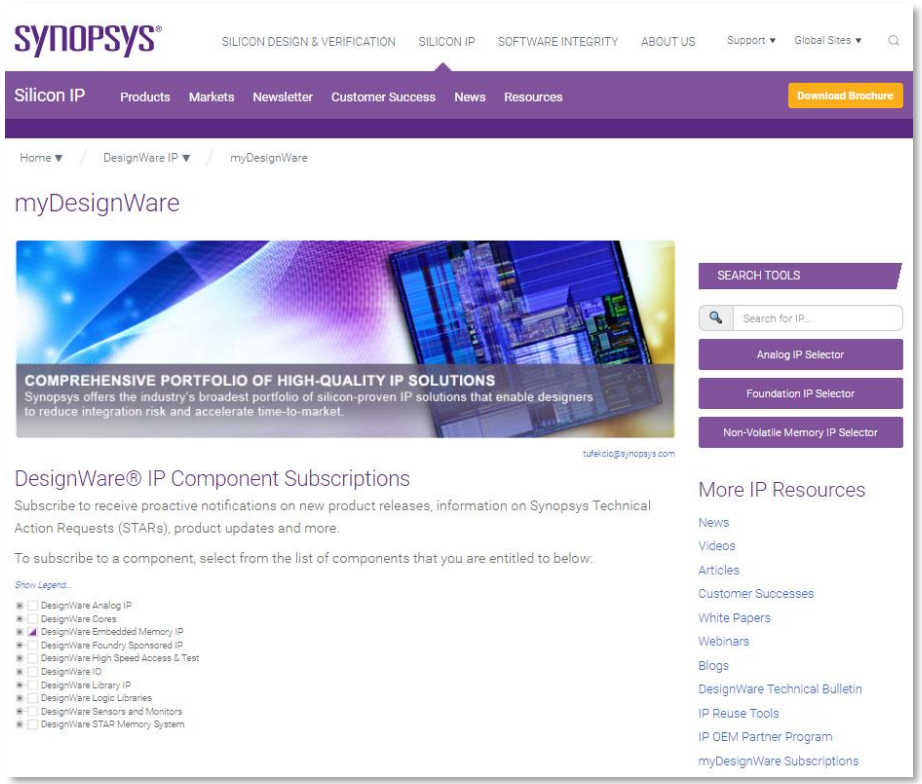
To export a project for use in batch mode, or for archiving, select “Project” → “Export..”
You can export an `.ish` file that can be run later to regenerate the project
Please see Integrator User Manual for details on `.ish` files

Congratulations!

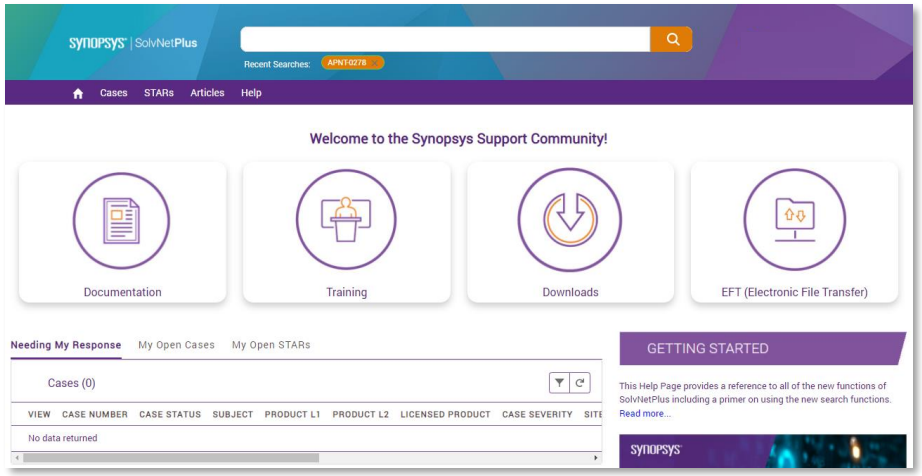
If you still have questions….

Comprehensive Online Support

myDesignWare
Subscribe for proactive release and bug fix notifications



SolvNetPlus
Synopsys Support Portal



DesignWare IP Support

For products under a valid core support agreement

SolvNetPlus

ONLINE

solvnetplus.synopsys.com

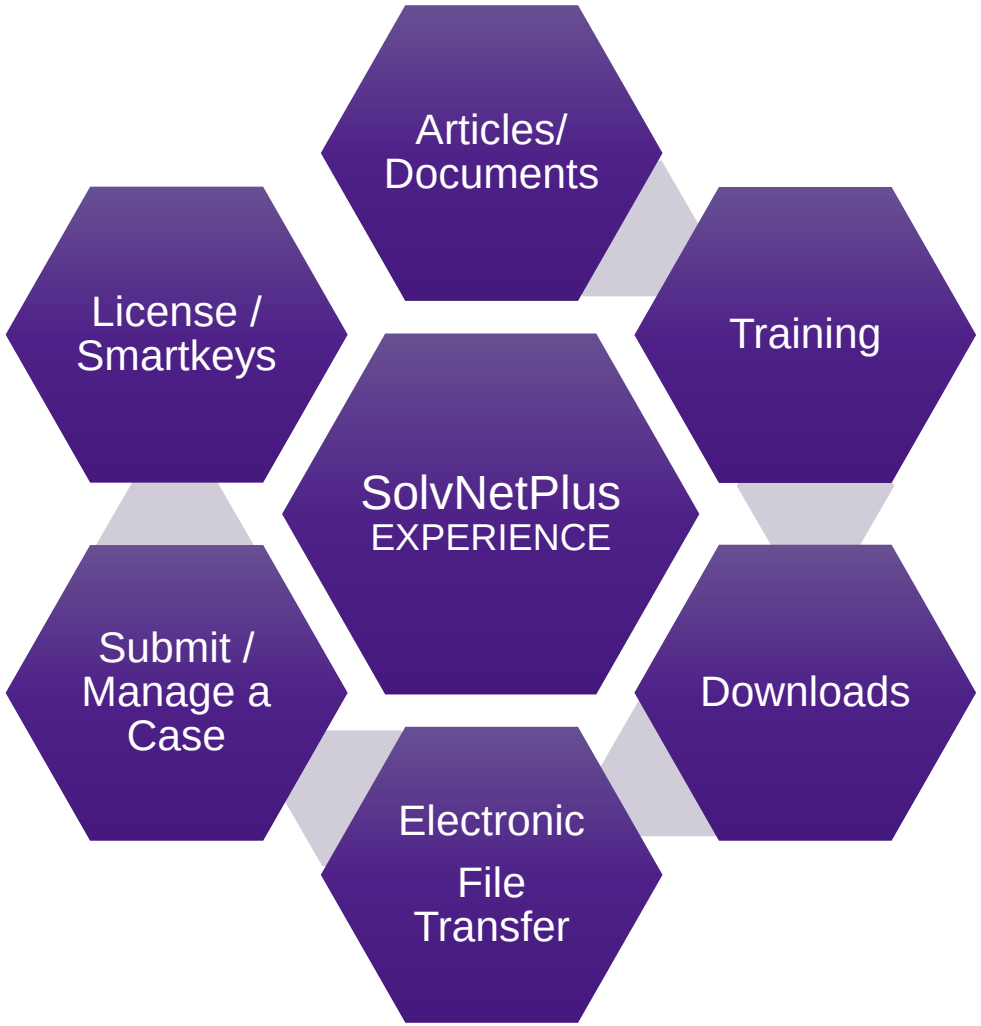
Most efficient method
Extensive Knowledgebase
Support by Worldwide Experts
Acknowledged Within 24hrs

EMAIL

support_center@synopsys.com

Opens SovNetPlus case
Less efficient routing

SolvNetPlus



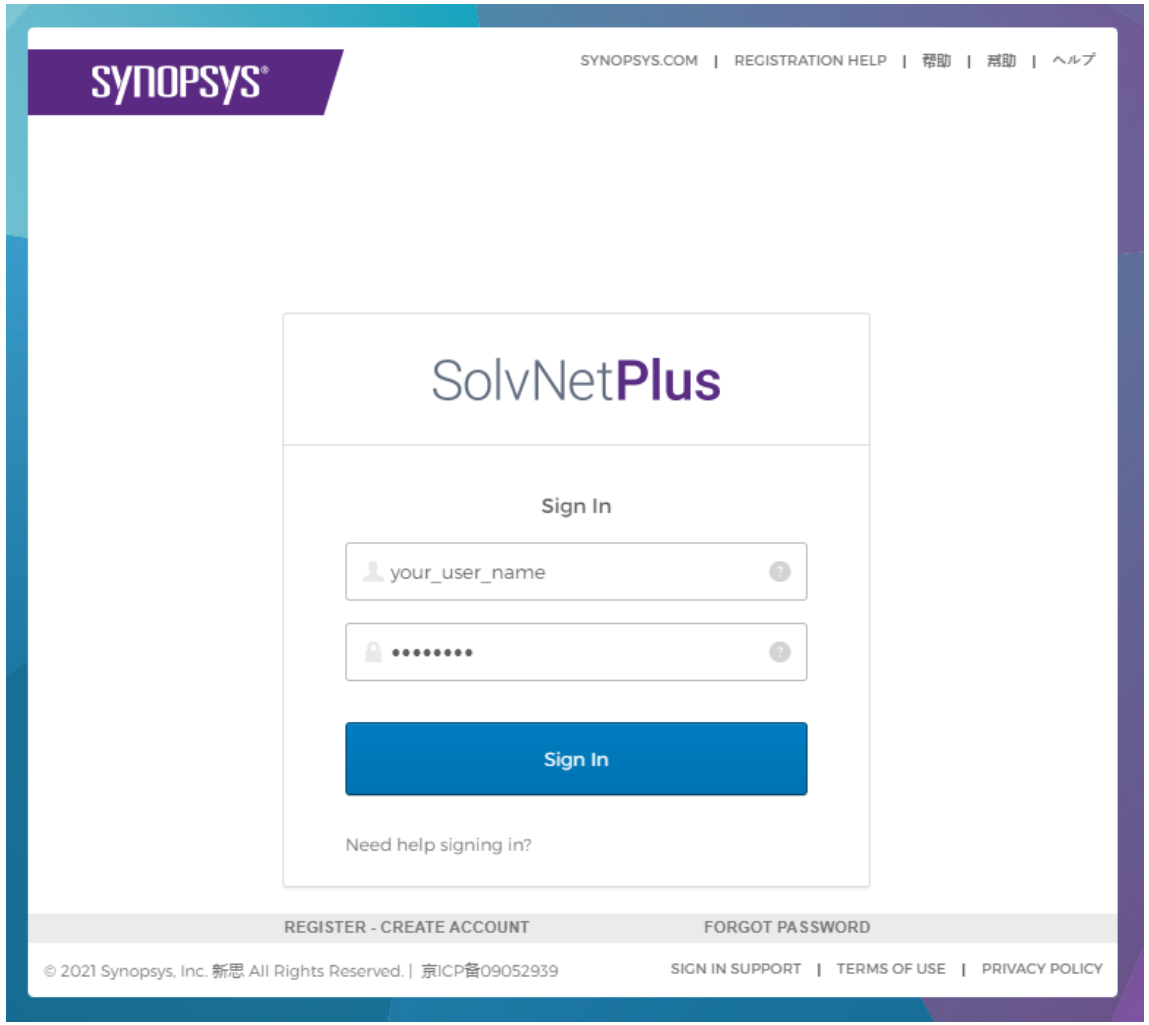
SYNOPSYS®

Integrated Customer Experience Platform

- Enhanced Search Experience
- Curated Technical Content
- Improved Case Self Service
- Intelligent Recommendations
- Secure Access

SolvNetPlus Access

Be kind and consult all available documentations before contacting support



solvnetplus.synopsys.com

No SolvNetPlus Account?

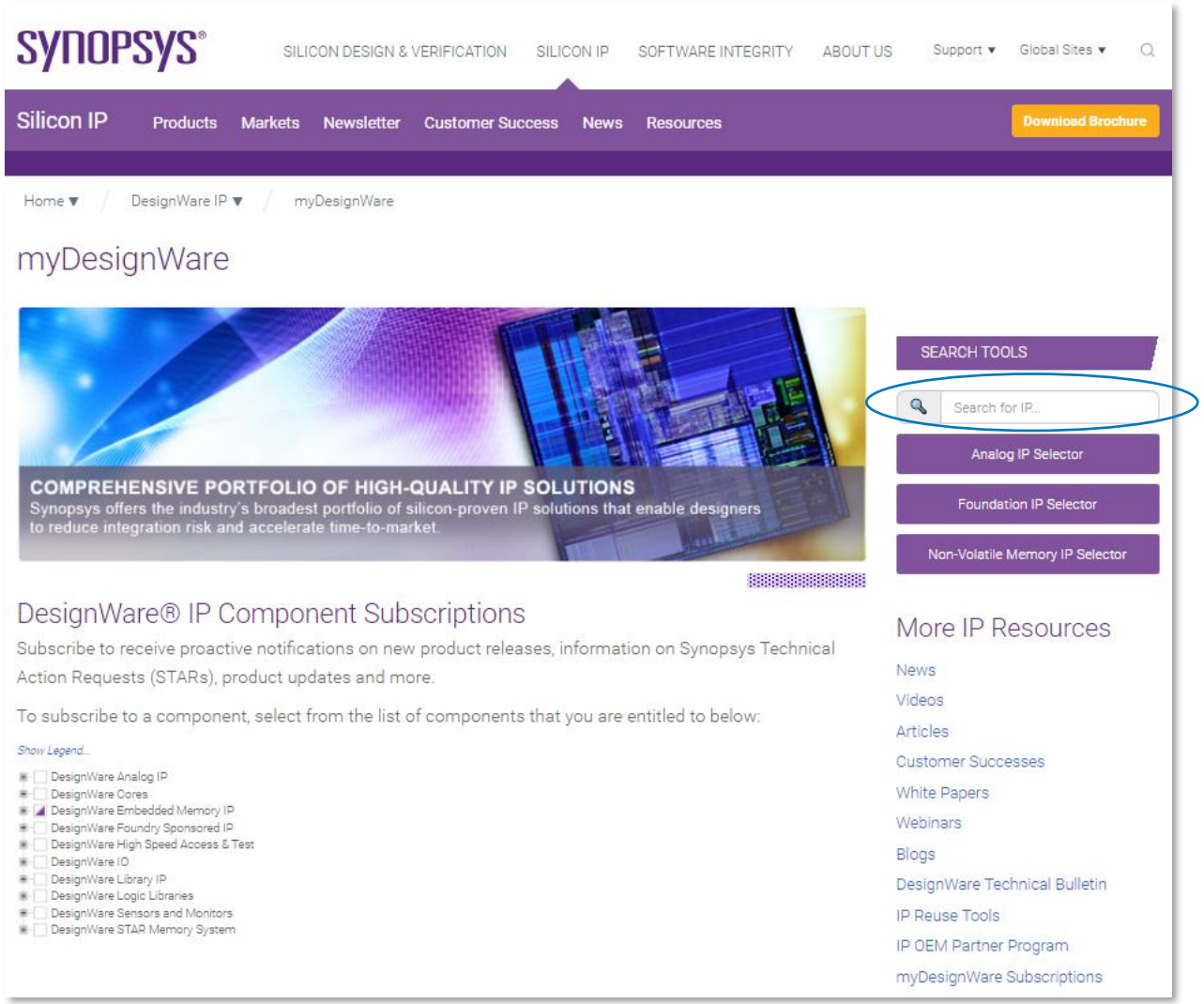
REGISTER – CREATE ACCOUNT

No Site ID?

Please contact your Synopsys account manager to have an account set-up for your company

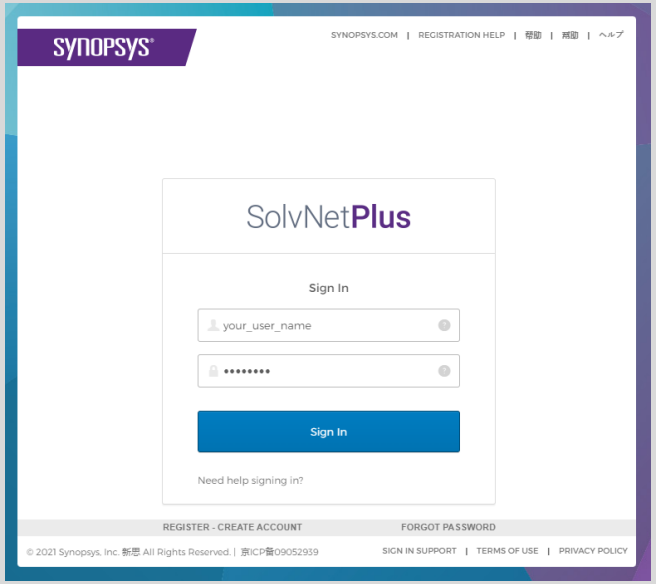
myDesignWare

Search for IP



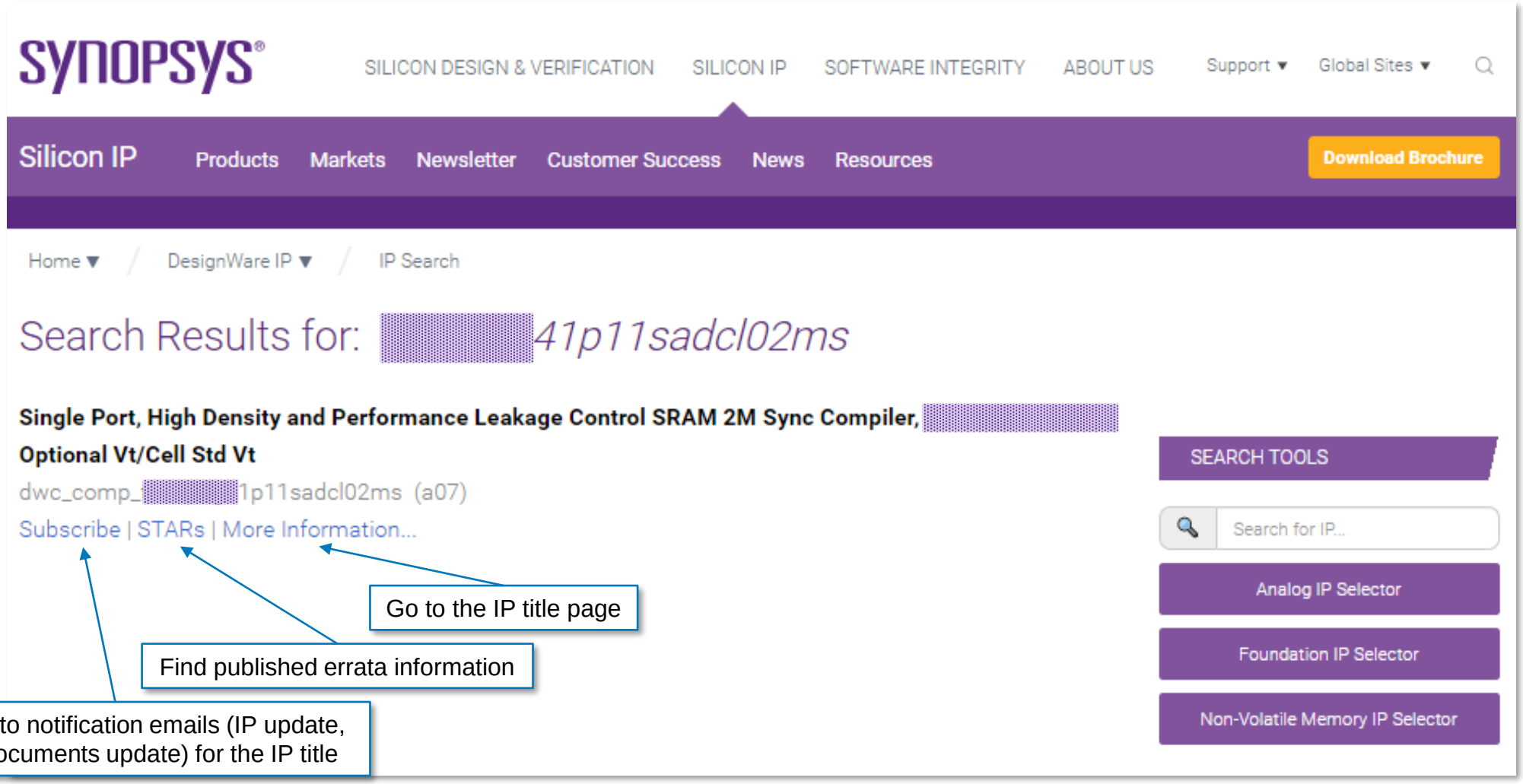
mydesignware.com

Login with your SolvNetPlus UserID and Password



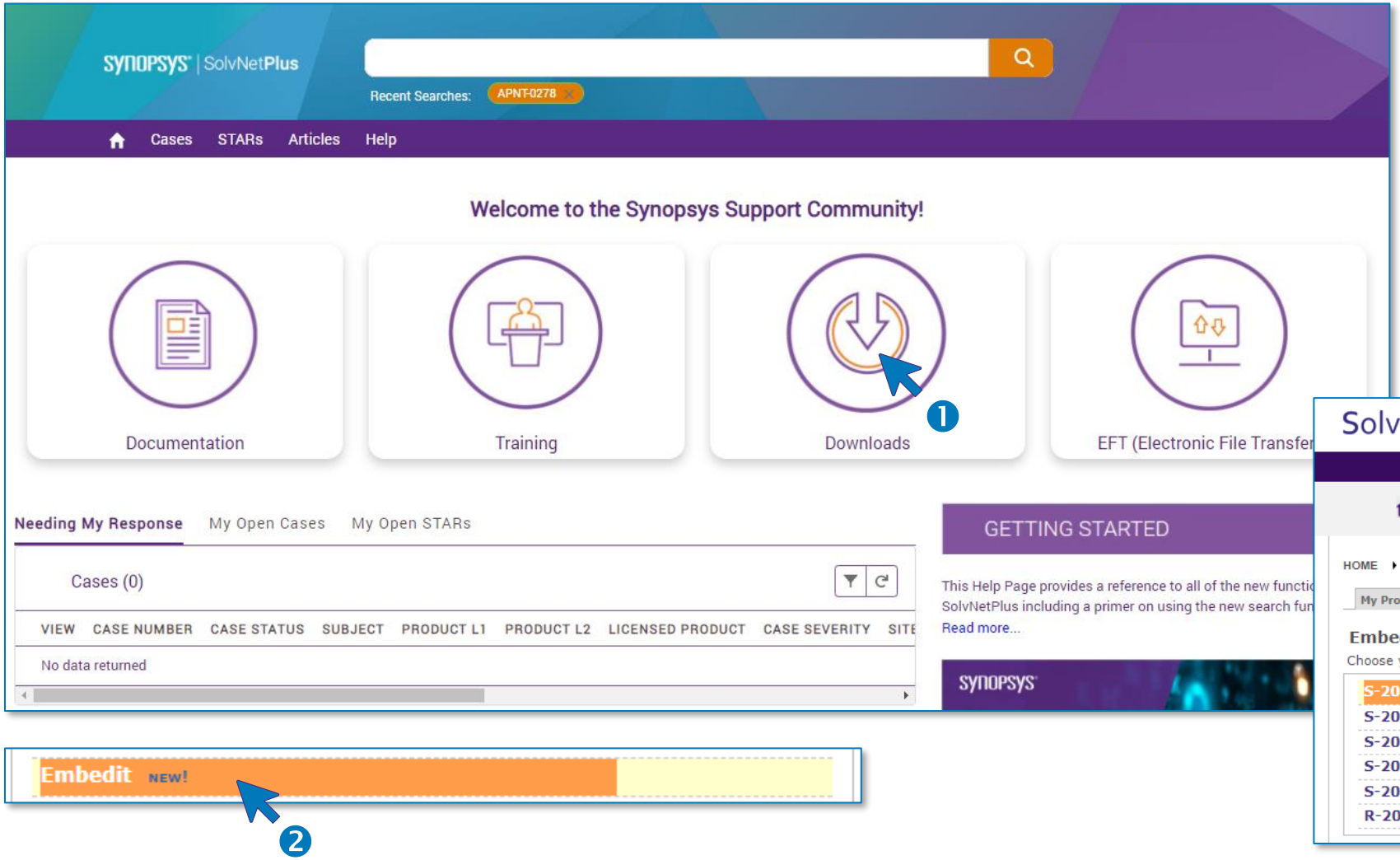
myDesignWare

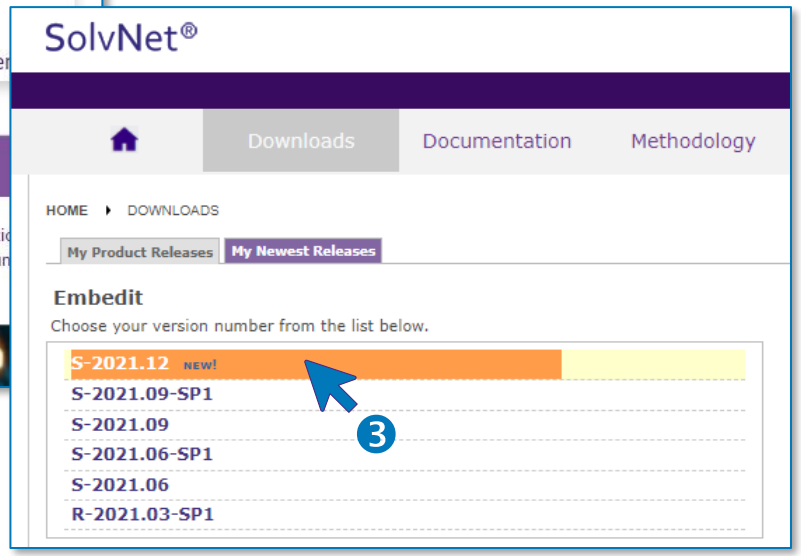
Search Results



Embed-It! Integrator

Use SolvNet**Plus**



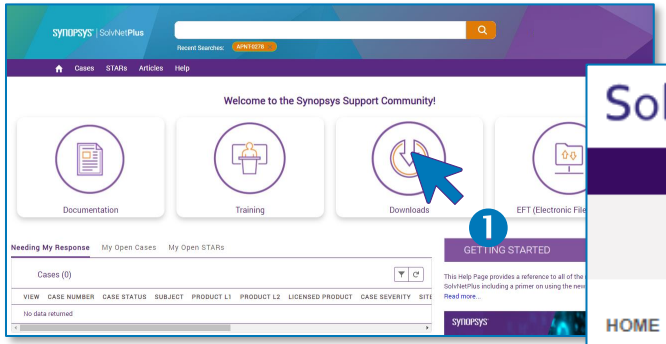


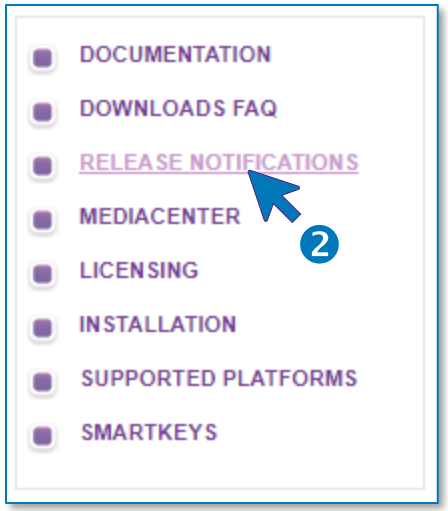
1. Select “Downloads”
2. Scroll down, find and select “Embedit”
3. Select the latest version for download

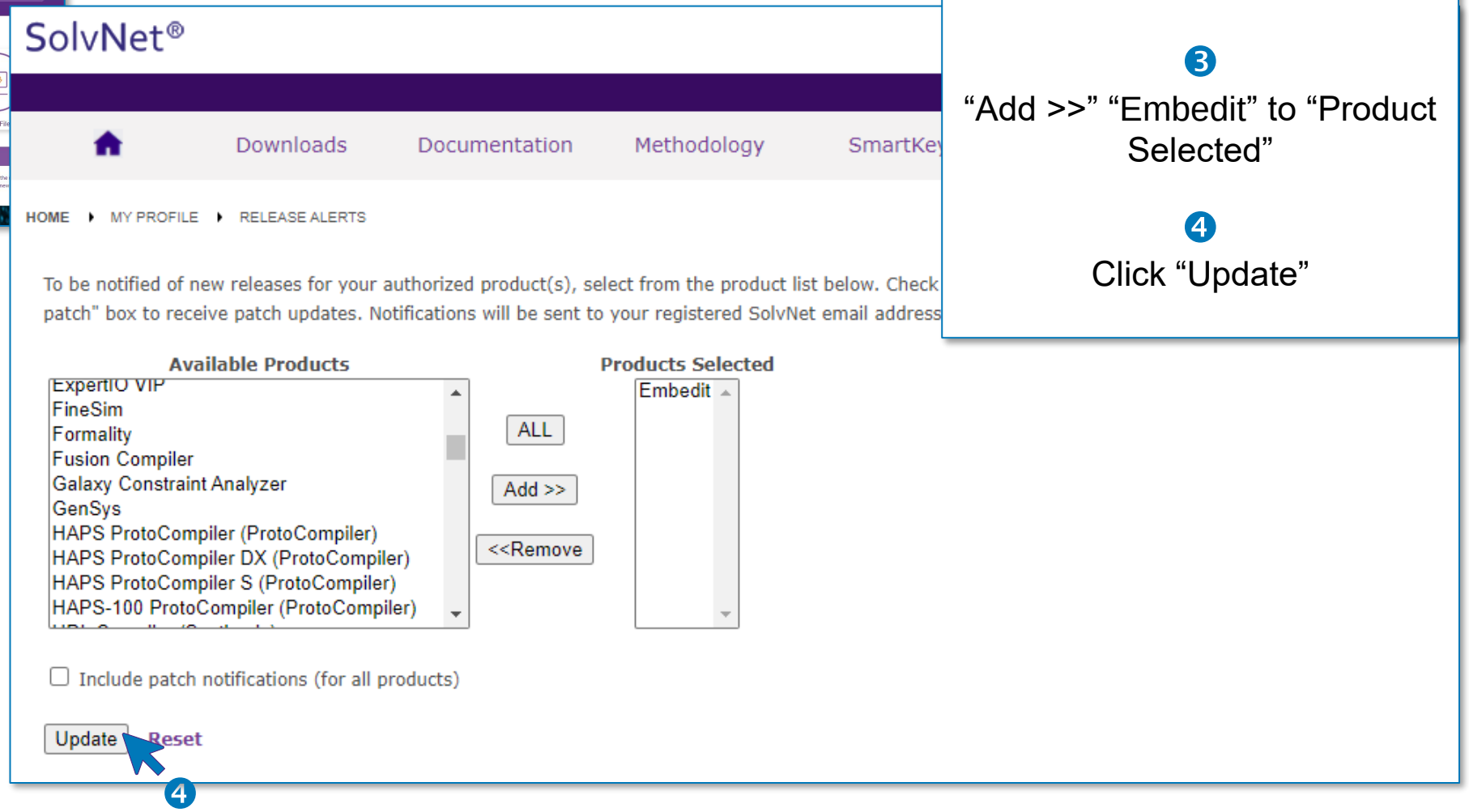
Recommendation is to update with *SP* releases as well as they contain bug fixes and enhancements

Embed-It! Integrator

Subscribing to Release Alerts







1. Select “Downloads”
2. Scroll down, find and select “Release Notifications”
3. “Add >>” “Embedit” to “Product Selected”
4. Click “Update”

SolvNetPlus Importance of Site ID and Project ID

- The Site ID is a unique number, that Synopsys uses to identify one specific customer site. A customer can have multiple Site IDs.

- For each new project, Synopsys and Customer define a unique Project ID.
  - IP licenses are cut for one specific Site ID and one specific Project ID.

- When entering a new SolvNetPlus ticket, users must enter their Site ID, a valid Project ID. and select the related Licensed product.

- The Project ID is also used during IP installation.
  - During execution of .run file, when prompted, enter the Project ID for source code installation (if no Project ID is entered, then IP is installed encrypted and/or without back-end views).

- The Project ID was communicated to you by your Synopsys account team.
  - It does not appear in “clear text” in the license file you have received.

Appendices

Appendix A: Example `viewselect` List

```
viewselect = {
        "allpvt"
        "allpvthtml"
        "allpvtjson"
        "atpg_netlist"
        "avmcfg"
        "bitmap"
        "cellmatch"
        "coord"
        "core"
        "cpf"
        "ctl"
        "custom_bitmap"
        "dssum"
        "emul_upf"
        "fast_func_verilog"
        "fastscan"
        "gds"
        "ikos"
        "lvlib"
        "masis"
        "mask"
        "oasis"
        "params"
        "plef"
        "power_verilog"
        "spf"
        "spice"
        "std_cells.fs_lib"
        "std_cells.lib"
        "std_cells.max"
        "std_cells.v"
        "stim"
        "syn"
        "tetramax"
        "tpf"
        "tr_count"
        "upf"
        "verilog"
        "verilog_bus_wrapper"
        "verilog_netlist"
        "verilog_stub"
        "verilog_vhd_stim"
        "vhd_rtl"
        }
```

Please note that not all views will be available across all the compiler families

Appendix B: Useful Settings

PWL

- Set the following parameters to output the Piece-wise Linear (PWL) in-rush current profile in the instance datasheet

```
define_peak_current_attribute_datasheet = true
define_peak_power_attribute = true
```

- PWL data is provided for Read, Write, and Power mode cycles (***NOTE:*** Some older compilers only support Read PWL current).

Worst Power

```
report_worst_power  =      TRUE          /* Boolean, If TRUE; reports the
worst case power in the datasheet, default is Typical Power  */
```

Appendix C: Batch Mode Scripts

Please file a SolvNet**Plus** support Case to request an example of a batch mode script.

Appendix D: ish Commands

To create an `.ish` file with all the user settings, use the following command:

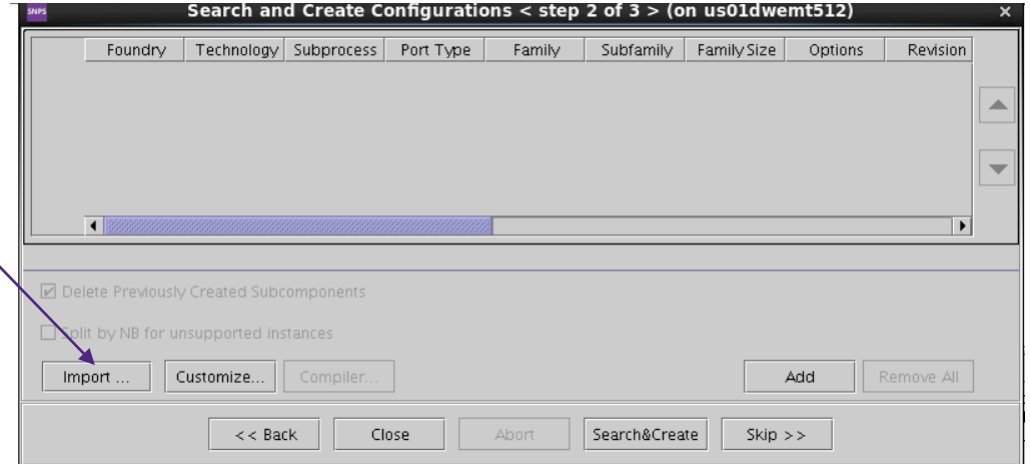
```
integrator2ish -custom <project_name> <output_ish_file_name>
```

Appendix E: Integrator Setup File

- Locate this file in your home directory
  - `.integratorrc`
- You can edit this file (make sure all Integrator projects are closed).
- To setup custom Group Wizard parameters and report formats, edit the Customize and Report sections:
  - `<Actions>`
    - `<Report>`
    - `<Parameter value="memory_name compiler_name NW NB CM BK center_decode periphery_Vt power_gating dual_rail bist_enable redundancy_enable timing_mode SW report_worst_power Memory_area Tile_ext_height Tile_ext_width Tcc Tcq Tac Read_Power Write_Power Idd_leak Idd_leak_ls Idd_leak_ds Idd_leak_sd" name="Mycustom_report_format"/>`
  - `<GroupWizard>`
    - `<Customize>`
    - `<Parameter value="center_decode bist_enable scan_enable redundancy_enable periphery_Vt pg_enable vdda_enable pvt_enable timing_mode report_worst_power output_drive SW" name="Mycustomsetup"/>`
- Other Report Parameters:
  - `.datasheet.timing_rme` (adds timing data based on RM settings)

Appendix F: Importing .csv Files into Group Wizard

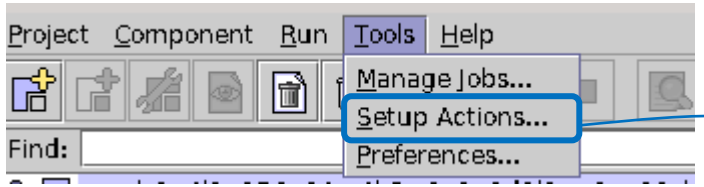
- Click the “Import” button in the Group Wizard Configuration window.
- Column headings must match memory compiler parameters.
- Wildcards can be used “*”.
- Importing additional .csv files will not erase/overwrite existing data, however, uncheck “Delete Previously Created Subcomponents” before hitting “Search&Create”, if you wish to keep existing instances.



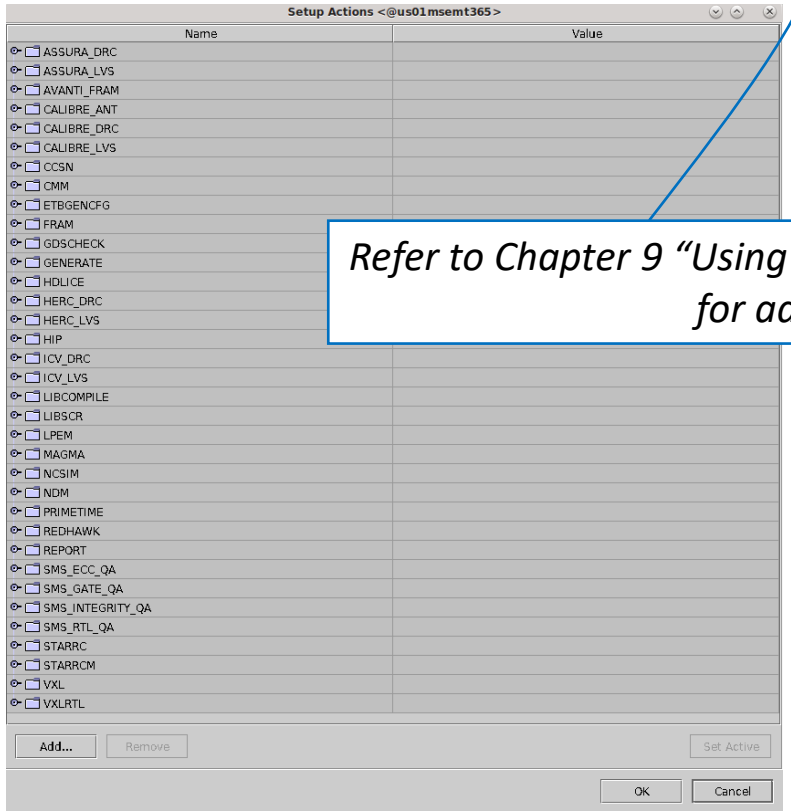
- Example

compiler_name	NW	NB	CM	BK	center_decode	SW	periphery_Vt	vdda_enable	pg_enable	bist_enable	redundancy_enable	pvt_enable
[redacted]2p11sacul256sa19	64	16	2	1	FALSE	0	STANDARD	TRUE	TRUE	FALSE	FALSE	{ 1 2 3 4 }
[redacted]2p11sacul256sa19	64	32	2	1	0	0	STANDARD	1	1	0	0	{ 1 2 3 4 }
[redacted]2p11sacul256sa19	128	60	*	*	*	0	*	TRUE	TRUE	FALSE	FALSE	{ 1 2 3 4 }
[redacted]2p11sacul256sa19	256	64	2	1	1	1	STANDARD	*	*	FALSE	FALSE	Default

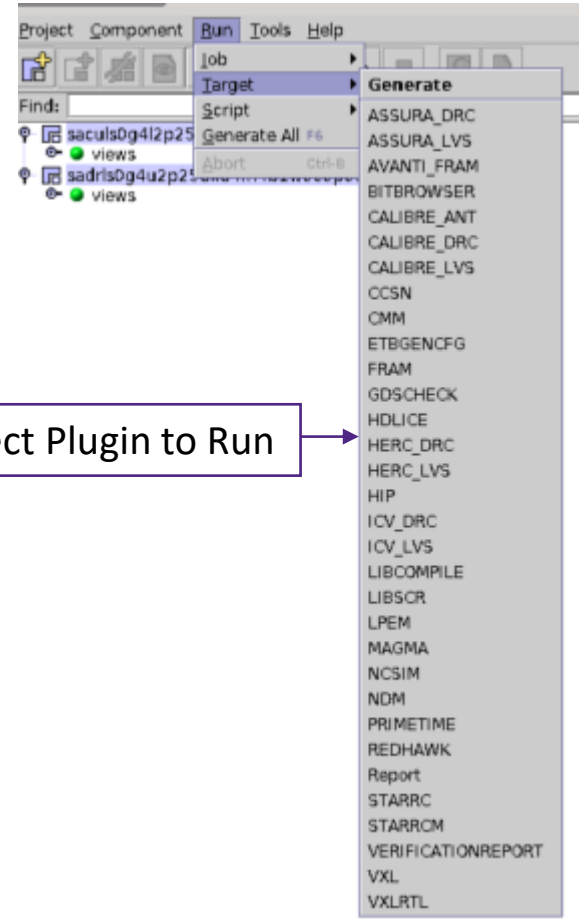
Appendix G: Using Plugins



Select “Setup Actions…” in the “Tools” menu to bring up the Setup Actions dialog to configure the target (action) methods available for generation.
See Setup Actions (Plugins) in the Integrator User Manual for detailed information.



Refer to Chapter 9 “Using Plugins” of Integrator User Manual for additional details



Select Plugin to Run

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Thank You