GF 22nm SiWare™ Read and Write Margin

APNT - 0339

GF 22nm SiWare™

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Version 1.1

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Revision History

Version	Date	Note
1.0	September 2020	Initial release
1.1	May 2021	1. Added two consumer grade compilers. 2. Removed "Table 1 Truth Table for timing mode". Please refer to each compiler release.txt on the RM setting at different voltage.

1 Introduction

This application note provides users with information regarding the Read/Write Margin (RM), Read Assist and Write Assist on the Synopsys GF 22nm SiWare™ memory compilers listed below.

- Automotive Grade 1 Memory Compilers
  - ✓ ROM (gf22nsd41p10s1dvl01ms)
  - ✓ HD SP SRAM (gf22nsd41p11s1dcl02ms)
  - ✓ UHD 2P RF (gf22nsd42p11s1cul256s)
  - ✓ HD 1P RF (gf22nsd41p11s1crl256s)
  - ✓ HD 2P RF (gf22nsd42p11s1drl128s)
  - ✓ HS 1P RF (gf22nsd41p11s1srl256s)
- Consumer-Only Grade Memory Compilers
  - ✓ UHD 1P SRAM (gf22nsd81p11sadul02ms)
  - ✓ UHD 1P RF (gf22nsd81p11sadul256s)

2 Memory Self Time Circuitry Adjustment with Compile-time Options

The memory array bitlines are pre-charged prior to a memory cell access. After accessing the memory (Read/Write cycle), a differential signal develops between the bitlines (bitline and bitline bar). This differential signal is fed to the input of the bitline sense amplifier to determine what data is stored in the bitcell. Since it takes time for the differential signal on the bitlines to develop, the greater the time delay prior to strobing the sense amplifier, the greater will be the differential signal at the input to the sense amplifier. A low sense amplifier differential signal is susceptible to noise and sense amplifier input voltage offset. Higher input differential voltage results in greater reliability of the sensed data. However, delaying the time when the sense amplifier is strobed results in a longer cycle time, reducing maximum operating speed and increasing access time (Tcq increase). Hence the tradeoff of memory speed versus yield/reliability.

A parameter in the <memory_compiler_name>_custom.glb file allows the user to tune the memory instance timing during compile. The timing_mode GLB parameter enables the selection between high yield or high performance READ/WRITE margin settings. All memories are characterized with six timing_mode settings: RM0, RM1, RM2, RM3, RM4, and RM5. Please check the SECTION VI in <compiler>/release.txt for the voltage ranges of RM settings.

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3 Read/Write Control Pins Description

There are four Read/Write RM [3:0] pins available in the Synopsys SiWare™ memory compilers. Three of the pins, RM [3:0] are used to trade-off between speed and robustness (yield). There is also a Read/Write Enable (RME) pin that selects between the internal default RM [3:0] value set during compile, and the external, user provided RM [3:0] settings. It is required that external access to all RM pins, including RME, is provided for choosing different timing modes. Registers can be used to access the RM pins for debug. If Synopsys' STAR Memory System is used, the RM pins will be automatically registered during compile.

Table 1A: Read/Write Control Pins

Signal	< >_custom.glb Setting	Description
RME	None, always enabled	Read/Write Enable pin. Selects between internal and external RM[3:0] settings. RME = 0: Internal settings; RME = 1: External settings
RM[3:0]	None, always enabled	RM[3:0] are used to change Read/Write settings.

Table 1B: Read/Write Control Pins Summary

Memory Type	PortA	PortB	Comments
UHD 2P RF, HD 1P RF, HD SP SRAM, HS 1P RF, UHD 1P SRAM, UHD 1P RF	Write/Read: RME, RM[3:0]	N/A	Write/Read use same RM values
ROM	Read: RME, RM[3:0]	N/A	Only RM values for Read
HD 2P RF	Write: RMEA, RMA[3:0]	Read: RMEB, RMB[3:0]	Write/Read use different RM values

4 Read/Write Control pins – Timing Adjustment

The Read/Write RM [3:0] settings are user adjustable. The RM interface to the user is encoded so that all compilers have the same default RM [3:0] values. The user can select from the settings shown in SECTION VI of <compiler>/release.txt based on their application requirements. The memory compiler generated RM values are listed in the output file <memory_instance_name>_params.tcl located in the “compout/views/<memory_instance_name> directory”. RME pin needs to be set to 1 for changes to RM[3:0] to have an effect.

Note: Changes to RM[3:0] settings will be reflected in the memory instance timing.

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5 RME and RM[3:0] Hold Time Reduction

Latches are added to RME and RM[3:0] to reduce hold time requirement. RM setup/hold timings will not change with Timing modes.

6 Dynamic Voltage and Frequency Scaling Considerations Using RM pins

Applications requiring Dynamic Voltage and Frequency Scaling (DVFS) that include operation at low voltages or high voltages will require changing the values of the RM[3:0] settings dynamically during operation (i.e. “on the fly”). The Read/Write Enable (RME) pin controls the override of the internal timing mode (RM[3:0]) values set during compile. When running in the application, if the voltage is lowered or

increased, then the user is required to change the RM[3:0] pin values to choose correct RM modes based on voltage. The user should ensure timing is correct with all RM[3:0] settings that will be used in the application. RME and/or RM pin setup/hold times have to be met. Setup/hold violations on RME and/or RM pins are not supported by compiler design.

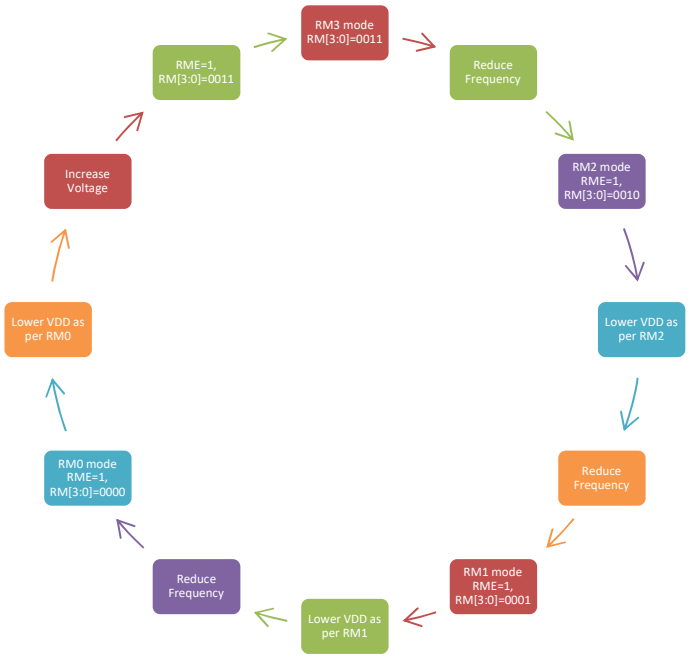

Figure 1 - DVFS

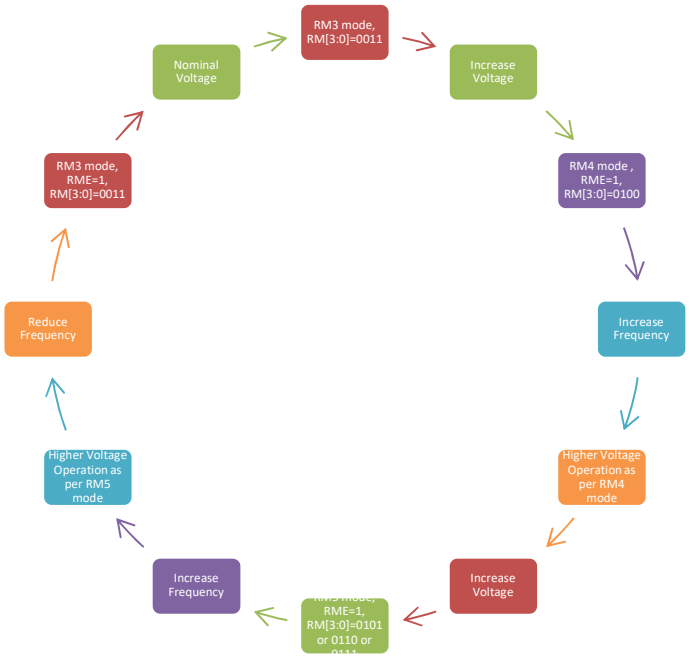

Figure 2 - DVFS with High Voltage Operation

7 Dual Rail Operation

When implementing Dual Rail to separately control the memory array voltage and the periphery voltage, it is necessary to set vdda_enable=TRUE. If the product also requires low voltage then refer to different RM settings operation.

8 Simulation Considerations

Use set_case_analysis to ensure that simulation tools utilize the correct timing data for the timing mode (RM setting) being used.

e.g.

set_case_analysis 0 dig_rdd_delay_sram/LS

set_case_analysis 0 dig_rdd_delay_sram/TCLKEB

set_case_analysis 1 dig_rdd_delay_sram/RMEB

set_case_analysis 1 dig_rdd_delay_sram/RMB[0]

set_case_analysis 0 dig_rdd_delay_sram/RMB[1]

set_case_analysis 0 dig_rdd_delay_sram/RMB[2]

set_case_analysis 0 dig_rdd_delay_sram/RMB[3]

9 RM[3:0] and RME pins when STAR MEMORY SYSTEM is used

- To provide direct access to the RM[3:0] and RME pins through the STAR Memory System wrapper, for each SMS processor used, set the following parameter in the Integrator GUI (SMS processor > Edit > Advanced > External RM), or project ish file:
  - GUI parameter: true
  - ish file syntax: component $c set_parameter ext_rm_enable 1
- To control RM[3:0] and RME for scan ATPG by SMS, refer to the dft_ops_file option in chapters “Wrapper Compiler Options for SRAM” and “Setting DFT operation” of SMS Wrapper Compiler User Manual.
- If low voltage issues are observed during scan ATPG test, please set RM[3:0] to 0000(timing_mode=RM0) or RM[3:0] to 0001(timing_mode=RM1) or RM[3:0]=0010 to (timing_mode=RM2).

10 Self Time Bypass Mode

The Self Time bypass mode is controlled by toggling the TEST1 pin. In this mode (TEST1=1), the memory self time circuitry is bypassed. The memory timing is controlled by the external clock signal (CLK). The Self Time bypass mode is initiated after the rising edge of CLK and is terminated by the falling edge. The Self Time bypass mode may be used to determine the margin of the internal self-timed circuitry.

For UHD 2P RF compilers, TEST1 functionality is as following:

- When MEB=0 and MEA=1, there is a dummy Read before Write cycle. The read self-time is not disabled, Write starts after Read and stops at the falling edge of the CLK.
- When MEB=1 and MEA=0, Read self-time is disabled. Read pulse is controlled by external CLK rising and falling edge. No Write cycle will happen.

- MEB=MEA=1 is not a valid state for TEST1 mode.

In addition to TEST1 pin, UHD 2P RF has TESTRWM mode for Read Write margin control. TESTRWM mode works as follows:

- Read cycle will start at the rising edge of the CLK and finish self timed.
- Write cycle will start at the falling of the CLK and finish self timed.
- If TEST1 and TESTRWM are set to 1, it is the same as TEST1 mode. This is not a recommended setting.

11 Read Assist

Read Assist is a compiler option enabled with the switch read_assist.. When this swtich is set to TRUE (read_assist=TRUE), Read Assist pins RA[1:0] will be visible. RA[1:0] is used to modulate the level of the word line to control WL under-drive.

Table 2 RA setting effect on WL

RA [1:0] setting	WL under drive percent
00	0%
01	5%
10	7.5%
11	10%

Refer SECTION VI in release.txt for RA pin settings based on different timing modes.

12 Write Assist

WA[1:0] and WPULSE[2:0] are visible as default. Write Assist is always required to be enabled.

WA[1:0] is used to modulate the level of coupling for the negative bitline by tuning the coupling cap to generate VnegBL (negative bitline voltage). WA[1:0] = 01 is the smallest coupling and 11 is the highest coupling.

WPULSE[2:0] is used to modulate the internal pulse width of Write window.

WPULSE[2:0] = X00 is the smallest pulse width setting and WPULSE[2:0] =X11 is the largest pulse width setting.

WPULSE[2] is not currently used in the design.

Refer SECTION VI in release.txt for settings of WA and WPULSE pins based on timing modes.

13 Voltage Operating Range with RM/RA/WA settings

Refer SECTION VI in release.txt present inside the compiler directory for the settings of RA/WA/WPULSE based on different timing modes. For Dual Rail memories:

- VDDA-VDDP <= 270mV for all timing modes
- VDDP-VDDA <= 100mV for all timing modes

14 ROM

There is no Read Assist, Write Assist, WPULSE, and Dual Rail. The RM and RME pins are present and operating voltages are mentioned in on page 5.

15 Automotive Grade

The voltage supply maximum for Automotive Grade 1 is +5% above Vnom for the core (thin oxide transistor) and should not exceed Vmax of 0.84v. Therefore, it is recommended to use only the PVT corners licensed (need em_gf22_ag1 license) for AG1 for automotive application, that are in the nominal voltage range.

If you have further questions, please contact Synopsys Customer Support by logging in to SolvNetPlus:

https://solvnetplus.synopsys.com