GF 22nm Memory Compilers

TEST_RNM, TESTRWM, and TEST1 modes

APNT-0358

May 2021
Version 1.0

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Revision History

Version	Date	Note
1.0	May 2021	First release

1 Introduction

This application note describes the three test modes (TEST1, TESTRWM, TEST_RNM) of the following Synopsys SiWare™ Memory Compilers on GF 22nm.

- Automotive Grade 1 Memory Compilers
  - ✓ ROM (gf22nsd41p10s1dvl01ms)
  - ✓ HD SP SRAM (gf22nsd41p11s1dcl02ms)
  - ✓ UHD 2P RF (gf22nsd42p11s1cul256s)
  - ✓ HD 1P RF (gf22nsd41p11s1crl256s)
  - ✓ HD 2P RF (gf22nsd42p11s1drl128s)
  - ✓ HS 1P RF (gf22nsd41p11s1srl256s)
- Consumer-Only Grade Memory Compilers
  - ✓ UHD 1P SRAM (gf22nsd81p11sadul02ms)
  - ✓ UHD 1P RF (gf22nsd81p11sadul256s)

TEST_RNM is a test pin, and it is enabled by setting test_rnm_enable=TRUE. The expectation of this mode is to stress bit cells but not corrupt data. TEST_RNM can be used for screening weak bit cells.

When it is enabled, it puts the memory bitcell in stress mode for the address applied by turning ON the word line and at same time keeping the bitlines pre-charged. Read and Write operations are disabled in this mode.

RM settings are taken into account during TEST_RNM. The RM setting will change the word line pulse width and so in case of slow RM setting, the stress on the bit cell will last longer.

***Note: TEST_RNM is not supported in ROM memory compiler.**

TESTRWM can be used to extend the read to write operation delay to debug any read to write operation margins. Read cycle starts with positive edge of clock and terminates self timed. Write starts on the negative edge of clock and terminates self timed. Please refer to diagram TESTRWM operation. TESTRWM pin is enable by test_rwm_enable=TRUE.

***Note: TESTRWM is only supported in UHD2PRF memory compiler.**

In TEST1 mode, the self-timed circuit is bypassed so that the external clock can control the Read and Write control signals. TEST1 mode is available on all Synopsys memories. TEST1 pin comes by default as an input pin.
The memory enters TEST1 mode when a High is applied to the input pin, TEST1. In TEST1 mode, the signal on the CLK input will override the internal “self-timed” clock. The internal cycle is activated on the rising edge and terminated on the falling edge of the CLK signal.

The timing diagram is shown in Figure 4. The external clock, CLK, controls activities like asserting and negating wordlinesas well as firing of sense-amps and output latches.

TEST1 Mode Usage: Whenever the TEST1 pin is asserted, the internal self-timed circuit is disabled allowing the user to debug the self-timed circuitry.

2 TEST_RNM, TESTRWM, and Related Parameters and Pins

- read_assist=FALSE (default setting) and write_assist=FALSE (not default setting)
  - read_assist=FALSE is required, so that the test is done without Read sasist. read_assist ON may not detect a weak bit as it will improve the bitcell SNM (Static Noise Margin).
  - write_assist can be FALSE or TRUE since it is disabled by TEST_RNM mode.
- DFTMASK needs to set to 0
  - If DFTMASK is set to 1, TEST_RNM model will not work properly because the word lines are turned off.
- LS, DS, and SD need to be set to 0
  - Both TEST_RNM, TESTRWM modes do not work in LS, DS, and SD modes.

3 Model Support

- TEST_RNM, TESTRWM, and TEST1 functionality is not supported for ATPG netlist.
- Setup and hold requirements are in timing model.
- Data is retained in the Verilog model.

4 Test TEST_RNM with SMS

TEST_RNM is not an at speed memory pin, hence the following test sequence can be applied with SMS. Assign TEST_RNM to SMS SMPR/PMPR register which will allow to control it through Jtag through SMPR_SEL/PMPR_SEL instruction.

- With disabled TEST_RNM write data background into the memory, using SMS algorithm programmability, run (W(D); R(D)).
- Next, enable TEST_RNM and run (RI) where RI is Read Ignore operation available in SMS.
- Next, turn off TEST_RNM and run R(D); if fail then RNM issue has been found.
- Do the same for ~D since marginal bits have dependency on the written data.

Note: HD2PRF compiler (gf22nsd42p11s1drl128s) uses single-end bitcell, which needs to use write operation to activate the WL when enable TEST_RNMA. The following test sequence can be applied with SMS.

- With disabled TEST_RNMA write data background into the memory, using SMS algorithm programmability, run (W(D); R(D)).
- Next, enable TEST_RNMA and run W(D) operation in SMS.
- Next, turn off TEST_RNMA and run R(D), if fail then RNM issue has been found.
- Do the same for ~D since marginal bits have dependency on the written data.

To simplify the test pattern applied in chip level, it is okay to use Write operation (instead of RI) for all type of memories.

5 Timing diagram

Figure 1: READ Operation (TEST_RNM)

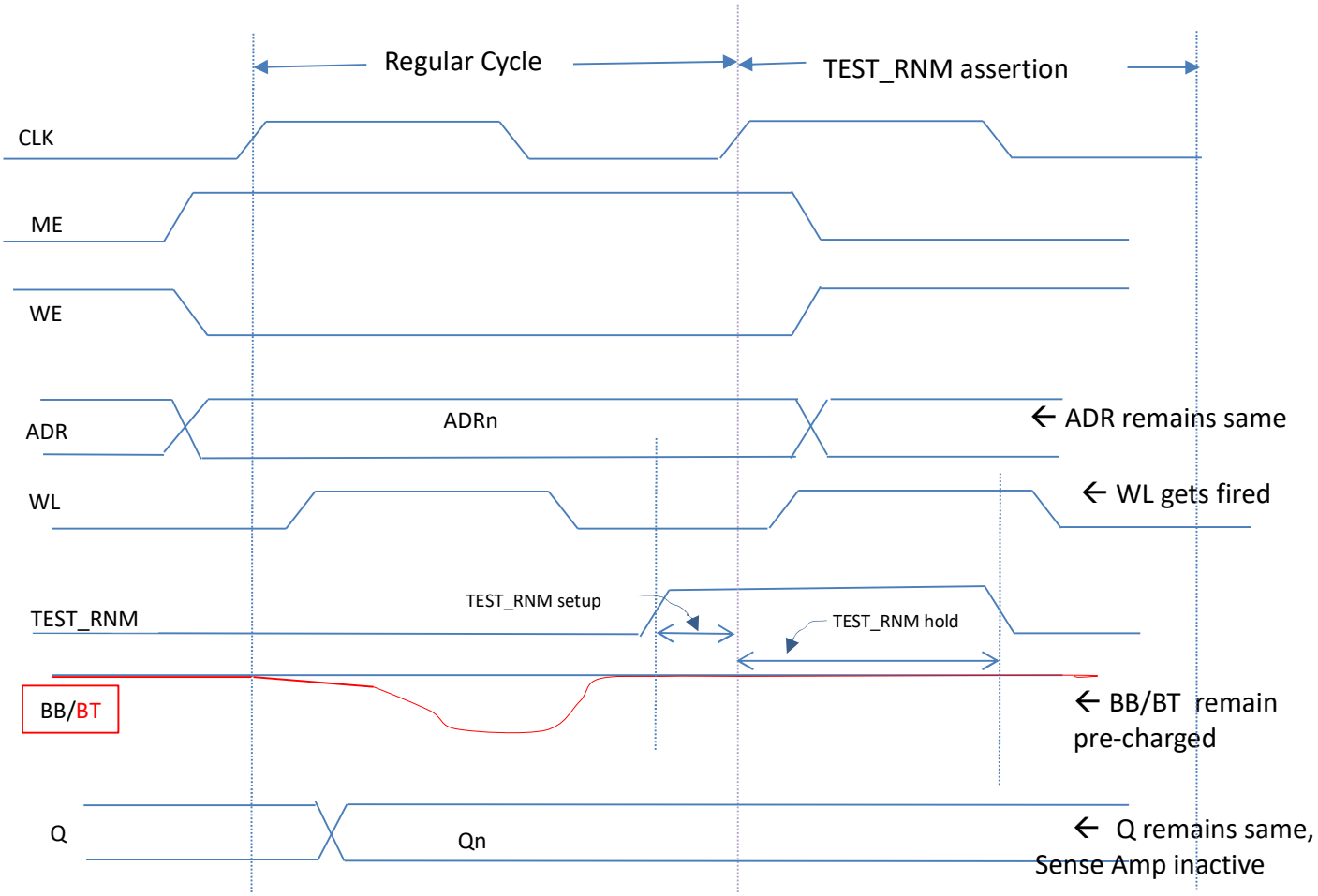


Figure 2: Write Operation (TEST_RNM)

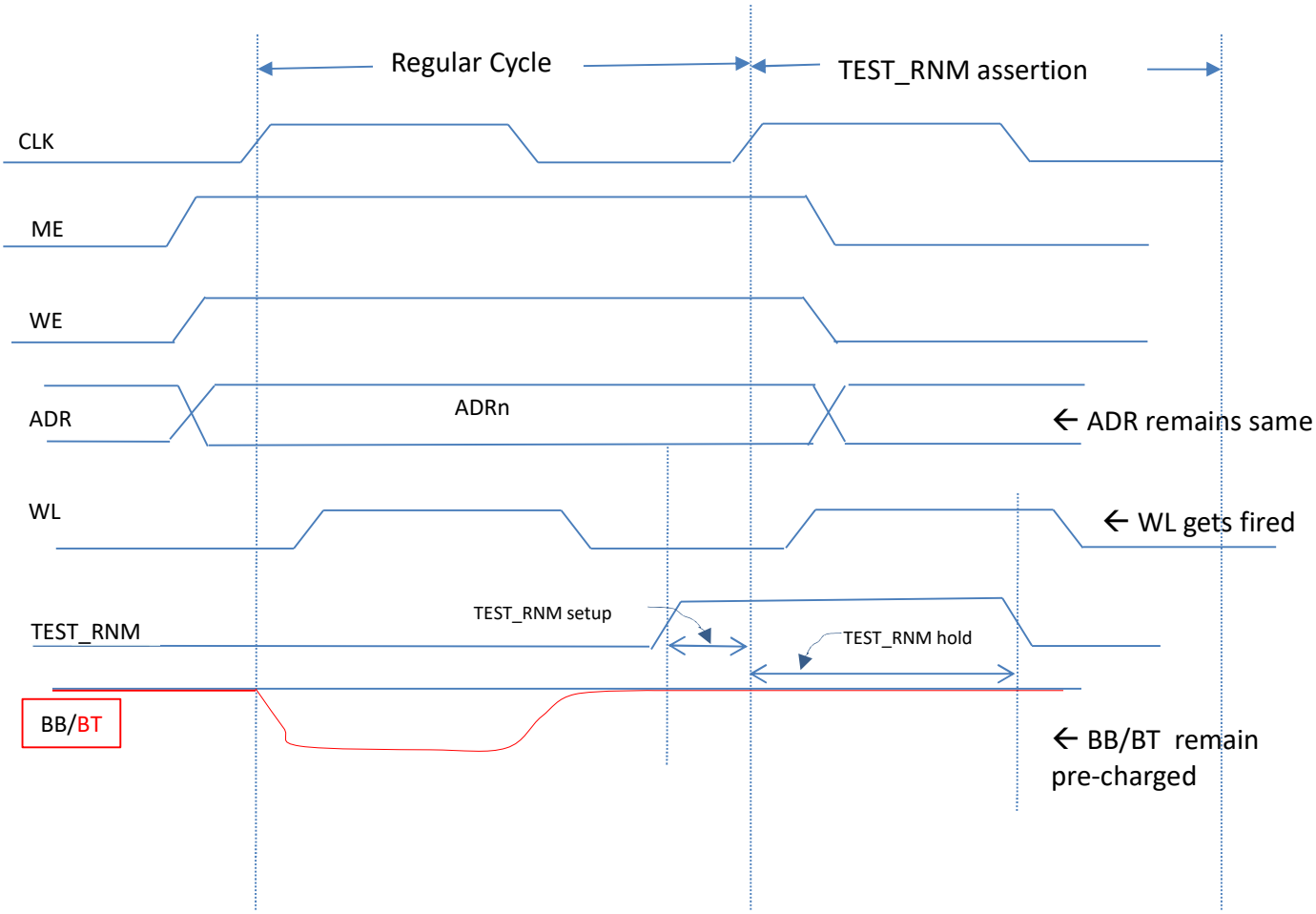


Figure 3: TESTRWM Operation

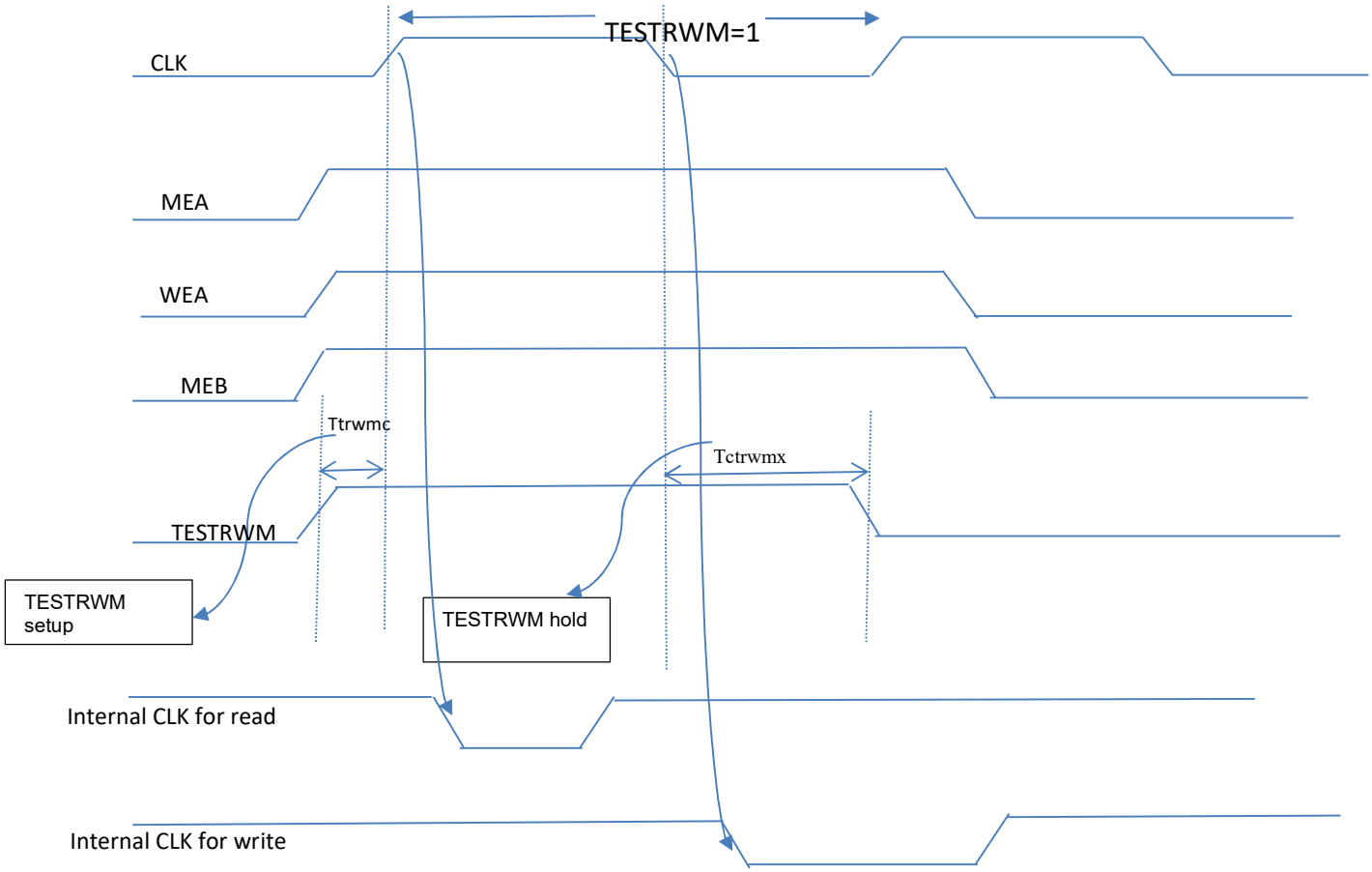
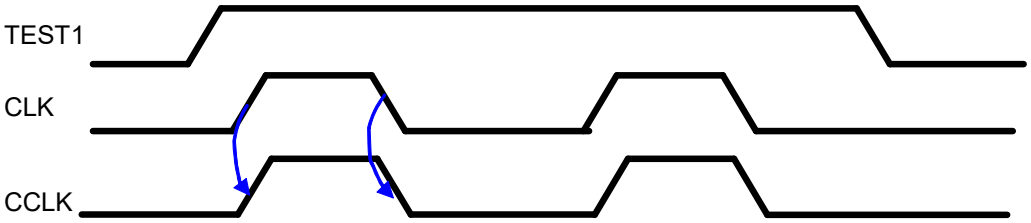


Figure 4: Test1 Mode Timing Diagram



- word-line active
- bit-line discharged
- sense amp enabled
- input latches close
- output latches open

- word-line inactive
- bit-line precharged
- sense amp disabled
- input latches open
- output latches close

6 Truth table for Test modes

TEST_RNM	TEST1	TESTRWM	Memory Array Contents	Memory Output	Comments
1	0	0	Unchanged	Unchanged (Q-1)	No RD / WR operation
1	1	0	Current location => X	X	In case of RD, Q goes to X. For write , accessed location contents => X
1	0	1	Unchanged	Unchanged (Q-1)	No RD / WR operation
1	1	1	X	X	Non Recommended. Q goes to X, memory contents => X
0	0	1			Normal TESTRWM operation
0	1	0			Normal TEST1 operation
0	1	1	X	X	Non Recommended. Q goes to X, memory contents => X
0	0	0			No test mode selected

Notes:

***X means unknown/corrupted*TESTRWM is only supported in UHD2PRF memory compiler.**
***For all three test modes (TEST1, TESTRWM, and TEST_RNM) there are setup and hold time requirements. For details, refer instance datasheets.**