SYNOPSYS®

GF 22FDX Memory Compilers

Routing Guidelines

Application Note 0372

DesignWare® Embedded Memories

March 2022
Version 1.0

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Revision History

Version	Date	Note
1.0	March 2022	Initial release

1 Introduction

Memory instances can often require a significant amount of power. Some planning should therefore be done to ensure that a robust power supply is provided and avoid actions that can overwhelm chip power supplies. This document is applicable to Synopsys 22FDX Embedded Memory compilers (dwc_comp_gf22nsd* and dwc_comp_in_gf22fdx_*).

2 GF22FDX Memory Compiler Routing for VHV/HVH Architectures

Synopsys GF22FDX memory compilers support both VHV and HVH architectures. Signal and PG routing scheme of the Memory compiler depends on the standard cell usage. The Memory compilers can be used alongside both HVH (M1 Horizontal) and VHV (M1 Vertical) Logic Libraries. However, the user needs to follow the guidelines published in subsequent sections of this document to avoid any issues after PNR.

- Memory Instance Pin Structure
  - Metal4/C2 PG pins in horizontal direction (orthogonal to Poly direction)
  - Metal2 OR Metal3/C1 signal pins in horizontal direction (orthogonal to Poly direction)

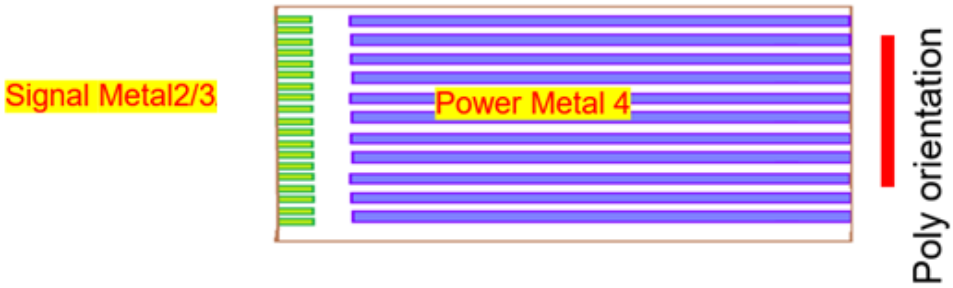

Figure 1 Signal and PG Metal Orientation

- PG Pin Routing: PG pins in Metal4/C2 for VDDP/VDDA/VSS/VBN/VBP work with both VHV and HVH LL Architectures
  - For VHV scheme, Metal4/C2 in the memories is in the expected/same orientation as Chip-level Routing. User can build a PG Grid in Metal5/C3 (orthogonal to memory PG Pins) and drop VIA4/A2 at every cross-over point.
  - For HVH scheme, Metal4/C2 in the memories is in the same direction as Metal5/C3 of Chip-level Routing. User is expected to build a PG Grid in Metal6/C4 and directly supply PG to memory Metal4 PG Pins using VIA5/A3 and VIA4/A2 stacks.
- Signal Pin Routing: User can choose between Metal2 and Metal3/C1 for memory Signal Pins at the time of instance generation (Compiler option – SIG_METAL)
  - For VHV scheme, user must choose SIG_METAL to be Metal2 as Metal2 is in expected orientation for VHV scheme.
  - For HVH scheme, user must choose SIG_METAL to be Metal3 as Metal3/C1 is in expected orientation for HVH scheme.

Note: SIG_METAL is only available for the dwc_comp_gf22nsd* compilers.

2.1 PG and Signal Connections Requirement

— For VHV scheme, the Chip-level PG routing runs in M5/C3 vertical mesh. User must connect memory PG Pins (C2-horizontal) at every C3 to C2 intersection. The vertical C3 mesh is to be connected at a minimum of every 5u for all the VDD, VSS, and VDDA Rails (Every 10um for VBP and VBN Rails). Minimum C3 width in PG mesh must be wide enough for at least 2 vias.

— For HVH scheme, the Chip-level PG routing must run in C4 vertical mesh. User must connect memory PG Pins (C2-horizontal) at every C4 to C2 intersection using Stacked VIA5/VIA4 vias. The vertical C4 mesh is to be connected at a minimum of every 5u for all the VDD, VSS, and VDDA lines (Every 10um for VBP and VBN Rails). Minimum C4 width in PG mesh must be wide enough for at least 2 vias, both VIA5 and VIA4.

3 Memory Signal and PG Routing with VHV Scheme

Synopsys 22FDX compilers support HVH scheme and following is an example of Memory control, address and data signal, and PG routing with example of 8T library.

3.1 Memory Block - PG Connection

- Memory PG Connections from C3 layer PG Strap to C2 layer macro pins (Via Stacking)

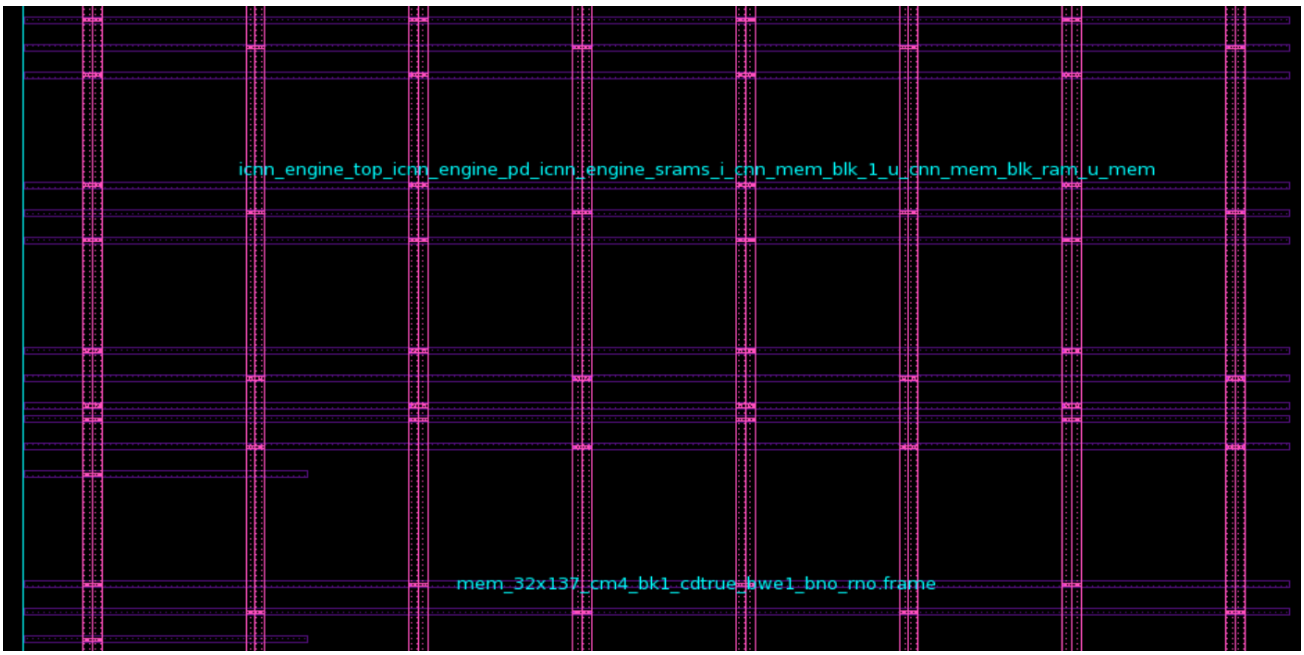

Figure 2 PG Connections to Memory PG Pins

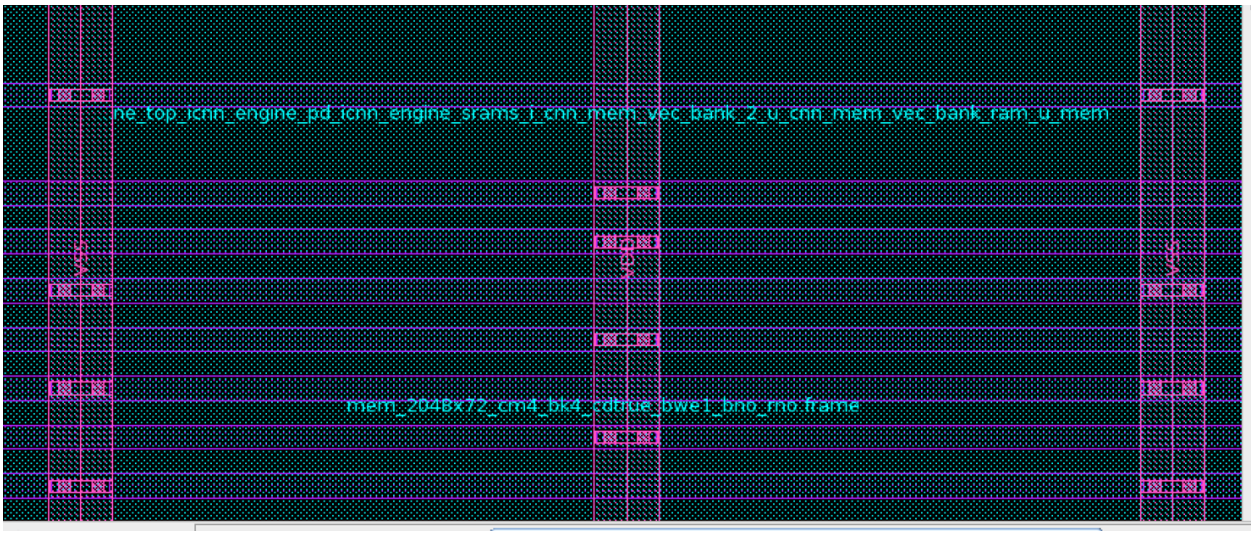

Figure 3 PG Connection to Memory PG Pins (2 VIA4 at every cross-over of C3 and C2)

3.2 Memory Signal Routing: Signal Pins in M2

- Memory signal pin connections after signal routing

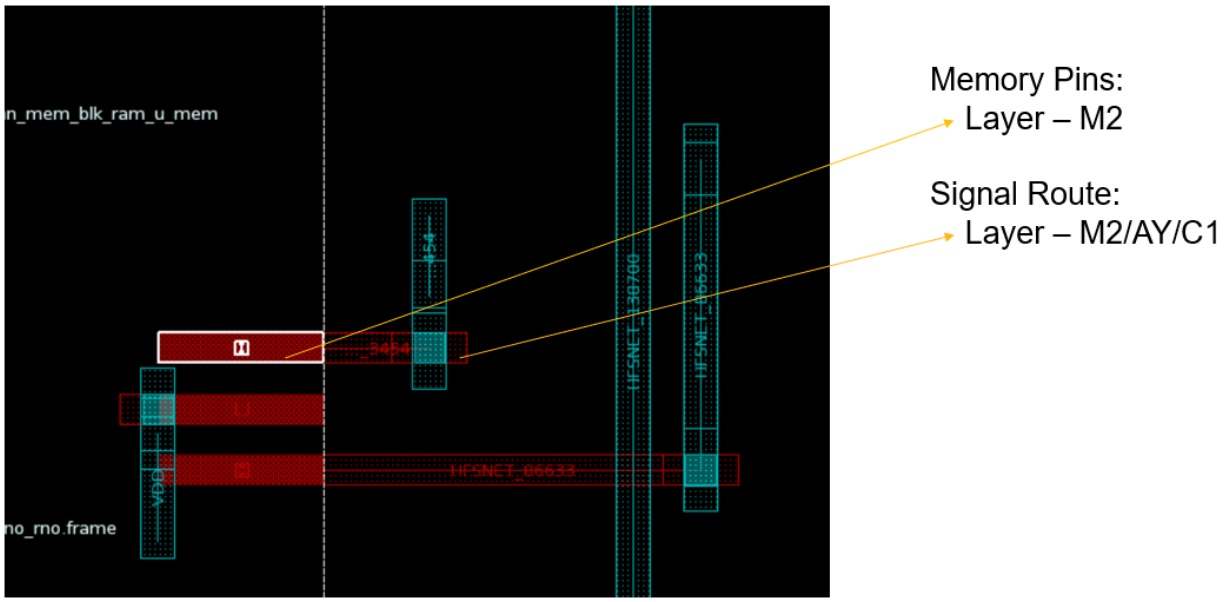

Figure 4 M2 Signal Routing from Memory Pins

4 Memory Signal and PG Routing with HVH Scheme

Synopsys 22FDX compilers support HVH scheme and following is an example of Memory control, address, and data signal and PG routing with example of 6.5T library.

4.1 Memory Signal Routing: Signal pins in M3/C1

- Memory signal pin connections after signal routing

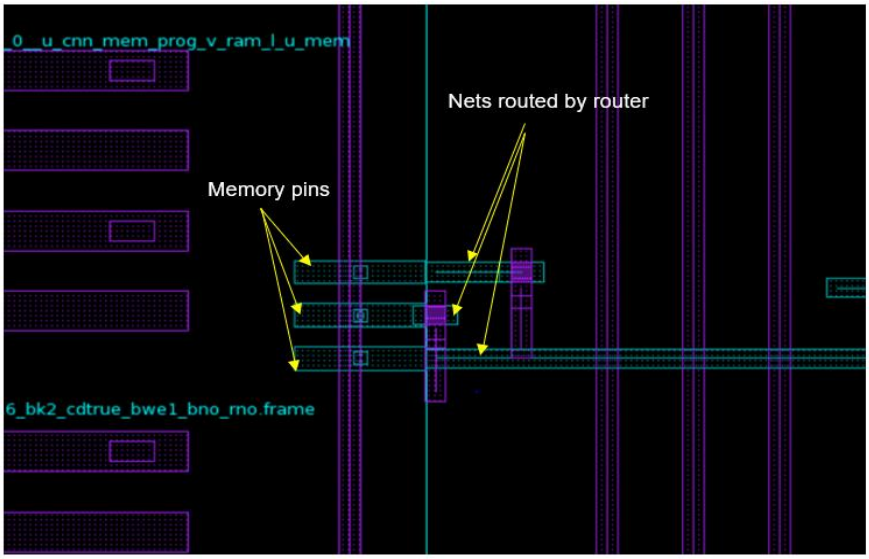

Figure 5 C1 Signal Routing from Memory Pins

– Memory pins layer – C1

– Signal route layer – C1/A1/C2

4.2 Memory Block - PG Connection

- Memory PG Connections from C4 layer PG Strap to C2 layer macro pins (Via Stacking)

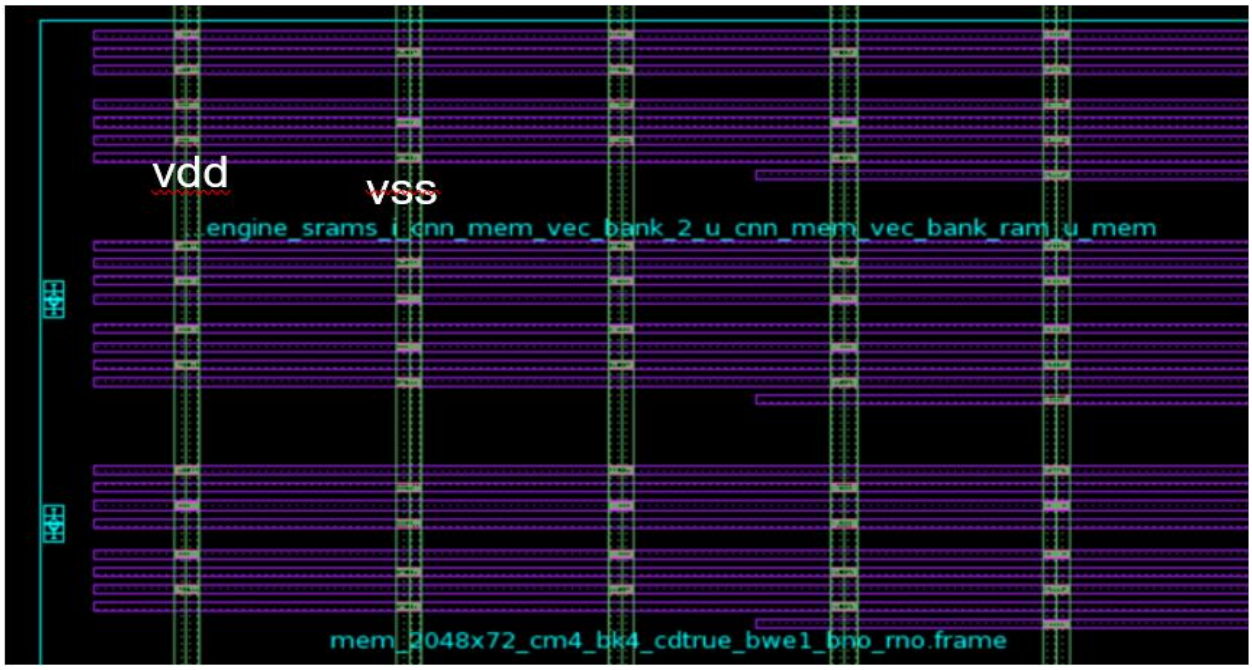

Figure 6 Top Level PG Connection (C4 to C2 connection)

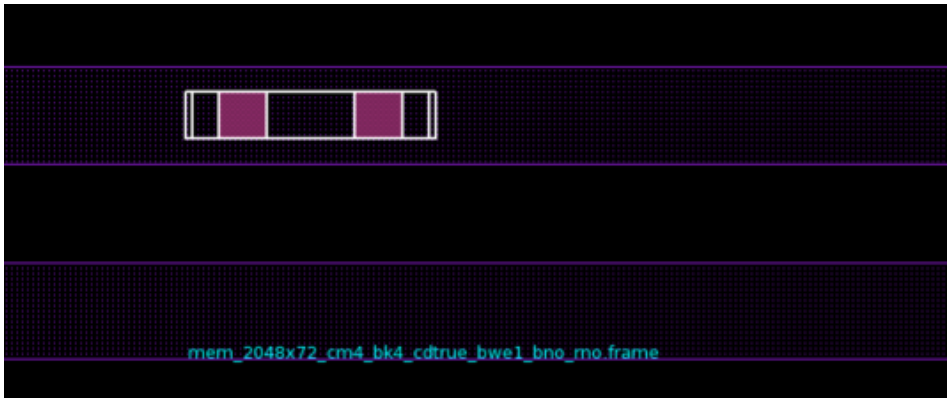

Figure 7 PG Pins Connections (VIA4)

– Memory VDD pin Layer – C2

– VIA04 (via def): Layer – C2/A2/C3

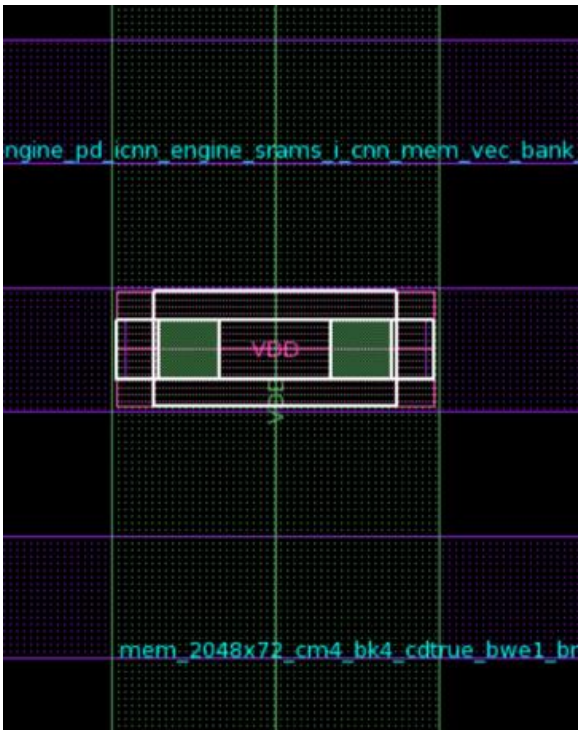

Figure 8 PG Pins Connections (VIA5)

- Memory VDD pin Layer – C2
- VIA05 (via def): Layer – C3/A3/C4

4.3 Memory PLEF for HVH Scheme (Applicable to dwc_comp_gf22nsd* compilers)

This family of memory compilers uses special M5 Routing Blockages to prevent Signal Routing in M5 over the memory for HVH Scheme. This has been done to avoid potential Coupling issues between memory M4 Signal Routes and Chip-level M5 Signal Routes. For HVH scheme, memory M4 and Chip-level M5 Routing will be in same direction.

The LEF should have below syntax to have blockage which allows C3 or M5 layer for PG routing but blocks for signal routing:

LAYER C3 EXCEPTPGNET SPACING 0;

RECT -0.135 -0.135 83.827 88.678;

This C3 or M5 blockage is required for HVH options only.

Note: Currently, all compilers may not have this syntax. Users may have to add it manually if they want to use it.

Figure 9 Memory-IP PLEF Prohibits Signal Routing in M5

5 Abutment Spacing Requirements

Following are the Abutment spacing requirements for memory to memory and memory to standard cell at chip level:

1. Memory to Memory Spacing

   - in perpendicular to poly direction: 1.200um

   - in poly direction: 1.200um

2. Memory to STD cell Spacing

   - in perpendicular to poly direction: 0.596um

   - in poly direction: 0.950um

This information can also be found in the release notes of the compiler.

6 Body Biasing in GF 22FDX Compilers

The main feature of FDSOI technology is to be able to control device characteristics by controlling bias value from the back of the device (Back Bias Scheme).

For back biasing, two type of device configuration can be used:
- RBB (Leakage optimization)
- FBB (Performance optimization)

Based on the application, user has to decide the one device configuration in their design. Memory documentation can be referred which type of configuration memory can be supporting. Both RBB and FBB IP types can be used on the same chip as well, if the DRC rules/Connectivity is followed as per technology requirement.

User always has an option to disable bias control for both schemes to ties these bias connections to ground.

Controlling Bias values are responsibility of chip level design with required range which can either be fixed value or Adoptive, based on the system design.

For dwc_comp_gf22nsd* memory compilers, if back_bias_enable flag is TRUE then bias pins will be available at top level for connection. For in_gf22fdx_* compilers, bias pins are available at the top level.

RBB or FBB support will be product level feature which can be checked in documentation for availability.

Please note that reverse body bias is only available for designs using a conventional Well approach and forward body bias can only be used for designs implemented in a flipped Well approach. VNW_N, VPW_P pins will show up in all the views including GDS/PLEF. Following are the supported voltages range for the bias voltages:

For FBB:
- Positive voltage on VNW_N (max 1.2V)
- Negative voltage on VPW_P (max -1.5V)

For RBB:
- Positive voltage on VNW_P (max 2.3)
- Negative Voltage on VPW_N (max -2.35)

We recommend using only the supported voltage levels for which memory is verified for voltage markers. If you are using any voltage levels outside the supported range for VNW_N and VPW_P, you might run into the DRC errors.
The SRAM well is independent from the logic well and the bias is also not related with that. The SRAMs are separated by construction.

6.1 Using No Body Bias

If body bias is not used for the memories, then it is recommended to connect VNW_N/VPW_P to VSS grid. It is OK to apply bias to other IP's and not memory as long as user is careful to use correct timing models and understands that memory performance will track differently vs. other IP's (timing closure may be more difficult).

6.2 Using Forward Body Bias

If the intent is to use body bias on the memories, then VNW_N/VPW_P on the memories needs to be connected to body bias supplies. Connecting VNW_N/VPW_P of all memories to VSS grid means NO body bias.

Please check the compiler documentation for PVTs that support FBB.

6.3 Using Reverse Body Bias

If the intent is to use body bias on the memories, then VNW_N/VPW_P on the memories needs to be connected to body bias supplies.

Please check the compiler documentation for PVTs that support RBB.

We would recommend users to check with the foundry regarding the methodology guidelines.

7 Appendix A: Supply Pin Details

GF 22FDX IN compilers and Synopsys native compilers use different naming conventions, as shown in the table below.

Pins	IN Compilers Naming	Synopsys Compilers Naming
Supply Pins	VDD	VDD
	VCS	VDDA
	VSS	VSS
Bias Pins	VBN	VNW_N
	VBP	VPW_P