# GF 22nm Memory Compiler Power Modes

## APNT - 0328

*GF22nm Memory Compilers*

May 2021
Version 1.2

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# Revision History

| Version | Date | Note |
|---|---|---|
| 1.0 | February 2020 | Initial release |
| 1.1 | August, 2020 | 1. Added compilers list.<br>2. Changed the format of the PVT statement, the norminal voltage, and VDDA/VDDP differential. |
| 1.2 | May 2021 | Added two consumer grade compilers. |

# 1 Introduction

This application note describes the operation of the Power Management modes of the following Synopsys SiWare™ Memory Compilers on GF 22nm.

- Automotive Grade 1 Memory Compilers
  - ✓ ROM (gf22nsd41p10s1dvl01ms)
  - ✓ HD SP SRAM (gf22nsd41p11s1dcl02ms)
  - ✓ UHD 2P RF (gf22nsd42p11s1cul256s)
  - ✓ HD 1P RF (gf22nsd41p11s1crl256s)
  - ✓ HD 2P RF (gf22nsd42p11s1drl128s)
  - ✓ HS 1P RF (gf22nsd41p11s1srl256s)
- Consumer-Only Grade Memory Compilers
  - ✓ UHD 1P SRAM (gf22nsd81p11sadul02ms)
  - ✓ UHD 1P RF (gf22nsd81p11sadul256s)

For details regarding ROM and HD 2P RF compilers, please refer Section 19 on page 22. Some of the capabilities described below are licensable features. Please refer to the memory compiler custom.glb file and manual (Edoc) for additional information.

# 2 Power Gating Truth Table

The following table lists the compile time options and Power Rail configurations available in the memory compilers.

| Compiler Setting Option | Single Rail, No Power Gate | Single Rail, Power Gate | Dual Rail, No Power Gate POFF pins | Dual Rail, Power Gate POFF pins |
|---|---|---|---|---|
| vdda_enable | FALSE | FALSE | TRUE | TRUE |
| pg_enable | FALSE | TRUE | FALSE | TRUE |

**Table 1: Power Rail Configurations**

**Note:** POFF pins will only appear when vdda_enable=TRUE.

The table below describes the valid combinations of VDDA and VDDP when vdda_enable=TRUE and pg_enable=TRUE/FALSE.

| VDDP | VDDA | Comments |
|---|---|---|
| OFF | OFF | Valid |
| OFF | ON | Permitted as per POFF table. |
| ON | OFF | Not permitted |
| ON | ON | Valid |

**Table 2: Power Rail Truth Table**

**Periphery Off feature**: Supports Periphery Off (VDD=0 or floating) during Periphery Off mode. This feature is controlled by the **vdda_enable** GLB parameter. When **vdda_enable=TRUE**, POFF pins will appear and users can shut off complete periphery power supply.

| POFF[1:0] | | Comments |
|---|---|---|
| 0 | 0 | No Periphery Off Mode* |
| 0 | 1 | Standard Periphery Off Mode. Allows VDDP to be tuned off (can be floating) while keeping VDDA as high. Output is X, memory contents are maintained. |
| 1 | 0 | BC0 Periphery Off Mode that allows bypass for Array Bias. Allows VDDP to be off (can be floating). Output is X and memory contents are maintained. |
| 1 | 1 | SD Periphery Off Mode that allows VDDP to be turned off(can be floating). Output is X, no memory retention. |

**Table 3: POFF Table**

*VDDP should not be OFF while VDDA is ON. This is to ensure that there is no crowbar through the level shifter and WL drivers.

# 3 Integrated Power Gating and Periphery Collapse

Light Sleep mode is available at all times. Deep Sleep and Shut Down modes are only available when the power management feature is enabled by setting the compiler option flag, pg_enable=TRUE (PG license required), prior to memory instance generation. The LS, DS, and SD pins are level sensitive to facilitate sleep mode exit without requiring a clock. In addition, when vdda_enable=TRUE, POFF pins will appear. These pins can be used to put memory in power down mode which will allow periphery supply to turn off completely. For POFF functionality please refer to Section 7 on page 11.

- **Light Sleep Mode (LS control pin)**
  - This mode is always available, regardless of the state of pg_enable
  - Activated when LS pin is asserted
  - All outputs maintain previous data during Light Sleep mode
  - Leakage reduction with fine grained power gating and source biasing
  - Data in memory array is retained

- Data stored in redundant memory bits is retained
- Redundancy reconfiguration registers are built into the memory compiler.
  - VDDF is the dedicated power supply for the built in reconfiguration registers.
  - If the power supply is switched off in LS mode, the redundancy reconfiguration registers require re-load from eFuse whenever power supply is enabled again. LS mode does not impact redundancy reconfiguration registers.

- **Deep Sleep Mode (DS control pin)**
  - Compile option: pg_enable=TRUE
  - Activated when DS pin is asserted
  - Integrated periphery power gating with Data Retention
  - Data in memory array is retained
  - Memory outputs are held low (Q and QP)
  - After DS is deactivated, the output Q will remain low but the output QP will be unknown until the next valid functional READ/WRITEoperation.
  - Memory SCAN registers are not active
  - Data stored in redundant memory bits is retained
  - Redundancy reconfiguration registers are built into the memory compiler.
    - VDDF is the dedicated power supply for the built in reconfiguration registers.
    - If the power supply is switched off in DS mode, the redundancy reconfiguration registers require re-load from eFuse whenever power supply is enabled again. DS mode does not impact redundancy reconfiguration registers.

- **Shut Down mode (SD control pin)**
  - Compile option: **pg_enable**=TRUE
  - Activated when SD pin is asserted
  - Complete shutdown (both periphery and array are power gated)
  - No memory array data retention
  - Memory outputs are held low
  - After SD is deactivated, the output Q will remain low but the output QP will be unknown until the next functional READ/WRITE operation
  - Memory SCAN registers are not active
  - Data stored in redundant memory bits is not retained
  - Redundancy reconfiguration registers are built into the memory compiler.
    - VDDF is the dedicated power supply for the built in reconfiguration registers which is not affected by LS/DS/SD modes.
    - If the power supply (VDDF) is switched off, the redundancy reconfiguration registers require re-load from eFuse whenever power supply is enabled again.

- **Periphery Collpase Mode T(POFF[1:0] pins)**

- Compile option: **vdda_enable**=TRUE
- Activated when POFF pins are asserted
- VDDP can be turned off, refer Table 5 on page 11 for Truth table
- Memory array data retention (only in POFF[1:0]=10, 01, 00)
- Memory outputs are held unknown
- Memory SCAN registers are not active
- Data stored in redundant memory bits is retained only when POFF[1:0]=01 or 10. In POFF[1:0]=11, data is not retained.
- Redundancy reconfiguration registers are built into the memory compiler.
  - VDDF is the dedicated power supply for the built in reconfiguration registers which is not affected by LS/DS/SD/POFF modes.
  - If the power supply (VDDF) is switched off, the redundancy reconfiguration registers require re-load from eFuse whenever power supply is enabled again.

# 4 Integrated Power Gating and Periphery Collapse Implementation

**Single Rail Option:**

The following diagram provides a general representation of how the three power management modes are implemented for the Single Rail option.

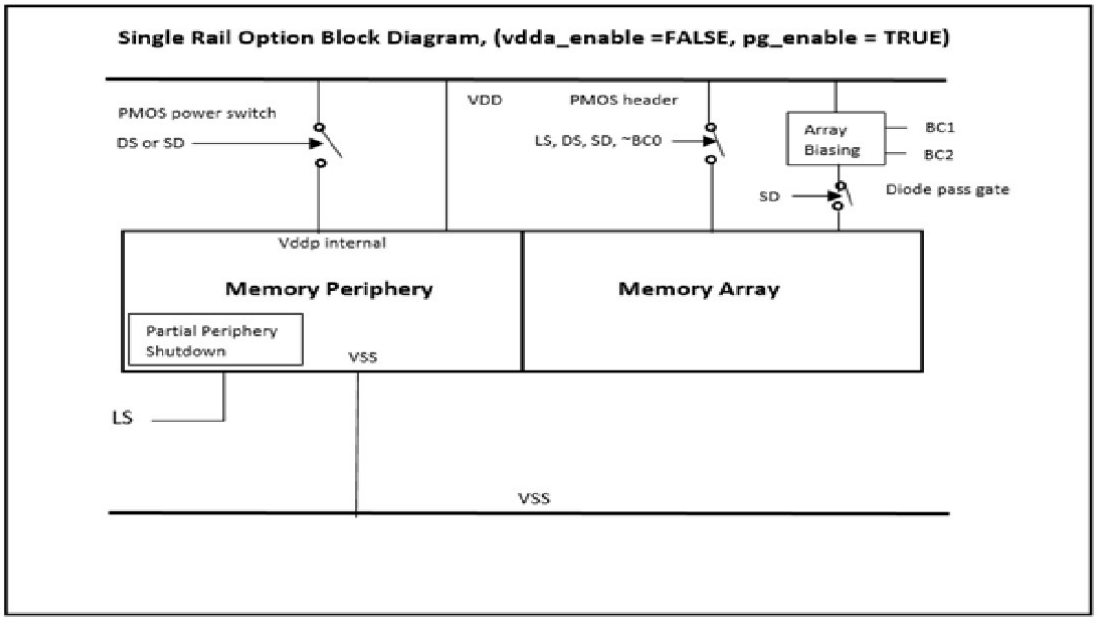



**Figure 1: Single Rail Block Diagram**

**Dual Rail Option:**

When the Dual Rail option is enabled, the Periphery Power Rail (VDDP) and the Array Power Rail (VDDA) are physically separated. To activate the Dual Rail option (PG license required), set the memory compiler option flag **vdda_enable** to TRUE. Level Shifters are added to interface between Periphery (VDDP) and Array (VDDA) voltage domains.

Dual Rail Conditions:

VDDA-VDDP <= 270mV for all timing modes
VDDP-VDDA <= 100mV for all timing modes

For the Dual Rail option, the parameter list describing the PVT conditions (i.e. in ISH scripts, settings file or <>_custom.glb file) requires an additional voltage definition, VDDA). The format of the PVT statement is:

<pvt_number> = {<process> <VDDP> <temp> <VDDA> <VBN> <VBP>}

e.g. pvt2 = {tt0p8v25c_0p8v_0v_0v}, pvt9 = {ssg_fcmax0p72vn40c_0p72v_0p7v_n1p5v}

The above format is used for Single Rail as well, however the user needs to ensure that both voltages are set to the same value (VDDP = VDDA).

Refer to the memory compiler documentation (edoc.pdf) for additional power sequencing, and timing requirements for the Dual Rail option. The documentation is included with every memory compiler shipment.

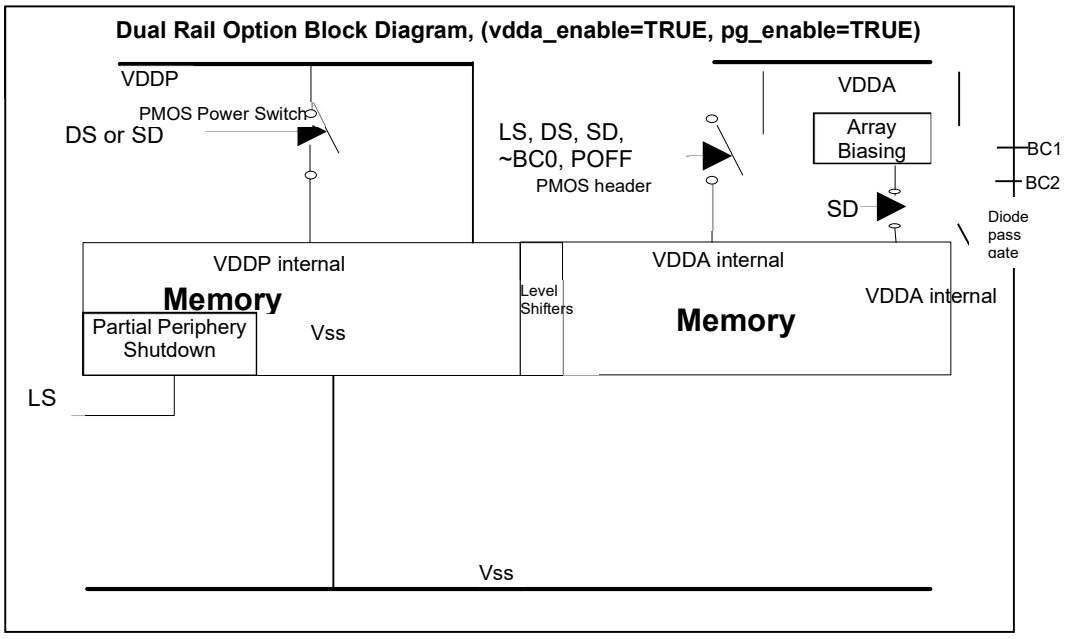



**Figure** 2**: Dual Rail Block Diagram**

# 5 Core bias control for Leakage Reduction (not applicable for ROM and HDRF2P)

| Mode | BC2 | BC1 | LS | DS | SD | BC0 | Usage | Mode |
|---|---|---|---|---|---|---|---|---|
| **Functional** | 0 | 0 | 0 | 0 | 0 | 0 | All pvts | BC1 and BC2 have no effect on Functional mode |
| | 0 | 1 | 0 | 0 | 0 | 0 | All pvts | BC1 and BC2 have no effect on Functional mode |
| | 1 | 0 | 0 | 0 | 0 | 0 | All pvts | BC1 and BC2 have no effect on Functional mode |
| | 1 | 1 | 0 | 0 | 0 | 0 | All pvts | BC1 and BC2 have no effect on Functional mode |
| **Light Sleep** | 0 | 0 | 1 | 0 | 0 | 0 | VDDA = Vnom | Both Diodes On (not recommended. Leakage data is not provided) |
| | 0 | 1 | 1 | 0 | 0 | 0 | VDDA = (Vnom – 10%) to Vmax | BC1 Diode (recommended setting for LS, DS modes) |
| | 1 | 0 | 1 | 0 | 0 | 0 | VDDA = Vnom to Vmax | BC2 Diode (additional leakage saving for LS, DS modes but at higher VDD) |
| | 1 | 1 | 1 | 0 | 0 | 0 | VDDA = (Vnom – 10%) to Vmax | Both Diodes On (not recommended. Leakage data is not provided) |
| **Deep Sleep** | 0 | 0 | X | 1 | 0 | 0 | VDDA = Vnom | Both Diodes On (not recommended. Leakage data is not provided) |
| | 0 | 1 | X | 1 | 0 | 0 | VDDA = (Vnom – 10%) to Vmax | BC1 Diode (recommended setting for LS, DS modes) |
| | 1 | 0 | X | 1 | 0 | 0 | VDDA = Vnom to Vmax | BC2 Diode (additional leakage saving for LS, DS modes but at higher VDD) |
| | 1 | 1 | X | 1 | 0 | 0 | VDDA = (Vnom – 10%) to Vmax | Both Diodes On (not recommended. Leakage data is not provided) |
| **Shut Down** | X | X | X | X | 1 | X | VDDA = Vnom | Both Diodes Off |

**Table 4: Core Bias Truth Table**

**Note**: VDDA is the memory array voltage. Vnom is 0.8 V.

# 6 Array Bias Bypass Mode (Not applicable for ROM and HDRF2P)

| Mode | BC2 | BC1 | LS | DS | SD | BC0 | Usage | Mode |
|---|---|---|---|---|---|---|---|---|
| **Light Sleep (LS) without array bias** | 0/1 | 0/1 | 1 | 0 | 0 | 1 | VDDA = Vmin to Vmax | Leakage saving only because of periphery<br>No saving from array bias |
| **Deep Sleep (DS) without array bias** | 0/1 | 0/1 | X | 1 | 0 | 1 | VDDA = Vmin to Vmax | Leakage saving because of complete periphery shutdown. No saving from array bias |
| **Shut Down (SD mode)** | X | X | X | X | 1 | X | N/A | Leakage saving because of array and periphery shutdown |

# 7 Normal, LS, DS, SD, and POFF truth table

| Mode | LS | DS | SD | POFF [1] | POFF [0] | VDDP | VDDA | Array Retention | Array Biasing | PMOS Header | Diode pass gate |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Normal** | 0 | 0 | 0 | 0 | 0 | VDDP | VDDA | Yes | No | ON | ON |
| **Light Sleep** | 1 | 0 | 0 | 0 | 0 | VDDP | VDDA | Yes | Yes | OFF | ON |
| **Deep Sleep** | X | 1 | 0 | 0 | 0 | VDDP | VDDA | Yes | Yes | OFF | ON |
| **Shut Down** | X | X | 1 | 0 | 0 | VDDP | VDDA | No | N/A | OFF | OFF |
| **Standard Periphery Off Mode** | X | X | X | 0 | 1 | X | VDDA | Yes | Yes | OFF | ON |
| **BC0 Periphery Off Mode** | X | X | X | 1 | 0 | X | VDDA | Yes | No | ON | ON |
| **SD Periphery Off Mode** | X | X | X | 1 | 1 | X | VDDA | No | N/A | OFF | OFF |

**Table 5: Power Supply (VDDP and VDDA) status during different modes**

# 8 Peak Current Protection

Current-limiting circuitry is integrated into the memory. Therefore peak current to the memory, both array and periphery, is internally limited during any power-up sequence.

# 9 Power Management Mode Power Supply Connections

The table below describes the power supply connection status for each power management mode.

| | Single Rail | | Dual Rail | |
|---|---|---|---|---|
| **Mode** | **VDDP internal** | **VDDA internal** | **VDDP internal** | **VDDA internal** |
| **Functional** | Vdd | Vdd | VDDP | VDDA |
| **Light Sleep** | Vdd | Array Bias | VDDP | Array Bias |
| **Deep Sleep** | Disconnected | Array Bias | Disconnected | Array Bias |
| **Shut Down** | Disconnected | Disconnected | Disconnected | Disconnected |

**Table 6: Power Supply Connection Status**

**Note:** The above table is valid for POFF[1:0]=00 and BC0=0.

# 10 Power Management Mode, Signal Pin Conditioning

The table below defines the input signal pin requirements and output signal pin status for the three power management modes.

| Mode | MEA | MEB (2P, DP) | LS | DS | SD | POFF[1:0] | BC0/ BC1/ BC2 | All Other Input Pins | Output (Q) | QP | SO | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Functional** | 0/1 | 0/1 | 0 | 0 | 0 | 00 | 0/1 | Normal input mode | Q | QP | SO | Normal operation |
| **Light Sleep** | 0/1 | 0/1 | 1 | 0 | 0 | 00 | 0/1 | Cannot float, must be driven | Q (hold last state) | QP (hold last state) | SO (hold last state) | Partial Periphery shutdown, Array source bias |
| **Deep Sleep** | X | X | X | 0->1<br>**1->0** | 0 | 00 | 0/1 | X | 0<br>**Q (retains 0)** | 0<br>X | 0<br>X | Periphery shutdown, Array source bias |
| **Shut Down** | X | X | X | X | 0->1<br>**1->0** | 00 | X | X | 0<br>**Q (retains 0)** | 0<br>X | 0<br>X | Periphery shutdown, Array shutdown |
| **Standard Periphery Off Mode** | X | X | X | X | X | 01 | X | X | X | X | X | VDDP can be removed. For more information please refer Section 7 |
| **BC0 Periphery Off Mode** | X | X | X | X | X | 10 | X | X | X | X | X | VDDP can be removed. For more information please refer Section 7 |
| **SD Periphery Off Mode** | X | X | X | X | X | 11 | X | X | X | X | X | VDDP can be removed. For more information please refer Section 7 |

**Table 7: Input Signal Requirements for Power Management Modes**

x = Don't care, can be floating once the power mode is stable (after mode setup time is met)

Q/QP will be clamped to "0" after Tsdrq (SD rise to Q/QP) or Tdsrq(DS rise to Q/QP) is met after SD/DS is asserted.

- All outputs maintain their last state during Light Sleep mode.
- All outputs are held low during Deep Sleep and Shut Down mode. Q/QP will be clamped to "0" after Tsdrq(SD rise to Q/QP) or Tdsrq(DS rise to Q/QP) is met after SD/DS is asserted.
- RME and RM signals need to be driven after coming out of DS or SD before memory operation.

# 11 Power Mode Sequencing

The following power mode sequences are permitted.

| Mode Transition | Pin Values |
|---|---|
| LS -> DS -> SD | [LS, DS, SD] [1, 0, 0] -> [x, 1, 0] -> [x, x, 1] |
| DS -> SD | [LS, DS, SD] [x, 1, 0] -> [x, x, 1] |
| LS -> SD | [LS, DS, SD] [1, 0, 0] -> [x, x, 1] |
| SD -> DS -> LS | [LS, DS, SD] [0/1, 0/1, 1] -> [0/1, 1, 0] -> [1, 0, 0] |
| DS -> LS | [LS, DS, SD] [0/1, 1, 0] -> [1, 0, 0] |
| SD -> LS | [LS, DS, SD] [0/1, 0/1, 1] -> [1, 0, 0] |
| standby mode -> LS-> standby mode | [ME, LS, DS, SD] [0, 0, 0, 0] -> [0/1, 1, 0, 0] -> [0, 0, 0, 0] |
| standby mode -> DS-> standby mode | [ME, LS, DS, SD] [0, 0, 0, 0] -> [x, x, 1, 0] -> [0, 0, 0, 0] |
| standby mode -> SD-> standby mode | [ME, LS, DS, SD] [0, 0, 0, 0] -> [x, x, x, 1] -> [0, 0, 0, 0] |
| Standby -> POFF -> standby mode | [ME,VDDP POFF] [0, 1, 00] -> [x, x, 01/10/11]** -> [0, 1, 00] |

**Table 8: Permitted Power Mode Sequences for normal, LS, DS, SD, and POFF**

Where: x = don't care, can be floating once the power mode is stable (after mode setup time is met).

0/1 = may be either 0 or 1.

** Please refer to Table 5 on page 11 for different POFF modes.

# 12 External Power Supply Sequencing for Dual Rail

The following is the recommended sequence of supply assertion/de-assertion in order to avoid large crow-bar current between interfaces of the supplies occurring at some parts of the memory.

| Mode | Sequence |
|---|---|
| **Powering Up** | VDDF → VDDP → VDDA |
| **Powering Down** | VDDA → VDDP → VDDF |

**Table 9: Dual Rail Power Supply Sequencing when input pins POFF[1:0]=00/01/10/11**

| Mode | Sequence* |
|---|---|
| **Powering Up** | VDDA → VDDF → VDDP |
| **Powering Down** | VDDP → VDDF → VDDA |

**Table 10: Dual Rail Power Supply Sequencing when input pins POFF[1:0]=01/10/11**

**Note***:* VDDF is required only when redundancy is enabled.

When VDDF and VDDP are connected together, VDDF and VDDP can be power up and power down at the same time.

If VDDF and VDDP are tied together, then during POFF modes, reconfiguration register contents will be lost.

***This sequence is valid only if POFF[1:0] pins are set to 01/10/11 as soon as VDDA ramps up completely**

**Note:** VDDF can be tied to VDDA, if VDDF>=VDDP

The sequence in Table 10 needs to be followed for Power ramp up and down.

VDDP > VDDA is supported for SNPS memories only if VDDF is separate third supply. Since VDDF is connected to VDDA, therefore VDDP > VDDF(VDDA) is not allowed in this case.

# 13 Latches for Power Management Modes

A latch is used to protect a normal legal READ/WRITE operation from an early power down.

If the LS, DS or SD signal is initiated (set HIGH) late in a READ/WRITE cycle then the power-mode is initiated immediately. A setup time to the next clock rising edge is specified to ensure that that a new READ/WRITE cycle is not entered. If the setup time is violated, then the RAM would try and enter a READ/WRITE operation while simultaneously going into a power management mode.

To exit the power management modes, the latch is designed in such a way that it is level sensitive to low voltages. Thus the system will come out of power mode when LS, DS and SD are all low independent of the clock state. It is required that the clock is stable (either high or low, but not switching, and not 'X') when exiting from a power mode. ME[A/B] can be used to disable the internal clock to satisfy the stable clock requirement.

There is no latch on BC0, BC1 and BC2 pins. There is no requirement to keep the clock running while switching BC1 and BC2 pins. There are no latches for POFF.

# 14 Power Management Mode Timing Requirements

The following timing diagrams and specifications apply to all three Power Management modes (LS, DS and SD) described in this Application Note.

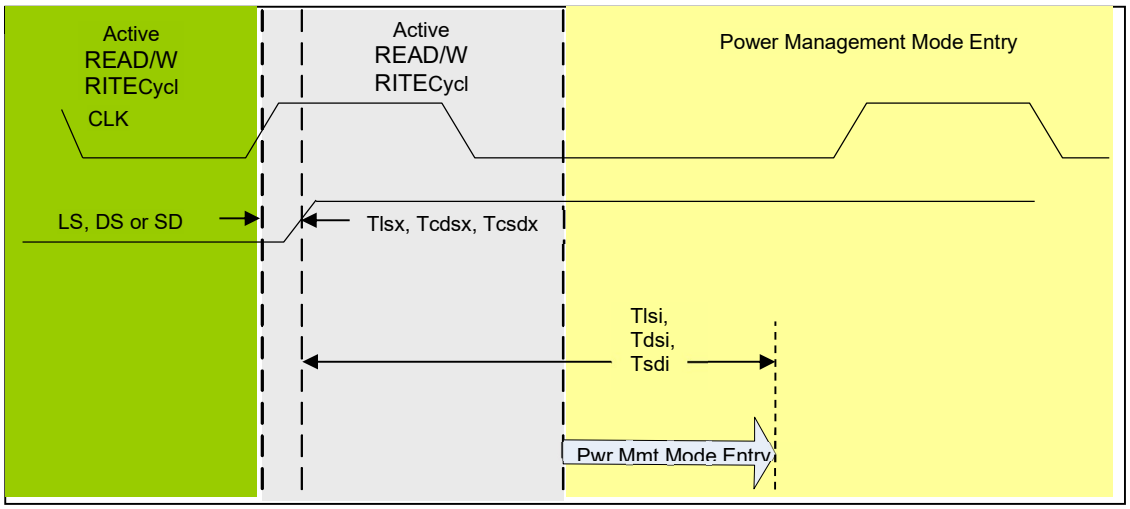



**Figure 3: Power Management Mode Entry, after Rising Clock Edge**

In Figure 3 above, the "hold time" refers to the amount of time after the rising clock edge. LS, DS or SD must be LOW to avoid possible contention (possible data corruption during Active cycle). The Hold time will be small. Figure 4 shows a clock cycle during Power Management mode. There is no requirement to keep the clock running during LS, DS or SD mode. This is shown in the figures only for completeness. The only restrictions on the rising edge of LS, DS or SD are the Hold time in Figure 3 and the Setup time in Figure 4 below.

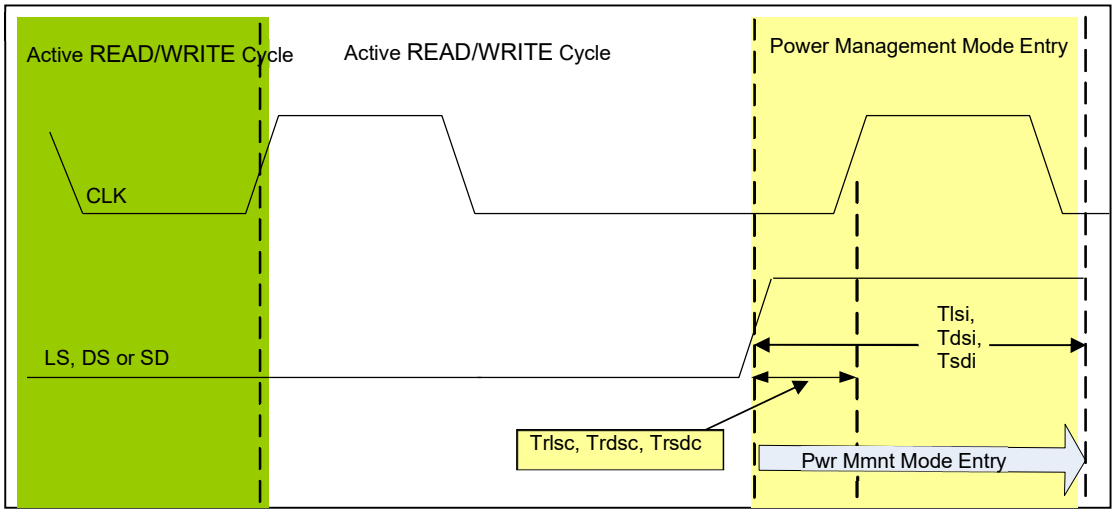



**Figure 4: Power Management Mode Entry, prior to Rising Clock Edge**

The rising clock edge shown in Figure 4 is not required; it is shown for the Setup reference. LS, DS or SD must go HIGH prior to the defined setup time, if the clock is running.

The following power management mode timing parameters are listed in the datasheets and are provided here for reference.

| Timing Parameter | Description |
|---|---|
| Trlsc | LS Setup time before rising clock |
| Trdsc | DS Setup time before rising clock |
| Trsdc | SD Setup time before rising clock |
| Tlsi | LS active to memory low-leakage state |
| Tdsi | DS active to memory low-leakage state |
| Tsdi | SD active to memory low-leakage state |
| Tlsx | LS Hold time after clock rises |
| Tcdsx | DS Hold time after clock rises |
| Tcsdx | SD Hold time after clock rises |
| Tflsc | LS inactive (Low) time before rising clock |
| Tfdsc | DS inactive (low) time before rising clock |

**Table 11: Timing Parameters**

In Figure 5, the Clock is held to a known state, either 0 or 1, during Power Management mode exit. The recovery time is defined as a setup of LS, DS or SD going LOW to the next rising edge of clock. A clock is not required to exit a Power Management mode; it is shown for reference only.

An alternate solution to keeping the clock stable during Power Management mode exit is to set the ME[A/B] pin to logic 0. This will effectively disable the internal clock for the memory and satisfy the stable clock requirements during the recovery time.

ROP pin can be used to daisy chain memory instances together to optimize the current profile (lower the in-rush current). Waking up memories one after another can lower the total peak currents. ROP is a static output pin for Deep Sleep and Shut Down modes. ROP is low in Deep Sleep or Shut Down mode.

It is recommended that the wake-up time be programmable so that in case Silicon requires longer time to wake up than expected, it will be possible to extend the wake-up time to attain a functional system.

The minimum HIGH time for LS, DS or SD mode is Tlsi, Tdsi, or Tsdi respectively.

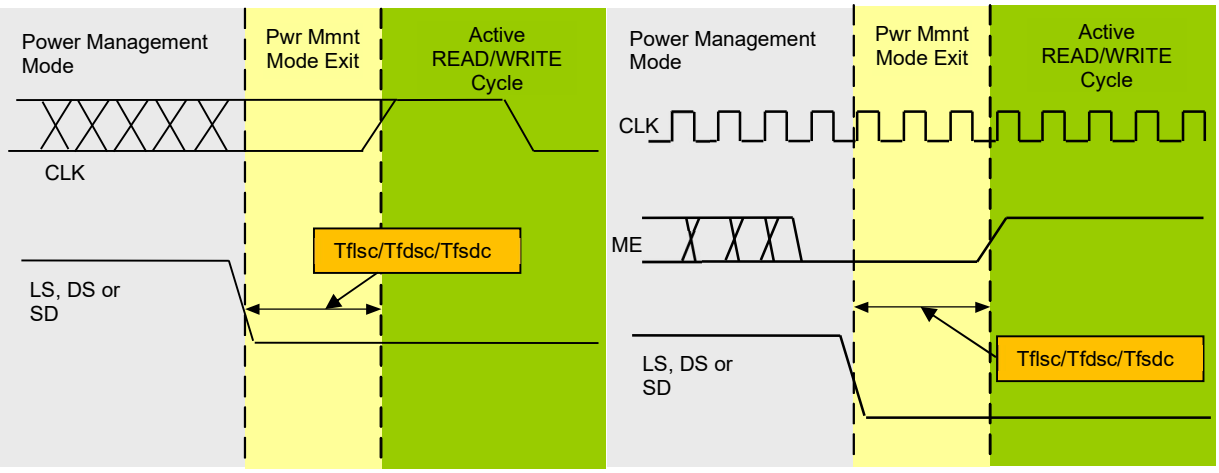



**Figure 5: Power Management Mode Exit**

**Note**: Please refer to the datasheets and .lib files for Power Management mode timing data.

# 15 POFF Mode Timing Requirements

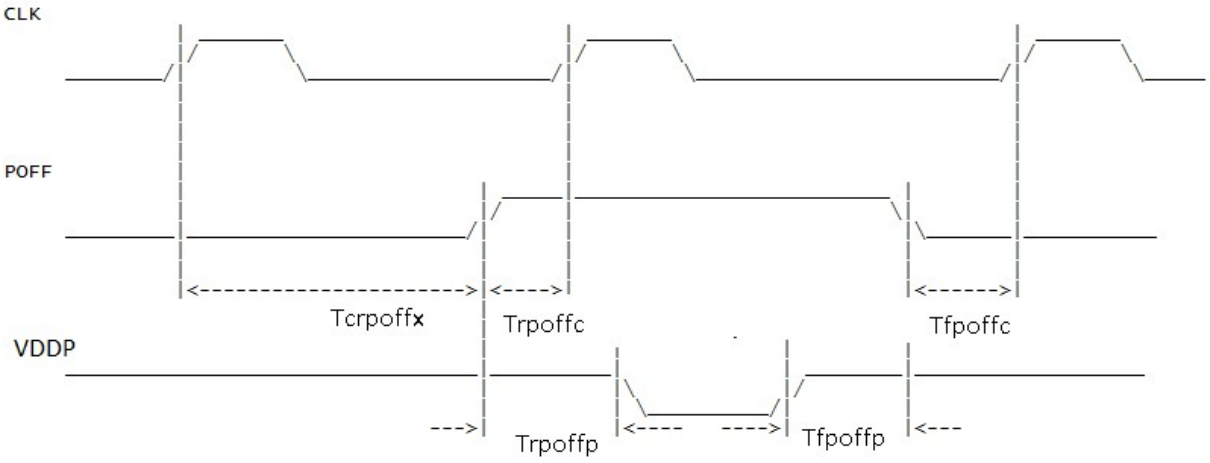



**Figure 6 : POFF timing diagram**

**Note**: An alternate solution to keeping the clock stable during POFF mode entry/exit is to set the ME[A/B] pin to logic 0. This will effectively disable the internal clock for the memory and satisfy the stable clock requirements during the setup/hold/recovery time.

| Timing Parameter | Description |
|---|---|
| Trpoffc | POFF rise setup time before rising clock |
| Tcrpoffx | POFF rise hold time after clock rises |
| Trpoffp | VDD removal with respect to Posedge POFF |
| Tfpoffp | VDD recovery with respect to Negedge POFF |
| Tfpoffc | POFF fall setup time before rising clock |

**Note**: Please refer to the datasheets and .lib files for POFF related timing data.

# 16 Power Management Timing when using Dual Port Memories

The clocks used for Dual Port (DP) memories are asynchronous. Therefore, both ports (Port A and Port B) may be active at the same time. The clocks for each port are CLKA and CLKB respectively. Since both ports may be active at the same time, the Power Management Mode entry Setup constraint would be determined by the early (1st) rising clock edge. E.g. if the Port B active cycle would have started first (CLKB is the early clock edge), then the Setup time is relative to the rising edge of the Port B clock (CLKB). If the separation between the two clock rising edges (CLKB to CLKA) is greater than the Setup plus Hold time, then the Power Management Mode Entry Hold time constraint is related to the early clock rising edge (CLKB in this example) and the later clock is ignored (since the memory will enter the power down mode). If the separation between the two rising clock edges is less than Setup plus Hold time, then the Power Management Mode Entry Hold time is related to the later clock edge (CLKA in this example).

# 17 When does Light Sleep make sense?

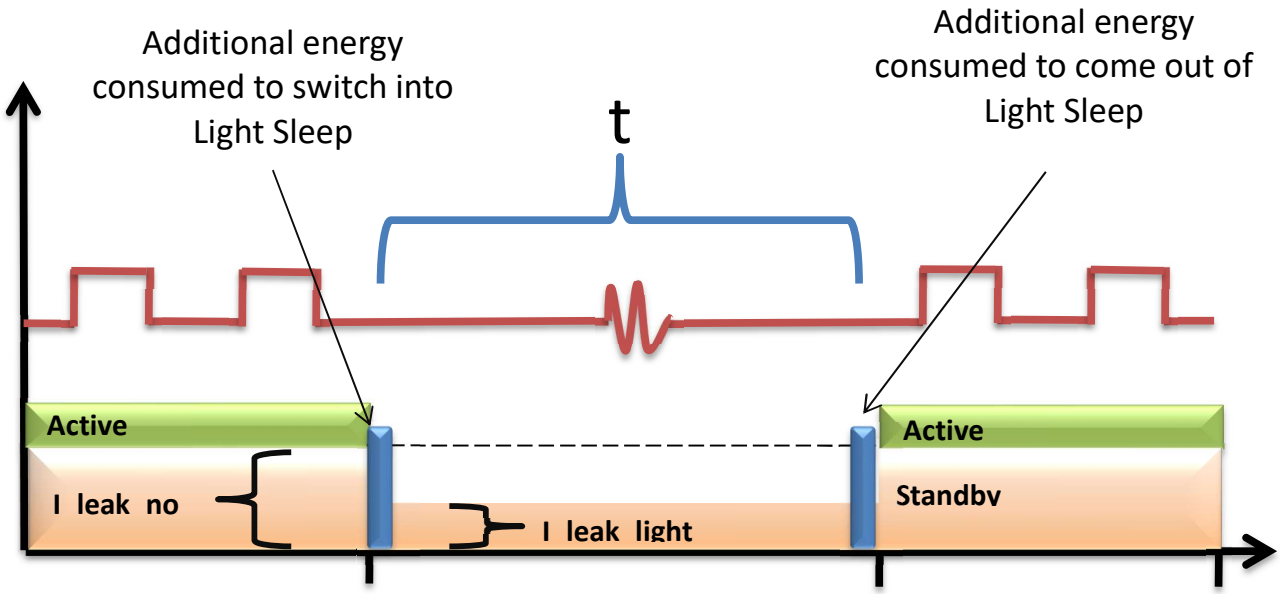



**Figure 7: Break-even Sleep Time**

**Break-even calculation:**

I_leak_normal = Leakage during normal mode

I_leak_light_sleep = Leakage during light sleep

$E_{LS}$ = Data sheet LS rise power + data sheet LS fall power

$t_{LSI}$ = Sum of going into LS and coming out of LS mode

t = Break-even time to be in light sleep

V * (I_leak_normal - I_leak_light_sleep) *( t – $t_{LSI}$) >= $E_{LS}$ OR

t>= ELS(Data sheet LS rise power + data sheet LS fall power)/ (V* (I_leak_normal – I_leak_light_sleep))

+ $t_{LSI}$

**Example calculations :**

| | |
|---|---|
| Compiler example | = HSSP |
| Bank | = 8 |
| Column Mux | = 16 |
| Number of Bits | = 32 |
| Number of Words | = 15872 |
| BIST | = true |
| Center decode | = true |

| | |
|---|---|
| memory_name | = "sasslsnh4m1p15872x32m16b8" |
| Power Gating | = false |
| PVT | = ff0p9v105c |
| Redundancy | = false |
| P_leak_normal = Leakage power during normal mode | = 12.84 mW |
| P_leak_light_sleep = Leakage power during light sleep | = 10.33 mW |
| $E_{LS}$ = Data sheet LS rise power + data sheet LS fall power | = 117.25 uW/Mhz |
| $t_{LSI}$ = Sum of going into LS and coming out of LS mode | = 0.599 ns |
| t = Break-even time to be in light sleep | = ? |

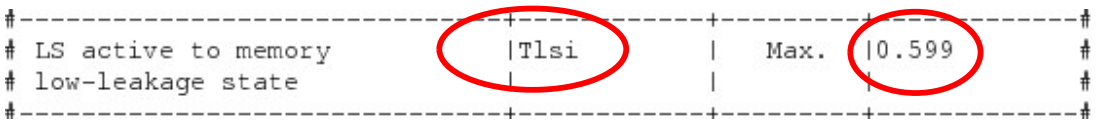
Leakage power during Normal mode and Light Sleep mode from liberty (in nW):

```
  leakage_power () {
    related_pg_pin : "VDD" ;
    when  : "!LS & !DS & !SD & BC1 & !BC2";
    value : 12843908.8006;
  }

 leakage_power () {
   related_pg_pin : "VDD" ;
   when  : "LS & !DS & !SD & BC1 & !BC2";
   value : 10335749.9221;
 }
```

Datasheet LS pin rise and fall power:

```
Power Control Pins Current
==========================

#======================+====================#
#  PVT corner          |    rfff0p9v105c    #
#======================+====================#
# Rise Power           |4.615e+01           #
# (uW/MHz) LS          |                    #
#----------------------+--------------------#
# Rise Current         |5.128e+01           #
# (uA/MHz) LS          |                    #
#----------------------+--------------------#
# Fall Power           |7.110e+01           #
# (uW/MHz) LS          |                    #
#----------------------+--------------------#
# Fall Current         |7.900e+01           #
# (uA/MHz) LS          |                    #
#----------------------+--------------------#
```

Sum of going into LS and coming out of LS mode - $T_{LSI}$ (in ns):



| LS active to memory low-leakage state | Tlsi | Max. | 0.599 |
|---|---|---|---|

t>= $E_{LS}$(Data sheet LS rise power + data sheet LS fall power)/ (V* (I_leak_normal – I_leak_light_sleep))

+ $t_{LSI}$

t>= (46.15+71.1)uW/Mhz / (12.84 - 10.33)mW + 0.599ns

t>= (117.25 x $10^{-3}$mW x $10^{-6}$s x $10^{9}$ns) / 2.51mW + 0.599ns

t>= 47.31ns

**Note:** These are not compiler values. This is just an example to show how user can calculate time.

# 18 Power Management with STAR Memory System

The power management mode pins (LS, DS, SD and POFF) are not controlled by the Synopsys STAR Memory System processor. The mode control pins are user accessible.

When using repairable memories, the user is responsible for managing the power supply to the redundancy reconfiguration registers (in the soft wrappers). If the voltage to these registers is removed, then the repair information stored in them will be lost and the user will need to reload the reconfiguration registers from the fuse bank. To minimize power management requirements, the user can select to have the reconfiguration registers be state retention registers (assuming state retention registers are available in the standard cell library being used).

# 19 ROM and HD2PRF

- In ROM and HD2PRF, some of the features are different
  - vdda_enable flag is not supported in ROM, hence there are no POFF pins. DS mode is not present for ROM.
  - In HD2PRF, array bias is not supported. BC0, BC1, BC2 are not supported. RM3A pin is for Write and is a reserved pin for future use. RM3A pin can be tied to low. RM3B pin is for Read function is to bypass keeper on bitline. Basically a debug mode. Recommendation for user is to have this pin as controllable.
  - In LS mode, leakage reduction is done using fine grained power gating, bitlines are floating and source biasing is not done in HD2PRF.

# 20 Back Bias Supply

The 22nm FDX (Fully Depleted Silicon-on-Insulator) technology provides improved speed, reduced power and a simpler manufacturing process compared to bulk silicon technologies. It delivers a good power/performance/cost tradeoff compared to both bulk and FinFET technologies, which has led to adoption in automotive, IoT and other applications.

22FDX enables control of the behavior of transistors not only through the gate, but also by polarizing the substrate underneath the device, similar to the body bias available in Bulk technology.

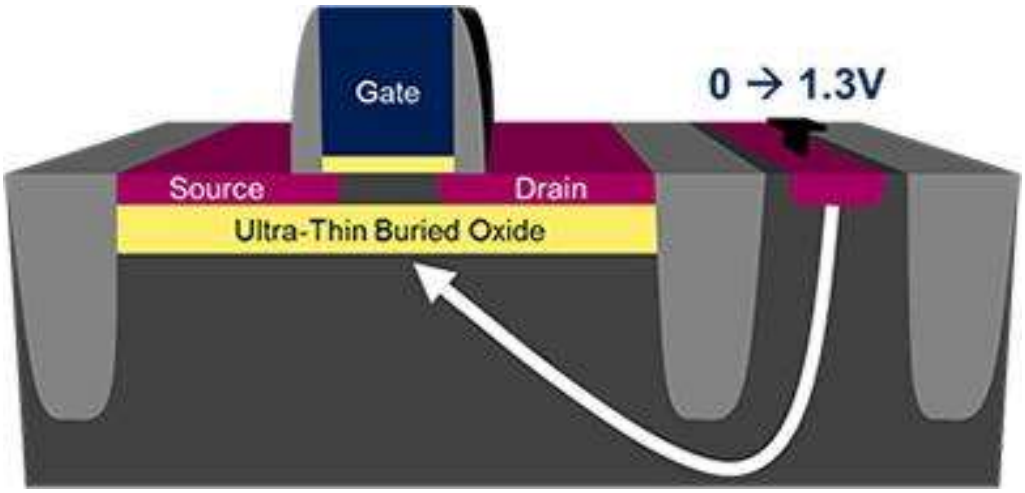



**Figure 8 Body Bias in 22FDX**

Body Biasing is much more efficient with minimal leakage impact in 22FDX due to transistor construction and its ultra-thin insulator layer. Also, the presence of the buried oxide allows the application of higher biasing voltages. Reverse Body Bias (RBB) reduces leakge, while Forward Body Bias (FBB) improves the performace.

The power supply pins VNW_N and VPW_P will be available at memory instance level to control back bias feature for memory, when the option “back_bias_enable” is set to 1. However, the bitcell devices are not applied with back bias.

Back bias supply can be changed independent of VDDA/VDDP for any functional / power down mode. There is no power up / down sequence requirement wrt to other supply voltages. The Operation of the Back bias is controlled by onchip sensors and biasing scheme.

The default value of the back bias is VNW_N=VPW_P=0. The value of the forward back bias can be changed according to the following allowed voltage range.

VNW_N: 0v ~ 1.2v
VPW_P: -1.5v ~ 0v

The supported PVT corners with back bias are listed in the table below.

| Domain | Process | Extraction Corner | Voltage (V) | Temp (C) | VBN [V] | VBP [V] |
|---|---|---|---|---|---|---|
| Deep Underdrive (0.5V) | SSG | FuncCmax | 0.45 | -40 | 1.20 | -1.50 |
| | SSG | FuncCmax | 0.45 | 125 | 0.60 | -0.85 |
| Underdrive (0.65V) | SSG | FuncCmax | 0.59 | -40 | 0.85 | -1.50 |
| | SSG | FuncCmax | 0.59 | 125 | 0.60 | -0.80 |
| Normal (0.8V) | SSG | FuncCmax | 0.72 | -40 | 0.70 | -1.50 |
| | SSG | FuncCmax | 0.72 | 125 | 0.60 | -1.00 |
| | SSG | FuncCmax | 0.72 | 150 | 0.60 | -0.85 |
| OverDrive (0.9V) | SSG | FuncCmax | 0.81 | -40 | 0.60 | -1.50 |
| | SSG | FuncCmax | 0.81 | 105 | 0.60 | -0.90 |

**Table 12 Bias Value Range**

# 21 FAQ

1) How often can the LS pin be toggled and how quickly do the RAMs enter or leave Light Sleep mode?

   The LS signal must meet the setup and hold time requirements listed in the datasheet and .lib files. The maximum toggle rate is once per clock cycle. The LS entry and exit times are listed in the memory instance datasheet and .lib files.

2) Can the LS pin be toggled on every cycle similar to the ME pin?

   Toggling LS every clock cycle may consume more power than leaving the memory powered up for a brief period. The LS signal must meet the setup and hold time requirements listed in the datasheet and .lib files.

3) Is it required to wait multiple cycles after the de-assertion of the LS pin before the RAM becomes fully functional again?

   The recovery time is not defined by a predetermined number of clock cycles. Refer to the memory compiler manual, memory instance datasheet, and .lib files for details on the recovery (exit) times for each memory type.

4) Does VDDF need to equal VDD in mission-mode i.e. functional mode?

   Not necessary

5) Would VDDF < VDD cause any problems in mission-mode?

   Yes, Leakage and Functional Issues, if VDDF < VDD.

6) What is the permissible tolerance on VDDF relative to VDD?

   VDDF >= VDD is supported.

7) After the memory exits SD Periphery Off Mode (POFF[1:0] from 11 to 00), will the ROP pin get high to indicate that the memory is ready for operation?

   No. ROP is used for SD mode only. It is not used for POFF[1:0] = 11. This is because with POFF, the external supply VDDP is being switched. Since the VDDP switches and it's ramp rate are external to the memories, memory cannot indicate when VDDP is ready. For memories, need to follow the timing Tfpoffp (VDD recovery with respect to Negedge POFF) and then POFF setup time before accessing the memory.

8) When VDDP and VDDA power up together, POFF[1:0]=11, is it ok? Will the large crow-bar current occur?

   POFF pins are on VDDA domain. So POFF = 11 cannot happen without VDDA supply being there. If VDDP and VDDA are being powered up, this is similar to a regular power up sequence where sequence of power ramp up should be VDDF -> VDDP -> VDDA.

9) When memory is in Periphery OFF mode (POFF=01/10/11), if VDDP is not removed, what is the status of Q? Is it X or not?

   Q will be X which means that output will be ambiguous/random. Output will not be floating/HiZ. However if VDDP is removed output will be floating/HiZ.

10) When memory is in Periphery OFF mode (POFF=01/10/11), if VDDP is not removed, is there any current induced by read and write command?

    No, there is no current induced by Read or Write command.