rilib_gf22dfx_io_EG1d80V

Racyics® 1.80V EG I/O-cell library in GLOBALFOUNDRIES 22FDX® (22nm FDSOI)

Application Note

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1 Introduction

This Application Note is about the Racyics® 1.80V EG I/O-cell library in GLOBALFOUNDRIES 22FDX® (22nm FDSOI)
It contains detailed information about the structure and concepts of this I/O cell library. This document provides the user with special hints and guidelines for deploying this IP.

2 Document Structure

2.1 Revision History

Rev	SVN	Date/Editor	Description
0.1		12/10/17, MD	initial version
0.2		07/02/18, MD	- add new cells VDDQ/04, VSSQ/04, RTERM_CAL, WELLFILTER - new Metal Stack Option supported
1.0		15/01/19, JS	New library structure for metal stacks, VT options added
1.0.1		18/12/19, JS	Clarification of ESD in VNW/VPW/VNWINT/VPWINT cells
1.0.2		2021/05/10 JS	Reflect changes in lib for lib release v1.0.17
1.1.0		2021/07/15 JS	New version number to match with lib release
1.2.0		2021/10/18 JS	Added 45° Corner cells, layout fixes

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2.2 Related Documents

- Product Sheet: riio_gf22fdx_eg1d80v_product_sheet

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2.6 Abbreviation

SSN	Simultaneous Switching Noise
HBM	Human Body Model
MM	Machine Model
CDM	Charged Device Model
LVDS	Low Voltage Differential Signalling
GPIO	general purpose input/output
PDK	Process Design Kit

3 General Information

IP-Name: Racyics® 1.80V EG I/O-cell library in in GLOBALFOUNDRIES 22FDX®
IP-Identifier: riio_gf22fdx_eg1d80v

Technology: GLOBALFOUNDRIES 22FDX®
PDK Version: pdk-22FDX-EXT_V1.0_2.1

BEOL options:
10M_2Mx_6Cx_2Ix_LB
10M_2Mx_5Cx_1Jx_2Qx_LB
9M_2Mx_5Cx_1Jx_1Ox_LB
9M_2Mx_3Cx_2Bx_1Ix_1Ox_LB
8M_2Mx_4Cx_2Ix_LB
8M_2Mx_4Cx_1Ix_1Ox_LB
more BEOL options on request

Available Contents:
- Verilog behavioral simulation model
- .lib/db timing and power models
- .lef layout abstract views
- .oa database (schematic, symbol, layout)
- GDSII files
- LVS netlists

4 IO Lib & Concepts

4.1 General Information

4.1.1 Overview

Common features
- cell-size 60µmx80µm (cell width x cell height)
- digital and analog I/O cells
- diverse supply cells for digital and analog cores, IOs
- specific supply cells to tap back-bias networks
- ESD 4kV HBM, 500V MM, 200V CDM
- -40°C to 125°C characterization corners
- Various bond pads for wire-bond.
- CUP (bond over active) and flip-chip on request.

Digital I/O
- a highly configurable GPIO cell
- configurable general-purpose input and output cells
- self-biased digital IOs and/or shared biasing with biasing reference cell
- core-logic portion of IO cells in 5 VT flavors to optimize both performance and leakage over a wide core voltage range from 0.4V to 0.9V nominal

High-Speed IO

- High-Speed (3 Gbps) LVDS cell
- Calibration cell for accurate on-die termination

Metal Stacks

The IO Library is available for a number of BEOL (metal stack) options.
Available and planned BEOL (metal stack) options:

Table 1 BEOL metal stacks for IO lib

BEOL	available for I/O Lib	planned / on request
10M_2Mx_6Cx_2Ix_LB. (LB thick)	X	
10M_2Mx_4Cx_2Bx_2Jx_LB. (LB thick, MRAM)		X
6M_2Mx_3Cx_1Ix_LB__VZ. (700nm LB thickness)		X
9M_2Mx_ 5Cx_1Jx_1Ox_LB. (LB thick)	X	
7M_2Mx_3Cx_1Ix_1Ox_LB. (LB thick)		X
7M_2Mx_4Cx_1Ix_LB. (LB thick)		X
8M_2Mx_4Cx_2Ix_LB. (LB thick)	X	
8M_2Mx_4Cx_1Ix_1Ox_LB. (LB thick)	X	
10M_2Mx_5Cx_1Jx_2Qx_LB. (LB thick)	X	
9M_2Mx_3Cx_2Bx_1Ix_1Ox_LB. (LB thick, MRAM)	X	
9M_2Mx_5Cx_2Ix_LB. (LB thick)		X
8M_2Mx_5Cx_1Ix_LB. (LB thick)		X

Mask Layers

Used devices and mask layers in all VT flavors

Devices	Mask Layers
eglvtnfet	HY, MY, NW, BF, N3, ZG, PG, GN, 3PL, TJ, BN, OP
eglvtpfet	
egslvtnfet	
egslvtpfet	
nfet	
pfet	
egncap	
ncap	
opnpcres	
vpnp	
esdegpdnw_poly	
esdegvnpn_poly	
esdnfet_soi	

Additional process options for digital I/O cells depending on core (SG) devices for VT flavour:

Library / VT Flavour	Devices	Additioal Mask Layers
RVT28 regular Vt 28nm gate length	nfet	*None*
	pfet	
HVT28 high Vt 28nm gate length	hvtnfet	XW, LW
	hvtpfet	
LLHVT28 low-leakage high Vt 28nm gate length	llhvtnfet	XW, LW
	llhvtpfet	
LVT28 low Vt 28nm gate length	lvtnfet	XW, LW
	lvtpfet	
SLVT28 super-low Vt 28nm gate length	slvtnfet	*None*
	slvtpfet	

Devices and mask layers for High-Speed differential IO RIIO_GF22FDX_HSIO_EG1D80V_<BEOL>

Devices	Mask Layers
apmom1v8	HY, MY, NW, BF, N3, XW, LW, ZG, PG, GN, 3PL, TJ, BN, OP
eglvtnfet	
eglvtpfet	
egncap	
egslvtnfet	
lvsres	
lvtnfet	
lvtpfet	
opnpcres	
slvtnfet	
slvtpfet	
esdegpdnw_poly	
esdegvnpn_poly	

4.2 Operation Conditions

Table 2 Operating conditions for characterization

Parameter	Description	Min	Nom	Max	Units
V_{VDD}	core supply	0.72	0.80	0.88	V
		0.54	0.60	0.66	
		0.45	0.50	0.55	
		0.40	0.45	0.50	
		0.34	0.40	0.44	
V_{VDDIO}	I/O supply	1.62	1.80	1.98	V
V_{PAD}	Signal pad voltage	0.00		V_{VDDIO}	V
T	temperature	-40		125	°C

4.3 Libraries Overview

The library is composed of several sub-libraries. All of them are available for a number of BEOL (metal stack) options. In the following table <BEOL> can be one of

- 10M_2Mx_6Cx_2Ix_LB
- 10M_2Mx_5Cx_1Jx_2Qx_LB
- 9M_2Mx_5Cx_1Jx_1Ox_LB
- 9M_2Mx_3Cx_2Bx_1Ix_1Ox_LB
- 8M_2Mx_4Cx_2Ix_LB
- 8M_2Mx_4Cx_1Ix_1Ox_LB.

Other metal stacks can be delivered upon request.

Table 3 Sub-Libraries

Sub-Library	Description
RIIO_GF22FDX_GPIO_EG1D80V_RVT28_<BEOL>	• General purpose digital I/O cells. Core side logic in several Vt flavours • Common biasing cell • Power-on-reset threshold
RIIO_GF22FDX_GPIO_EG1D80V_HVT28_<BEOL>	
RIIO_GF22FDX_GPIO_EG1D80V_LLHVT28_<BEOL>	
RIIO_GF22FDX_GPIO_EG1D80V_LVT28_<BEOL>	
RIIO_GF22FDX_GPIO_EG1D80V_SLVT28_<BEOL>	
RIIO_GF22FDX_BASEIO_EG1D80V_<BEOL>	• Supply • analog signal IO • supply rail cut cells • IO-filler, corner • Wire-bond pads
RIIO_GF22FDX_HSIO_EG1D80V_<BEOL>	• LVDS cell • Termination resistor calibration

4.4 Library Contents

4.4.1 Digital Signal I/O Cells

General purpose digital input, output and bidirectional cells are available with different Vt options in their core-side logic contents, according to the sub-libraries

- RIIO_GF22FDX_GPIO_EG1D80V_RVT28_<BEOL>
- RIIO_GF22FDX_GPIO_EG1D80V_HVT28_<BEOL>
- RIIO_GF22FDX_GPIO_EG1D80V_LLHVT28_<BEOL>
- RIIO_GF22FDX_GPIO_EG1D80V_LVT28_<BEOL>
- RIIO_GF22FDX_GPIO_EG1D80V_SLVT28_<BEOL>

Table 4 Digital Signal IO Pad Cells

cellname	nominal output drive strengths [mA]				open drain		slew control	current mode output	tri-state pad	pad state keeper	pull-up	pull-down	schmitt trigger	comment
	4	8	12	16	nmos	pmos								
RIIO_EG1D80V_GPIO_vto	x	x	x	x	x	x	x	x	x	x	x	x	x	**bidirectional** digital I/O cell
RIIO_EG1D80V_GPI_vto										x	x	x	x	digital **input** cell
RIIO_EG1D80V_GPI_PD_vto												x	x	digital **input** cell with pull-down
RIIO_EG1D80V_GPI_PU_vto											x		x	digital **input** cell with pull-up
RIIO_EG1D80V_GPO_vto	x	x	x	x	x	x	x	x	x					digital **output** cell
RIIO_EG1D80V_GPO_X040_vto	x				x	x		x	x					digital **output** cell with driver strength 4mA
RIIO_EG1D80V_GPO_X080_vto		x			x	x		x	x					digital **output** cell with driver strength 8mA
RIIO_EG1D80V_GPO_X120_vto			x		x	x	x	x	x					digital **output** cell with driver strength 12mA
RIIO_EG1D80V_GPO_X160_vto				x	x	x	x	x	x					digital **output** cell with driver strength 16mA
RIIO_EG1D80V_GPO_X160_vto				x	x	x	x	x	x					digital **output** cell with driver strength 16mA
RIIO_EG1D80V_POR_CORE_V0D3_vto														power-on-reset threshold detector 0.3V
RIIO_EG1D80V_POR_CORE_V0D5_vto														power-on-reset threshold detector 0.5V
RIIO_EG1D80V_BIAS_vto														common biasing reference generation

In the above table *vto* is a placeholder for a name component indicating Vt option and cell orientation. Cells are available in nearly all combinations, according to the following table:

Table 5 Vt Flavours available for digital signal IO cells

vto	RVT28_H	RVT28_V	HVT28_H	HVT28_V	LLHVT28_H	LLHVT28_V	LVT28_H	LVT28_V	SLVT28_H	SLVT28_V
cellname										
RIIO_EG1D80V_GPIO_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPI_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPI_PD_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPI_PU_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPO_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPO_X040_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPO_X080_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPO_X120_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPO_X160_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_GPO_X160_vto	x	x	x	x	x	x	x	x	x	x
RIIO_EG1D80V_POR_CORE_V0D3_vto	x	x	x	x	x	x				
RIIO_EG1D80V_POR_CORE_V0D5_vto	x	x	x	x	x	x				
RIIO_EG1D80V_BIAS_vto	x	x	x	x	x	x	x	x	x	x
orientation	horizontal	vertical	horizontal	vertical	horizontal	vertical	horizontal	vertical	horizontal	vertical

The full cell names are derived from the cellnames given above, with *vto* replaced by one of RVT28_H … SLVT28_V.

Digital outputs have optional slew rate limitation and current output modes. These modes can either use coarse internal biasing individual in each output cell. Alternatively, common biasing can be used, which requires one bias cell per output domain. The bias cell can be trimmed for higher accuracy.

4.4.2 Basic Cells for I/O

Basic cells include

- Supply cells for I/O domains, core-side logic of I/O cells and core
- Cut cells to separate different power domains
- Filler and corner cells
- Wire-bond pads

Table 6 Supply and Analog Signal IO Cells

cellname	VT option *vt*		orientation *hv*		voltage range	comment
Supply cells	RVT	HVT	H	V		
RIIO_EG1D80V_VDD_*vt_hv*	x	x	x	x	0.4 ... 0.8V	core supply (core side of IO plus core) with ESD RC clamp
RIIO_EG1D80V_VSS_*vt_hv*	x	x	x	x	0V	
RIIO_EG1D80V_VDD04_*hv*			x	x	0.4V	core supply (core side of IO plus core) with forward biased
RIIO_EG1D80V_VSS04_*hv*			x	x	0V	PN-diode as ESD clamp - 0.4V nominal only
RIIO_EG1D80V_VDDX_*vt_hv*	x	x	x	x	0.4 ... 0.8V	core supply (core area only) with ESD RC clamp and back-to-
RIIO_EG1D80V_VSSX_*vt_hv*	x	x	x	x	0V	back diodes VSSX to VSSIO
RIIO_EG1D80V_VDDX04_*hv*			x	x	0.4V	core supply (core area only) with forward biased PN-diode
RIIO_EG1D80V_VSSX04_*hv*			x	x	0V	as ESD clamp (0.4V only) and back-to-back diodes VSSX to
RIIO_EG1D80V_VDDQ_*vt_hv*	x	x	x	x	0.4 ... 0.8V	IO supply (IO side of IO plus core area) with ESD RC clamp
RIIO_EG1D80V_VSSQ_*vt_hv*	x	x	x	x	0V	
RIIO_EG1D80V_VDDQ04_*hv*			x	x	0.4V	IO supply (IO side of IO plus core area) with forward biased
RIIO_EG1D80V_VSSQ04_*hv*			x	x	0V	PN-diode as ESD clamp - 0.4V nominal only
RIIO_EG1D80V_VDDIO_*hv*			x	x	1.8V	IO supply (IO side of IO plus core area) with ESD RC clamp
RIIO_EG1D80V_VSSIO_*hv*			x	x	0V	
RIIO_EG1D80V_VDDIOX_*hv*			x	x	1.8V	IO supply (core area only) with ESD RC clamp
RIIO_EG1D80V_VSSIOX_*hv*			x	x	0V	
RIIO_EG1D80V_VNW_*hv*			x	x	-0.2 ... 3.6 V	N-well back bias networt tap with reduced ESD protection
RIIO_EG1D80V_VNWINT_*vt_hv*	x	x	x	x		N-well back bias networt tap **without ESD** protection for VNW. Additional ESD RC clamp on VDD/VSS
RIIO_EG1D80V_VPW_*hv*			x	x	-3.6V ... 0.2V	P-well back bias networt tap with reduced ESD protection
RIIO_EG1D80V_VPWINT_*vt_hv*	x	x	x	x		P-well back bias networt tap **without ESD** protection for VPW. Additional ESD RC clamp on VDD/VSS
Analog I/O Cells						
RIIO_EG1D80V_ANAIO_*hv*			x	x	see text	analog signal, with ESD resistor and ESD diodes to IO voltage
RIIO_EG1D80V_ANACORE_*hv*			x	x	see text	analog signal, with ESD resistor and ESD diodes to core voltag
RIIO_EG1D80V_VSUP_IO_GND_*hv*			x	x	see text	analog signal or core circuit supply, only primary ESD protective diodes to IO voltage rails
RIIO_EG1D80V_VSUP_IO_PWR_*hv*			x	x	see text	
RIIO_EG1D80V_VSUP_IO_SIG_*hv*			x	x	see text	
RIIO_EG1D80V_VSUP_CORE_GND_*hv*			x	x	see text	analog signal or core circuit supply, only primary ESD protective diodes to core voltage rails
RIIO_EG1D80V_VSUP_CORE_PWR_*hv*			x	x	see text	
RIIO_EG1D80V_VSUP_CORE_SIG_*hv*			x	x	see text	

Analog IO signal pad cells provide ESD protection. Full ESD protection for input and output is achieved with the ANAIO and ANACORE pad cells. They contain primary ESD protective diodes, an ESD resistor and secondary ESD protective diodes. Return paths are either the IO voltage rails VDDIO/VSSIO or core voltage rails VDD/VSS within the IO ring.

Supply cells provide an ESD discharge path from either VDD to VSS or VDDIO to VSSIO or VDDX to VSSX or VDDIOX to VSSIOX, respectively, by means of RC-triggered active

clamps. For the core voltages VDD and VDDX, the clamps are available with RVT devices to save masks, and with HVT devices for leakage reduction.

Table 7 Filler and Corner Cells

cellname	orientation *hv*		comment
Filler cells	H	V	
RIIO_EG1D80V_FILL1_*hv*	x	x	IO filler cell 1µm
RIIO_EG1D80V_FILL2_*hv*	x	x	IO filler cell 2µm
RIIO_EG1D80V_FILL4_*hv*	x	x	IO filler cell 4µm
RIIO_EG1D80V_FILL8_*hv*	x	x	IO filler cell 8µm
RIIO_EG1D80V_FILL16_*hv*	x	x	IO filler cell 16µm
RIIO_EG1D80V_FILL32_*hv*	x	x	IO filler cell 32µm
RIIO_EG1D80V_FILL16B2B_*hv*	x	x	IO filler cell 16µm, with additional back-to-back diodes VSS <-> VSSIO
Corner cells			
RIIO_EG1D80V_CORNER_RVT	*none*		Corner cell with ESD RC clamp on VDD/VSS core voltage rails
RIIO_EG1D80V_CORNER_HVT	*none*		Corner cell with low-leakage ESD RC clamp on VDD/VSS core voltage rails
RIIO_EG1D80V_CORNER_EG	*none*		Corner cell with ESD RC clamp on VDDIO/VSSIO IO voltage rails
RIIO_EG1D80V_CORNER_45	*none*		45° Corner cell back-to-back diodes between VSSIO and VSS rails

Corner and filler selection w.r.t. ESD protection:
Corner cells with names ending on RVT, HVT and EG contain ESD clamp circuits providing additional discharge paths between VDD and VSS (RVT, HVT) or VDDIO and VSSIO (EG). Depending on the number of VDD/VSS pairs as well as VDDIO/VSSIO pairs and their distances in the IO ring, appropriate corner cells can improve ESD robustness by providing additional parallel discharge paths for ESD events.
The 45° beveled corner cell is targeted to flip chip designs allowing the IO ring to be closer to the chip edge, than what is possible with the full corner cells. See Figure 1 and Figure 2 for placement.

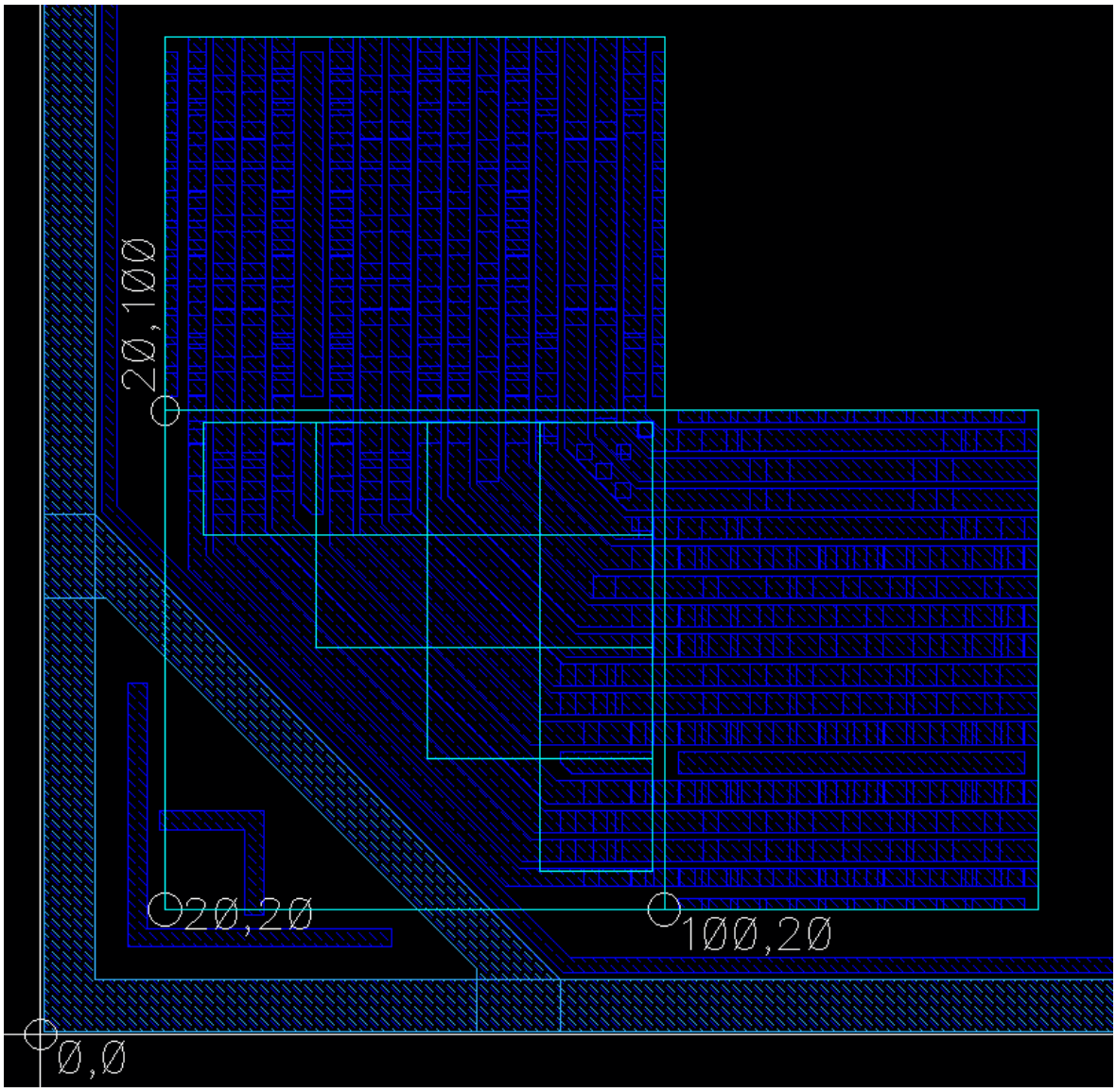


Figure 1 CORNER_45 placement with narrow crack stop

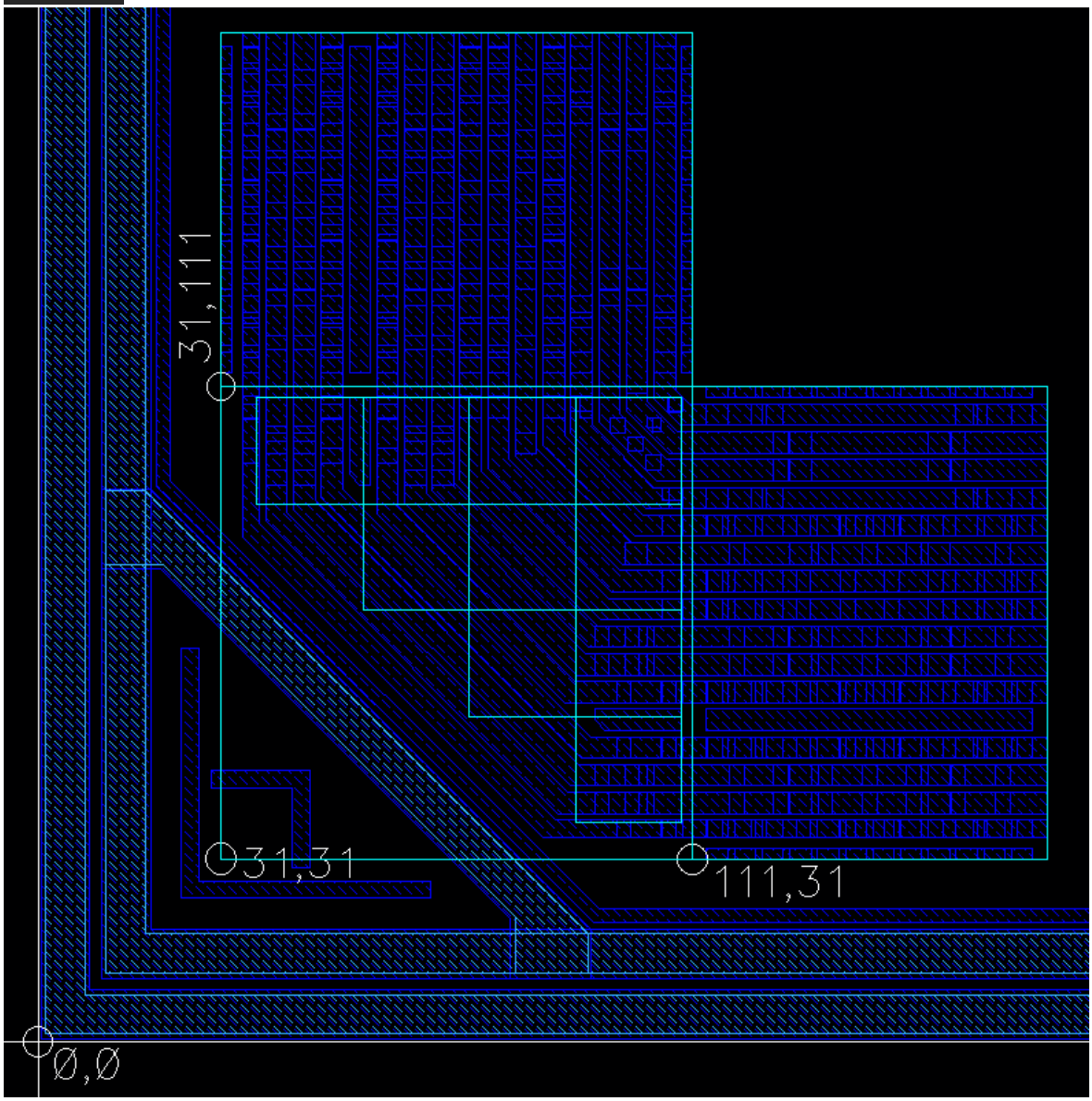


Figure 2 CORNER_45 placement with narrow wide stop

4.4.3 Bond-pad, Bumps and Probe Cells

Wire bond pads are available in a few sizes for inline as well as 2-row staggered arrangements. The following figure gives an overview.

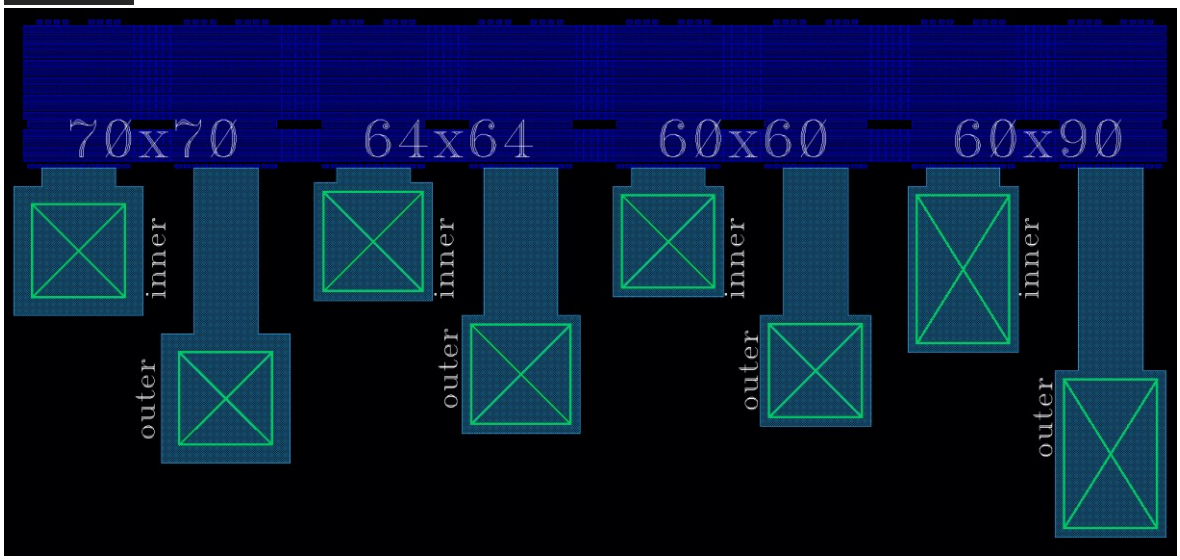


Figure 3 Wire bond pad types layout overview

Bond pad names have the following structure: RIIO_BOND*size*_*row*_*signal*, where *size*, *row* and *signal* can be combined from the following table:

Table 8 Wire Bond Pads

bond pad name *size* component	**comment**
RIIO_BOND**60**_*row* _*signal*	60µm x 60µm bond pad, 50µm x 50µm passivation opening
RIIO_BOND**64**_*row* _*signal*	64µm x 64µm bond pad, 54µm x 54µm passivation opening
RIIO_BOND**70**_*row* _*signal*	70µm x 70µm bond pad, **50**µm x **50**µm passivation opening
RIIO_BOND**60x90**_*row* _*signal*	60µm x 90µm bond pad, 50µm x 80µm passivation opening
bond pad name *row* component	**comment**
RIIO_BOND*size* _**INNER**_*signal*	inline or inner row staggered, 10µm collar
RIIO_BOND*size* _**OUTER**_*signal*	outer row staggered, collar fits inner row pad size
RIIO_BOND*size* _**PLAIN**_*signal*	inline, no collar
bond pad name *signal* component	**comment**
RIIO_BOND*size* _*row* _**SIG**	signal pad, no ESD checking label
RIIO_BOND*size* _*row* _**PWR**	supply pad, ESD checking label ESD_LC_POWER_GND
RIIO_BOND*size* _*row* _**GND**	ground pad, ESD checking label ESD_LC_POWER_GND
RIIO_BOND*size* _*row* _**SIG_CESD**	signal pad, CUSTOM_ESD label
RIIO_BOND*size* _*row* _**PWR_CESD**	supply pad, CUSTOM_ESD label
RIIO_BOND*size* _*row* _**GND_CESD**	ground pad,CUSTOM_ESD label

4.5 Cell Sizes

The tables below summarize the sizes of all cells. Please note the Figure 4 for definition of cell width and height.

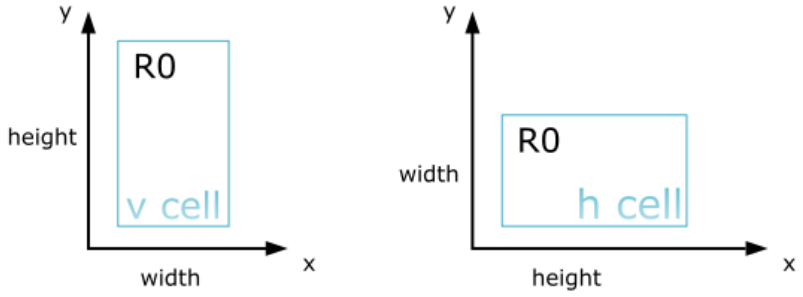


Figure 4 definition for cell size

General I/O cell size is 60µm x 80µm.
Filler cells have a height of 80µm and widths as given in Table 7.
The High-Speed LVDS cell is 180µm x 80µm.

4.6 Cell Layout Structure (Rail Scheme)

4.6.1 Cell Orientation

GLOBALFOUNDRIES 22FDX® technology requires fixed orientation of poly (GT.C.1).
In Racyics® IO Lib IP the gate width direction is aligned along the Y axis (i.e. vertical gate).
Consequently, IO cells are non-rotatable and every cell type exist in two orientations.

Vertical Orientation

IO-Cell (PADCELLS) name ends with <*cellname*>**_V**
60x80

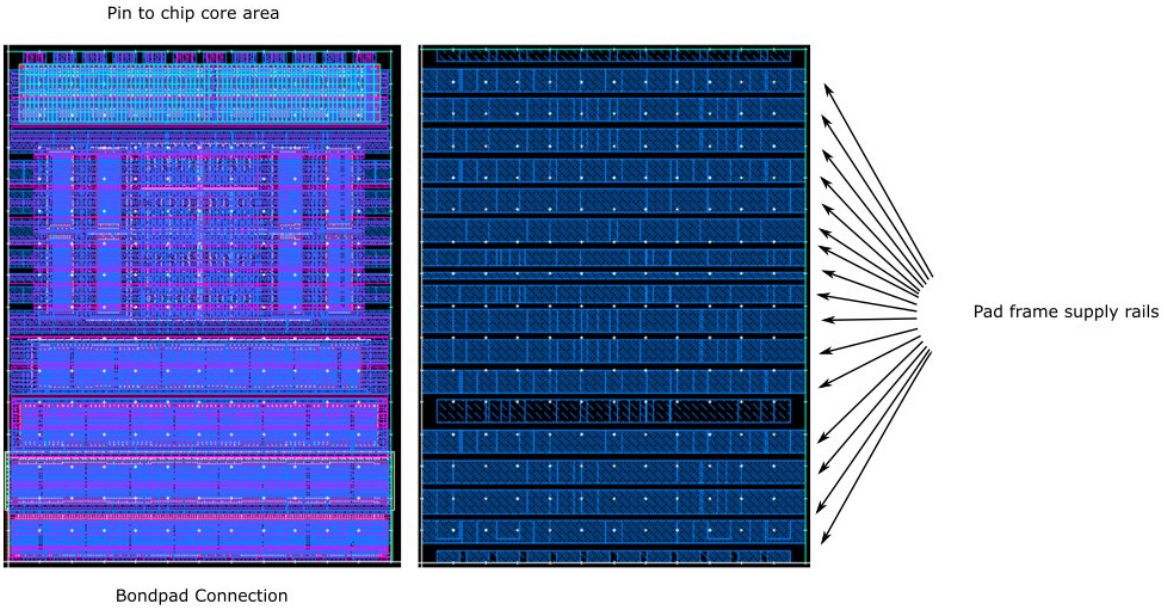


Figure 5 Screenshot of an I/O Cell with vertical orientation

Horizontal Orientation

Cell name ends with <*cellname*>**_H**
80x60

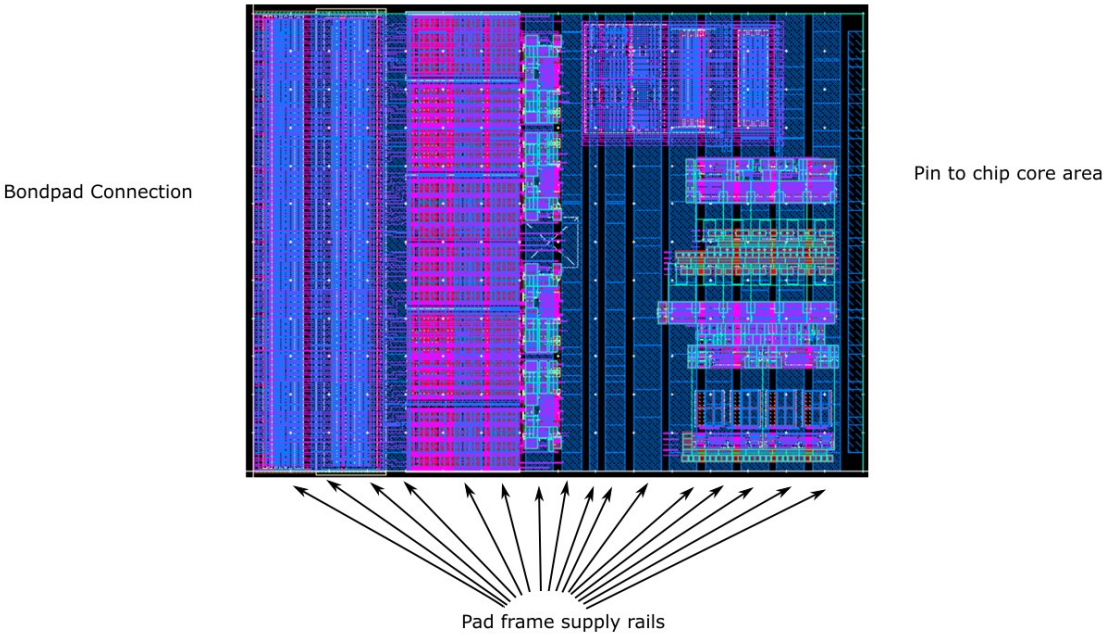


Figure 6 Screenshot of an I/O Cell with horizontal orientation

Sub-cell name endings correspond with the related top cell name endings.
The table below summarize all layers that have a fixed or preferred orientation.

Layer	Vertical Cell Orientation	Horizontal Cell Orientation
	Preferred / Fixed Layer Orientation	
GC	Y (vertical)	Y (vertical)
M1	free	free
M2	free / X (horizontal)	free / X (horizontal)
C1	Y (vertical)	Y (vertical)
C2	X (horizontal)	X (horizontal)
C3	Y (vertical)	Y (vertical)
C4	X (horizontal)	Y (vertical)
C5	Y (vertical)	X (horizontal)
JA	X (horizontal)	Y (vertical)
OI	Y (vertical)	X (horizontal)

Starting from metal layer C4, the metal orientation follows the I/O ring rails.

4.7 I/O Concept (I/O Cell Structure)

4.7.1 GPIO Concept

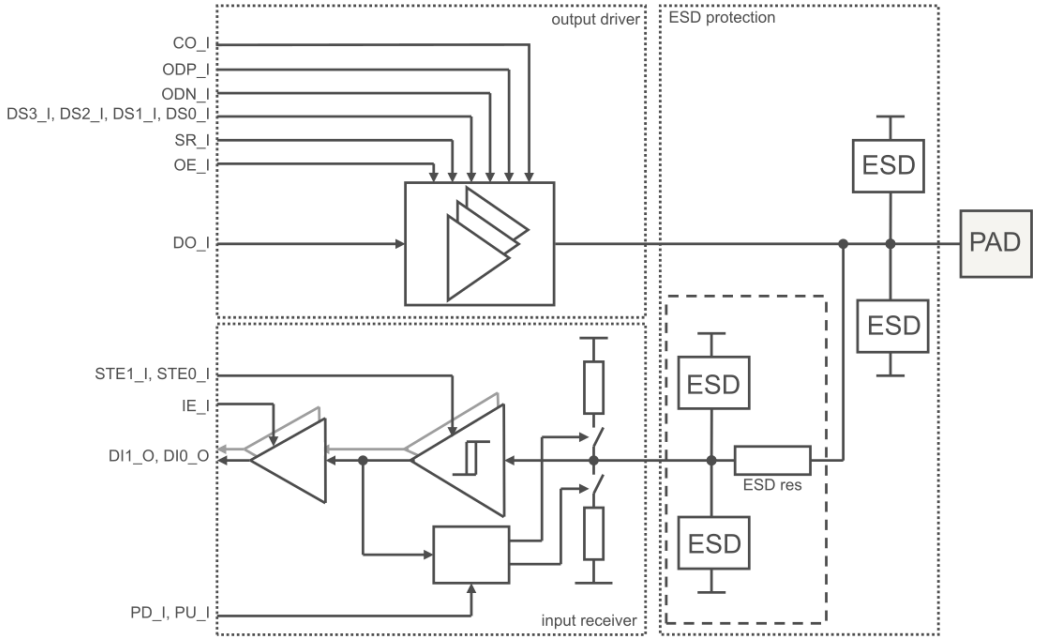


Figure 7 Block level schematic of the digital I/O cell

The GPIO Cell including different setting options, that allow the use in a wide field of use case scenarios.
Output-only GPO cells follow the same concept, but have no input receiver and no secondary ESD protection.
Input-only GPI cells follow the same concept, but have no output driver.

Pin List
OUT: pin connected to the output path within the cell, IN: input path within the cell
Pin direction: *_I input to the pad cell, *_O output from the pad cell.
For pin direction see also standard formats of the library.

Pin/Bus Name	Description	Recom. Setting
DO_I	**OUT: Data input from core to drive PAD**	
OE_I	**OUT: Active-high output enable. 0=High-Z at PAD**	
DS_I[3:2]	OUT: Drive Strength Selection	2'b10
DS_I[1:0]	OUT: Bias Selection to modifiy drive strength 0=internal/no BIAS cell, +/- 30% drive strength tolerance 1..3=tighter tolerance, needs BIAS cell 1=50%, 2=100%, 3=125% of nominal drive strength	2'b00
SR_I	OUT: 1=Slew-Rate limitation, 0=no slew rate limitation	1'b1
CO_I	OUT: 1=constant current output, 0=voltage output	1'b0
ODN_I	OUT: 1=open drain output N-FET, 0=PMOS push	1'b0
ODP_I	OUT: 1=open drain output P-FET, 0=NMOS pull	1'b0

DI_O[1]	**IN: core-side output received from PAD, higher thresholds**	**open**
DI_O[0]	**IN: core-side output received from PAD, lower thresholds**	**use this**
IE_I	IN: high-active input enable. 0→DI_O=2'b00	1'b1
STE_I[1:0]	IN: Schmitt-Trigger setting. See Figure 8 and table	*2'b00**
PD_I	IN: high-active enable for pull-down at PAD	1'b0
PU_I	IN: high-active enable for pull-up at PAD	1'b0

DI_O[1:0] provide parallel inputs with different switching levels. For general purpose signals the lower thresholds at DI_O[0] are more appropriate in many situations.
The parallel inputs can be combined in core logic, e.g. to implement a wider hysteresis with a RS-FF.

* Schmitt-Trigger Setting: There is no general rule whether Schmitt-Trigger input or input without hysteresis is appropriate for an input signal.

Pull-Up and Pull-Down can be activated together, creating a weak keeper for the PAD signal: pulling down while the received input is low and pulling up while the received input is high.

Output driver

The output driver of the GPIO cell has 9 config signals.

- OE_I Output enable high active enable. Pad is at high-impedance of OE_I=0.

Driver Strengths – Output Stage

- Signals: DS_I<3:2>

There are four different output driver strength available.
The output driver stage is present four times.

DS_I<3>	DS_I<2>	Drive Strength	Unit
0	0	4	mA
0	1	8	
1	0	12	
1	1	16	

Drive Strengths - Bias

- Signals: DS_I<1:0>

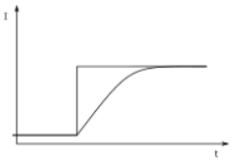
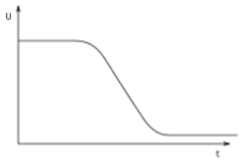
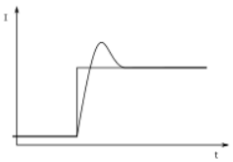
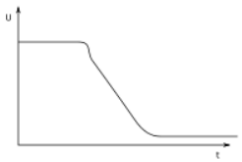
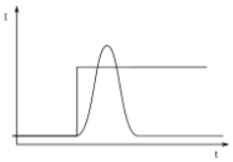
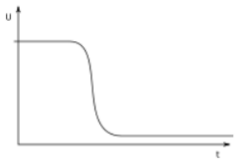
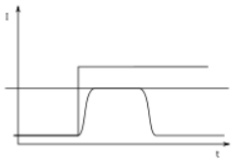
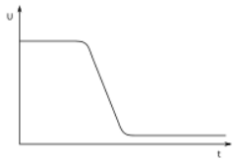
Drive strength and current mode output derive their current intensities from a biasing which can be either self-biasing within the GPIO or GPO cell, or can be provided as common biasing from the BIAS cell. Common biasing has a higher accuracy and can be trimmed to compensate process variations. Common biasing requires one BIAS cell per IO frame segment with continuous IO ground (VSSIO) rail. GPO and GPIO cells configured to use common biasing exhibit an additional static power dissipation, with approx. 40µA from VDDIO.

DS_I<1>	DS_I<0>	Description
0	0	internal self-biasing
0	1	common biasing, 50 % of nominal current
1	0	common biasing, 100% of nominal current
1	1	common biasing, 125% of nominal current

Output Modes

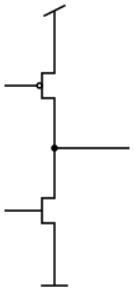
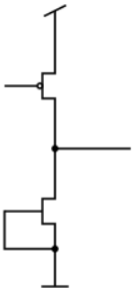
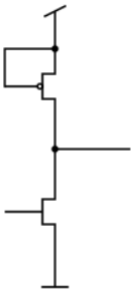
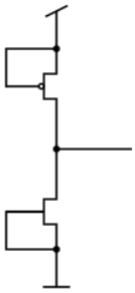
- Signals: CO_I, SR_I

CO_I=1 selects current output mode, i.e. the data pin DO_I controls output current.
CO_I=0 selects voltage output mode, i.e. the data pin DO_I controls output voltage.
SR_I=1 selects slew-rate controlled operation, i.e. current or voltage rises only gradually.
SR_I=0 de-selects slew-rate control, i.e. current or voltage rise as quick as the selected driver strength and load at the pad allow.

CO	SR	description	DO_I and typical current waveform	typical voltage waveform
1	1	current output with slew rate control		
1	0	current output without slew rate control		
0	0	voltage output without slew rate control		
0	1	voltage output with slew rate control		

Open Drain for NMOS and PMOS

- Signals: ODN_I, ODP_I

ODN \ ODP	0	1
0	 Tri-State	 Open Drain PMOS
1	 Open Drain NMOS	 High Impedance Output Z

ODP_I and ODN_I are recommended as static configuration inputs. It is not recommended to use ODN_I and ODP_I inputs to actively switch between high-impedance (Z) state and active output states, as timing is not guarantied for those paths.
OE_I is recommended to be used for active tri-state control in operation.

Input Receiver

The input receiver of the GPIO cell has 5 config signals.

- IE_I Input enable
  IE_I=0 → DI_O[1:0]=2'b00
  IE_I=1 → DI_O[1:0]={PAD,PAD}

Schmitt Trigger

- Signals: STE_I<1:0>

The input receiver includes two Schmitt triggers in parallel, connected to core-side data outputs DI_O[1] and DI_O[0].
Threshold levels of the two Schmitt triggers can be selected commonly with STE_I<1:0>. Both Schmitt-triggers are off when both STE_I<1:0>=0.

Schmitt trigger	core signal	config setting		Threshold			
		STE_I<1>	STE_I<0>	V_{IL} vddio → 0	V_{IH} 0 → vddio	I[µA]	
V1D00	DI_O<1>	1	0|1	0.846	1.35	91	86
		0	1	0.990	1.134	51	56
		0	0	1.026		~ 43	
V0D75	DI_O<0>	1	0|1	0.414	0.990	69	75
		0	1	0.594	0.882	54	47
		0	0	0.774		~ 36	

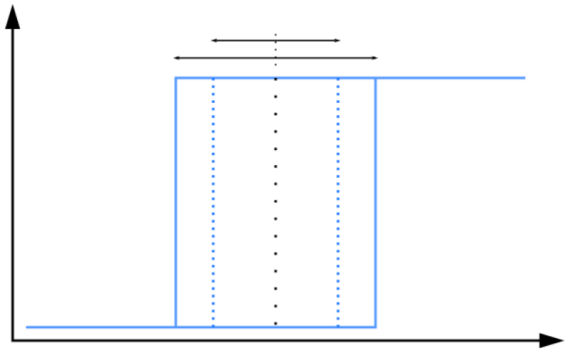


Figure 8 Schmitt trigger with three different options for thresholds

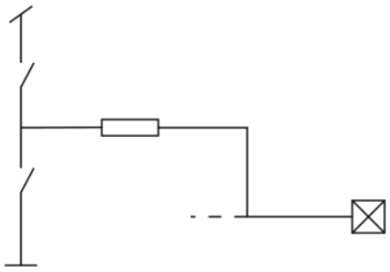
Core-side data outputs DI_O<1> and DI_O<0> can be combined in the core logic for further processing.

Pull-up and pull-down Resistor

- Signals: PU_I, PD_I
  PU_I=1 enables the pull-up path at the pad connection.
  PD_I=1 enables the pull-down path at the pad connection.

  Pad signal keeper
  When PU_I=1 and PD_I=1, the pull-up and pull-down paths are controlled by the received input data signal, such that a signal-keeper function is achieved at the pad connection. When the pad voltage is low, the pull-down path is activated and kept active until the pad voltage exceeds the high threshold V_{IH} of the V1D00 Schmitt-trigger. When the pad voltage is high, the pull-up path is activated and kept active until the pad voltage falls below the low threshold V_{IL} of the V0D75 Schmitt-trigger.

Resistance of the pull-up and pull-down paths is approximately 60kΩ.



PU_I	PD_I	Description
0	0	pull resistance disabled
0	1	pull-down
1	0	pull-up
1	1	keeper (data dependent pull-up/pull-down keeper)

4.7.2 Analog I/O Cell Concept

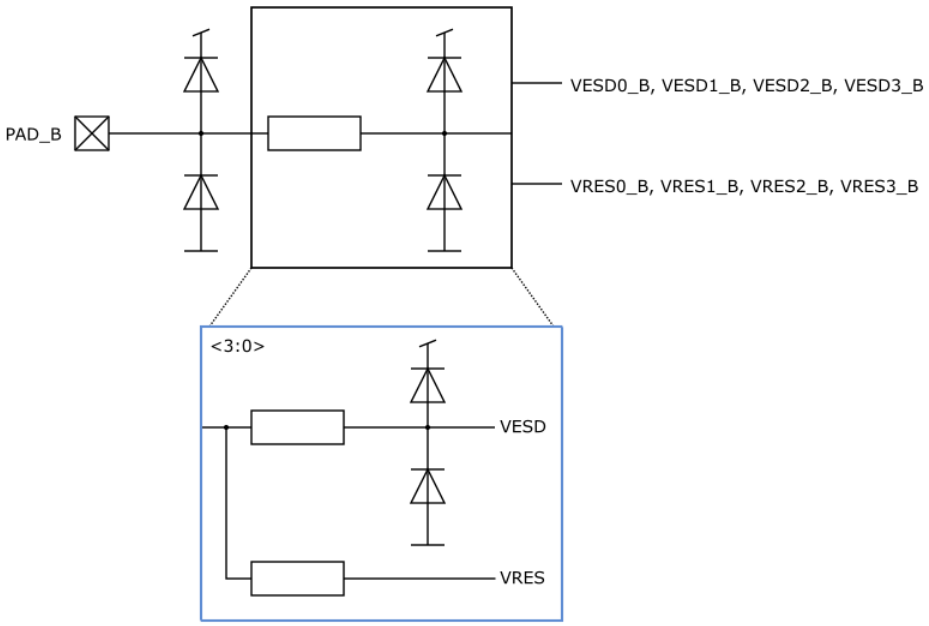


Figure 9 Block level schematic of analog I/O Cell

The analog I/O cells include primary and secondary ESD protection. Secondary ESD protection is split in four identical paths, each including one 400 Ohms resistor and an individual pin VESD0_B…VESD3_B at the core side. Additionally, four more instances of the 400 Ohms are accessible at the core side through pins VRES0_B…VRES3_B.
The eight core-side signal VESD0_B…VESD3_B and VRE0_B…VRES3_B can be combined arbitrarily (e.g. connected in parallel) to yield various resistance values and ESD protection levels.

Signal Combination	Description
VRES	400 Ohms, primary ESD protection only
VRES0 || VRES1	200 Ohms, primary ESD protection only
VRES0 || VRES1 || VRES2 || VRES3	100 Ohms, primary ESD protection only
VESD	400 Ohms with full ESD protection
…	
VRES0 || VRES1 || VRES2 || VRES3 || VESD0 || VESD1 || VESD2 || VESD3	50 Ohm with primary and reduced secondary ESD protection

4.7.3 BIAS Cell Concept

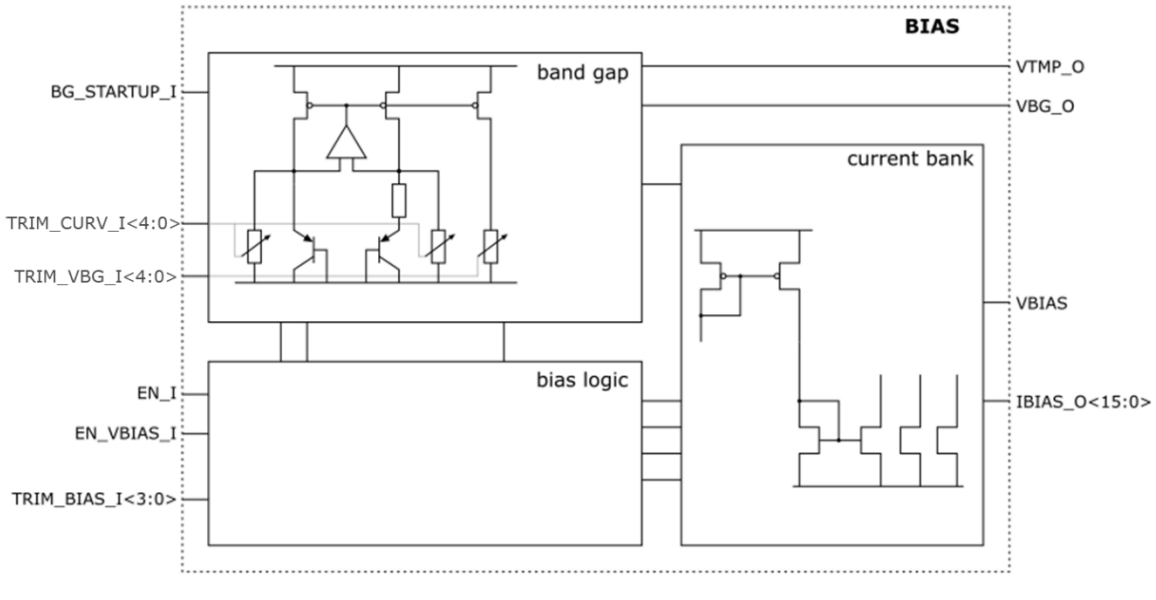


Figure 10 BIAS cell structure

Common biasing of digital signal IO cells requires one instance of the BIAS cell, see section 4.4.1.
The BIAS cell provides these signals:

- VBIAS signal in supply/ground rails of the IO frame
- Bandgap-Reference voltage of 1.0V
- Temperature-Voltage with approx. -2mV/K temperature coefficient
- 16 bias current outputs for analog core circuits

A wire bond pad can be connected to the BIAS cell. It connects to the VSSIO power rail without ESD protection.

The BIAS cell allows trimming with two 5-bit signals, TRIM_CURV_I<4:0> and TRIM_VBG_I<4:0> for adjusting the band gap voltage and its temperature dependency.

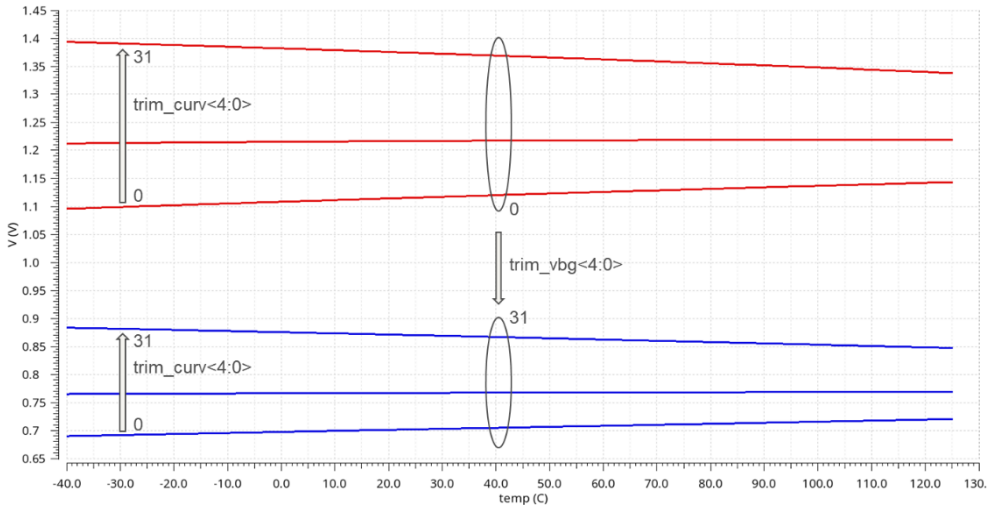


Figure 11 BIAS cell bandgap reference trimming overview

The binary coded signal TRIM_BIAS_I<3:0> allows to adjust the bias current as well as to scale the GPIO and GPO output drive strength.

BIAS_I<3:0>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
current @ BIAS_O [µA]	0	2.0	2.2	2.4	2.6	2.8	3.2	3.4	3.6	3.8	4.0	4.4	4.6	4.8	5.0	5.2
PAD drive strength [%]	off	40	44	48	52	56	64	68	72	76	80	88	92	96	100	104

Other input signals of the BIAS cell:

- EN_I – high active enable (core voltage)
- EN_VBIAS – high active enable for generation of common biasing and bias current outputs
- BG_STARTUP_I – force activation of the auto-startup circuit. For test only. Keep at core VSS in normal operation.

4.7.4 Back Bias Tap Cells

Tap cells for N-well and P-well back bias nets support body-bias voltages from -3.6 to +0.2V for p-well and -0.2V to +3.6V for n-well.
The RIIO_EXTRA_WELLFILTER cell can additional placed at the core side of the back-bias tap cells. An additional resistor improves ESD robustness and helps to filter back bias ripple (see Figure 12).

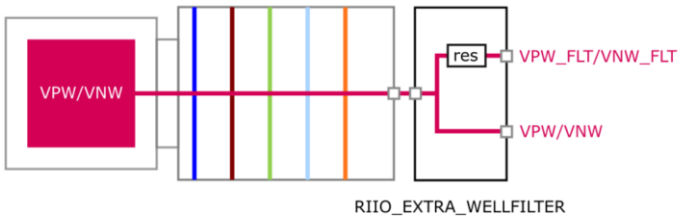


Figure 12 VPW or VNW cell with RIIO_EXTRA_WELLFILTER cell

4.7.5 Auxiliary Cells

Corner Cell

The IO cell library contains three corner cells. Corner cells contain ESD RC clamps, see Table 7.
This corner cell can optionally connect to wire bond pads (see Figure 13) for VDDIO and VSSIO. The corner cell can be flipped N/S and E/W but cannot be rotated because of the poly orientation. Therefore, the additional VDDIO bon pad is always at the north and south side and the additional VSSIO bond pad is always at the west and east side of the chip area.

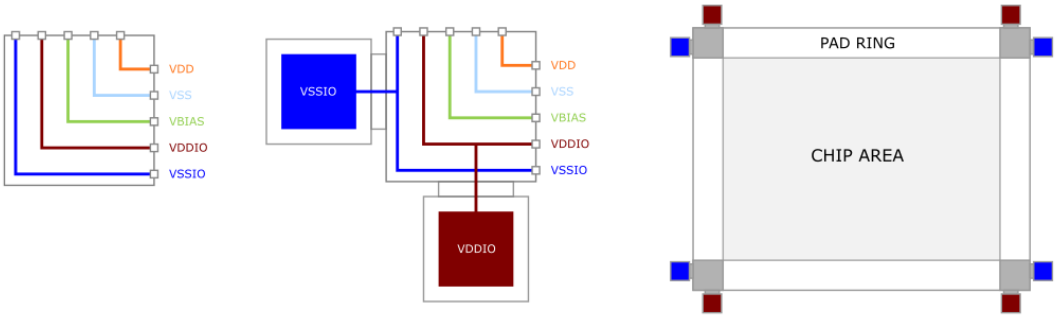


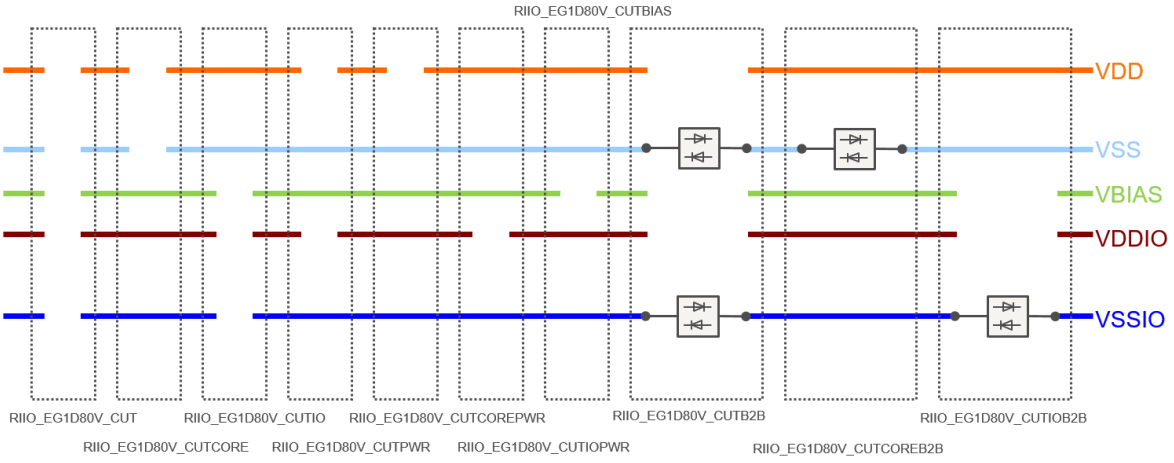
Figure 13 Corner cell

Filler Cells

The I/O cell library supports 6 different sizes of filler. The filler cells from size 8 and larger contain VDDIO/VSSIO decoupling caps. The last number in the cell naming corresponds to the cell width. All filler cells are available in vertical and horizontal orientation.

Cut Cells

The I/O cell library supports 10 different cut cells in both orientations. Cut cells are 4 µm wide, cut cells with back-to-back diodes (B2B) are 16µm wide.



4.8 ESD Protection Concept

ESD paths are provided through RC Clamps, Back2Back diodes and free-wheeling diodes. Figure 14 to Figure 19 illustrate the ESD concept.

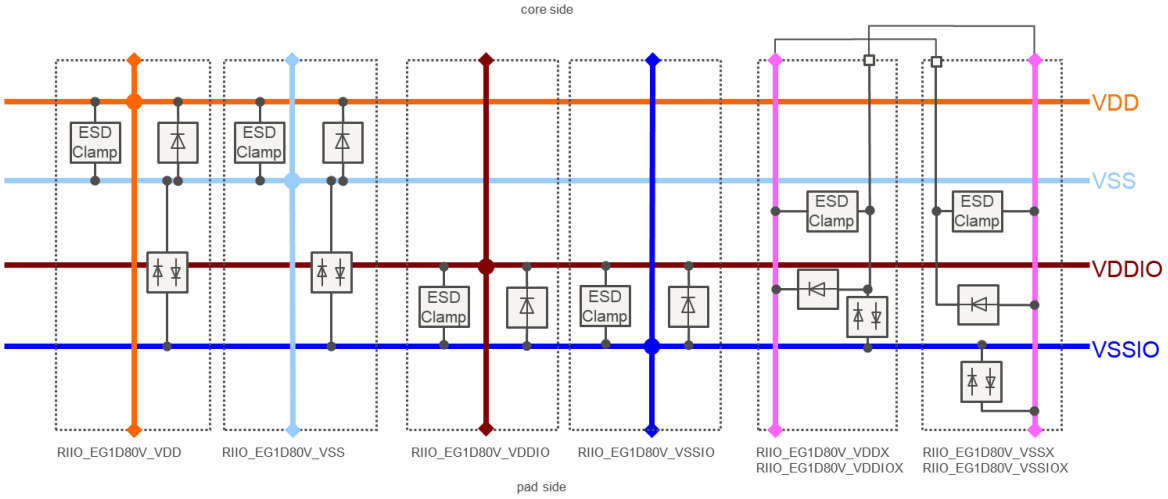


Figure 14 ESD Clamp Scheme Part 1

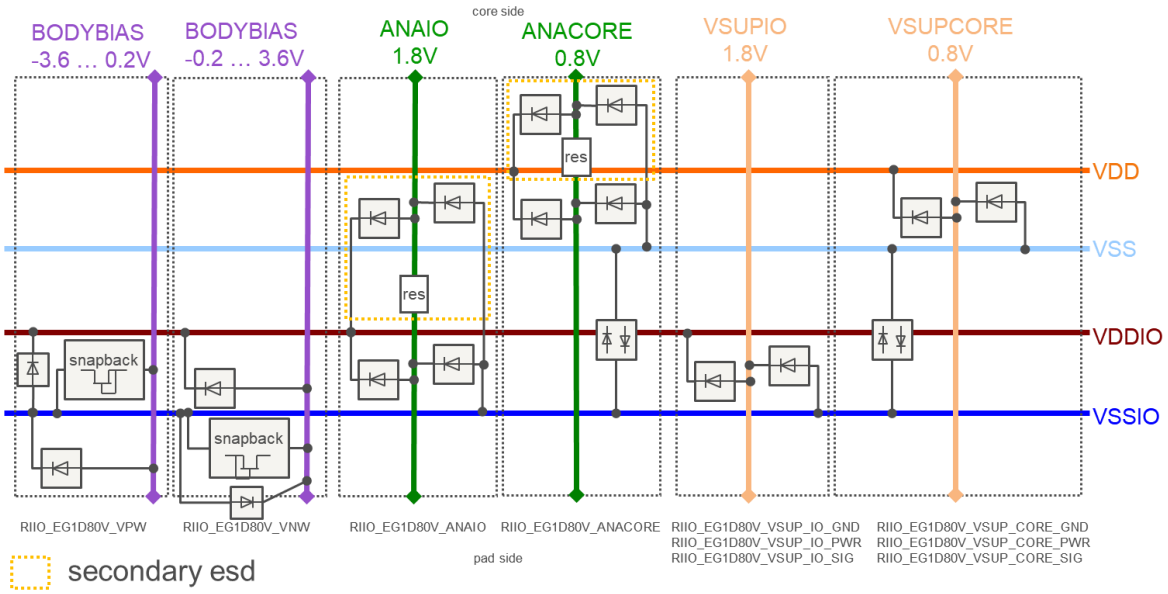


Figure 15 ESD Clamp Scheme Part 2

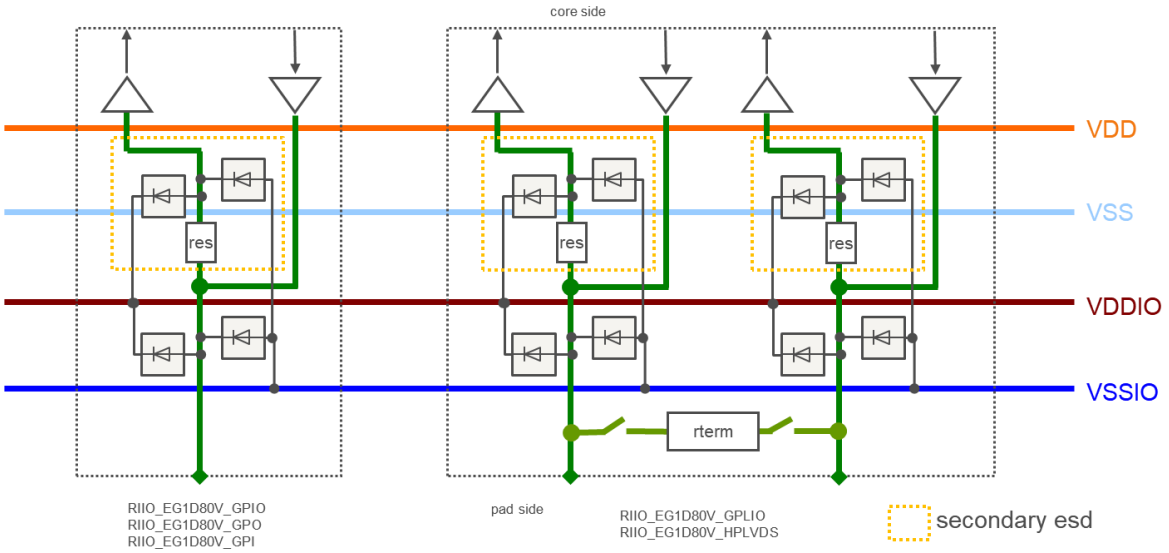


Figure 16 ESD Clamp Scheme Part 3

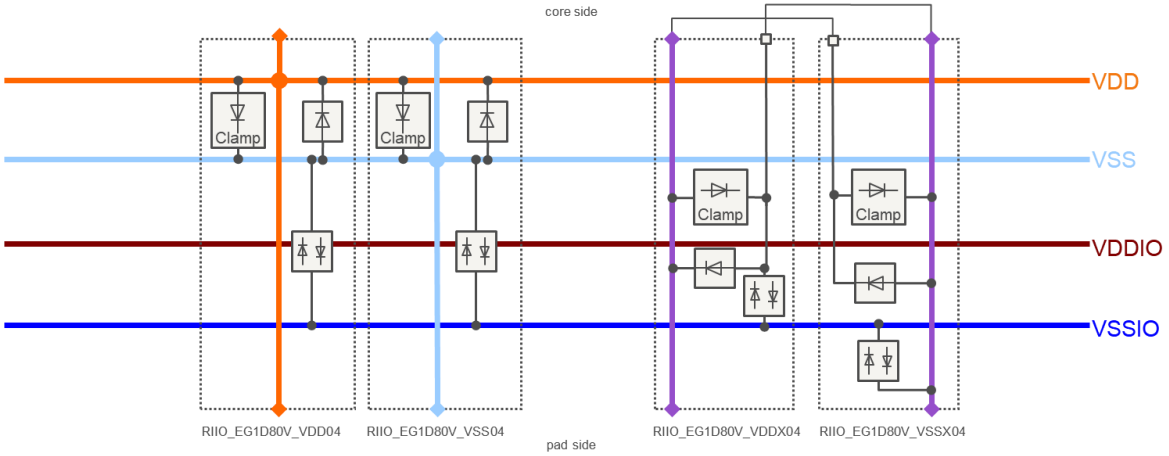


Figure 17 ESD Clamp Scheme Part 4

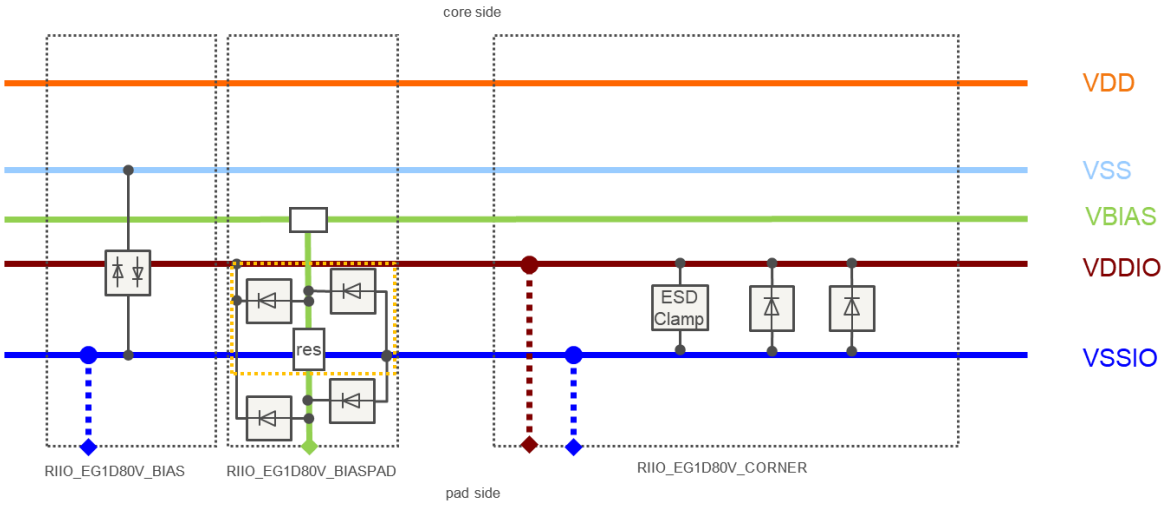


Figure 18 ESD Clamp Scheme Part 5

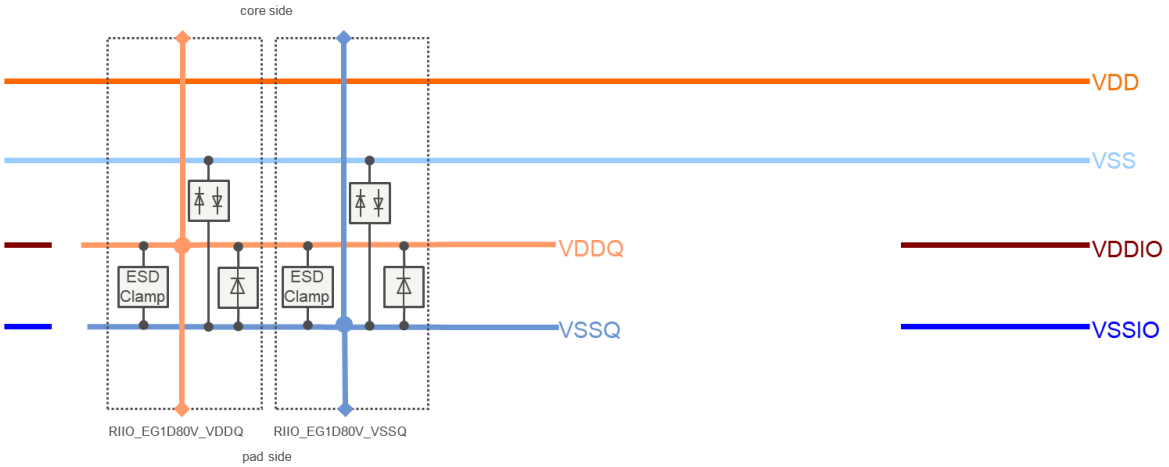


Figure 19 ESD Clamp Scheme Part 6

5 Configuration

5.1 Rail Dimensioning

One pwr/gnd supply cell pair is required for a total of 64mA drive strength.
Following the scheme of Figure 20, it is possible to place up to eight GPIO cells with full drive strength alongside, if two pwr/gnd supply cell pairs (one left, one right) are placed beneath this GPIO cell group.
When overdrive settings of the GPIO cells results in drive strengths higher than 16 mA, less GPIO cells can be placed between supply/ground cell pairs.

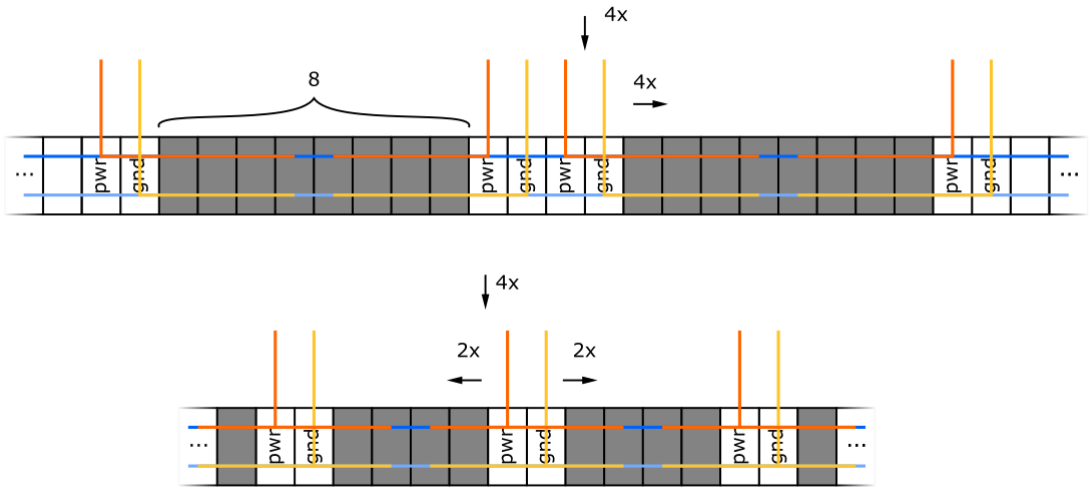


Figure 20 Supply I/O cell placement example