**Section 1 : DUT Description**

Dut receives input packet at Data\_in port (each bit on posedge of clk, so 64 bit packet need 64 clk cycles). After processing, DUT send packet to output port based on configured value in register “Output\_port\_enable”.

When valid\_in is high data\_in will be valid. When valid\_out is high data\_out is valid.

In output data packet, DUT interchange the src addr & dest\_addr.

Id & data remains same in packet. Each packet has unique id and DUT send out transaction in out of order.

DUT registers can be programmed by APB interface.

**Section 2 : Design Diagram**

DUT

Data\_in Data\_out\_P1

Valid\_in Data\_out\_P2

Clk Data\_out\_P3

Rst Data\_out\_P4

Valid\_out

P\_addr

P\_wdata

P\_write

P\_sel

P\_en

P\_rdata

**Pin List:**

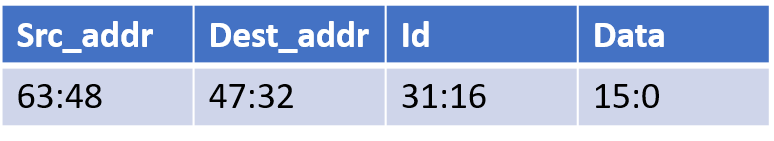
|  |  |  |
| --- | --- | --- |
| **Pin** | **Width** | **Description** |
| Clk | 1 bit | Input |
| RST | 1 bit | Input |
| Data\_in | 1 bit | Input |
| Valid\_in | 1 bit | Input |
| P\_addr | 32bit | Input |
| P\_wdata | 32bit | Input |
| P\_write | 1bit | Input |
| P\_sel | 1bit | Input |
| P\_en | 1bit | Input |
| P\_rdata | 32bit | Output |
| Data\_out\_P1 | 1 bit | Output |
| Data\_out\_P2 | 1 bit | Output |
| Data\_out\_P3 | 1 bit | Output |
| Data\_out\_P4 | 1 bit | Output |
| Valid\_out | 1 bit | Output |

**Section 3 : Registers**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Sr.No | Address | Name | Type | Default Value | Reg. Width | Description |
| 1 | 0x0 | Chip\_enable | RW | 0x1 | 1 bit | 0: Chip Disable , no output  1:Chip Enabled,normal working mode |
| 2 | 0x4 | Chip Id | RO | 0xAA | 8 bit | Chip Id |
| 3 | 0x8 | Output\_Port\_enable | RW | 0x1 | 4 bit | 4’b0001= Output Port P1 enable  4’b0010= Output Port P2 enable  4’b0100= Output Port P3 enable  4’b1000= Output Port P4 enable |

**Section 4 : Packet formats**

Input packet format



Output Packet format

