



80286

Presented by
Dr. Md. Abir Hossain
Dept. of ICT
MBSTU



Intel 80286

✓ Salient features of 80286

- High performance microprocessor with memory management and protection
 - 80286 is the first member of the family of advanced microprocessors with built-in/on-chip memory management and protection abilities primarily designed for multi-user/multitasking systems
- Available in 12.5MHz, 10MHz & 8MHz clock frequencies

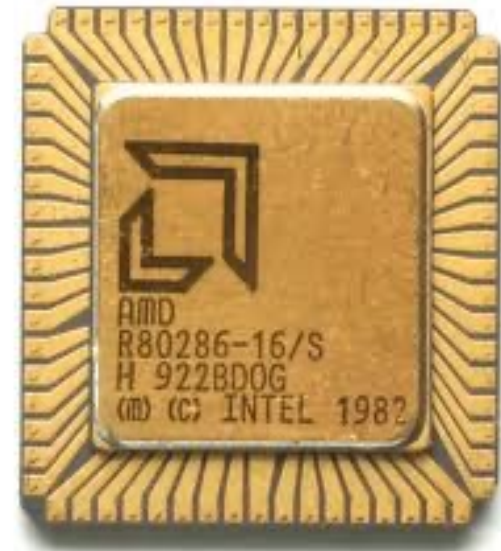
✓ Salient features of 80286(cont...)

- The 80286 CPU, with its 24-bit address bus is able to address 16MB of physical memory.
- ✓ ➤ 1GB of virtual memory for each task

Microprocessor	Data bus width(Bit)	Address bus width(Bit)	Memory size
8086	16	20	1M
80186	16	20	1M
80286	16	24	16M

✓ Salient features of 80286 (cont...)

- 286 includes special instructions to support operating system.
 - for example, one instruction can
 - i) ends the current task
 - ii) save its states
 - iii) switch to a new task
 - iv) load its states and
 - v) begin executing the new task
- housed in 68-pin package



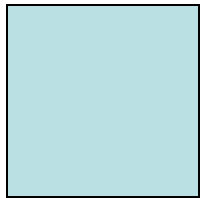
80286 Operating Modes

Intel 80286 has 2 operating modes:

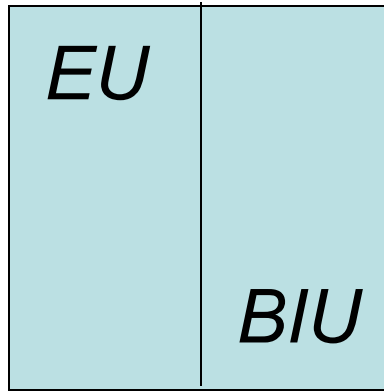
- **Real Address Mode :**
 - 80286 is just a fast 8086 --- up to 6 times faster
 - All memory management and protection mechanisms are disabled
 - 286 is object code compatible with 8086
- **Protected Virtual Address Mode**
 - 80286 works with all of its memory management and protection capabilities with the advanced instruction set.
 - it is source code compatible with 8086



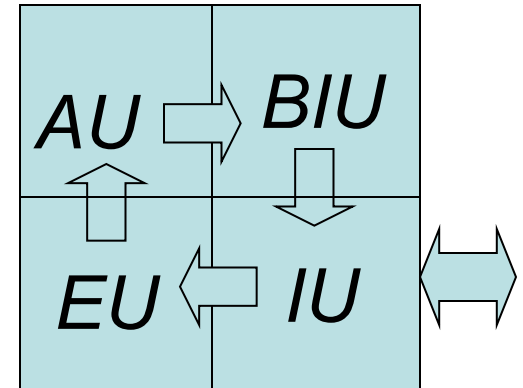
Internal Block Diagram of 80286



8085

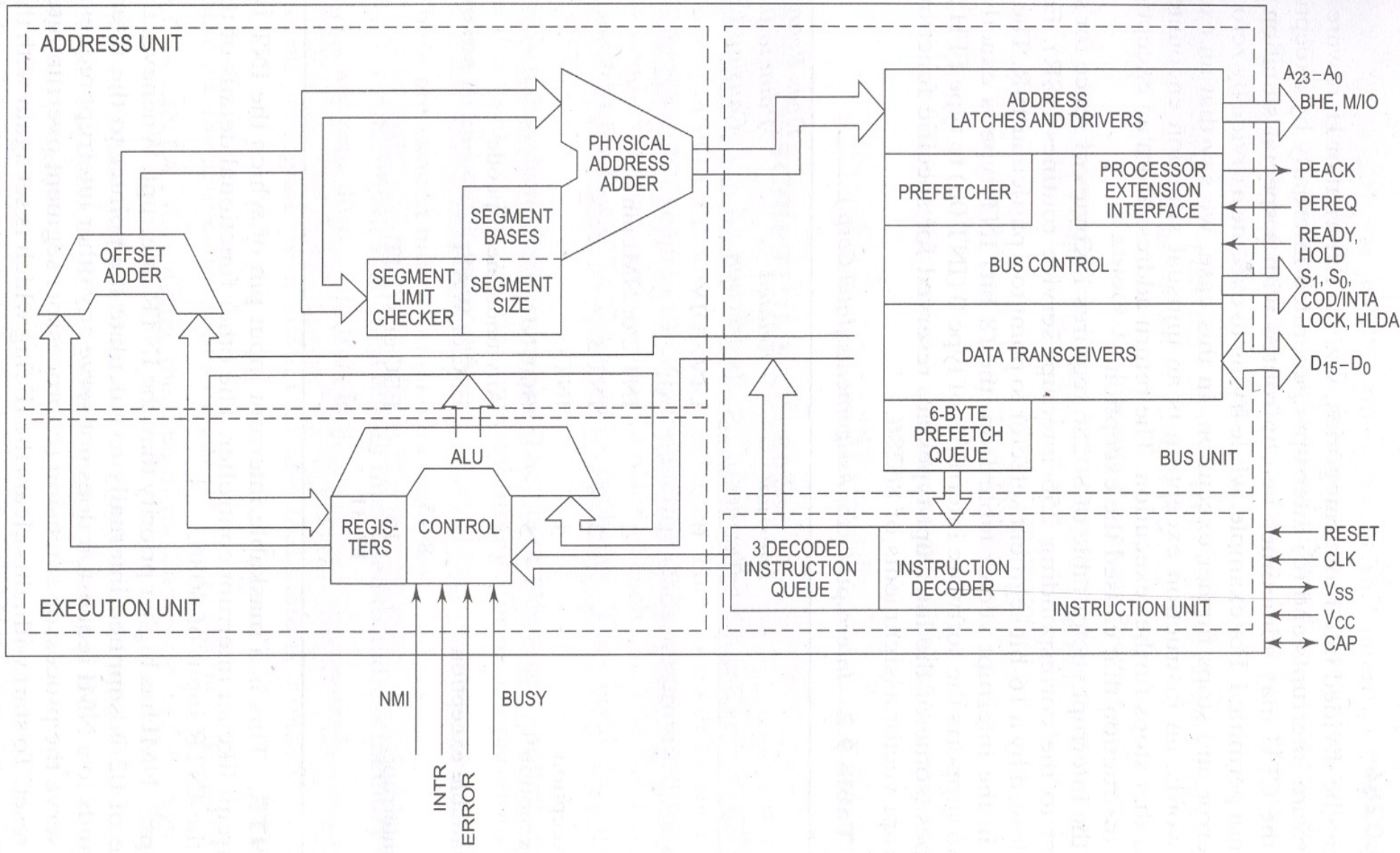


8086



80286

Functional Block diagram 80286



✓ Functional Parts

- ✓ 1. Address unit
- ✓ 2. Bus unit
- ✓ 3. Instruction unit
- ✓ 4. Execution unit

✓ Address Unit (AU)

- Calculate the 20-bit physical addresses based on the 16-bit contents of a segment register and 16-bit offset.
- 80286 addresses 1 Mbyte of physical memory.
- 80286 has 24 address pins
- In real addressing mode, pins A23-A20 are ignored and A19-A0 are used.
- In protected virtual address mode, AU operates memory management unit and utilizes all 24 address lines.
- Physical address computed by the address unit is handed over to the BUS unit.

✓ Bus Unit

- Performs all memory and I/O read and write operations.
- Take care of communication between CPU and a coprocessor.
- Transmit the physical address over address bus $A_0 - A_{23}$.
- Prefetcher module in the bus unit performs this task of prefetching.
- Bus controller controls the prefetcher module.
- Fetched instructions are arranged in a 6 – byte prefetch queue.

Instruction Unit

- Receive arranged instructions from 6 byte prefetch queue.
- Instruction decoder decodes up to 3 prefetched instruction and are latched them onto a decoded instruction queue.
- Output of the decoding circuit drives a control circuit in the Execution unit.

Execution unit (EU)

- EU executes the instructions received from the decoded instruction queue sequentially.
- Contains a 16-bit ALU, an 8086 flag register, general purpose registers, pointer registers, index registers and
- Contains one additional 16-bit special register called **Machine status word (MSW)** register --- lower 4 bits are only used.
- ALU is the heart of execution unit.
- After execution, ALU sends the result either over data bus or back to the register bank.

Register organization of 80286

The 80286 CPU contains the same set of registers, as in 8086.

1. Eight 16-bit general purpose registers.
2. Four 16 bit segment registers.
3. Status and control register.
4. Instruction pointer.

16-BIT
REGISTER
NAME

BYTE
ADDRESSABLE
(16-BIT
REGISTER
NAMES
SHOWN)

	7	07	0
AX	AH	AL	
DX	DH	DL	
CX	CH	CL	
BX	BH	BL	
BP			
SI			
DI			
SP			

Special
Register
Functions

MULTIPLY/DIVIDE
I/O INSTRUCTION

LOOP/SHIFT/REPEAT COUNT

BASE REGISTERS

INDEX REGISTERS

STACK POINTER

GENERAL
REGISTERS

15	0	
CS		CODE SEGMENT SELECTION
DS		DATA SEGMENT SELECTION
SS		STACK SEGMENT SELECTION
ES		EXTRA SEGMENT SELECTION

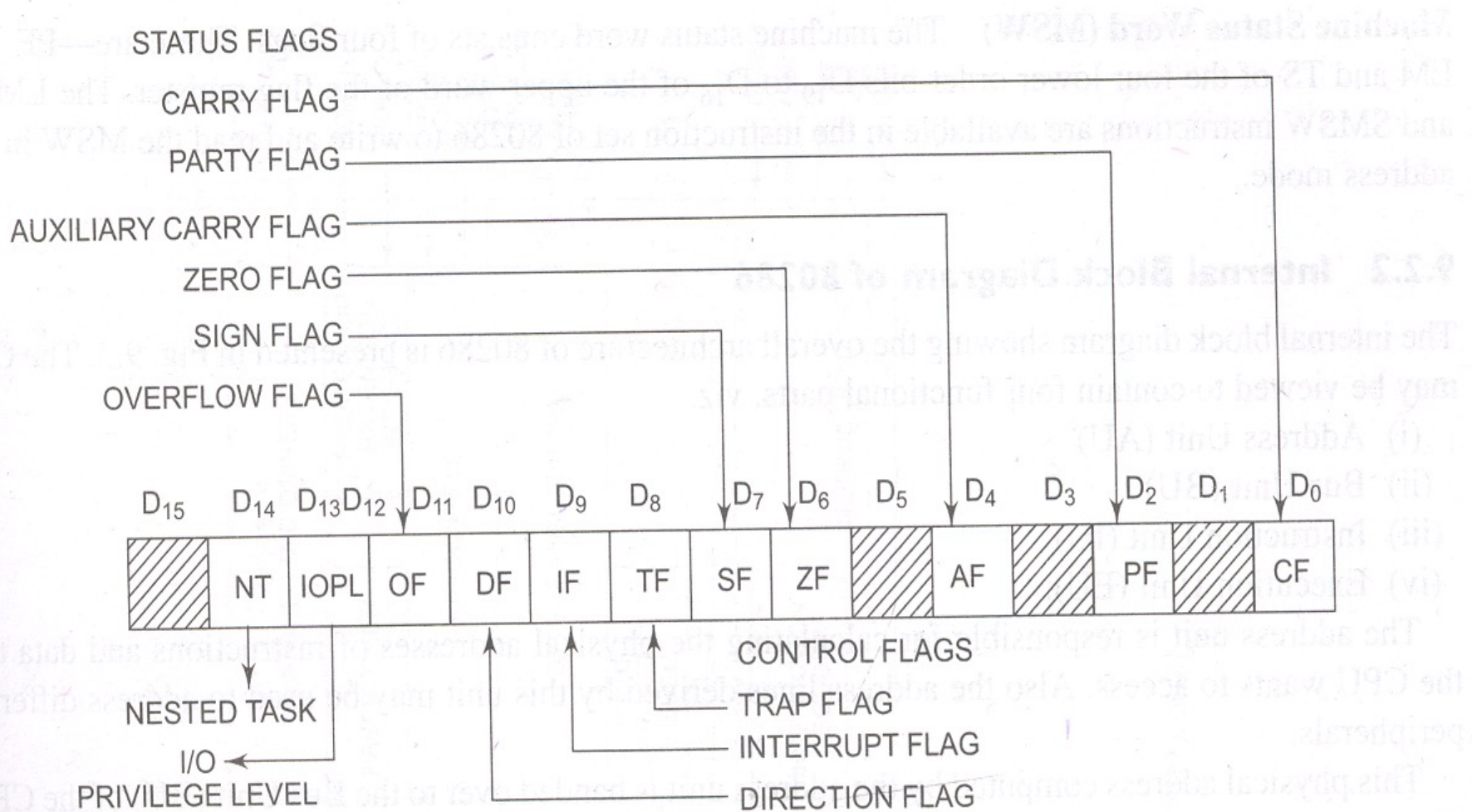
SEGMENT REGISTERS

15	0	
F		STATUS WORD
IP		INSTRUCTION POINTER
STATUS AND CONTROL REGISTERS		

✓ Flag Registers

✓ In the 80286 microprocessor, the flag register is a special-purpose register that stores the status of various operations performed by the CPU.

80286 Flag Registers



Input Output Privilege Level(IOPL)-D12,13

- IOPL is used in protected mode operation to select the privilege level for I/O devices.
- If the current privilege level is higher or more trusted than the IOPL, I/O executed without hindrance.
- If the IOPL is lower than the current privilege level, an interrupt occurs, causing execution to suspend. Note that IOPL 00 is the highest or more trusted; and IOPL 11 is the lowest or least trusted.

Nested task(NT) flag - D14

- When set(NT=1), it indicates that one system task has invoked another through a CALL instruction as opposed to a JMP.
- For multitasking this can be manipulated to our advantage

✓✓✓

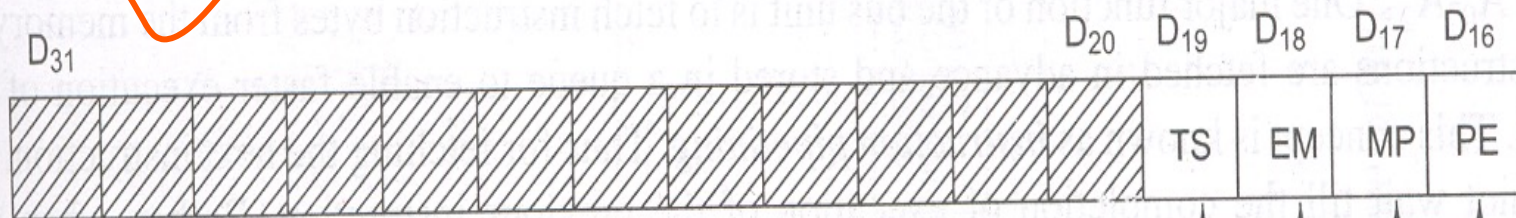
Machine Status Word

- Consist of four flags. These are – PE, MP, EM and TS

✓✓✓
diff

• LMSW & SMSW instruction are available in the instruction set of 80286 to write and read the MSW in real address mode.

- ✓ Loads the contents of a memory location into the machine status word register (MSW)
- ✓ Stores the contents of the machine status word register (MSW) into a memory location



PE - Protection enable

- Protection enable flag places the 80286 in protected mode, if set. This can only be cleared by resetting the CPU.

MP – Monitor processor extension

- If set, flag allows WAIT instruction to generate a processor extension not present in the exception.

EM – Emulate processor extension flag,

- if set , causes a processor extension absent exception and permits the emulation of processor extension by CPU.

TS – Task switch

- if set this flag indicates the next instruction using extension will generate exception 7, permitting the CPU to test whether the current processor extension is for current task.

Additional Instructions of Intel 80286

Sl no	Instruction	Purpose
1.	CLTS	Clear the task – switched bit
2.	LDGT	Load global descriptor table register
3.	SGDT	Store global descriptor table register
4.	LIDT	Load interrupt descriptor table register
5.	SIDT	Store interrupt descriptor table register
6.	LLDT	Load local descriptor table register
7.	SLDT	Store local descriptor table register
8.	LMSW	Load machine status register
9.	SMSW	Store machine status register

Sl no	Instruction	Purpose
10.	LAR	Load access rights
11.	LSL	Load segment limit
12.	SAR	Store access right
13.	ARPL	Adjust requested privilege level
14.	VERR	Verify a read access
15.	VERW	Verify a write access

➤ CLTS

- The **clear task – switched flag** instruction clears the TS (Task - switched) flag bit to a logic 0.

➤ LAR

- The **load access rights** Instruction reads the segment descriptor and place a copy of the access rights byte into a 16 bit register.

➤ LSL

- The **load segment limit** instruction Loads a user – specified register with the segment limit.

➤ VERR

- The **verify for read access** instruction verifies that a segment can be read.

➤ VERW

- The **verify for write access** instruction is used to verify that a segment can be written.

➤ ARPL

- The **Adjust request privilege level** instruction is used to test a selector so that the privilege level of the requested selector is not violated.

Thank You