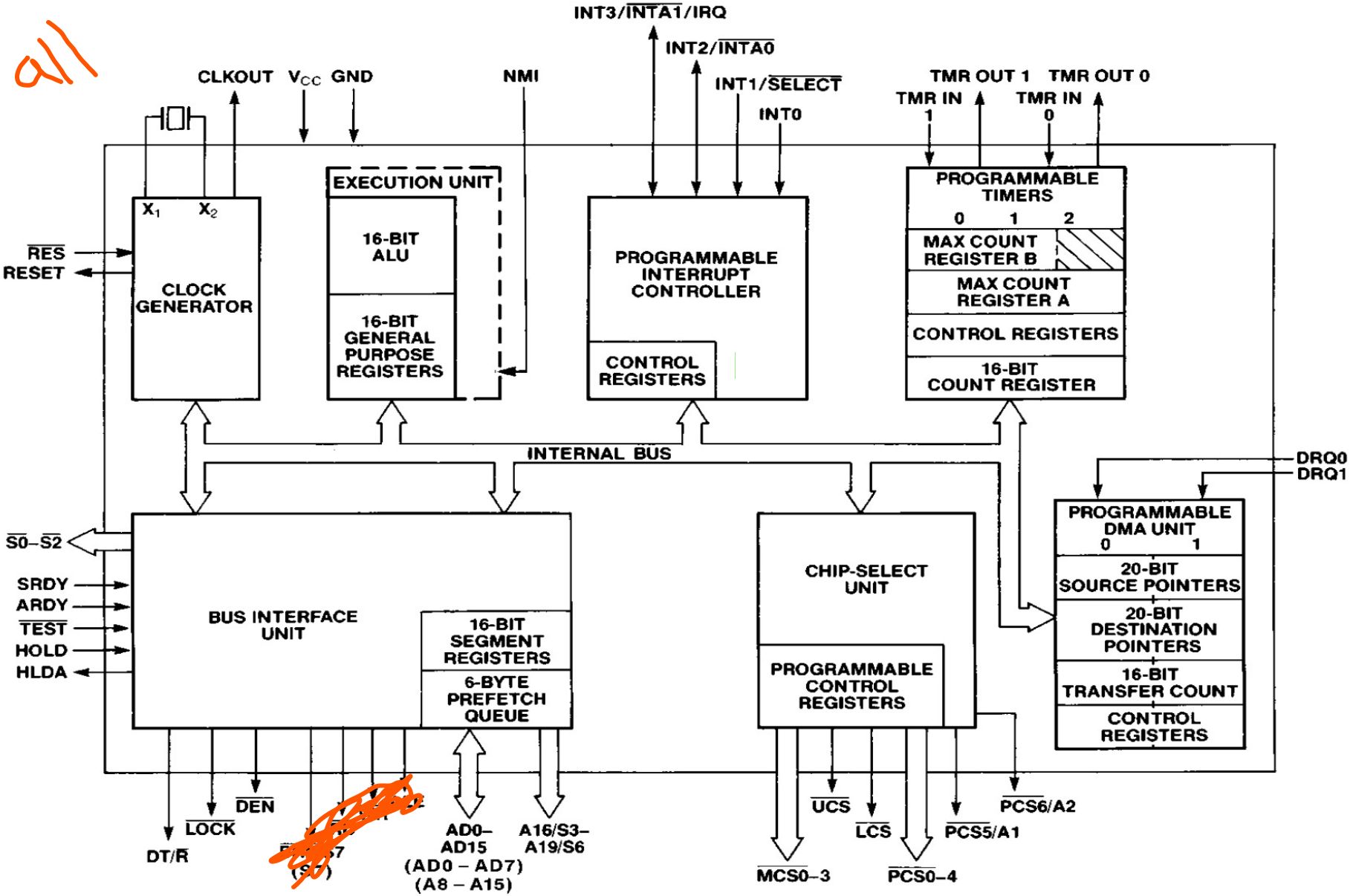
80186

Presented by
Dr. Md. Abir Hossain
Dept. of ICT
MBSTU

General Features of 80186

- Doubles the performance of 8086 microprocessor.
- Fabricated using HMOS technology.
- Has two version: 80186 and 80188
- 80186 -16 bit data bus and
- 80188 has 8-bit data bus
- 80186 includes 68 pins
- Able to operate in 3 different clock speed: 8MHz, 10MHz and 12.5 MHz.
- Address 1 Mbyte of memory.
- 80186 contains 8086 processor and several additional functional chips:
  - clock generator
  - 2 independent DMA channels
  - Programmable interrupt controller.
  - 3 programmable 16-bit timers
- used mostly in industrial control applications

Functional Block diagram of 80186



80186 Functional Block

- ***Clock Generator:***
- Built-in clock generator instead of the external 8284A clock generator used in 8086 microprocessors. This reduces the component count in a system.
- Connected at 80186 X1 and X2 pins.
- ***Execution unit:***
- 80186 has execution unit like 8086 microprocessor.
- Execution unit includes 16-bit ALU and 16-bit general purpose registers.
- ***Programmable Interrupt Controller(PIC):***
- Allows 80186 to receive interrupts from external or internal sources.
- Has 5 pins as **NMI, INT3/$\overline{INTA1}$, INT2/ $\overline{INTA0}$, INT1, INT0**
- The priority sequence of pins as **INT0, INT1, INT2/ $\overline{INTA0}$, INT3/$\overline{INTA1}$**

80186 Functional Block

- ***Programmable Interrupt Controller(PIC)(con..):***
- The PIC arbitrates all internal and external interrupts and controls up to two external 8259A PICs. When an external 8259 is attached, the 80186 microprocessors function acts as the **master** and the 8259 functions as the **slave.**
- ***Programmable Timers:***
- contains three programmable 16-bit timers/counters as counters 0, 1, and 2.
- timers 0 and 1 generate wave-forms for external use and driven by either the master clock of the 80186 or by an external clock
- The third timer, timer 2 is internal and clocked by the master 80186 clock.

80186 Functional Block

- ***Programmable DMA unit:***
- The programmable DMA unit contains two DMA channels, or four DMA channels in some models
- Each channel can transfer data between memory locations, between memory and IO, or between IO devices
- For two DMA channels, has two DMA request input pins **DRQ_0**, **DRQ_1**
- One input signal used for external device as disk controller to request a data transfer between the memory and disk via DMA techniques.
- Each 80186 DMA channel contains
  - Two 20 bit registers
  - One 16 bit counter

80186 Functional Block

- ***Programmable Chip Selection unit:***
- Built-in chip selection unit act as address decoder
- Programmed to generate 6 memory chip selects among them **LCS(**Lower chip select**),** **UCS(**Upper chip select**),** and **MCS0 -**3 pins and several I/O or peripheral chip selection 3 pins are **PCS0-4, PCS5/A1, PCS6/A2.**
- The lower chip select activates when 80186 wants to access a memory in between 00000H to higher address in the range of 1K to 256K range.
- The higher chip select activates when 80186 wants to access a higher memory location in which higher address in the range of FFFFFH.
- The middle chip select activates when 80186 wants to access a midrange memory location.
- The peripheral chip select helps to access a port address located in a block of address up to 128 bytes

80186 additional Features

- ***Power save/Power Down Feature***:
- The power save feature allows the system clock to be divided by 4, 8, or 16 to reduce power consumption
- The power saving feature is started by software and exited by a hardware event such as an interrupt

- ***Refresh Control Unit:***
- The refresh control unit generates the refresh row address at the interval programmed. The refresh address is provided to the memory system at the end of the programmed refresh interval, along with the RFSH control signal.

80186 Functional Block

- 80186 has 8 addressing modes.
- [Assignments 1.]-list out the all addressing modes of 80186
- 80186 has 10 additional instruction beyond 8086
- [Assignments 2.]-list out the 10 new addition instruction of 80186 beyond 8086