

Q. Start

* Write the addressing technique of "READ and WRITE" operation of Intel-8255A.

Read = (port → Data bus)
Write = (Data bus → port)

Answer :-

Addressing technique of READ operation of 8255A :-

A ₁	A ₀	\overline{RD}	\overline{WR}	\overline{CS}	Function Input operation (Read)
0	0	0	1	0	Port A → Data bus
0	1	0	1	0	Port B → Data bus
1	0	0	1	0	Port C → Data bus
1	1	0	1	0	Control Registers → Data bus

Addressing technique of WRITE operation of 8255A :-

A ₁	A ₀	\overline{RD}	\overline{WR}	\overline{CS}	Function Output operation (Write)
0	0	1	0	0	Data bus → Port A
0	1	1	0	0	Data bus → Port B
1	0	1	0	0	Data bus → Port C
1	1	1	0	0	Data bus → Control Register

8255A

Operational Modes and Initialization:

Mode 0 :

When we want to use a port for simple input or output without handshaking, we initialize that port in mode 0.

If both port-A and port-B are initialized in mode 0, then the two halves of port-C can be used together as an 8-bit port.

The two halves of port C are independent, so, one can be initialized as input and another can be initialized as output. ✓

* Mode 1 :

When we want to use port-A or port-B for a handshake input or output operation, we initialize that port in mode 1.

In this mode, some pins of port-C used as handshake lines. pins PC0, PC1, PC2 function as handshake lines for port B.

If port A is initialized as a handshake input port, then the pins PC3, PC4 and PC5 function as handshake signals and PC6 and PC7 are used as input or output lines.

If port A is initialized as a handshake output port, then the pins PC3, PC6 and PC7 function as handshake signals and PC4 and PC5 are used as input or output lines.

Mode 2 :

Only port-A can be initialized in mode 2. Here port A can be used for bidirectional handshake data transfer.

If port A is initialized in mode 2, then pins PC3 through PC7 are used as handshake lines for port-A. The other three pins PC0 through PC2 can be used for I/O if port-B is in Mode 0.

And the three pins will be used for port-B handshake lines if port-B is initialized in mode 1.

8255 A control register format :

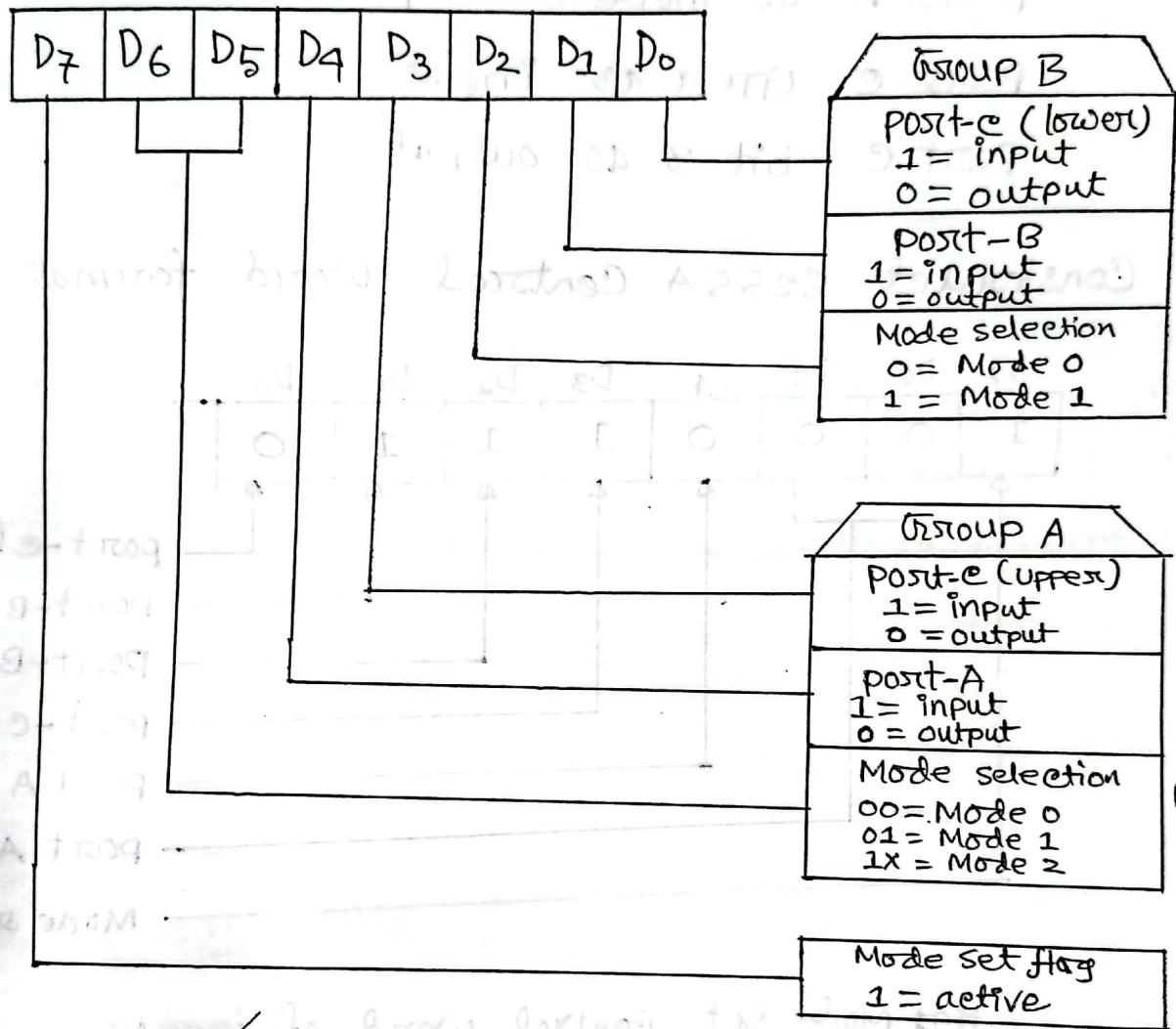


Fig: Mode-set Control Word Format

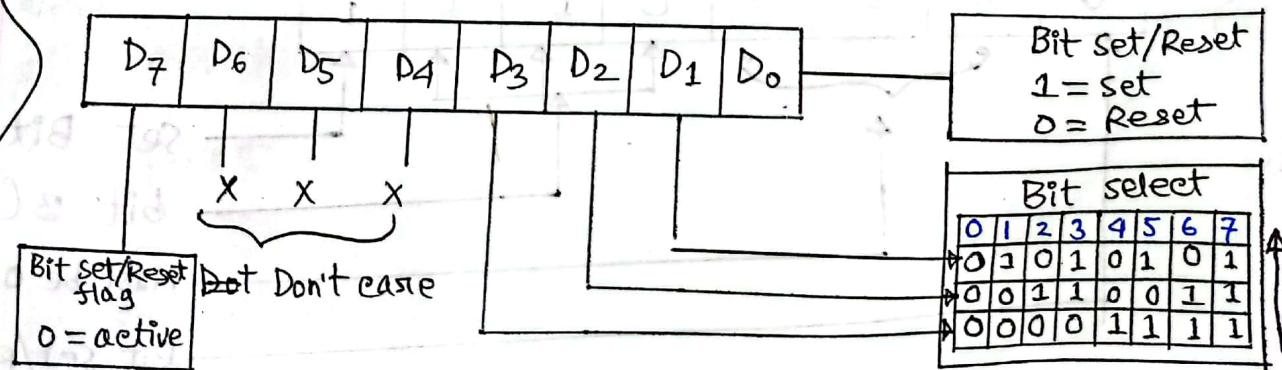


Fig: Port-C bit set/Reset Control Word format.

~~Example:~~

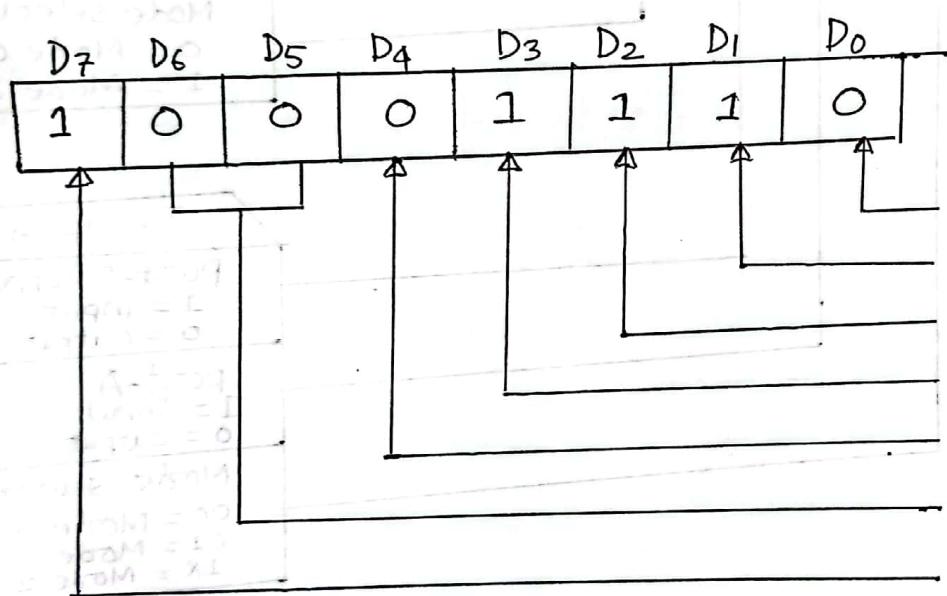
port B as mode 1 input

port A as mode 0 output

port C upper as input

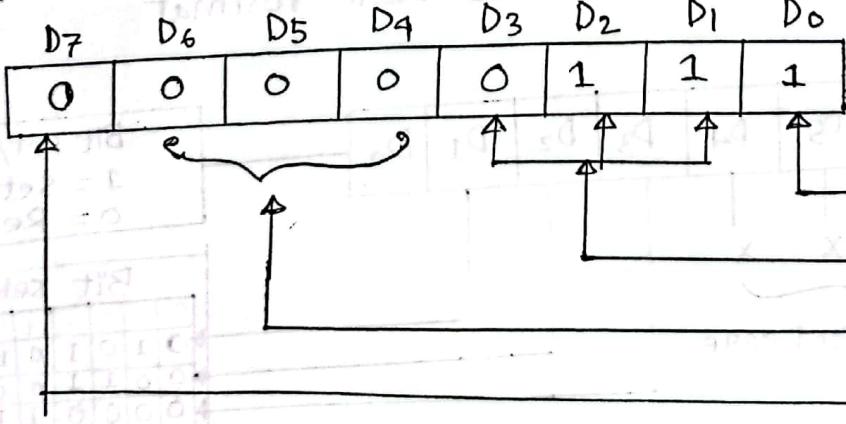
port C bit 3 as output

Construct 8255A Control Word format :-



port-C (lower) as output
port-B input
port-B mode 1
port-C (upper) as input
port-A output
port-A mode 0
Mode set word (active)

~~Fig: Mode set control word of 8255A~~



Set Bit
bit 3 (011)
Must be 0 (Don't care)
Bit set/Reset (active)

~~Fig: port-C bit set/reset control word to set bit 3.~~

(end)

* Write down the mode set control word needed to initialize an intel-8255A as follows:

- (i) port A - handshake input
- (ii) port B - handshake output
- (iii) port C - bits PC6 and PC7 as outputs.

Answer:

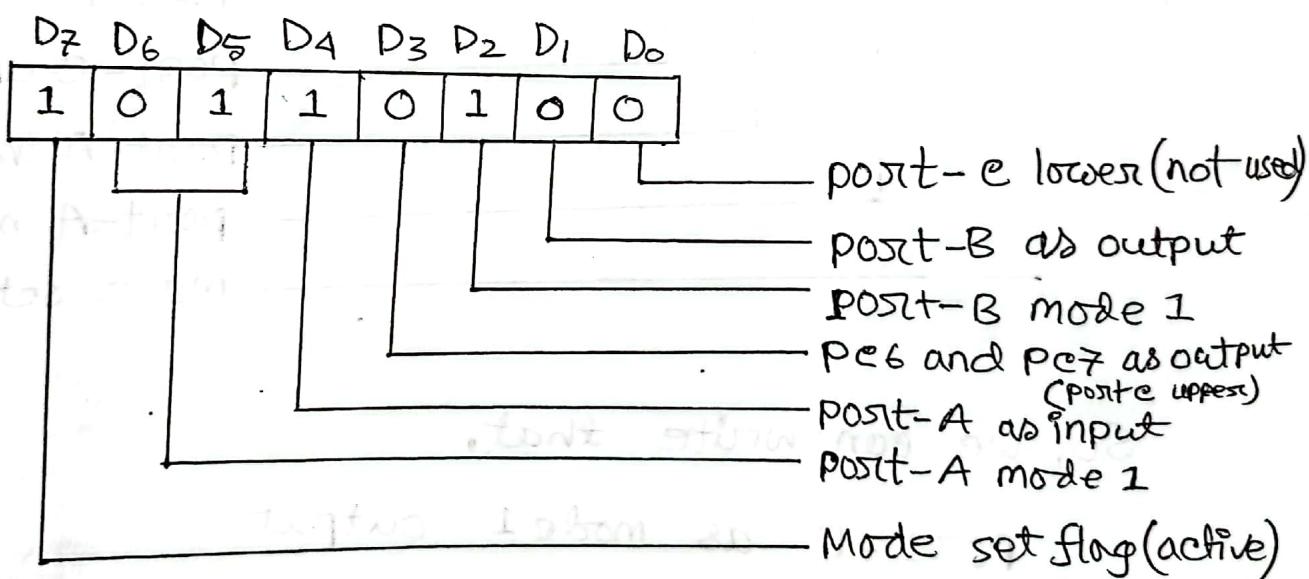


fig: Mode Set control word of 8255A

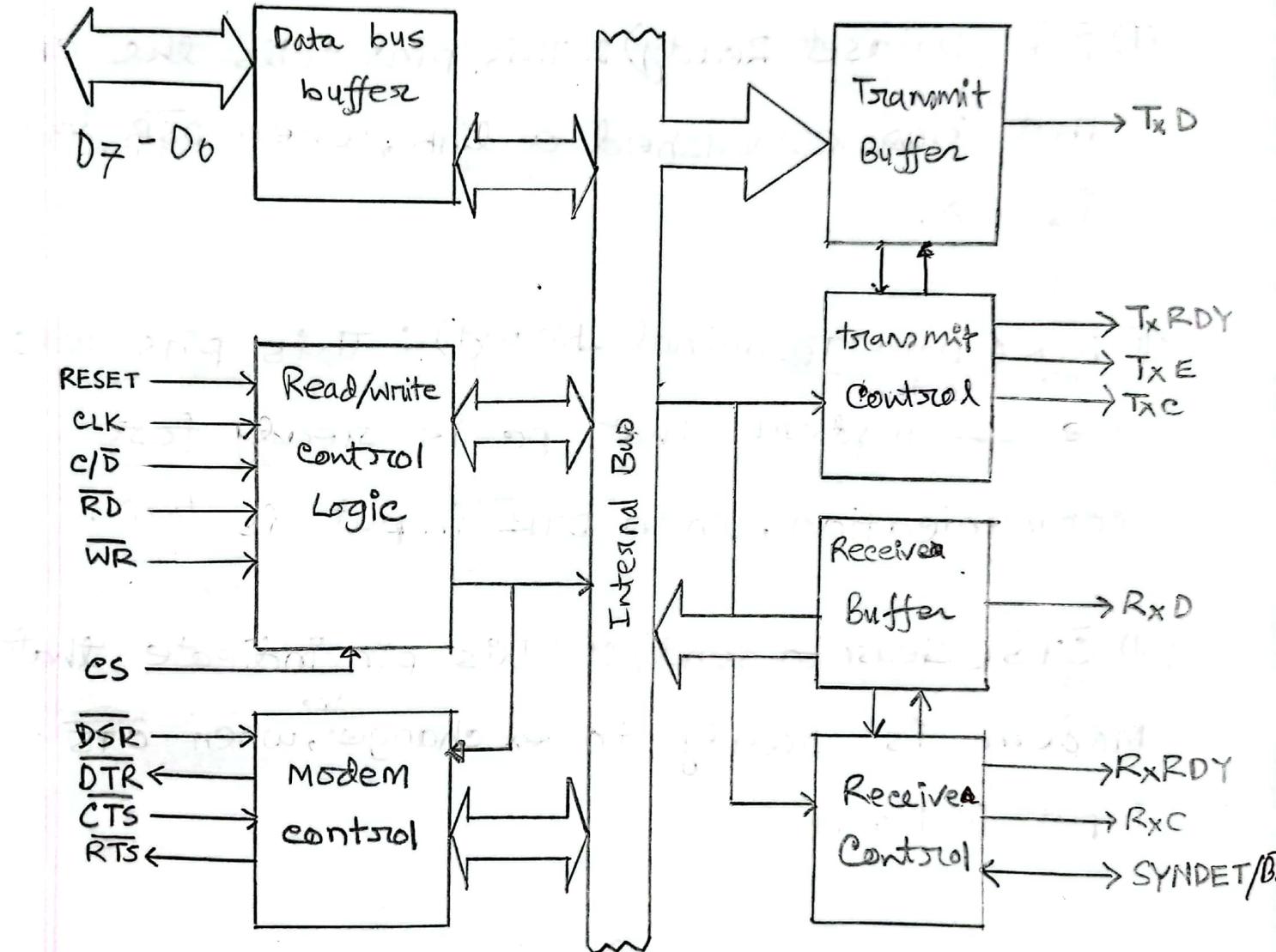
so, we get the control word is $(10110100)_2$,

$$= (B4)_{16}$$

(Start) 8251 PCI (programmable communication interface)

(2014)

* Block diagram of Intel-8251 A :





Pin Description of 8251A :-

(I) Data Bus Buffer :- (D₀-D₇)

→ It is bidirectional 8-bit buffer used to interface 8251A with the system bus of the microprocessor.

→ It has 8 pins (D₇-D₀).

→ It is used to transfer data, control word, command word, status information to the system bus.

(II)

Read/Write control logic : /Control Signal

→ CS :- (chip select) It active for low signal.

12# Control active, 02# Data active

→ CD :- (Control data) If it is high control register is addressed. If it is low data buffer is addressed.

→ RD :- (Read) It active for low signal.

→ WR :- (Written) It active for low signal.

→ RESET :- A high input resets 8251A and forced it to idle mode.

→ CLK :- (Clock) If it is high, then CLK signal is sent.

<u>CS</u>	<u>C/D</u>	<u>RD</u>	<u>WR</u>	Description
0	1	1	0	Microprocessor Unit writes instruction in Control register.
0	1	0	1	MPU reads instruction in control register.
0	0	1	0	MPU writes data to USART.
0	0	0	1	MPU reads data to USART.
1	x	x	x	Chip is not selected.

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III Modem Control:

① DSR (Data Set Ready): It is an input signal. This pin tells the CPU that modem has established a link, when DSR input is low.

② DTR (Data Terminal Ready): It is an output signal. This pin tells the modem that a PC / CPU is ready for communication, when DTR is low.

⑩ CTS (Clear to send) :- It is an input signal. This pin indicates that modem is ready to exchange data, when CTS is low.

⑪ RTS (Request to send) :- It is an output signal. This pin informs model that the CPU wants to exchange data, when RTS is low.

⑫ Transmitter control pins:

(1) TxD (Transmit data) :- This pin is the actual Serial data output.

⑩ TxRDY (Transmitter is Ready) :- This pin tells the CPU that the terminal is ready to access data from CPU.

⑪ TxE (Transmitter Empty) :- This pin tells the CPU that the transmitter is empty.

IV) T_xC (Transmitter clock) :- This pin is the transmitter shift register clock input.

V) Receiver Control Pins

(I) R_xD (Receiver Data) :- This pin is the actual serial data output input.

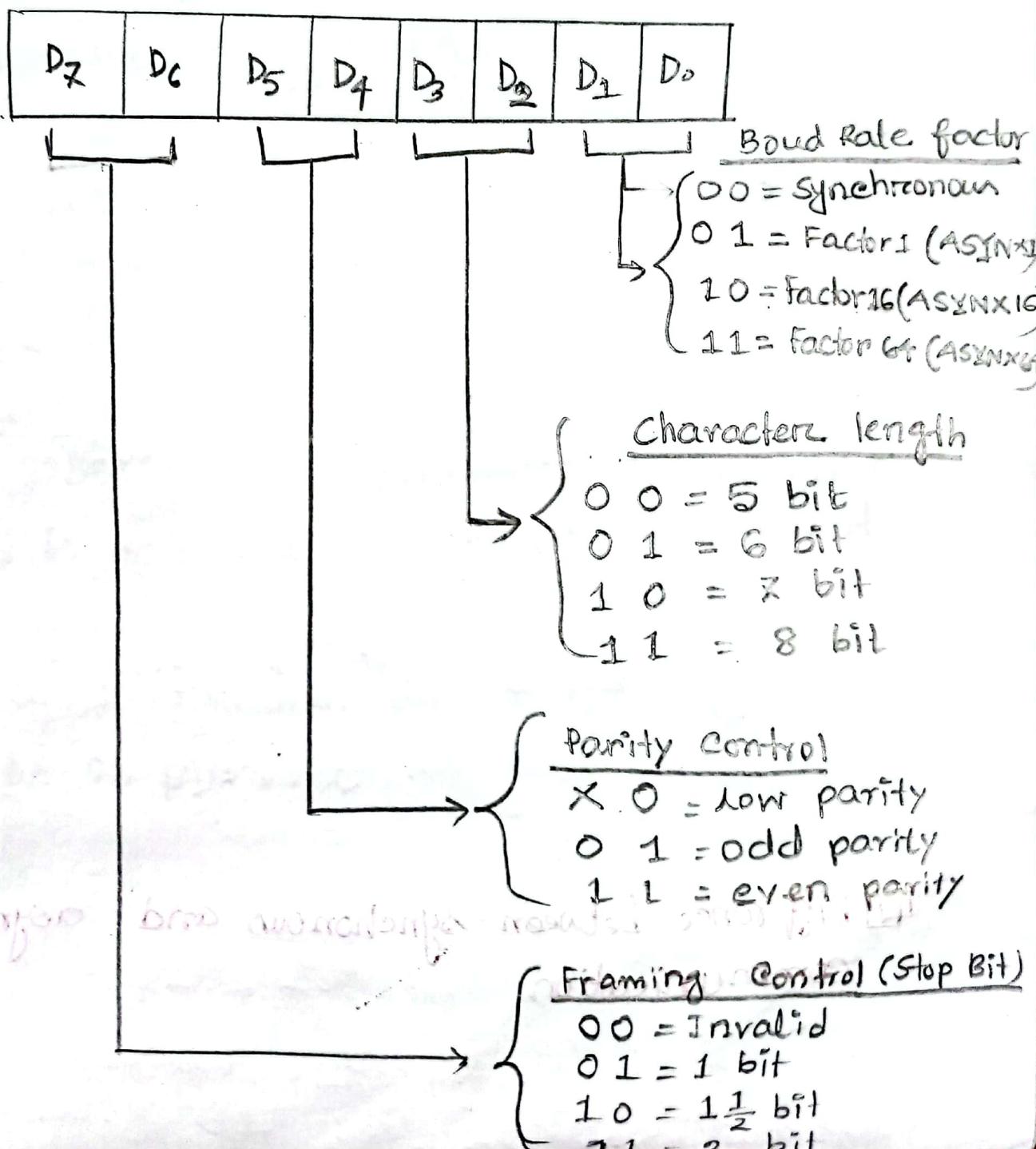
(II) R_xRDY (Receiver is Ready) :- This pin indicates the terminal is ready with data.

(III) R_xC (Receiver clock) :- This pin is the receiver shift register clock input.

(IV) SYNDET (Synchronous detect) :- This pin uses for synchronous communication.

* 1 sec এ কঙ্গুলা Sample মার ব্য → Baud Rate

~~Q7~~ Draw the format of 8251A mode register for both synchronous and asynchronous communication :-



Q:- How is 8251A configured when the mode instruction value is X3H ?

$$(\text{X3})_{16} = 0111\ 0011$$

Difference between synchronous and asynchronous communication.

Difference between synchronous and asynchronous communication:

Synchronous Communication Asynchronous communication

- | | |
|---|--|
| 1, There are clock signal between transmitter & receiver. | 1, There is no clock signal between transmitter and receiver |
| 2, There is no gap between data. | 2, There is gap between data. |
| 3, Data transfer rate is higher. | 3, Data transfer rate is lower. |
| 4, Time interval is constant. | 4, Time interval is random. |