

Report

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08 November 2021

1 Abstract

Through this assignment, we have upgraded the processor that we have built to include caches to the memory system. We added one cache between the IF stage and the main memory. This is the level 1 instruction cache. We also added one more cache between the MA stage and the main memory. This is the level 1 data cache.

1.1 Configuration of The Cache

Table 2 lists the configuration of the cache.

Cache Size	8B	32B	128B	1kB
Latency (in Cycles)	1	2	4	8
Line Size	4B			
Associativity	2			
Write Policy	Write Through			

Table 1: Cache Configuration

1.2 IPC Values For Different Cache Parameters

Table 2 lists the configuration of the cache.

Program	IPC								
	Without Cache	L1d = 1024 B				L1i = 1024 B			
		L1i = 8 B	L1i = 32 B	L1i = 128 B	L1i = 1024 B	L1d = 8 B	L1d = 32 B	L1d = 128 B	L1d = 1024 B
descending	0.0235	0.0233	0.0318	0.0869	0.0701	0.0521	0.0755	0.0752	0.0701
evenorodd	0.0232	0.0220	0.0217	0.0209	0.0195	0.0197	0.0197	0.0197	0.0195
fibonacci	0.0224	0.0216	0.0276	0.0543	0.0464	0.0481	0.0478	0.0473	0.0464
palindrome	0.0238	0.0232	0.0713	0.0598	0.0485	0.0486	0.0486	0.0486	0.0485
prime	0.0239	0.0229	0.0224	0.0216	0.0201	0.0202	0.0202	0.0202	0.0201

Table 2: Cache Configuration

2 Graphs and Observations

When L1d cache size is fixed to 1kB and L1i cache size is changed, we got the graph in figure 1. It is observed that latency increases with increases in L1i cache size and so does the hit rate. There is an optimum size of L1i cache where IPC is at its peak.

When L1i cache size is fixed to 1kB and L1d cache size is changed, we got the graph in figure 2. It is observed that latency increases with increases in L1d cache size until a certain point and then stays the same. It can be inferred that increasing instruction cache size does not lead to better performance after reaching a certain cache size.

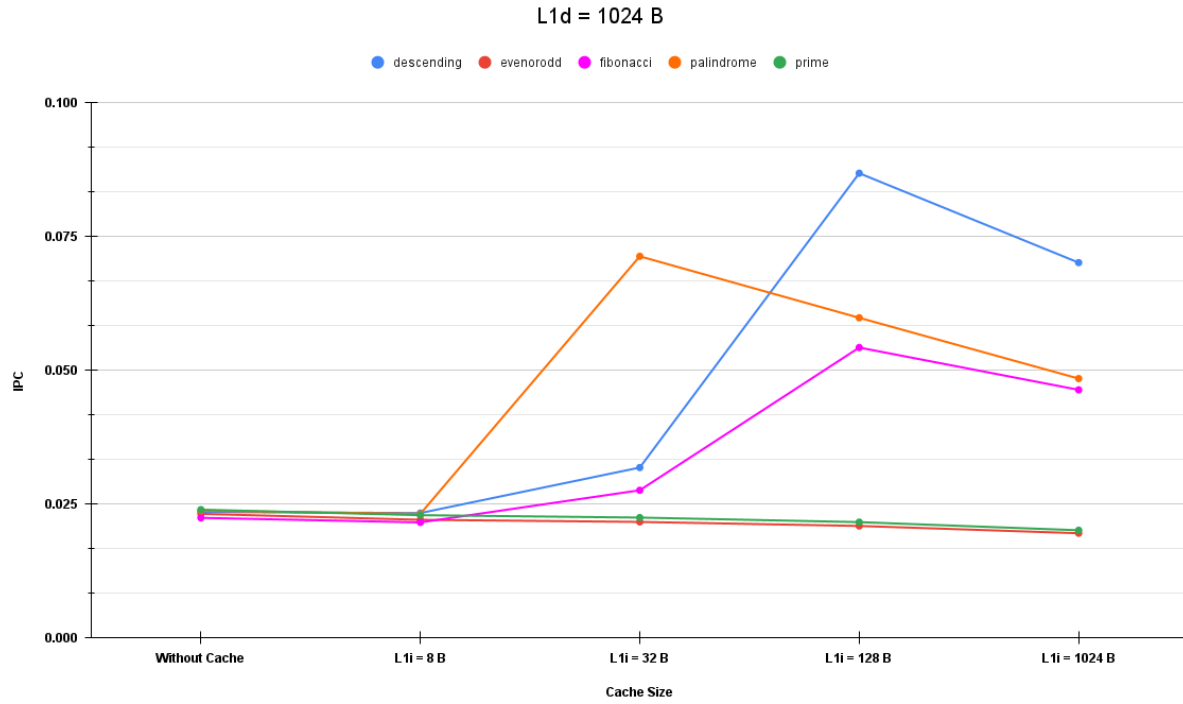


Figure 1: IPC when L1d = 1kB

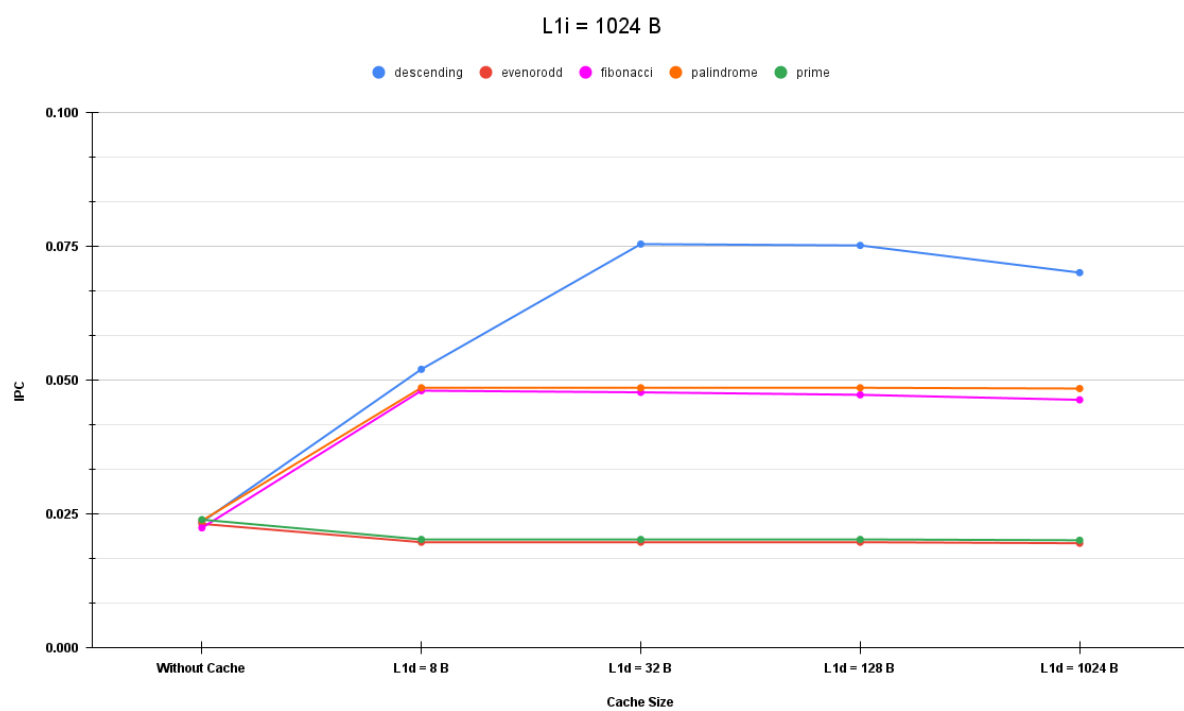


Figure 2: IPC when L1i = 1kB