Report

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1 Abstract

Through this assignment, we have upgraded the processor that we have built through labs 1-4 to a discrete event simulator.

1.1 Discrete Event Simulator Model

Event is the tuple < event time, event type, requesting element, processing element, payload >. Event queue is a list of events w.r.t. time. Event fire corresponds to the clock becoming equal to the event time. When an event is fired, handleEvent() method of the processor is invoked. Handling an event might trigger other events to be invoked in the current cycle or any future cycle.

1.2 Functionalities Implemented

- Modeled the latency of the main memory
- Modeled latencies of different functional units like ALU, Multiplier etc.

2 Tabulation of Results

Program Name	Cycle Count	IPC
prime.asm	334	0.023952097
palindrome.asm	2062	0.023763336
fibonacci.asm	4995	0.022422422
even-odd.asm	259	0.023166023
descending.asm	11779	0.023516428

Table 1: Table of Results

3 Comments on Observations

It is observed that the IPC of all the benchmark programs is between 0.022 and 0.024. Benchmarks with higher number of hazards and thus more number of iterations have higher number of cycles.