

Assignment-6

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4th November 2022

1 Abstract

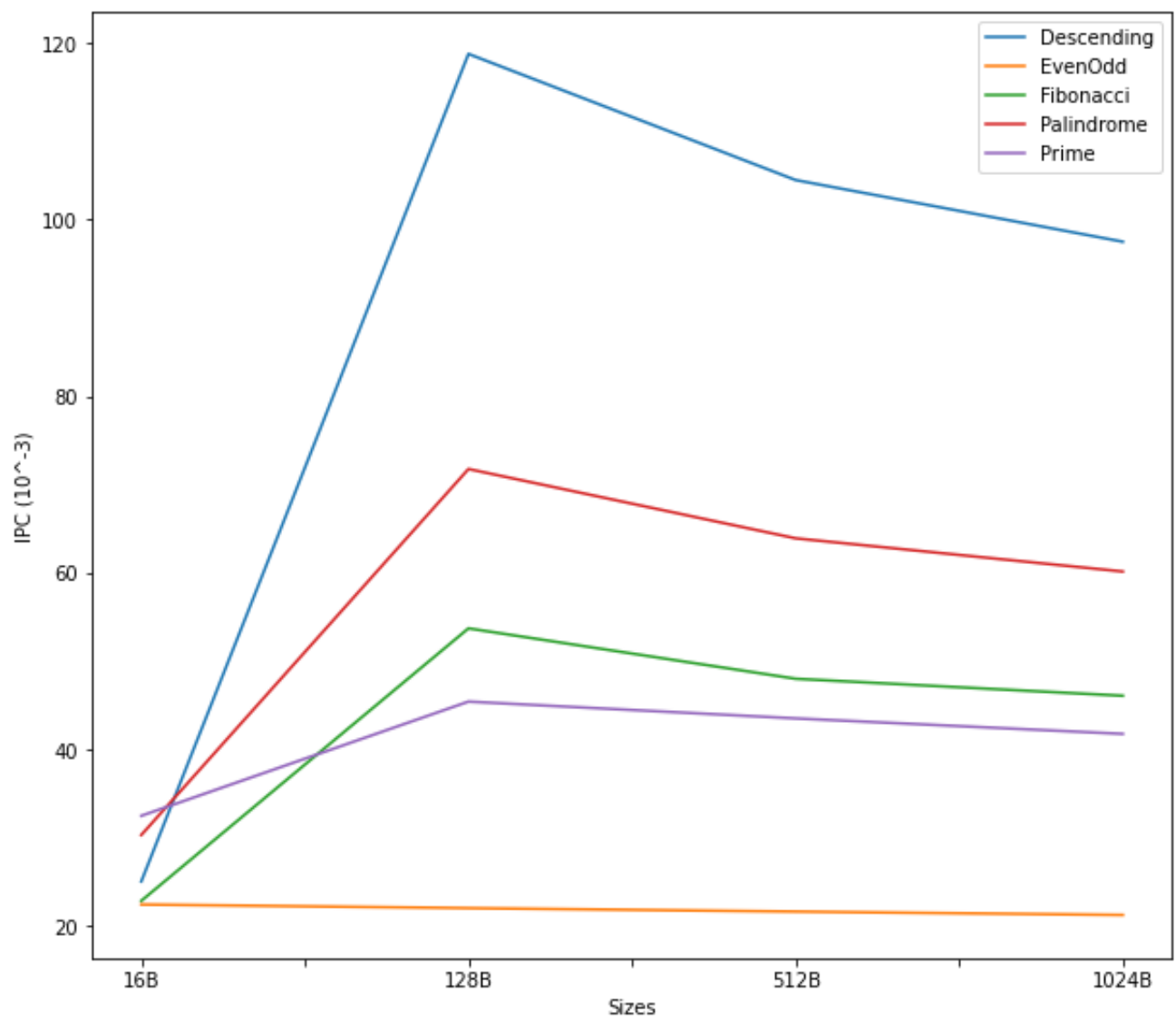
Through this assignment, we have improved the processor we constructed by adding memory system caches. Between the IF stage and the main memory, we implemented a cache. The level 1 instruction cache is shown here. Between the MA stage and the main memory, we additionally placed another cache. The level 1 data cache is this.

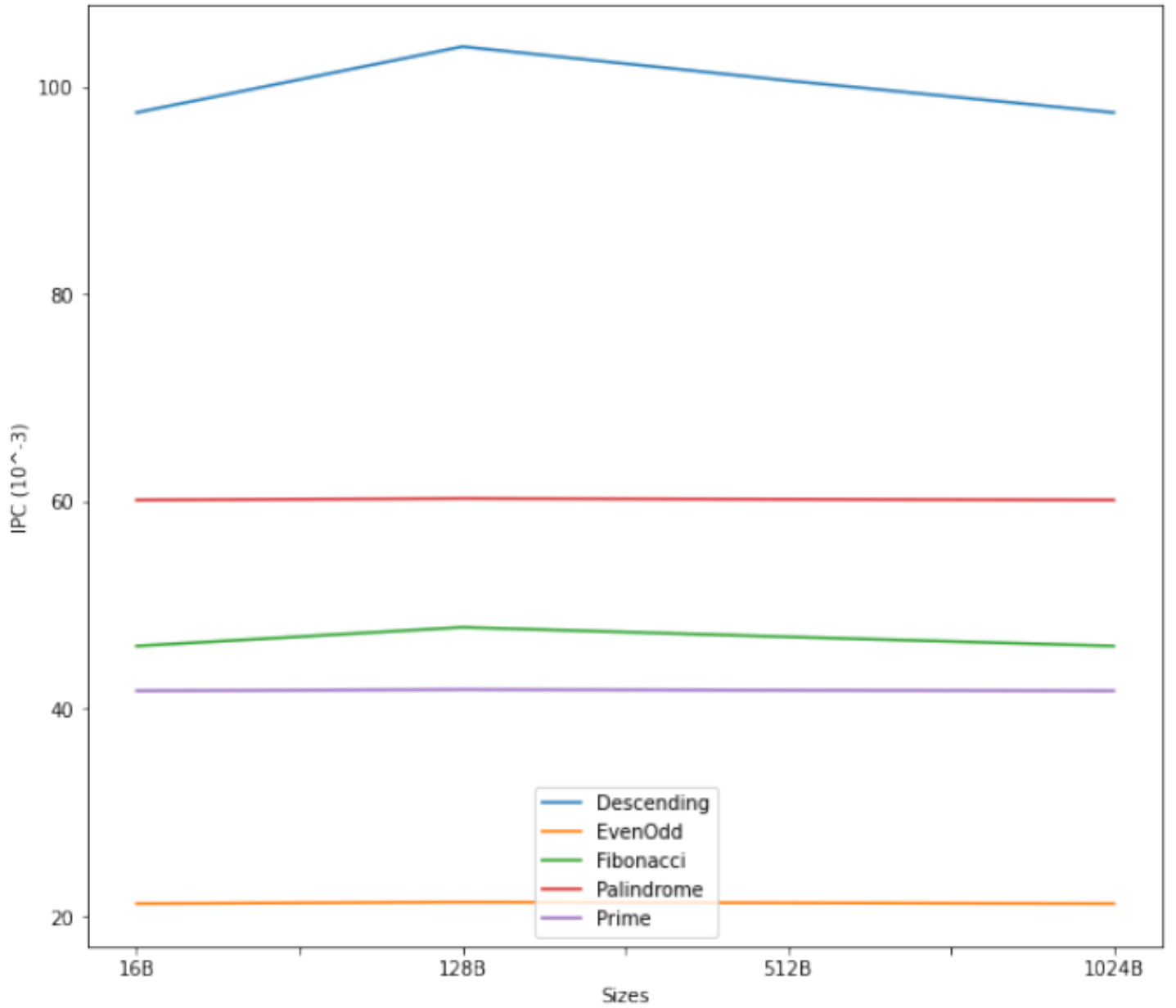
1.1 Configuration of the Cache

Program				IPC						
			L1d = 1kB					L1i = 1kB		
		L1i = 16B	L1i = 128B	L1i = 512B	L1i = 1kB		L1d = 16B	L1d = 128B	L1d = 512B	L1d = 1kB
descending		0.025002256	0.11878216	0.10448887	0.09750088		0.09750088	0.10386202	0.100580975	0.09750088
evenorodd		0.02238806	0.021978023	0.021582734	0.021201413		0.021201413	0.021352313	0.021276595	0.021201413
fibonacci		0.022807017	0.053682037	0.04797048	0.046044864		0.046044864	0.047852762	0.04693141	0.046044864
palindrome		0.030265596	0.07174231	0.063885264	0.0601227		0.0601227	0.060270604	0.06019656	0.0601227
prime		0.03243848	0.045383412	0.04347826	0.04172662		0.04172662	0.041847043	0.041786745	0.04172662

2 Graphs and Observations

We obtained the graph in figure 1 when the L1d cache size was set to 1 kB and the L1i cache size was altered. It has been found that both the hit rate and latency rise as the size of the L1i cache rises. When IPC is at its highest, the size of the L1i cache is optimal. We obtained the graph in figure 2 when the L1i cache size was set to 1 kB and the L1d cache size was altered. Up until a certain point, latency is seen to rise with increasing L1d cache size before remaining constant. It can be concluded that, after a certain cache size, increasing the size of the instruction cache does not result in improved performance.





3 Q-4 and 5

For Toy benchmark we have used greatest program which find greatest element from given element. The results are: For **L1d = 1024**:

1. L1i = 16B, IPC = 0.022680413
2. L1i = 128B, IPC = 0.022312373

For **L1i = 1024**

1. L1d = 16B, IPC = 0.022
2. L1d = 128B, IPC = 0.021868788