Assignment-4

Patel Shahil Manishbhai - 200010039, Rajat Lavekar - 200010045

7th October 2022

1

In the following table we have documented number of cycles and number of OF stalls and number of wrong Branches taken.

Program Name	**Cycles**	**No. of OF stages Stalled**	**No. of Wrong Branch Instructions**
descending.asm	658	126	220
evenorodd.asm	19	10	4
palindrome.asm	124	51	18
fibonacci.asm	157	44	36
prime.asm	79	19	28

2 Comments on Observations

The cycle count of the programs dropped to almost half when they are run on pipelined processor when compared to the non-pipelined processor. In ideal conditions, the cycle count should drop to around one fifth of the number of cycles in processor without pipelining. The ideal conditions are mostly not met due to various data hazards occuring in execution of the programs.
The number of wrong branch instructions and the number of OF stages stalls are also affected depending on the number of data hazards in the program.